A 1.1 μW CMOS Smart Temperature Sensor With an Inaccuracy of $\pm$0.2 °C (3σ) for Clinical Temperature Monitoring

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***Abstract*— In this paper, an ultra-low power, high accuracy CMOS smart temperature sensor customized for clinical temperature monitoring based on substrate p-n-p bipolar junction transistors (BJTs) is presented. A power efficient analog front end with a sensing-range customized multi-ratio pre-gain stage is proposed to effectively utilize the input range of the incremental analog-to-digital converter to relax the conversion speed and resolution requirement. A block-based data weighted averaging technique is also proposed to achieve highly accurate pre-gain ratios while significantly reducing the implementation complexity. The complete temperature sensor is implemented in a standard 0.18 μm CMOS process occupying an active area of 0.198 mm^2. Measurement results from 20 test chips show that an inaccuracy of $\pm$0.2 °C (3σ) is achieved from 25 °C to 45 °C after one-point calibration. The average power consumption is 1.1 μW at a conversion speed of 2 Sa/s.**

***Index Terms*— Smart temperature sensor, ultra-low power, high accuracy, incremental analog-to-digital converter (I-ADC), multi-ratio pre-gain, block-based data weighted averaging (BDWA).**

I. Introduction

With the aim of improving human healthcare, wearable and/or implantable biomedical devices which can provide long-term monitoring for detecting critical and abnormal body conditions are becoming increasing popular. Being one of the most important physiological parameters, temperature sensing with high accuracy is generally required in such systems. According to [1], human body temperature sensors should achieve an accuracy of $\pm$0.1°C from 37 °C to 39 °C, and $\pm$0.2°C both below 37 °C and above 39 °C. To achieve a prolonged operation lifetime with low cost, the temperature sensor should preferably have ultra-low power consumption. These stringent application specific requirements mandate the design of high accuracy low power smart temperature sensors [2].

Traditional temperature sensors are generally discrete devices such as thermistors, platinum resistors, Pt wire, which are bulky, consume high power or incompatible with CMOS process. Smart temperature sensors based on low-cost standard CMOS technology are becoming more and more popular as the sensor interface and readout electronics can be readily fabricated in a single chip, producing a readily interpretable temperature reading in a digital format [3]–[5]. In CMOS technology, two types of popular temperature sensing devices, namely MOSFET and BJT, have been exploited in detail. For MOSFET [2]–[4], due to the spread in gate oxide thickness and channel doping, two-point calibration is required to achieve a high sensing accuracy [6]. The induced extra production cost makes it unfavorable for mass production. BJT-based sensors are proven to be more accurate and can achieve an inaccuracy below $\pm$0.2 °C with only one-point calibration [5], [7]. To achieve this level of accuracy, a high precision readout circuit is necessary. Due to the one-shot operation required, incremental ADCs (I-ADCs) together with precision techniques including dynamic element matching (DEM) and system level chopping have been widely used. This, however, results in relatively high power consumption (in the order of few μW to tens of μW) as a high resolution I-ADC requires much power budget which dominates the sensor power consumption. For emerging applications such as passively powered wireless temperature sensing systems focusing on ultra-low power consumption [2], [3], MOSFET-based designs are becoming prevalent to achieve ultra-low power consumption, with the penalty of higher production cost as a result of increased calibration efforts to ensure high accuracy [2].

In this work, a CMOS temperature sensor is designed with high accuracy and ultra-low power consumption especially suitable for passively-powered clinical temperature monitoring

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applications where the human body temperature can be readily measured non-invasively [2]. In the targeted applications, as only a narrow temperature sensing range is required, the input range of the readout circuit is poorly utilized. Also, a relatively low sampling rate is generally required that can not only reduce the sensor power, but also relaxes the back-end processing and wireless power. Based on these observations, instead of using a high resolution I-ADC employing a high-order modulator with a large integrator bandwidth as in [7], a multi-ratio pre-gain stage is proposed to relax the resolution requirement of the I-ADC by optimizing its input range utilization. BDWA is also proposed to alleviate the capacitor mismatch error while effectively relaxing the control overhead. Our proposed temperature sensor features ultra-low power consumption (less than 1/4.6X as compared to [7]) which is of utmost importance in passively powered applications where the energy storage in the remote sensing system is limited for cost reduction. This paper is organized as follows. Section II illustrates the operation principle of BJT-based temperature sensors. Section III describes the proposed multi-ratio pre-gain stage as well as the detailed analysis on the BDWA technique. A detailed error analysis is presented in Section IV. The circuit level implementation is illustrated in Section V. Measurement results are shown in Section VI. Section VII ends with the conclusions.

II. Operating Principle

Due to its well-defined temperature behavior, BJT shows high temperature accuracy and is generally utilized in CMOS temperature sensor designs. For a BJT, the base-emitter junction voltage ($V_{\rm BE}$) and the collector current is defined as

$$\mathrm{V}_{BE} = \frac{k\mathrm{T}}{q} \ln\left(\frac{I_C}{I_S}\right) \tag{1}$$

where k is the Boltzmann constant, T is the temperature in K, q is the electron charge, and I_C and I_S are the collector current and saturation current, respectively. The temperature characteristic of $V_{\rm BE}$ is mainly defined by I_S, which shows a temperature dependence defined as

$$I_s = ABT\bar{u}_p(T)\mathrm{n}_i^2(T) \tag{2}$$

where B is a constant related to the process and A is the emitter area. The effective hole mobility $\bar{u}_p$ and the intrinsic carrier concentration n_i exhibit the following temperature characteristics

$$\bar{u}_p(T) \propto T^{-n} \tag{3}$$

$$\mathrm{n}_i^2 \propto T^3 \exp\left(\frac{-qV_g(T)}{kT}\right) \tag{4}$$

where V_g is the bandgap voltage of silicon, with

$$V_g(T) = V_{g0} - \beta T \tag{5}$$

where V_{g0} (approximately 1.2V) is the extrapolated bandgap voltage at 0 K and β is a proportional constant. By substituting (2)-(5) into (1), the temperature dependence of V_{BE} can be obtained

$$V_{BE} = V_{g0} + \frac{kT}{q} \ln\left(\frac{I_C}{CT^{4-n}}\right) \tag{6}$$

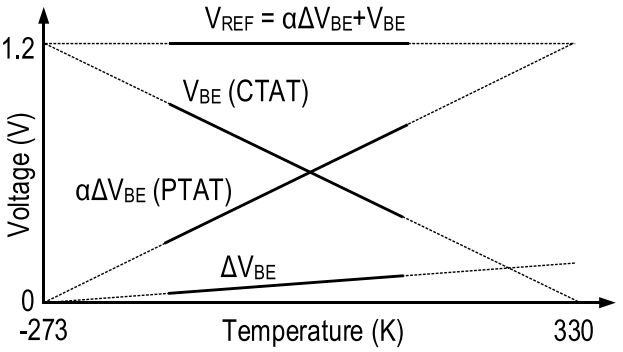

Fig. 1. Temperature dependence of key voltages in conventional CMOS temperature sensor designs.

where C is a constant. It can be observed that V_{BE} shows a complementary-to-absolute temperature (CTAT) characteristic, with a slope of roughly -2 mV/K. High-order curvature is introduced by the term T^{4-n}. By using two identical BJTs biased with a current density ratio of $1:p$, a voltage different between the two base-emitter junctions can be obtained, and can be expressed as

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} ln(p) \tag{7}$$

It can be observed in (7) that ΔV_{BE} is process independent and exhibits a proportional-to-absolute-temperature (PTAT) characteristic. It should be noted that the non-ideality factor of a BJT is very close to 1 when compared with a diode, resulting in a better linearity in ΔV_{BE} to enhance the sensing accuracy [8]. By applying a proportional constant α to ΔV_{BE}, the temperature dependence between ΔV_{BE} and V_{BE} can be cancelled, resulting in a reference voltage which can be expressed as

$$V_{REF} = V_{BE} + \alpha \Delta V_{BE} \tag{8}$$

The temperature dependent voltage ΔV_{BE} and the reference voltage V_{REF} form the basis for CMOS temperature sensing. Fig. 1 shows the temperature dependence of key voltages for a BJT-based temperature sensor.

When $\alpha \Delta V_{BE}$ and V_{BE} are readout using an I-ADC, a ratiometric output (μ) can be obtained as defined by

$$\mu = \frac{\alpha \Delta V_{BE}}{V_{REF}} = \frac{\alpha \Delta V_{BE}}{V_{BE} + \alpha \Delta V_{BE}} \tag{9}$$

By using a digital filter, μ serves as a representation of the instantaneous temperature

$$D_{out} = A\mu + B \tag{10}$$

where A and B are constants with $A \approx 600$ and $B \approx 273$. As shown in Fig. 2(a), the conventional design suffers from a relatively small sensitivity in ΔV_{BE}, requiring a high resolution ADC to achieve high accuracy (e.g. 16-bit for 0.1 °C in [8]). This results in an inefficient use of the I-ADC input range, especially in applications which require only a small temperature sensing range (e.g. clinical temperature monitoring). This paper exploits the use of multiple pre-gain ratios to achieve high accuracy without significantly increasing the implementation complexity.

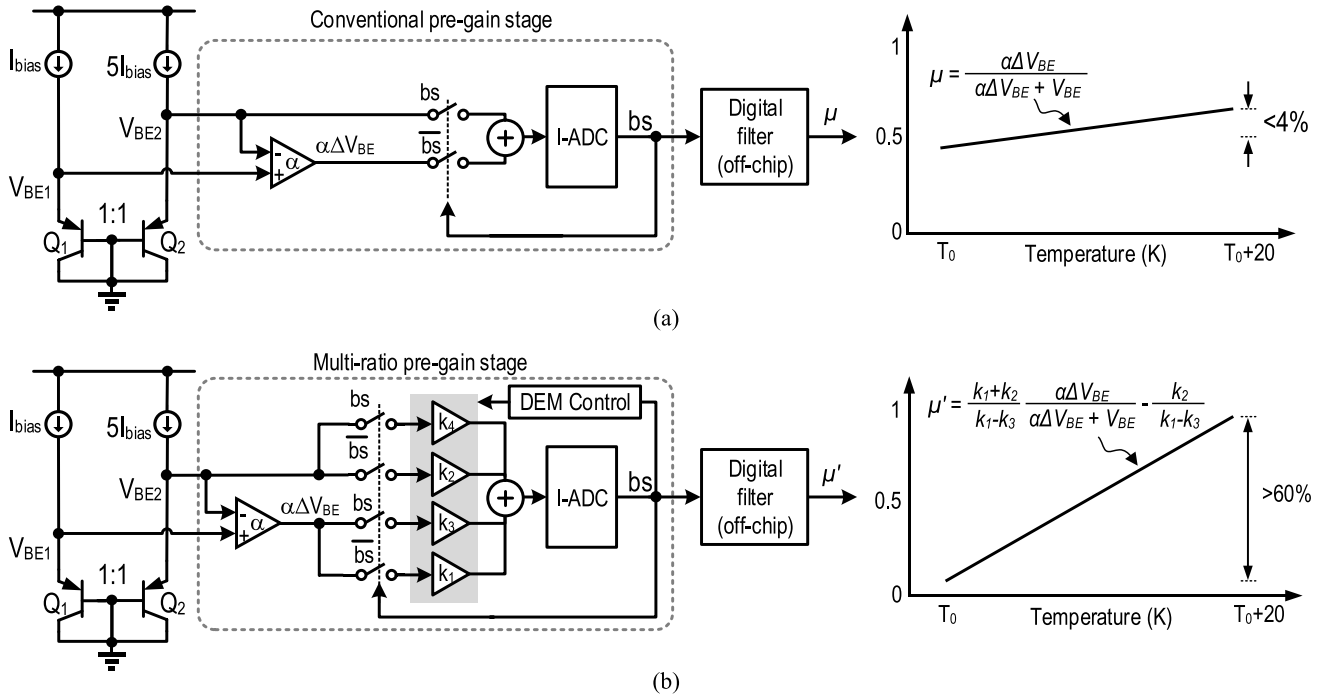

Fig. 2. Block diagrams of the (a) conventional and (b) proposed smart temperature sensor with multi-ratio pre-gain stage.

III. Proposed Structure

Fig. 2(b) shows the block diagram of the proposed smart temperature sensor. Instead of using a fixed pre-gain stage as in conventional temperature sensor designs, we propose to integrate a multi-ratio pre-gain stage (k_{1-4}) to amplify the temperature signal while providing an offset to prevent integrator saturation under low voltage operation. This also relaxes the I-ADC requirement as only a moderate resolution is required (e.g. 12-bit for 0.1°C). To achieve the required sensing accuracy, different error sources (i.e. quantization noise, mismatch noise, thermal noise) are designed to result in less than 0.01°C error separately. The output bit-stream bs is then fedback for pre-gain update as well as processed by the off-chip digital filter to obtain the ratiometric output μ'.

A. Multi-Ratio Pre-Gain Stage

During temperature signal conversions, ΔV_{be} and V_{be} are amplified using the multi-ratio pre-gain stage according to bs. The gain ratios (including α and k_{1-4}) are implemented by the first stage integrator using capacitors to balance the temperature coefficients of V_{BE} and ΔV_{BE}. Based on charge balancing, the integrator is charged with gain ratios αk_1, k_2 when $bs = 0$, and discharged with gain ratios αk_3, k_4 when $bs = 1$, respectively. The integrated charge in each case can be expressed by

$$Q_0 = C_{int} \cdot (\alpha k_1 \cdot \Delta V_{BE} - k_2 \cdot V_{BE}) \tag{11}$$

$$Q_1 = C_{int} \cdot (\alpha k_3 \cdot \Delta V_{BE} - k_4 \cdot V_{BE}) \tag{12}$$

where Q_0 and Q_1 are the transferred charge for $bs = 0$ and $bs = 1$, respectively, and C_{int} is the integration capacitor. With large enough number of integration cycles N_{total}, the residue charge can be assumed to be much smaller than the total charge and the following equation results

$$(N_{total} - N_1) \cdot Q_0 + N_1 \cdot Q_1 = 0 \tag{13}$$

where N_1 is the number of cycles with $bs = 1$. By using (11), (12) and (13), a redefined ratiometric output (μ') can be deduced as

$$\mu' = \frac{k_1 + k_2}{k_1 - k_3} \cdot \frac{\alpha \Delta V_{BE}}{V_{REF}} - \frac{k_2}{k_1 - k_3} = G \cdot \mu - C \tag{14}$$

where G is the gain factor and C is the offset. To ensure proper operation, the following constraints on k_{1-4} should be met

$$\begin{cases} k_1 > k_3 \\ k_4 > k_2 \\ k_1 - k_3 = k_4 - k_2 \end{cases} \tag{15}$$

It should be noted that as k_{1-4} can be realized with DEM, both G and C in (14) can achieve high accuracy. An accurate C can also effectively ensure low voltage operation without saturating the integrator while avoiding extra trimming steps. With an application specific sensing range from 25 °C to 45 °C, G and C can be optimized using a system model based on Matlab to scale the conventional μ to μ'. Table I shows the optimized pre-gain values. As illustrated in Fig. 2, our proposed scheme extends the I-ADC input range coverage from less than 4% to more than 60%, which can significantly improve the power-efficiency and simplify the hardware design.

B. Block-Based Data Weighted Averaging (BDWA)

Even though the proposed multi-ratio pre-gain stage can better utilize the input range of the I-ADC, it also imposes

TABLE I
PRE-GAIN VALUES AND REQUIRED UNIT CAPACITORS

Gain Stage	Value	
α	18	
k_1	6	
k_2	9	
k_3	5	
k_4	10	
bitstream (bs)	Unit capacitors	
	ΔV_{BE}	V_{BE}
0	108 (αk_1)	9 (k_2)
1	90 (αk_3)	10 (k_4)

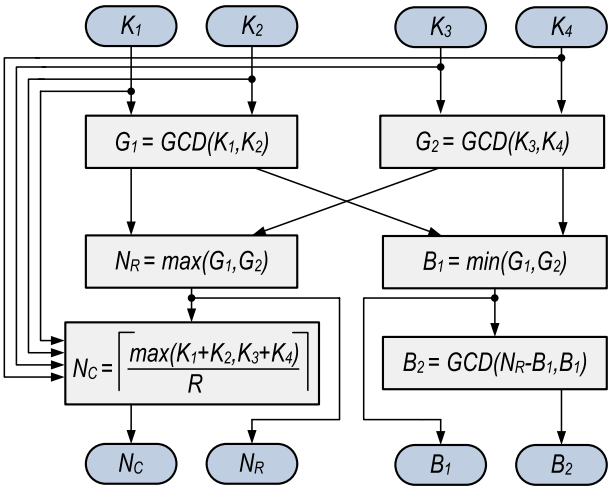

Fig. 3. Implementation of BDWA control line allocations. N_C, N_R are the number of columns and rows of the unit capacitor array, and B_1 and B_2 are the selection block sizes, respectively.

an increase in the number of capacitors required. For the proposed design, the worst case number of unit capacitors happens during the integration of ΔV_{BE} when $bs = 0$ (requiring a total number of 117 unit capacitors). Despite the fact that conventional DEM techniques like data weighted averaging (DWA) can achieve an accurate gain value with the presence of capacitor mismatch, the implementation complexity can lead to significant design overhead. For simplicity, we denote the required gain ratios to be K_{1-4}. For any arbitrary gain ratios (K_1, K_2) and (K_3, K_4), a total of $N_{DWA} = \max(K_1 + K_2, K_3 + K_4)$ unit elements with individual control is required when applying the conventional DWA. This can result in potential routing congestion and area inefficiency issues that ultimately limit its use especially when a large gain ratio is required.

To resolve this problem, BDWA is proposed to achieve multi-ratios with high accuracy while significantly reducing the routing cost. Fig. 3 illustrates the control resource allocations for the proposed BDWA, where the key idea is to group a maximum number of unit capacitors into blocks while still providing the flexibility offered by the DWA. With the two ratios (K_1, K_2) and (K_3, K_4), first their corresponding greatest common divisor (GCD) is found. The required number of rows N_R is assigned to be the maximum of G_1 and G_2.

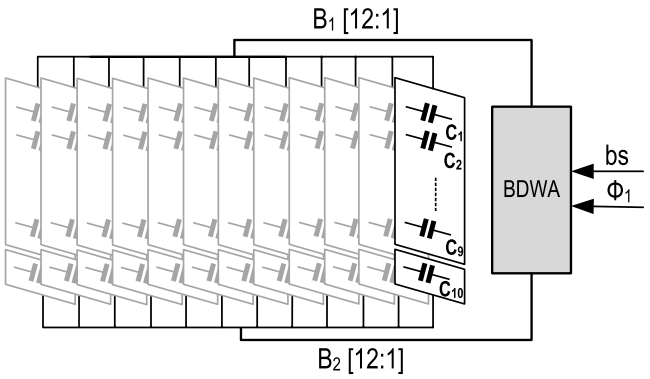

Fig. 4. BDWA implementation using the gain ratios in Table I.

The number of columns N_C can then be selected as the smallest integer which can realize the required gain ratios. As a result, a total number of $N_{BDWA} = N_R \times N_C$ unit elements are required. The BDWA algorithm results in two block control allocations B_1 and B_2 to realize dynamic block-level matching. The following observations can be drawn between DWA and BDWA:

- If K_{1-4} are relatively prime to each other, BDWA and DWA essentially result in the same control allocations.
- $B_1 = T \times B_2$ where T is an integer.
- $N_{BDWA} \geq N_{DWA}$ for all possible integer gain sets.

By using the gain ratios as shown in Table I, we can assign $K_1 = \alpha k_1$, $K_2 = k_2$, $K_3 = \alpha k_3$ and $K_4 = k_4$, respectively. The corresponding values for N_R, N_C, B_1, B_2 can also be calculated as 10, 12, 9 and 1, respectively. Fig. 4 shows the corresponding BDWA implementation. It can be observed that the number of control lines required is significantly reduced to 24, which is 4.8x less than that required for the conventional DWA.

IV. ERROR ANALYSIS

To achieve the target accuracy in the order of $\pm$0.1°C, every error source is limited to a level of 0.01°C. This section describes all major error sources and the corresponding design considerations and analysis for noise minimization.

A. Capacitor Mismatch

As described in section III-B, the increased number of unit capacitors required in BDWA can lead to an increase in averaging cycles. Also, the increased mismatch between B_1 and B_2 can also lead to an inferior noise performance. To better understand the issue, a theoretical analysis of the mismatch error is provided for an arbitrary ratio (K_1, K_2) to compare the performance of the DWA and the proposed BDWA. It is assumed that every capacitor exhibits a mismatch δ_i, where i is the index of the unit capacitor within the capacitor array.

For DWA, the corresponding accumulated mismatch error and the total number of cycles are defined as

$$\Delta K_{j,DWA} = \frac{1}{M}\left(M' \sum_i^{N_{DWA}} \delta_i + \sum_i^{MK_{j,DWA} - M'N_{DWA}} \delta_i\right) \tag{16}$$

$$M' = \left\lfloor \frac{MK_{j,DWA}}{N_{DWA}} \right\rfloor \tag{17}$$

The first term in (16) represents the global mismatch error where all the elements in the capacitor array are utilized the same number of times, while the second term shows the residue error. The minimum residue error (which is achieved when the second term for both K_1 and K_2 is zero) and the corresponding minimum required number of cycles can be expressed as

$$\Delta K_{j,DWA,min} = \frac{K_{j,DWA}}{N_{DWA}} \sum\nolimits_i^{N_{DWA}} \delta_i \tag{18}$$

$$M_{min} = max\left(\frac{LCM\,(K_1, N_{DWA})}{K_1}, \frac{LCM\,(K_2, N_{DWA})}{K_2}\right) \tag{19}$$

where $LCM(.)$ is the least common multiple function. As every DEM algorithm will ultimately converge to the minimum residue error with large enough cycles, it will be used for performance comparison between DWA and BDWA.

For BDWA, it is defined first that the fundamental selection block B_f for selecting B_1 and B_2. As shown in Fig. 3, the possible selections for $B_f = \{N_{C,i}\}$ or $\{B_{1,i}, T \cdot B_{2,i}\}$, i.e. the selection of an entire column or a subset of B_1 and B_2. Without loss of generality, it is assumed $K_1 \geq K_2$ and B_f should include K_2 unit capacitors in a particular cycle. K_1 can then be realized using integer multiples of B_f. The block mismatch error $\delta_{B_{f,j}}$ in each fundamental block $B_{f,j}$ is expressed as

$$\delta_{B_{f,j}} = \sum\nolimits_i^{B_f} \delta_{j,i} \tag{20}$$

for all the unit elements in block $B_{f,j}$.

In the case of $B_f = \{N_{C,i}\}$, the accumulated mismatch error for N number of cycles is

$$\Delta K_{j,BDWA} = \frac{1}{N}\left(N' \sum\nolimits_i^{N_{BDWA}} \delta_i + \sum\nolimits_i^{\frac{NK_{j,BDWA} - N'N_{BDWA}}{N_R}} \delta_{B_{f,i}}\right) \tag{21}$$

where

$$N' = \left\lfloor \frac{NK_{j,BDWA}}{N_{BDWA}} \right\rfloor \tag{22}$$

The minimum error and the corresponding minimum required number of cycles are

$$\Delta K_{j,BDWA,min} = \frac{K_{j,BDWA}}{N_{BDWA}} \sum\nolimits_i^{N_{BDWA}} \delta_i \tag{23}$$

$$N_{min} = N_C \tag{24}$$

Notice that (18) and (23) are similar as N_{BDWA} is an integer multiple of $K_1 + K_2$, except that $N_{min} \geq M_{min}$. As a result, BDWA and DWA should achieve a similar performance.

For $B_f = \{B_{1,i}, T \cdot B_{2,i}\}$, if $B_{1,i}$ is an integer multiple of $T \cdot B_{2,i}$, N_{BDWA} is also an integer multiple of $K_1 + K_2$. This is essentially the same as the case for $B_f = \{N_{C,i}\}$, and (21)-(23) are still applicable. The corresponding minimum number of cycles to achieve the minimum accumulated error is

$$N_{min} = N_C + \frac{N_C \cdot (N_R - B_1)}{B_1} \tag{25}$$

If $B_{1,i}$ is not an integer multiple of $T \cdot B_{2,i}$, not all the unit elements in the capacitor array can be evenly utilized during the averaging process, resulting in a residue error. The accumulated mismatch in this case is

$$\Delta K_{j,BDWA} = \frac{1}{N}\left(N'' \sum\nolimits_i^{N_{BDWA}} \delta_i - N_{B1} \sum\nolimits_i^{N_{B1}} \delta_{B_{f1,i}} - N_{B2} \sum\nolimits_i^{N_{B2}} \delta_{B_{f2,i}} - \sum\nolimits_i^{N_E} \delta_{B_{f2,i}}\right) \tag{26}$$

where

$$N'' = \left\lceil \frac{NK_{j,BDWA}}{N_{BDWA}} \right\rceil \tag{27}$$

$$N_E = N_C \cdot (N_R - B_1) - B_1 \cdot \left\lfloor \frac{N_C \cdot (N_R - B_1)}{B_1} \right\rfloor \tag{28}$$

with N_{B1} and N_{B2} denoting the number of B_{f1} and B_{f2} blocks that are not utilized for completely using up all the N_{BDWA} capacitors in the averaging process. The exact value for N_{B1} and N_{B2} depends on how different blocks are selected. However, the minimum accumulated error occurs when $N_{B1} = N_{B2} = 0$, and can be readily expressed as

$$\Delta K_{j,BDWA} = \frac{1}{N}\left(N'' \sum\nolimits_i^{N_{BDWA}} \delta_i - \sum\nolimits_i^{N_E} \delta_{B_{f2,i}}\right) \tag{29}$$

where

$$N_{min} = N_1 \cdot (N_C + 1) \tag{30}$$

$$N_1 = \frac{LCM\,(N_C \cdot (N_R - B_1), B_1)}{B_1} \tag{31}$$

It should be noted that N_E depends on the actual ratios to be realized. However, this error should be negligible for $N_E \ll N_{BDWA}$, which is valid when the required ratio is large. Also, the error associated to each gain should cancel out each other as only a ratio is required. The theoretical accumulated mismatch error defined in (18), (21), (23), (26) and (29) are utilized to estimate the corresponding ratio error using simulation. Fig. 5 shows the simulated performance comparison between DWA and BDWA with K_{1-4} equal to 108, 9, 90 and 10, respectively, assuming a capacitor mismatch of 1% and 4%. The capacitor array size for the DWA is 117 while that for the BDWA is 120 ($N_R = 1\,0$ and $N_C = 12$). B_1 and B_2 are set to 9 and 1, respectively. Table II summarizes the performance comparison between the DWA and the proposed BDWA. For BDWA, the error for K_1/K_2 and K_3/K_4 are attenuated to the minimum level after 52 cycles and 12 cycles, respectively. Moreover, the achieved error level for K_3/K_4 is very close to that achieved by DWA. For K_1/K_2, even though each gain exhibits a residue error as shown in (28), that is canceled to the first order as expected since only a ratio is required, resulting in a similar performance in the DWA. This clearly demonstrates the practicality of BDWA for high gain ratio implementations. It can also be observed in Fig. 5 that the ratio error quickly converges to a level which is well below the required 74 dB to achieve 12-bit resolution even with a mismatch error as large as 4%. Also, the increase in mismatch due to routing parasitic in the BDWA should limit its minimum mismatch error.

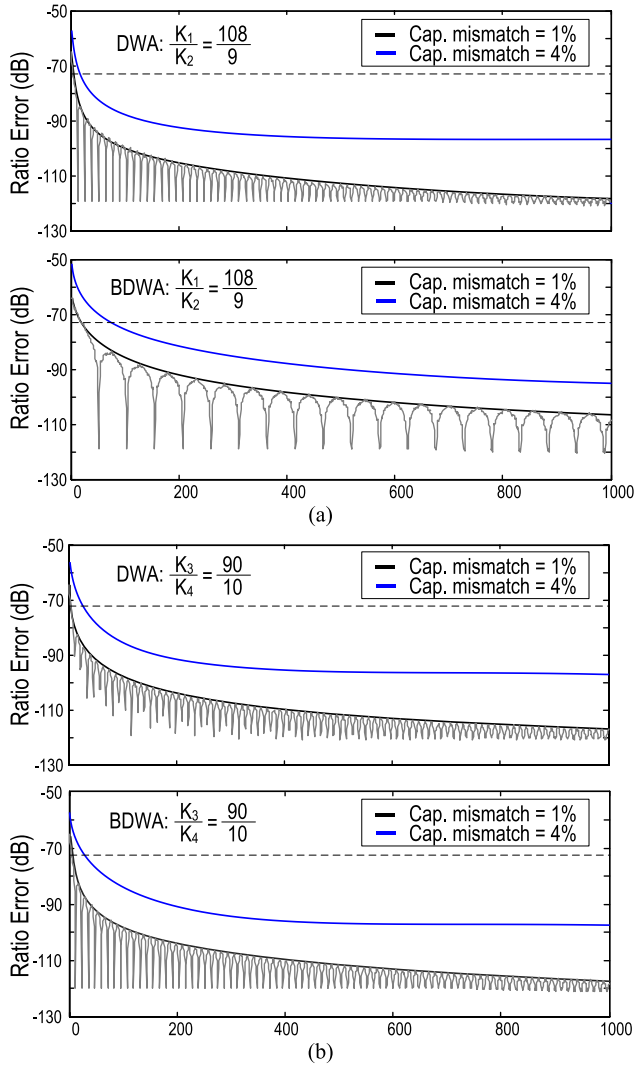

Fig. 5. Performance comparison of DWA and BDWA for (a) K_1/K_2 = 108/9; and (b) K_3/K_4 = 90/10. The black and blue bold lines illustrate the convergence trend with a capacitor mismatch of 1% and 4%, respectively.

TABLE II
PERFORMANCE COMPARISON BETWEEN DWA AND BDWA

	DWA		BDWA	
Ratio	108/9	90/10	108/9	90/10
Total number of unit cap.	117		120	
Control lines	117		24	
Min. cycles	13	117	52	12
Min. ratio error (dB)	-119.3	-119.0	-118.8	-119.9

B. Quantization and Finite Gain Error

To achieve the target accuracy, the quantization level is set to 0.01°C. The proposed multi-ratio pre-gain stage achieves this level of accuracy with only a 12-bit ADC (instead of 16-bit in the conventional design) which can significantly reduce the ADC design complexity.

For the integrator, the Opamp finite DC gain can result in integrator leakage which can cause the modulator to generate a periodic sequence of bs with a range of input called the "dead zone". The effect-number-of-bit (ENOB) of the ADC is determined by the width of the largest dead zone, and the width of dead zone ($\Delta\mu$) can be expressed by [10]

$$\Delta\mu = \frac{1-p}{1+p} \approx \frac{a}{2A_0} \tag{32}$$

where a is the close-loop gain, A_0 is the Opamp DC gain and $p = 1 - a/A_0$ is the leakage gain. $\Delta\mu$ should be smaller than 0.5LSB to achieve the resolution requirement. Based on simulation results, this effect becomes insignificant when the Opamp DC gain is larger than 77 dB. This significantly relaxed DC gain requirement allows the utilization of a simple integrator implementation based on a two-stage amplifier with miller compensation, improving the power efficiency.

C. Settling Time and Thermal Noise

In ultra-low power applications, the settling condition of the sample-and-hold circuit is dominated by the frontend bias current I_{bias} for charging the sampling capacitor. If a half-clock sampling period is available for settling, the error due to incomplete settling can be evaluated as [11]

$$\sum_{i=1}^{M} C_{s,i} \le \frac{1}{2\frac{kT}{q} f_{clk}} \left[-\frac{I_b}{ln(\varepsilon)} \right] \tag{33}$$

where C_s is the unit capacitor, M is the maximum number of sampling capacitors (the sampling capacitor number varies alternately according to $bs = 0$ or 1), f_{clk} is the sampling clock and ε is the relative inaccuracy. In this work, $I_b = 25nA$ and $f_{clk} = 8kHz$. As a result, the corresponding maximum sampling capacitance should be roughly $8pF$. When compared with the thermal noise $\overline{n^2} = 4kT/(N \cdot C_s)$ (N is the number of cycles in one temperature conversion), the estimated minimum unit capacitance is 0.8fF, which implies that the thermal noise is relatively insignificant in this design.

V. CIRCUIT IMPLEMENTATION

Fig. 6 shows the simplified schematic of the complete temperature sensor implementation. It is composed of an analog frontend followed by a first-order I-ADC. The analog frontend consists of a bias current generator and a bipolar core. The bias current I_{bias} is PTAT to enhance the linearity of V_{BE} and V_{REF}, improving the sensing accuracy [5]. In order to achieve ultra-low power consumption while fulfilling the sensing accuracy and readout speed requirements, the values for I_{bias}, I_b and R are designed to be 8.3 nA, 25 nA and 6.5 MΩ, respectively. The Opamp is adaptive self-biased [12] and draws only 85 nA at 37°C from a 1V supply. Two V_{BE} signals (V_{BE1} and V_{BE2}) are derived using 6 identical current branches from the bias current generator with DEM to minimize the mismatch error, with $I_b = 25nA$ for complete V_{BE} settling using a sampling clock f_{clk} of 8 kHz. To enhance the output impedance and mirror the current to the branches more accurately, cascading has been used. As the targeted temperature sensing range is from 25 °C to 45 °C, the corresponding V_{BE} is expected to be close to 620 to 500 mV, respectively. As a result, a supply

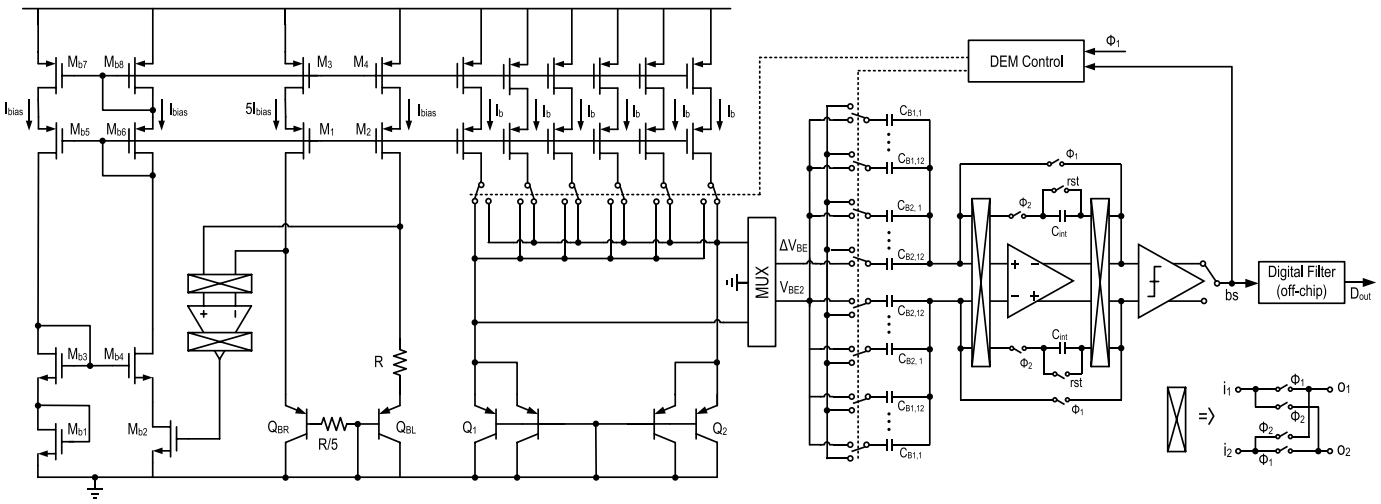

Fig. 6. The proposed smart temperature sensor simplified architecture.

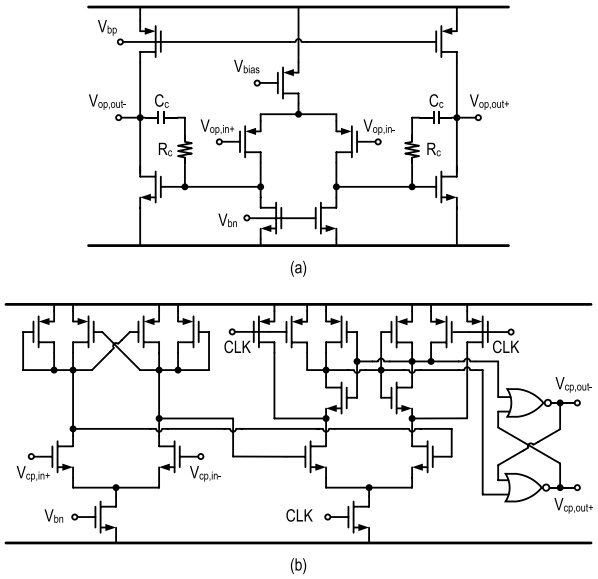

Fig. 7. Simplified schematic of the (a) operational amplifier (integrator) and (b) latched comparator.

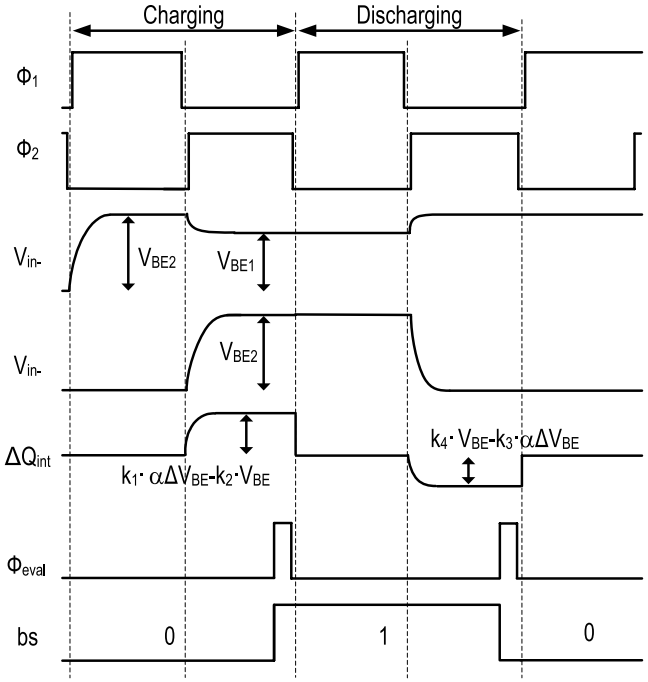

Fig. 8. Timing diagram of one typical charging/discharging cycle.

voltage of 1 V for the analog blocks would suffice for proper circuit operations. The proposed multi-ratio pre-gain stage is implemented using a fully differential integrator, and a unit capacitor array of 120 elements, with $C_{unit} = 28fF$ and $C_{int} = 40C_{unit}$. The capacitor blocks $C_{B1,i}$ and $C_{B2,i}$ are designed according to the proposed BDWA algorithm described in section III-B. By using the proposed multi-ratio pre-gain stage and BDWA technique, the specification of the I-ADC can be greatly relaxed. Fig. 7(a) shows the implemented miller-compensated two-stage amplifier with bias voltages generated using I_{bias} (common-mode feedback not shown). The corresponding GBW, DC gain and phase margin are 240 kHz, 84 dB and 74°, respectively, while drawing only 520 nA at 37 °C. A latched comparator for determining the polarity of the quantization error is shown in Fig. 7(b). A pre-amplifier is utilized to reduce the kickback noise and achieve the required temperature resolution. The mismatch of the sampling capacitors is averaged by BDWA, while the remaining offsets from the Opamp and comparator are minimized using system level chopping. Various noise sources are minimized to achieve the target accuracy according to section IV. Simulation results show that the analog frontend, I-ADC and the control logic consume 0.27 μW, 0.57 μW and 0.25 μW, respectively.

Fig. 8 shows the waveform of the half-circuit conversion process. In ϕ_1, V_{BE2} is sampled from terminal V_{in1-} while V_{in2-} is connected to ground. In ϕ_2, V_{BE1} is sampled from terminal V_{in1-} and terminal V_{in2-} is utilized to sample V_{BE2}. The stored V_{BE2} and ΔV_{BE} are then amplified using the multi-ratio pre-gain stage, and a charge package proportional to $(\alpha k_1 \Delta V_{BE} - k_2 V_{BE})$ is integrated in the charging phase.

TABLE III
PERFORMANCE COMPARISON WITH STATE OF THE ART

Ref.	Temp. range (°C)	Inaccuracy (°C)	Resolution (°C)	Power (μW)	Samp. Rate (Sa/s)	Chip Samples	Calibration	Process (μm)
[2]	35 to 45	±0.1	< 0.035	0.11	10	3	2-point	0.35
[3]	-10 to 30	+1/-0.8	N/A	0.12	33	9	2-point	0.18
[13]	27 to 47	±1	1	0.9	N/A	N/A	2-point	0.18
[14]	0 to 100	+1/-0.8	0.3	0.405	1k	4	2-point	0.18
[15]	-55 to 125	±0.1*	0.025	62.5	10	20	1-point	0.7
This work	25 to 45	±0.2*	0.01	1.1	2	20	1-point	0.18

* 3σ values from multiple chip results.

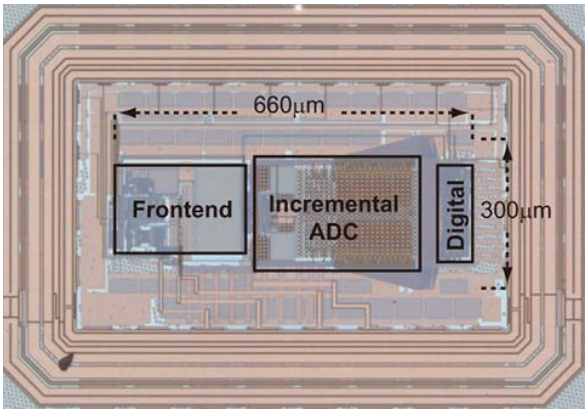

Fig. 9. Chip micrograph of the proposed smart sensor.

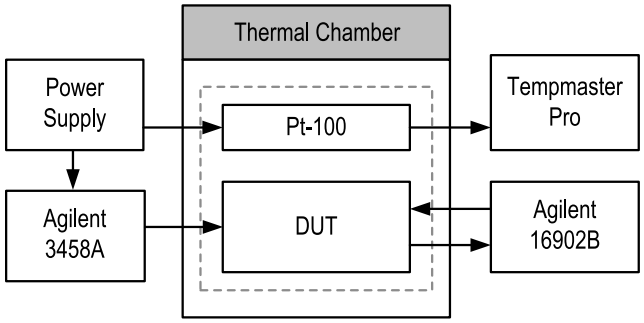

Fig. 10. Illustrative diagram of the measurement setup.

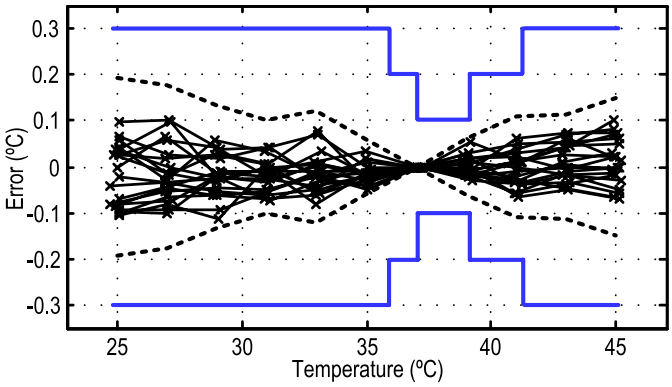

Fig. 11. Measured inaccuracy from 20 chips samples after one-point calibration at 37 °C. Bold dashed lines indicate the $\pm 3\sigma$ values, while blue solid lines show the accuracy requirement from [1].

Similarly, $(k_4 V_{BE} - \alpha k_3 \Delta V_{BE})$ is integrated in the discharging phase. The output of the integrator is then fed to the input of the comparator for bs evaluation. The output bs is then processed to obtain the instantaneous temperature. One-point digital calibration is exploited to tackle the variation V_{BE} due to BJT process spread.

VI. MEASUREMENT RESULTS

This proposed smart temperature sensor is implemented in a standard 0.18μm CMOS process, occupying an active area of 0.198 mm^2. Fig. 9 shows the die microphotograph. With the analog and digital supply set to 1V and 1.8V respectively, the sensor dissipates a measured power of 1.1μW (0.9 μW from 1 V supply and 0.2μW from 1.8 V supply) at 37 °C with a conversion rate of 2 Sa/s.

Fig. 10 shows the measurement setup. The device under test (DUT) is characterized using a thermal chamber (SU-261, ESPEC). During measurement, the DUT is placed next to a reference sensor (platinum Pt-100 resistor) inside a metal box which serves as a thermal low-pass filter. The Agilent Modular Logic Analyzer System 16902B is employed for input pattern generation as well as to monitor and analyze the temperature data, which is directly compared with the reading from the thermal meter (Tempmaster PRO) the processor outputs. Both the reference sensor and thermal meter are calibrated to achieve a ±0.05 °C accuracy. Power consumption is measured using Agilent 3458A. The sensor is calibrated at 37 °C with the sensing error estimated using a linear master curve.

Fig. 11 shows the measured temperature error from 25 °C to 45 °C using 20 sample chips after one-point calibration at 37 °C. It can be observed that an inaccuracy of ±0.1 °C(3σ) is obtained from 37 °C to 39 °C (±0.2 °C from 25 °C to 45 °C). The maximum error tolerance for human body temperature monitoring [1] is also indicated (blue bold line). It can be concluded that the temperature sensor achieves an accuracy which is well within the specification, making it suitable for human body temperature monitoring applications. Table III shows the performance comparison of our proposed temperature sensor with the state of the art. The proposed work achieves high accuracy using only one-point calibration. The application specific sampling rate is designed to not only reduce the sensor power, but also relax the back-end processing and wireless power. When compared with [2]

which requires two-point calibration for each of the 3 measured samples, the proposed temperature sensor achieves high sensing accuracy (3σ) from 20 measured chip samples while using only one-point calibration.

VII. Conclusions

This paper has presented an ultra-low power, high accuracy CMOS smart temperature sensor based on substrate BJT and a first-order I-ADC with a multi-ratio pre-gain stage and BDWA to relax the ADC resolution requirement and the routing complexity. An inaccuracy of ± 0.2°C (3σ) is achieved after one-point calibration at normal human body temperature while the power consumption is only $1.1\,\mu$W, which is suitable for passive temperature sensing systems of clinical temperature monitoring applications.

References

[1] *Standard Specification for Electronic Thermometer for Intermittent Determination of Patient Temperature*, Standard ASTM E1112, 2011.

[2] A. Vaz *et al.*, "Full passive UHF tag with a temperature sensor suitable for human body temperature monitoring," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 2, pp. 95–99, Feb. 2010.

[3] M. K. Law, A. Bermak, and H. C. Luong, "A sub-μW embedded CMOS temperature sensor for RFID food monitoring application," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1246–1255, Jun. 2010.

[4] Y. S. Lin, D. Blaauw, and D. Sylvester, "An ultra low power 1 V, 220 nW temperature sensor for passive wireless applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 507–510.

[5] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.

[6] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Procedia Eng.*, vol. 5, pp. 930–939, Sep. 2010.

[7] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ± 0.15 °C (3σ) from -55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[8] M. A. P. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Dordrecht, The Netherlands: Springer, 2006.

[9] M. A. P. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.5 °C from -50 °C to 120 °C," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 454–461, Feb. 2005.

[10] O. Feely and L. O. Chua, "The effect of integrator leak in Σ-Δ modulation," *IEEE Trans. Circuits Syst.*, vol. 38, no. 11, pp. 1293–1305, Nov. 1991.

[11] A. L. Aita and K. A. A. Makinwa, "Low-power operation of a precision CMOS temperature sensor based on substrate PNPs," in *Proc. IEEE Sensors*, Oct. 2007, pp. 856–859.

[12] K. Souri and K. A. A. Makinwa, "A 0.12 mm^2 7.4 μW micropower temperature sensor with an inaccuracy of ± 0.2 °C (3σ) from -30 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1693–1700, Jul. 2011.

[13] Z. Shenghua and W. Nanjian, "A novel ultra low power temperature sensor for UHF RFID tag chip," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2007, pp. 464–467.

[14] M. K. Law and A. Bermak, "A 405-nW CMOS temperature sensor based on linear MOS operation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 12, pp. 891–895, Dec. 2009.

[15] A. L. Aita, M. A. Pertijs, K. A. A. Makinwa, J. H. Huijsing, and G. C. M. Meijer, "Low-power CMOS smart temperature sensor with a batch-calibrated inaccuracy of ± 0.25 °C ($\pm 3\sigma$) from -70 °C to 130 °C," *IEEE Sensors J.*, vol. 13, no. 5, pp. 1840–1848, May 2013.

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