Generalized Circuit Techniques for Low-Voltage High-Speed Reset- and Switched-Opamps

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***Abstract*—This paper presents several comprehensive and novel circuit techniques that can be efficiently applied to low-voltage (LV) high-speed reset-opamp (RO) and switched-opamp (SO) in LV switched-capacitor circuits. The first, designated as virtual-ground common-mode (CM) feedback with output CM error correction, allows the design of fully differential RO circuits that could only be traditionally implemented before in pseudo-differential mode, and it leads to considerable savings of half of the opamps' power. The second, uses a crossed-coupled passive sampling interface to avoid the extra track-and-reset stages as required in both RO and SO circuits, further saving one front-end opamp's power. The third, employs a voltage-controlled level-shifting (LS) technique that utilizes the charge redistribution property to process the CM LS in an LV environment, avoiding the degradation of the feedback factor by the use of extra LS circuits. Finally, the fourth, the LV finite-gain compensation technique allows the use of low-gain high-speed single-stage amplifier in contrast to the conventional high-gain, low-speed two-stage opamp to achieve a high-speed operation in both RO and SO circuits. Without any clock boosting or bootstrap circuits, all of the above techniques can be applied in LV applications without any floating switches limitations. Measurement results of a 1.2-V 10-bit 60 MS/s pipelined analog–digital converter in 0.18-μm CMOS with RO are presented to verify the effectiveness of the proposed techniques, achieving a signal-to-noise distortion ratio of 55.2 dB with 85-mW power consumption.**

***Index Terms*—Common-mode feedback (CMFB), finite-gain compensation (FGC), low voltage (LV), reset-opamp (RO), switched-capacitor (SC) circuits, switched-opamp (SO).**

I. Introduction

LOW-VOLTAGE (LV) designs continue to play important roles, as well as creating challenges, in modern analog and mixed-signal integrated circuits (IC) that are expected to operate under low supply voltage. This is either due to the technology scaling into sub-100 nm CMOS, or in the context of low-power battery-operated devices that force the ICs to function under the nominal supply voltage at the specific technology node [1]–[7]. Both situations create stringent requirements in analog and mixed-signal IC designs due to low-supply voltage headroom, especially when the supply voltage is lower than the nominal value of that technology, e.g., an analog IC designed in 0.18-μm CMOS must tolerate the reduced voltage headroom of a 1.2-V supply voltage while it cannot benefit from smaller parasitics and higher speed of more advanced CMOS technologies, like 130 or 90 nm.

Designing switched-capacitor (SC) circuits in an LV environment is especially problematic when comparing it with other analog circuits due to the large dependency on the operation of the switches. Floating switches that are designed to pass signals with large swings cannot be turned on [4], but, even if they can be switched on, a large distortion will appear as a result of signal-dependent on-resistance imposed by very small gate overdrive voltage as expressed in (1), for nMOS transistors

$$R_{\rm on} = \frac{1}{\mu_n C_{\rm ox}\left(\frac{W}{L}\right)\left(V_{\rm DD} - V_{\rm in} - V_{\rm th}\right)} \tag{1}$$

where $R_{\rm on}, \mu_n, C_{\rm ox}, W/L, V_{\rm DD}, V_{\rm in}$, and $V_{\rm th}$ represent the on-resistance, mobility, oxide unit capacitance, transistor aspect ratio, supply voltage, input voltage and threshold voltage, respectively. To alleviate the problems of floating switches, two state-of-the-art techniques, namely reset-opamp (RO) [2], [4]–[6] and switched-opamp (SO) [1], [3], [7], [8] are available in modern LV designs. These two techniques do not require generation of on-chip high voltage therefore they are truly compatible with future LV deep-submicron CMOS processes.

While both RO and SO can be utilized to avoid the floating switches at the opamp output nodes, many design challenges still exist in the LV environment, resulting in overall performance degradation when compared to a conventional design. The virtual-ground (VG) common-mode (CM) level of the opamp is always biased near the supply rails in LV operation, while the opamp output CM level is usually biased at the middle of the supply rails to maximize the output swing. The difference between the and output CM level requires an extra level-shifting (LS) circuit [2] which can degrade the feedback factor and thus the speed performance. Furthermore, the absence of floating switches still prevents the usage of many useful conventional circuit techniques. Firstly, the traditional CM feedback (CMFB) circuit [9] which is necessary in the implementation of fully differential opamps cannot be applied. To overcome this problem well established SO techniques are available [1], [10], however for RO circuits no truly CMFB circuit is available to allow fully differential operation (for instance the CMFB circuits from [2], [4], [11] can only be applied in pseudo-differential circuits, i.e., two single-ended opamps instead of a fully differential one). Secondly, both the

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RO and SO techniques rely on the previous stage's opamp to be reset/switched off, which will create problems in the foremost front-end stage (that directly coupling with the continuous-time input signal). As a result, traditional active solutions require extra front-end track-and-reset (T/R) stages [12]–[14], while a passive solution creates a continuous-time signal feedthrough problem [1]. Finally, traditional finite-gain compensation (FGC) techniques, such as correlated double sampling (CDS) [15], cannot be applied due to the unavailability of floating switches, imposing the utilization of two-stage opamps to achieve enough gain with low-speed in LV designs. In addition to the previous drawbacks, the limitation to utilize conventional circuits also places a large penalty on the overall performance (power or/and speed) of RO and SO circuits when compared to traditional designs, due to the impossibility of applying various useful design techniques such as double sampling [16] and opamp sharing [17], as well as difficulties induced by architectural constraints, e.g., the degradation of the feedback factor.

This paper serves two purposes: initially, it summarizes comprehensively these four kinds of advanced LV problems, namely CMFB, input interface, LS and FGC; finally, it proposes solutions for simultaneously achieving LV, power efficient, high-speed operation for both RO and SO circuits. Section II starts with a detailed description of CMFB implementation difficulties. This will be followed by the presentation of the VG-CMFB technique, as a solution to use fully differential opamps and to save half of the opamp power [18]. Based on this initial idea, a novel output CM error correction (O-CMEC) circuit will also be proposed in this paper to correct the output CM accumulation error in integrators or consecutive gain-stages [e.g., in pipelined analog–digital converter (ADC)] for high-speed operation. Session III continues to address the problems arising in the input front-end interface, and a crossed-coupled passive sampling interface (CCPSI) is introduced as a solution, thus eliminating the need for power-hungry active front-end T/R stage and the unwanted continuous-time direct signal feedthrough [19]. The analysis here is further extended to include the influence of capacitor matching in the feedthrough cancellation performance of crossed-coupling branches. Then, in Section IV details for LV LS will be discussed together with the inefficient existing solutions, paving the way for the introduction of a novel solution, namely the voltage-controlled LS (VCLS) that will lead to improved speed performance. Finally, in Section V the LV-FGC technique will be presented, which uses a low-gain single-stage amplifier to achieve high-speed operation [20], and in this paper an extensive and additional mathematical analysis on the effect of the feedback factor mismatch will be further provided. In Section VI, chip measurement results of an RO 1.2-V 10-bit 60 MS/s pipelined ADC will be given as an example to demonstrate and verify the effectiveness of the proposed techniques, followed by the Conclusions drawn in Section VII. The novel techniques here proposed have been generalized and they can be effectively applied to both RO and SO SC circuits, including integrators in sigma-delta converters, sample-and-hold (S/H) and multiplying digital-to-analog converters (MDACs) used in pipelined ADCs. The first two techniques are concentrated

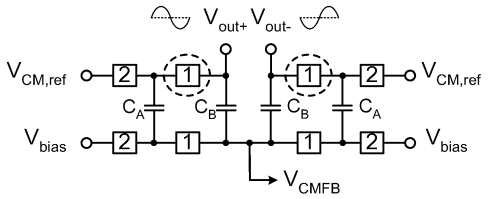

Fig. 1. Traditional SC-CMFB circuit.

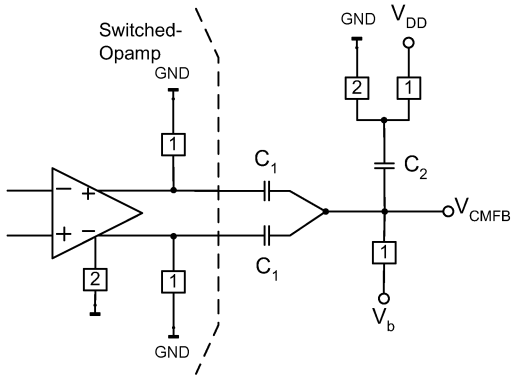

Fig. 2. SC-CMFB circuit used in SO [1].

in power consumption reduction while the last two target high-speed operation. For simplicity, the forthcoming analysis will utilize RO S/H, amplifier and MDAC circuits for demonstration purposes.

II. VG-CMFB AND O-CMEC

A. LV CMFB Design Challenges

Designing CMFB for a fully differential circuit constitutes a great challenge in an LV environment. Fig. 1 shows a traditional SC-CMFB implementation [9] that is widely used in conventional SC circuits. In the presence of a large voltage swing in both $V_{\text{out}+}$ and $V_{\text{out}-}$, the floating switches (inside the dashed circles) connected to these two output nodes cannot be easily turned on.

In the context of SO circuits [1], [3], [7], [8] the opamps are switched off in one phase to produce an high-impedance state in the opamp output, thus allowing it to be pulled up to a well- defined voltage (typically supply or ground potential, but other fixed potential can also be used) as shown in Fig. 2, [1]. This allows resetting the capacitor C_1 in the SC-CMFB circuit and thus the CM voltage in the next phase can be controlled by those well-defined voltages in a similar way as in traditional SC-CMFB techniques, then permitting fully differential implementation of SO circuits.

The same principle cannot be applied to the RO architectures [2], [4]–[6] where the opamps are reset in an unity-gain configuration to discharge the next stage sampling capacitors. This operation produces a well defined 0-V differential mode resetting voltage, but the CM output at this phase is still undefined without the use of any CMFB. Due to the lack of such well-defined resetting voltage in the reset phase, the CMFB circuit from Fig. 2 cannot be utilized. Currently, all RO techniques employ pseudo-differential opamps [2], [4]–[6] (which actually are two single-ended opamps) as it is exemplified by the RO SC

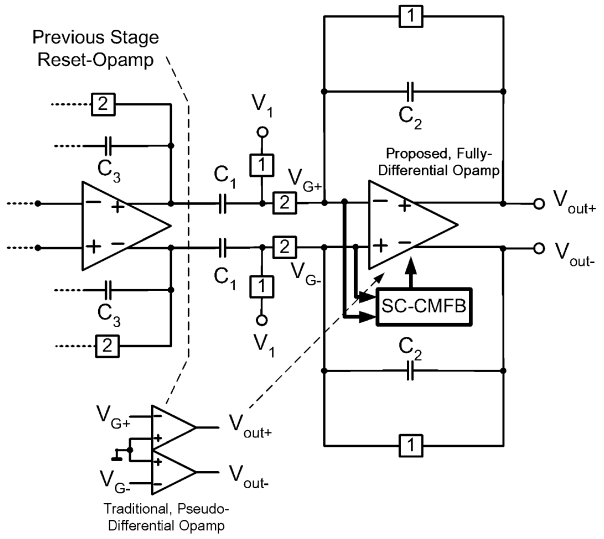

Fig. 3. LV SC amplifier circuit using fully differential RO.

amplifier circuit (which can be used as an S/H or an MDAC) from Fig. 3 in order to stabilize the opamp output CM voltage in both phases. However, it implies doubling the number of opamps as well as the corresponding power consumption. Furthermore, single-ended opamps are slower than their fully differential counterparts due to the additional current-mirror pole created by the differential-to-single-ended converter.

B. Novel VG CMFB Technique

Instead of directly controlling and stabilizing the output CM voltage, the same purpose can be achieved indirectly by controlling the VG CM voltage [18], and this possibility will be addressed here first before a solution is presented. As shown in Fig. 3, the previous stage RO circuit resets at phase 2 to discharge the sampling capacitors C_1, while in phase 1 the stage resets itself to a level of $V_{G,\mathrm{CM}}$ to discharge the next stage sampling capacitors, where $V_{G,\mathrm{CM}} = (V_{G+} + V_{G-})/2$. It is assumed that the previous stage RO is similar to the current stage, also resetting at $V_{G,\mathrm{CM}}$, and having an output CM voltage of $V_{\mathrm{in,CM}}$ in amplification mode (i.e., phase 1), which is actually the input CM voltage in the current stage. A simple mathematical relationship between various signal's CM level in phase 2 can be easily derived as follows:

$$V_{\mathrm{out,CM}}[\phi 2] = \frac{C_1}{C_2} V_{\mathrm{in,CM}} + V_{G,\mathrm{CM}} - \frac{C_1}{C_2} V_1 \qquad (2)$$

where V_1 is a known fixed potential that can be used to achieve the LS function (please see Section IV for detailed analysis). Assuming $V_{\mathrm{in,CM}}$ has a known voltage value (as in the usual case which is set by the previous stage), (2) possesses two unknown variables $V_{\mathrm{out,CM}}[\phi 2]$ and $V_{G,\mathrm{CM}}$, i.e., only one constraint equation derived from the external SC networks. If a CMFB circuit (implying another constraint equation) is applied such that either $V_{\mathrm{out,CM}}[\phi 2]$ (the traditional output CMFB) or $V_{G,\mathrm{CM}}$ (the proposed VG-CMFB) are defined, then the other unknown variable can also be determined. This simple equation clearly shows how the control of the VG CM voltage can lead to the stabilization of opamps' output CM level, and in this way, the pseudo-differential opamp-pair in Fig. 3 can be replaced by one fully differential opamp, thus saving half of the power consumption. Notice also that the target value of the $V_{G,\mathrm{CM}}$ should be set with a voltage potential in the order of 0.1–0.3 V away from the supply rails, such that the opamp's output transistors always remain in the saturation region during the reset phase for high-speed operation. If biasing of $V_{G,\mathrm{CM}}$ to V_{DD} or ground is necessary, then an SC floating battery must be utilized [2].

Compared with the traditional output CMFB control, the proposed method can be easily implemented in a LV environment because: 1) the signal swing in the VG is much smaller than the one in the output of the opamps due to the opamp's differential gain, thus alleviating the floating switch problem; 2) the output CM level is usually different in the two phases of LV circuits and thus also difficult to be controlled, while the VG is usually fixed in both phases to allow a suitable biasing of the input differential pair. However, stabilizing the output CM by controlling the VG CM level is not as accurate as the traditional output CMFB method, since any inaccuracy in the VG CM voltage will be amplified by $1/\beta$ to the output CM voltage (with β as the feedback factor), and the CM charge injection error will also appear, both leading to output CM errors. On the other hand, these type of CM errors can be easily accumulated (e.g., in the integrating capacitors of SC integrators or pipelining stages). Since the CM output voltage is not required to be so accurate as the differential mode signal the proposed technique can be utilized alone in low-speed (with small switch sizes leading to smaller charge injection errors) or in small number of pipelining stages (where the CM error accumulation does not saturate the last-stage's opamp). While in high-speed circuits the CM error accumulations become significant (due to larger switches), as well as in integrators, this technique can be combined with the novel O-CMEC, as discussed later, to achieve an accurate output CM error control.

C. Practical Implementation of VG-CMFB

Fig. 4 shows the proposed VG-CMFB technique [18], including the differential pair in the main opamp and the reference generation circuit. In addition to the normal transconductance operation, the differential pair of an opamp can also serve as a VG CM voltage detector, requiring no extra CM detector circuits. As the CM bias currents of M1A and M1B are set by the tail current source M0 of the differential pair, then $V_{\mathrm{GS1}A,\mathrm{CM}} = V_{\mathrm{GS1}B,\mathrm{CM}} = V_{\mathrm{GS1,CM}}$ are kept unchanged and the differential pair reproduces the shifted version of the VG CM voltage at $V_{\mathrm{tail}} = V_{G,\mathrm{CM}} - V_{\mathrm{GS1,CM}}$. The reference generation circuit is a scaled-down version of the differential pair thus simulating its biasing condition and also reproducing $V_{\mathrm{tail,ref}} = V_{G,\mathrm{ref}} - V_{\mathrm{GS}B1}$, in which $V_{G,\mathrm{ref}}$ represents the desired VG potential. Since the reference is generated and the VG CM level has also been detected and represented through V_{tail}, conventional SC-CMFB circuit techniques can be employed. V_{CMFB} has a similar meaning as in conventional SC-CMFB which could be applied to the gate of one pair of current source transistors in the main opamp, providing adjustment of the output CM level, and also through the connection of an external SC network to the VG CM potential. V_{bias} is the nominal bias value of V_{CMFB}. Also, all the switches in Fig. 4 can be easily turned on since no

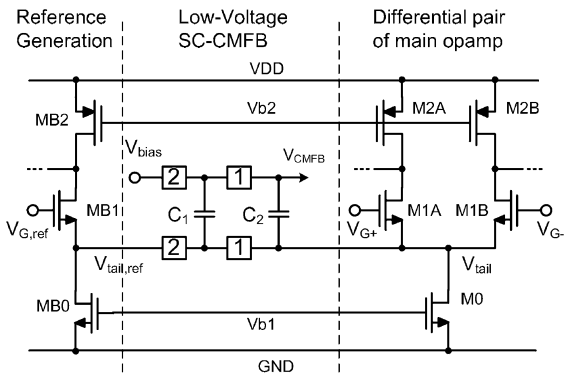

Fig. 4. Proposed VG CMFB technique.

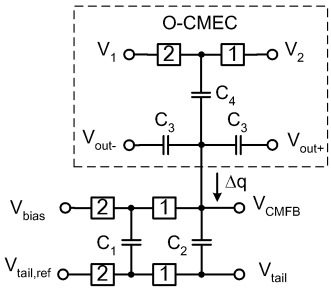

Fig. 5. Proposed O-CMEC circuit.

signal swings are presented in any nodes of the SC-CMFB circuit (thus can be biased near the supply rails).

D. Output CMEC

As discussed previously, the VG-CMFB technique controls the VG CM potential and through the external passive network stabilizes the output CM level. Then, any errors entering the external passive network (e.g., charge injection) can affect the output CM voltages, and the errors can be easily accumulated in the integrators or pipelining stages. When these errors become relevant the VG-CMFB technique can be enhanced further through the combination with a novel O-CMEC technique, also proposed here and shown in Fig. 5. This circuit is an improved version of the pseudo-differential implementation from [2]. If the output CM voltage is at the desired value, then the net charge Δq injected to $V_{\rm CMFB}$ node by the O-CMEC will be cancelled out, while any output CM deviation will imply a correction charge by the negative CMFB loop. For example, if a CM error is injected into the external feedback network, and the output CM voltage of the opamp, in phase 2 of Fig. 3, is being pulled down from the designed value (normally the mid-supply). Then, referring to Fig. 5, $V_{\rm out,CM}$ will be pulled down, disturbing the equilibrium and resulting in a negative charge Δq injected into the $V_{\rm CMFB}$ node. This action will pull down the node voltage $V_{\rm CMFB}$ leading the output CM voltage to be pulled up by the CM gain (since the CMFB must be designed as negative feedback loop). The Appendix describes in detail the operating principle of the $\rm VG-CMFB+O-CMEC$ technique and presents also the derivation of the following design equation for selection of the capacitor values:

$$V_{\rm out,CM}[\phi 1] - V_{\rm out,CM}[\phi 2] = \frac{C_4}{2C_3}(V_2 - V_1) \qquad (3)$$

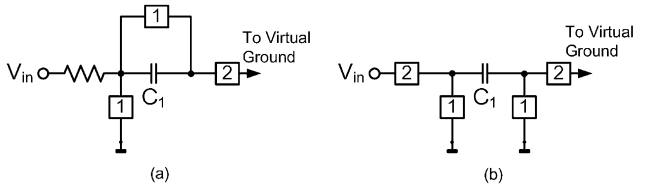

Fig. 6. (a) LV passive sampling circuit [14]; (b) a non-inverting, non-delay SC branch.

meaning that the capacitor ratio depends on the difference of the output CM voltage in the two phases and also the reference voltages V_1 and V_2 that can be either $V_{\rm DD}$ or ground.

Compared with the implementation from [2], the proposed technique offers the following improvements: (a) combined with the VG-CMFB circuit it is designed for fully differential opamps, instead of being only applied to the pseudo-differential mode as in [4]; (b) only one correction circuit is required here, while two circuits were required in the previous implementation [4]; (c) the O-CMEC injects charges into $V_{\rm CMFB}$ node which is an internal node of the CMFB loop, and this only reduces the CMFB factor and does not affect the differential-mode feedback factor. From [2] the injection point is the VG of the main opamp which will degrade both feedback factors thus leading to speed penalties. However, the O-CMEC circuit cannot be used independently since the VG-CMFB imposes the near-steady-state operating point of the output CM level first and only after that the output CM error can be corrected by O-CMEC.

III. Input Interfacing With CCPSI

A. Problems in Existing Solutions

Both RO and SO circuits rely on the precedent stage opamps, which simulate floating switches, to discharge the sampling capacitors. This creates a difficulty in the foremost front-end stage that directly interfaces with the input continuous-time signal. As a result, extra efforts must be devoted to design the front-end input sampling circuits. Several input interfaces have been already proposed before in both RO and SO circuits [1], [5], [12]–[14], [21] and one of such from [14] is presented in Fig. 6(a). In the figure a resistor is utilized as voltage divider during the resetting phase, thus allowing the discharge of the sampling capacitor. This passive circuit cannot be imbedded into normal SC front-end building blocks (e.g., S/H) because this interface actually simulates the normal non-inverting, non-delay SC branch (Fig. 6(b)) and, when combined with the opamp it can only provide a T/R output for the continuous-time input signal of Fig. 7 (and thus being an extra T/R stage, in addition to the S/H that normally is required). Similar techniques are also used in [5], [12], [13] where the input interface is actually an active inverting resistive amplifier, again implementing only the T/R function. An extra T/R stage not only consumes one extra front-end opamp's power, but it will also place severe limitations on the noise, linearity and speed, since the performance of such T/R is directly linked to the full resolution (or dynamic range) of the whole system.

Passive sampling interfaces also exist [1], [6], [21] that simulate the usual inverting, half-delay SC branches, thus allowing truly S/H/R waveforms (as shown in Fig. 7) and then it can be imbedded into normal front-end SC building blocks. However, extra clock phases are needed [1] and most importantly, direct

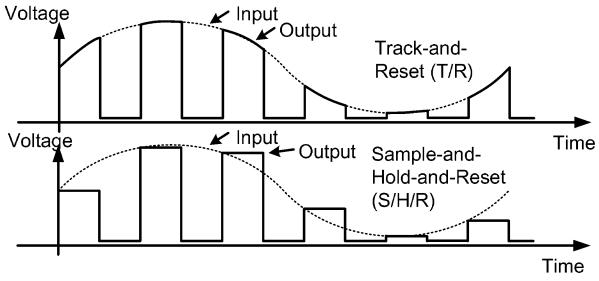

Fig. 7. T/R versus S/H-and-Reset (S/H/R).

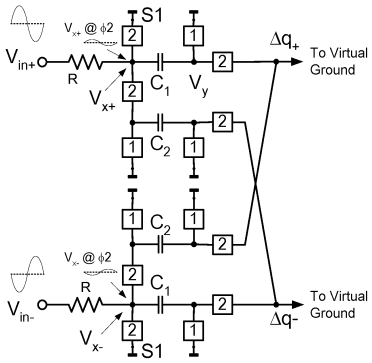

Fig. 8. Proposed LV CCPSI circuits.

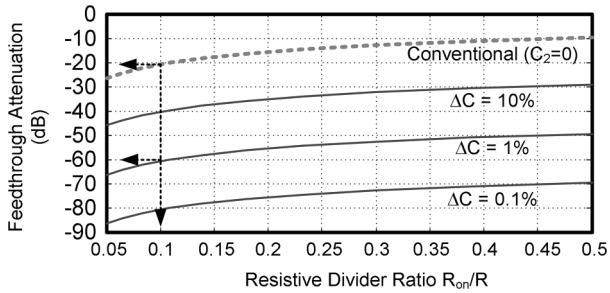

Fig. 9. A plot of signal feedthrough attenuation versus $R_{\rm on}$ and capacitor mismatch in C_1 and C_2.

signal feedthrough from continuous-time input to output can occur during the amplification phase [1], [6], [21]. To suppress such signal feedthrough some limitations are also placed on the size selection of various component values including switches and resistors. For example, to suppress the signal feedthrough, the value of the resistor must be large to form a high-ratio resistive divider with the switch on-resistance, and this will place large limitations on the sampling time constant and degrades the operating speed [6]. Also in [21], the signal feedthrough can be greatly suppressed by cascaded sampling network, with the trade-off of increasing series resistance during the sampling phase thus lowering the sampling bandwidth.

B. CCPSI

Fig. 8 shows the proposed low voltage CCPSI circuits (in differential configuration) [19] as a remedy for the drawbacks previously discussed. When compared with the sampling circuit from Fig. 6, this circuit is equivalent to the common inverting, half-delay SC branch. The resistor R (similarly as in Fig. 6) provides resistive division with the on-resistance of switches S1 and it will also allow the discharge operation of the sampling capacitor C_1 in phase $\phi 2$. An extra pair of capacitors C_2 is added, each with the same size of C_1. The circuit operates as follows: In phase $\phi 1$, the differential signal will be sampled by the capacitor pair C_1, while the capacitor pair C_2 is reset; In phase $\phi 2$, the switches S1 are turned on and form a voltage divider with the resistors R, thus the signal swing on nodes $\mathrm{V}_{x+}, \mathrm{V}_{x-}$ will be attenuated and all the switches connected to these nodes can now be easily turned on. In this phase the capacitor pair C_1 is discharged between the VG of the opamps and the attenuated signal, causing direct signal feedthrough interference in the charge transferring phase. The capacitor pair C_2 is now used to eliminate it since C_2 is connected between the VG and the attenuated signal in the opposite differential path. If $C_1 = C_2$, then the signal feedthrough will be cancelled and only the differential charge sampled in C_1, in phase $\phi 1$, is transferred to the VG.

A simple quantitative analysis of the differential charge transfer during phase $\phi 2$ in the circuit from Fig. 8 yields

$$\Delta q_+ - \Delta q_- = -C_1 V_{\rm in}[\phi 1] - \frac{R_{\rm on}}{R + R_{\rm on}} \times (C_2 - C_1) V_{\rm in}[\phi 2] \quad (4)$$

where $\Delta q_+ - \Delta q_-$ represents the amount of differential charge transferred to the VG at the end of $\phi 2$, $R_{\rm on}$ the on resistance of the switches S1, $V_{\rm in} = V_{\rm in+} - V_{\rm in-}$ the differential input signal, and $V_{\rm in}[\phi 1]$ the input signal at the end of $\phi 1$. From (4) it can be observed that the differential signal feedthrough will appear during $\phi 2$, but it will be cancelled if $C_1 = C_2$ through a cross-coupling action of the passive sampling branch. To gain a deeper insight on the effectiveness of the feedthrough cancellation mechanism, Fig. 9 shows a plot of the direct signal feedthrough attenuation (in dB) versus the resistive divider ratio on $R_{\rm on}/R$ and the mismatch in C_1 and C_2, compared with the conventional techniques (equivalent to $C_2 = 0$) [6]. This plot shows, for example, that even with moderate resistive divider ratio (e.g., 0.1) and capacitor matching (1%), the proposed circuit still provides high signal feedthrough attenuation (-60 dB) compared with the conventional structure (-20 dB only). To further demonstrate the effectiveness of the circuits in Fig. 8, Table I shows the performance comparison of the S/H circuit with and without the crossed-coupled capacitor C_2. The CCPSI circuit shows a superior signal feedthrough attenuation with the trade-off of reduced speed and a little-bit increased circuit noise (Assume 1.2 $V_{\rm pp}$ differential signal swing, see Appendix 2 for the analysis of the noise), due to the main reason of the extra capacitor and the reduced feedback factor.

The on resistance $R_{\rm on}$ of switches S1 depends on the gate-source voltage and then on V_{x+} and V_{x-}, modulating the voltage on those nodes by voltage division which causes harmonic distortion in phase 2. However, the proposed circuit is insensitive to such distortion because the produced even harmonics will be cancelled by fully differential operation, while those odd harmonics are cancelled by the action of the cross-coupled sampling branch, since they are similar to the attenuated signal feedthrough, and, only the differential input signal charges sampled in C_1 during phase 1 are transferred. In addition, the proposed circuit only needs simple two-phase clocking, and also the signal feedthrough will be cancelled provided that C_1 matches C_2 and the size of switches S1 are chosen such that S1 can

TABLE I
PERFORMANCE COMPARISON OF THE SAMPLING CIRCUITS FROM FIG. 8 WITH AND WITHOUT C_2

Case	Target Resolution	Value of C_2	Feedback Factor	Sampling capacitor	Capacitor Matching[2]	Normalized Speed	Normalized Thermal Noise	Signal to Noise	Signal to Feedthrough[3]	Signal to (Feedthrough+Noise)
1	10	$C_2 = C_1$	0.33	500fF	0.3%	8	12	62dB	70dB	61.5dB
2	10	$C_2 = 0$	0.5	500fF	0.3%	12	8	64dB	20dB	20dB
3	12	$C_2 = C_1$	0.33	4pF[1]	0.1%	1	1.5	71dB	80dB	70.6dB
4	12	$C_2 = 0$	0.5	4pF[1]	0.1%	1.5	1	73dB	20dB	20dB

[1]For 2-b increased resolution, the capacitor sized should be increased by a factor of 16, however 4pF is chosen here to reduce the power consumption.
[2]Extracted from the foundry datasheet. [3]Extracted from Fig. 9 with $R_{on} / R = 0.1$.

be turned on. This greatly relaxes the limitations of component values selection found before in [1], [6]. Also, since the input signal is sampled in phase $\phi 1$ while charge transfer is performed in phase $\phi 2$, the sampling circuit simulates the normal inverting, half-delay SC branches which can provide S/H/R output with reset- or SO, since the input continuous-time signal is decoupled in the charge transferring phase. This implies that the circuit can be imbedded in normal SC building blocks such as S/H and integrators, eliminating the need of additional T/R stages and thus reducing power consumption. Although extra passive components (capacitors C_2) are added, the proposed circuit consumes lesser area and power compared to other implementations since the added passive component is used to trade with the whole extra T/R stages that contain more passive components as well as one extra opamp. A drawback of the proposed circuit is its reduced feedback factor which would impose speed limitations, when compared with previous designs, because one additional pair of capacitors is connected to the opamp VG.

IV. VCLS

Handling CM voltage in LV designs is not as simple as in traditional circuits since the CM voltage at the VG of the opamp is usually biased near $V_{\rm DD}$ or ground for the proper operation of the input differential-pair, while the CM voltage at the opamp's output is usually at the midsupply to maximize the output swing. Also, due to the nature of RO and SO circuits the output CM level between two phases can be quite different. Such CM level difference originates the need for LS circuits [2] which can be implemented by an SC branch connected to the VG of the opamp to provide a constant dc charge per every clock cycle. However, this method brings along a speed penalty as an SC branch connected to the VG of the opamp degrades the feedback factor.

To avoid such disadvantage a novel technique is proposed here that can be designated as VCLS, which achieves the required LS through simple charge-redistribution principles. The operation principle can be demonstrated by considering again the RO S/H from Fig. 3 together with (2) that presented the dependence of the output CM voltage with the input CM level, VG CM level and the fixed potential V_1. Actually the last term in (2) already inherently provides the required LS function through the controlling voltage V_1, thus not requiring the extra LS SC branch and allowing higher speed of operation. For example in Fig. 3 with $C_1 = C_2$, if we choose $V_{\rm out,CM}[\phi 2] = V_{\rm in,CM} = 0.6$ V under $V_{\rm DD} = 1.2$ V, and $V_{G,\rm CM} = 0.9$ V for proper operation of opamp with nMOS differential pair, then V_1 should be chosen as $V_1 = 0.9$ V from (2).

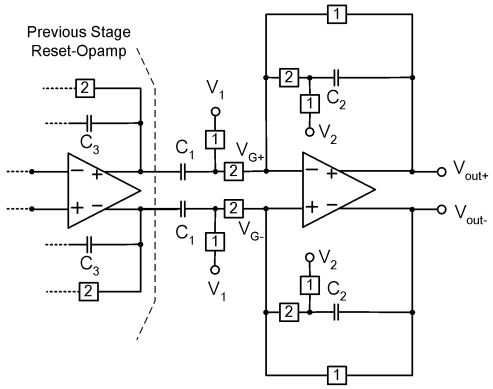

Fig. 10. Alternative for RO amplifier circuit.

Sometimes this technique cannot be directly applicable with some specific circuit configurations simply due to the improper value of V_1 in a LV environment, such as in the case of $V_1 > V_{\rm DD}, V_1 < {\rm GND}$ or V_1 near the midsupply leading to the floating switch difficulty. For example, considering Fig. 3 again with a gain-of-4 SC amplifier that will imply $C_1 = 4C_2$, and in this case V_1 would be calculated as 0.675 V, for a 1.2-V supply. In this case, the circuit can be rearranged to include more LS controlling potentials, as shown in Fig. 10. The functionality of this circuit is exactly the same as the one in Fig. 3, except that an extra LS controlling voltage V_2 has been added. The output CM voltage can now be evaluated as follows:

$$V_{\rm out,CM}[\phi 2] = \frac{C_1}{C_2} V_{\rm in,CM} + 2V_{G,\rm CM} - \left(V_2 + \frac{C_1}{C_2} V_1 \right). \quad (5)$$

The last term of the equation corresponds to the LS term and for the previous case with $C_1 = 4C_2$ it would be possible to choose $V_1 = 0.9$ V and $V_2 = 0$ V to achieve the required level-shift. Moreover, $V_{G,\rm CM}$ can also be adjusted to contribute to the level-shift, if necessary.

The proposed VCLS technique achieves the LS function without any extra SC branch connected to the VG, and even no modification of the original circuit is necessary except the change of the fixed potentials, then avoiding speed penalty when compared with the circuit from [2]. The drawback of this technique is the requirement for extra controlling voltages. However, in most applications the fixed potentials can be originated on the supply rails, and normally only 1 or 2 extra controlling voltages are required, as shown in the previous example, $V_1 = V_{G,\rm CM} = 0.9$ V implying that they can be obtained from the same voltage buffer. On the other hand, high accuracy of those controlling voltages is also not required since they only affect the CM output voltage.

V. LV-FGC

A. Need for FGC

In LV design,s the opamps are mainly restricted to traditional two-stage architectures [2], [18] (due to the impossibility of using cascode devices), which by their nature exhibit lower speed (due to the additional high-impedance node that needs miller compensation) and higher power consumption (more current branches). On the other hand, using single-stage opamps with low gain can cause serious systematic errors like nonlinearities in MDACs of pipelined ADCs or poles and zeros deviations in SC filters or sigma-delta modulators, unless the produced finite-gain error can be compensated, with, for example, traditional CDS techniques [15] and the buffer compensation technique [22]. However, they cannot be applied in a LV environment due to (a) limitations caused by floating switches problems and (b) by the fact that the opamp is switched-off or reset in one clock phase, which implies that it would not be idle and cannot be used to compensate the gain error. To overcome these drawbacks, a LV gain compensation technique was addressed before in [3] but it has also a restriction of narrowband operation (typically a bandpass sigma-delta modulator) that imposes a limitation to the signal band which must be located only and narrowly at $f_s/4$.

An LV-FGC technique is proposed for wide-bandwidth and high-speed circuits [20], and its analysis has been extended here in detail to include the investigation of the feedback factor mismatch effect. To illustrate the idea behind the LV-FGC technique it would be necessary to consider a LV RO MDAC used in a pipelined ADC, as shown in Fig. 11. Here, the upper part includes the usual main MDAC amplifier and only a single-ended version is shown for simplicity, although the real implementation is fully differential. Due to low supply voltage $V_{\rm ref}$ cannot be inserted directly into the signal path, and a reference injection circuit is used with a SC $C_{\rm ref}$ to inject the reference voltage into the VG, as in similar previous implementations [1], [4]. In phase 1, the input signal from the previous stage is sampled in C_{s1}, while in phase 2 the previous stage's opamp resets to discharge the sampling capacitor C_{s1} to VG. Again V_1 is a fixed potential that allows LS which does not affect the differential signal being processed and then it is not considered here (in Section VI the calculation to achieve the required level-shift will be addressed). Without considering the proposed auxiliary amplifier, it can be derived that the MDAC implements the following arithmetic function (considering only differential information signals and including the effects of input parasitic capacitance C_{P1} and finite gain A_1)

$$V_{o1} = \frac{C_{s1}}{C_{f1}} V_{\rm in} - mV_{\rm DD}\frac{C_{\rm ref}}{C_{f1}} + \frac{1}{\beta_1}\left(-\frac{V_{o1}}{A_1}\right) \tag{6}$$

where

$$\beta_1 = \frac{C_{f1}}{C_{s1} + C_{f1} + C_{\rm ref} + C_{P1}} \tag{7}$$

is the feedback factor and m would be equal to either 1, 0, or -1 depending on the sub-ADC decision. In the right-hand side of (6) the V_{o1} term will not be combined with V_{o1} in the left-hand side because the term

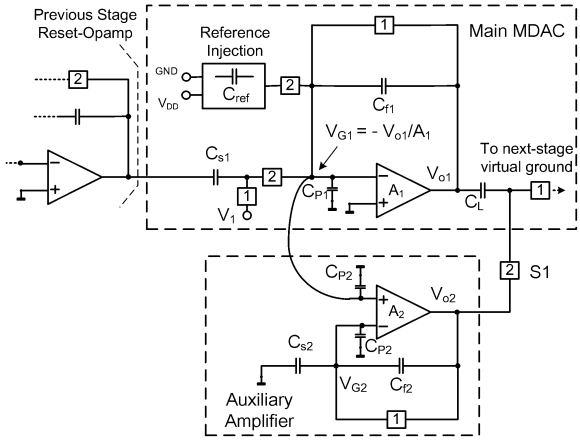

Fig. 11. Proposed FGC RO MDAC with main and auxiliary amplifier.

$$-V_{o1}/A_1 = V_{G1} \tag{8}$$

actually corresponds to the VG voltage of A_1 and it is clearly evident now that the VG error voltage is being amplified by the inverse of the feedback factor $(1/\beta_1)$ to the output, leading to a finite-gain error. As illustrated in Fig. 11, the fundamental idea of the proposed solution is to sense the main opamp VG voltage by an auxiliary amplifier in non-inverting configuration, amplify it by the same feedback factor, and then feed it into the bottom plate of C_L to cancel the gain error.

The output of the auxiliary amplifier can be derived as

$$V_{o2} = \frac{C_{s2} + C_{f2} + C_{P2}}{C_{f2}} V_{G2} = \frac{1}{\beta_2} V_{G2} \tag{9}$$

where

$$V_{G2} = V_{G1} - V_{o2}/A_2 \tag{10}$$

which means that the gain of the auxiliary amplifier will also contribute to the total gain error. Substituting (10) into (9) yields

$$\begin{aligned} V_{o2} &= \frac{1}{\beta_2} V_{G1} - \frac{V_{o2}}{\beta_2 A_2} = \frac{V_{G1}}{\beta_2[1 + 1/(\beta_2 A_2)]} \\ &= -\frac{V_{o1}}{\beta_2 A_1[1 + 1/(\beta_2 A_2)]}. \end{aligned} \tag{11}$$

Now for the main amplifier, the feedback factor should be modified in order to account for the input parasitic C_{P2} from the auxiliary amplifier

$$\beta_1' = \frac{C_{f1}}{C_{s1} + C_{f1} + C_{\rm ref} + C_{P1} + C_{P2}}. \tag{12}$$

Then the equivalent output voltage that is sampled into the capacitor C_L in phase 2 (Fig. 11) is

$$V_{o1} - V_{o2} = \frac{C_{s1}}{C_{f1}} V_{\rm in} - mV_{\rm DD}\frac{C_{\rm ref}}{C_{f1}} + \text{Gain error} \tag{13}$$

where the gain error can be evaluated as

$$\begin{aligned}\text{Gain error} &= \frac{1}{\beta_1'}\left(-\frac{V_{o1}}{A_1}\right) - \frac{-V_{o1}}{\beta_2 A_1[1+1/(\beta_2 A_2)]} \\ &= \left(-\frac{V_{o1}}{A_1}\right)\frac{\beta_2-\beta_1'+1/A_2}{\beta_1'\beta_2[1+1/(\beta_2 A_2)]} \\ &\approx \left(-\frac{V_{o1}}{A_1 A_2}\right)\frac{A_2(\beta_2-\beta_1')+1}{\beta_1'\beta_2} \end{aligned} \tag{14}$$

with the assumption of $\beta_2 A_2 \gg 1$. Also, supposing that a mismatch exists between β_1' and β_2 with $\beta_1' - \beta_2 = \Delta\beta, (\beta_1' + \beta_2)/2 = \beta, \beta_1' = \beta + \Delta\beta/2$ and $\beta_2 = \beta - \Delta\beta/2$, it implies that (14) can be simplified to

$$\begin{aligned}\text{Gain error} &= \left(-\frac{V_{o1}}{A_1 A_2}\right)\frac{1+A_2\Delta\beta}{\beta^2\left[1-\left(\frac{\Delta\beta}{2\beta}\right)^2\right]} \\ &\approx \frac{1}{\beta}\left(-\frac{V_{o1}}{A_1 A_2}\right)\left(\frac{1}{\beta}+A_2\frac{\Delta\beta}{\beta}\right) \\ &\approx \frac{1}{\beta}\left(-\frac{V_{o1}-V_{o2}}{A_1 A_2}\right)\left(\frac{1}{\beta}+A_2\frac{\Delta\beta}{\beta}\right) \end{aligned} \tag{15}$$

assuming $\Delta\beta/\beta \ll 1$ and $\beta A_1 \gg 1$ such that V_{o2} is small when compared with V_{o1} as indicated by (11). Comparing (15) with (6) it can be deducted that the effective gain can be expressed as

$$\text{Effective Gain} = \frac{A_1 A_2}{\frac{1}{\beta}+A_2\frac{\Delta\beta}{\beta}}. \tag{16}$$

If there is no mismatch between the two feedback factors, then $\Delta\beta = 0$ and the effective gain would have been boosted from A_1 to $\beta A_1 A_2$ by the proposed technique.

To achieve the proposed gain compensation, the feedback factor of both amplifiers should be matched as

$$\frac{C_{s1}+C_{\text{ref}}+C_{P1}+C_{P2}}{C_{f1}} = \frac{C_{s2}+C_{P2}}{C_{f2}}. \tag{17}$$

Note that C_{P1} and C_{P2} depend on the biasing condition of the differential pairs of both amplifiers. However, (17) can be easily satisfied by using the same sizes and biasing conditions for both of the input differential pairs (that makes $C_{P1} = C_{P2}$) and by choosing the following capacitor ratios:

$$C_{s1} + C_{\text{ref}} = 2C_{s2}, \quad C_{f1} = 2C_{f2}. \tag{18}$$

Alternatively, several choices satisfying (17) can be used, like for example a scaled-down version of the differential pair in the auxiliary amplifier, with the choice of the corresponding capacitor ratios also according to (17).

As indicated by (16), the mismatch between the feedback factors of the main and auxiliary amplifiers reduces the effective gain of the proposed technique. But, as it will be shown next, the mismatch-induced gain-reduction is not significant in the normal range of feedback factor mismatch values. A plot of the normalized effective gain (normalized to $\beta A_1 A_2$) vs $\Delta\beta/\beta$ is shown in Fig. 12 with $\beta = 0.23$ including the simulation result with a real opamp (described in detail in Section VI) that is provided here for verification purposes. The plot shows that the effective gain will be reduced as the feedback factor mismatch increases. For example, if we choose both of the opamp gains as 49 dB, the effective gain reduces from $\beta A_1 A_2 = 85$ dB with no mismatch to 81 dB for $\Delta\beta/\beta = 1\%$. Even for such large mismatch the proposed scheme still provides satisfactory performance compared with the one without gain-compensation. The reason for such insensitivity derives from the fact that the auxiliary amplifier is processing the main opamp gain error, as stated in (11), which has a relatively small magnitude in the order of a few millivolts (for instance, 10 mV), and the β mismatch (e.g., 1%) only causes negligible error (100 μV). In practice, the parasitic capacitance associated with the switches that are connected to VGs also contributes to mismatch in the feedback factor, and if this becomes a problem, dummy switches can be used to improve such type of matching. Also, the amount of gain reduction will also increase as the auxiliary amplifier gain increases due to the fact that as the effective gain error reduces (since the gain increases), the magnitude of the total gain error is reduced and thus it will be more sensitive to the mismatch of the feedback factor.

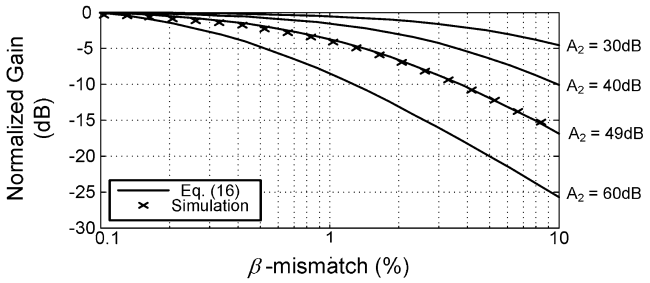

Fig. 12. Plot of normalized effective gain versus β mismatch.

In Fig. 11 a switch S1 is used in the auxiliary opamp output to disconnect C_L at phase 1, such that C_L can be discharged to the next stage VG. This switch can be turned on and off without any problem since the swing in the output of the auxiliary amplifier is quite small and can be set near the supply rails. Similarly, the nonlinearity produced by its on-resistance is also negligible.

Compared with the implementation presented in [22], the proposed technique also utilizes the auxiliary amplifier to sense the error voltage from the VG of the opamp, with the following advantages over that from [22] (the readers are referred to this reference for detailed discussion) : 1) the implementation in [22] cannot be used in LV environment due to the floating switches problem; 2) also in [22], the error signal needs to be fed into the subsequent stages for correction of the gain-error, which either leads to feedback factor degradation and thus to speed penalties (due to extra SC-branch injected to the next-stage VG) or to the requirement of extra "shadow" pipelined stages, adders, as well as analog delays which will increase the power consumption. The proposed scheme corrects the gain-error immediately in the current stage, avoiding extra injection to the VG and thus optimizing both the speed and the power consumption.

B. Auxiliary DDA

It might seem that the proposed technique will significantly increase the power consumption since an additional amplifier is needed. However, the additional power consumption can

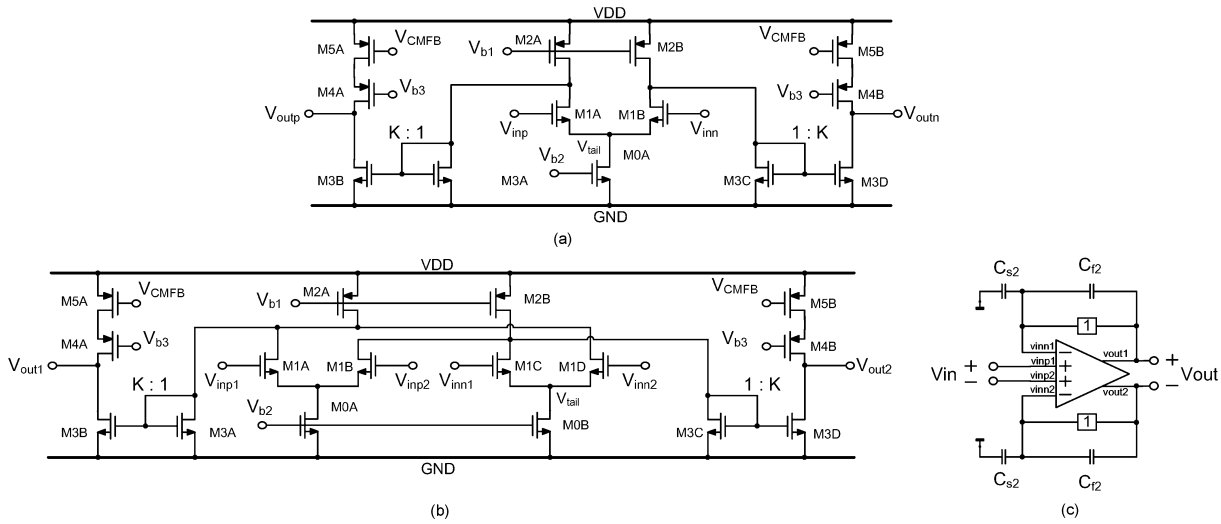

Fig. 13. Current mirror opamp topologies. (a) Main opamp. (b) A-DDA. (c) A-DDA used as noninverting amplifier.

be traded-off with the significant increase of the single-stage opamps' gain-bandwidth product (GBW). Moreover, fully differential operation can be utilized by applying the previously described LV VG-CMFB circuit, which can further cut half of the opamps' power when compared to pseudo-differential designs.

The implementation of this technique requires the use of a non-inverting amplifier, as shown in Fig. 11. The traditional implementation of a fully differential non-inverting auxiliary amplifier is not possible, since both opamp inputs are used as VGs in the differential circuit. Instead, the differential-difference amplifier (DDA) can be used to implement the fully differential non-inverting amplifier [23]. Fig. 13 presents the current-mirror opamps that will be used in the MDAC, including the main opamp [Fig. 13(a)] and the Auxiliary DDA [A-DDA, Fig. 13(b)] which will also be implemented in the real chip example of a pipelined ADC next. The A-DDA consists of two differential pairs with 4 inputs (2 for VGs and 2 for non-inverting inputs, as shown in Fig. 13(b)), with their currents sum at the drain of M2A and M2B, afterwards folded into the diodes M3A and M3C and later mirrored through M3B and M3D to the outputs. The output voltage and GBW of the opamp can be expressed as [3], [23]

$$V_{\rm out1} - V_{\rm out2} = Kg_{m1}[(V_{\rm inp1} - V_{\rm inp2}) - (V_{\rm inn1} - V_{\rm inn2})]R_{\rm out} \quad (19)$$

$$\mathrm{GBW} = Kg_{m1}/(2\pi C_{\rm Ltot}) \quad (20)$$

where $R_{\rm out}$ represents the equivalent output resistance, K is the current mirror ratio and $C_{\rm Ltot}$ is the total capacitive load. In Fig. 13(b) the VG-CMFB circuit can be applied from $V_{\rm tail}$ in the right-side differential-pair to $V_{\rm CMFB}$ to stabilize the CM voltage in the auxiliary amplifier, and the VG CM voltage of the other differential-pair will be set by the main opamp's VG CM level (See Fig. 11).

Several special techniques are used in the A-DDA of Fig. 13 to further improve its speed, namely: 1) nMOS differential pairs have inherently larger transconductance than their pMOS counterparts and their drain current is folded into the diodes M3A and M3C, which are also nMOS such that the phase margin is not degraded significantly by this current mirror pole in the signal path. Such configuration can achieve potentially higher speed than the traditional current mirror opamp with nMOS differential pair and pMOS current mirror; 2) Cascode transistors M4A and M4B are added into the output current branch to shield the pMOS current source transistors M5A and M5B from the Miller multiplication of the output node, which can significantly increase the input capacitance of the CMFB feedback point and thus slow down the CM response. Also, due to the cascode, it is possible to use minimum length transistors in M5A and M5B to further reduce their input parasitics. The cascode transistor may approach the vicinity of triode region in a LV environment, but since the output resistance is dominated by the nMOS side (M3B and M3D), the resulting nonlinearity will be suppressed. Such arrangement can still provide a 6 dB benefit to the gain as the output resistance now becomes $r_{o,M3B}$ rather than $r_{o,M3B}//r_{o,M5A}$.

VI. Measured Results of a 1.2 V Pipelined ADC

To verify the effectiveness of all the proposed LV circuit techniques, presented before, a 1.2-V, 10-bit, 60-MHz RO pipelined ADC was implemented in a 0.18-μm CMOS process with $V_{\rm thn} = 0.49$ V and $V_{\rm thp} = -0.48$ V. For floating switches in the midsupply (i.e., the bulk-source voltage $V_{\rm bs} = 0.6$ V) the threshold voltages increase to $V_{\rm thn} = 0.63$ V and $V_{\rm thp} = -0.65$ V due to the body effect (for high-speed consideration the bulk of the pMOS is connected to VDD instead of its source, to avoid driving the extra Nwell-to-substrate capacitance which will degrade the feedback factor and the MDAC transient response speed). In this case $V_{\rm DD} < V_{\rm thn} + |V_{\rm thp}|$ and floating switches are avoided as well as the RO technique will be employed in the design.

With the traditional 1.5 b/stage architecture, the pipelined ADC is implemented with a fully differential architecture using all the techniques presented in the paper, without the use of digital calibrations. The full-scale differential input range is 1.2 V_{PP} meaning that $V_{\rm ref} = 0.6$ V. The sampling capacitors are sized to suppress the thermal noise, and the input-referred noise of the whole ADC was simulated using Transient Noise Analysis in Spectre and the Signal-to-Noise (thermal, flicker and quantization noise) Ratio and it was designed to be 57 dB, which match also to the measured result of 56.5 dB.

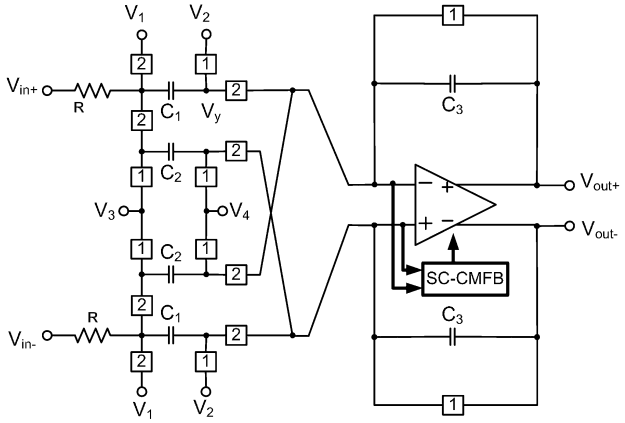

Fig. 14. Front-end S/H with CCPSI

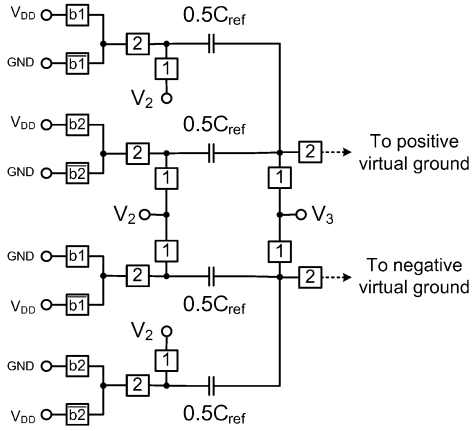

Fig. 15. Implementation of reference injection circuit in Fig. 11.

TABLE II
PERFORMANCE SUMMARY OF MAIN AND AUXILIARY AMPLIFIER IN 1ST STAGE MDAC

Performance	Main	Auxiliary
DC Gain	49 dB	49 dB
Feedback Factor β	0.23	
Unit-Gain Frequency	1.1GHz	640MHz
Phase Margin	79°	74°
Power Consumption (@ VDD=1.2V)	7.6mW	6.7mW

Fig. 14 shows the S/H circuit used in this example [24]. $C_1 = C_2 = C_3$ to implement a gain of 1, and V_1 to V_4 are fixed potentials used to obtain the required LS function. For this S/H circuit the following relationship holds:

$$V_{\text{out,CM}}[\phi 2] = \frac{C_1}{C_3}V_{\text{in,CM}} + \left(1 + \frac{C_1 + C_2}{C_3}\right)V_{G,\text{CM}} + \frac{1}{C_3}[C_2(V_3 - V_4) - C_1V_2 - (C_1 + C_2)V_1] \quad (21)$$

which shows large flexibility for adjusting the value of the level shift. For $C_1 = C_2 = C_3, V_{\text{in,CM}} = 0.6$ V and $V_{G,\text{CM}} = 0.75 \cdot V_{\text{DD}} = 0.9$ V and for a suitable biasing point of the nMOS differential pair it would be necessary to choose $V_1 = V_2 = V_3 = V_4 = 0.9$ V such that $V_{\text{out,CM}}[\phi 2] = 0.6$ V.

For the implementation of the MDAC the circuit of Fig. 11 will be used, and $C_{\text{ref}} : C_{f1} : C_{s1} = 1 : 2 : 4$ to implement the reference voltage injection and the 2x MDAC gain as presented in (6), with the auxiliary amplifier capacitor ratios specified by (18). On the other hand, only the 5 stages of the front-end MDACs have utilized the auxiliary amplifier to compensate the gain error, and the finite-gain error in the S/H will only imply an overall gain error of the ADC, which can be tolerated in most applications. All the main and auxiliary opamps use the topologies shown in Fig. 13. The sampling capacitors and the opamps are scaled down along the pipelined stages to save power. Table II summarizes the simulated performance of the 1st stage MDAC opamps with dc gains of 49 dB for both the main and the auxiliary amplifiers only. For traditional designs without gain compensation, the required dc gain for the opamp in the 1st MDAC would be at least 72 dB with $\beta = 0.23$ and a considerable margin should be added to reduce the settling-time requirement. The total power consumption of the main and the auxiliary amplifier is only 14.3 mW which is comparable to state-of-the-art designs with higher supply voltage (e.g., $V_{\text{DD}} = 1.8$ V) and with only one main opamp of similar GBW performance.

The implementation of the reference injection circuit is also shown in Fig. 15, in which C_{ref} is split into two halves (similar to [1]) such that the CM LS charge for the zero code ($b_1 = \overline{b_2}$) is the same as the other codes ($b_1 = b_2 = 1$ or 0). For the circuits from Figs. 11 and 15 it can be deducted the following CM relationship (assuming that both the main and auxiliary opamps in all stages have the same $V_{G,\text{CM}}$ and considering the previous stage reset to $V_{G,\text{CM}}$ in phase 2)

$$V_{o1,\text{CM}}[\phi 2] = \frac{C_{s1}}{C_{f1}}V_{\text{in,CM}} + \left(1 + \frac{C_{\text{ref}}}{C_{f1}}\right)V_{G,\text{CM}} + \frac{C_{\text{ref}}}{C_{f1}}(V_2 - V_3) - \frac{C_{s1}}{C_{f1}}V_1 - \frac{1}{2}V_{\text{DD}}\frac{C_{\text{ref}}}{C_{f1}}. \quad (22)$$

Here, the auxiliary amplifier is configured such that no CM LS charge is processed inside it and due to its small output swing it is possible to set its output CM level at $V_{o2,\text{CM}} = V_{G,\text{CM}} = 0.75V_{\text{DD}} = 0.9$ V. In this way, if the previous stage is also an MDAC with gain-compensation, then $V_1 = V_{o2,\text{CM}} = 0.9$ V. Also with $C_{\text{ref}} : C_{f1} : C_{s1} = 1 : 2 : 4$ and $V_{\text{in,CM}} = 0.6$ V, (22) can be simplified to

$$V_{o1,\text{CM}}[\phi 2] = 0.5(V_2 - V_3) + 0.45. \quad (23)$$

The output CM level of the MDAC can be chosen as $V_{o1,\text{CM}} = 0.6$ V by selecting $V_2 = V_{\text{DD}} = 1.2$ V and $V_3 = 0.75V_{\text{DD}} = 0.9$ V. Together with the S/H circuits the whole pipelined ADC requires only one fixed potential set to 0.75 $V_{\text{DD}} = 0.9$ V to define all LS functions. In addition, all the switches have at least 250 mV overdrive voltage to allow high-speed operation, and no floating switches are used to achieve higher linearity.

Fig. 16 shows the microphotograph of the ADC. The static performances of the ADC are measured using the traditional sine-wave histogram method. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC are $+0.7/-0.7$ LSB and $+1.2/-1$ LSB, respectively, and they are depicted in Fig. 17. The dynamic performances of the ADC are also measured by evaluating the spectrum of the captured data. Fig. 18 shows an FFT spectrum of the ADC with $f_{\text{in}} = 32.2$ MHz, amplitude of $A_{\text{in}} = -0.1$ dBFs input signal

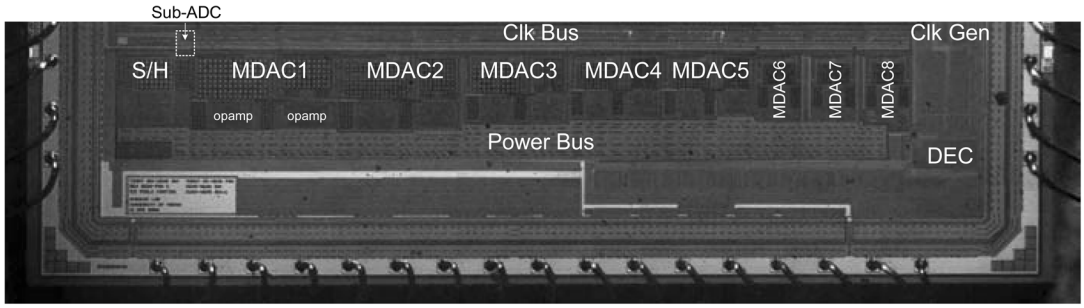

Fig. 16. Microphotograph of the LV ADC.

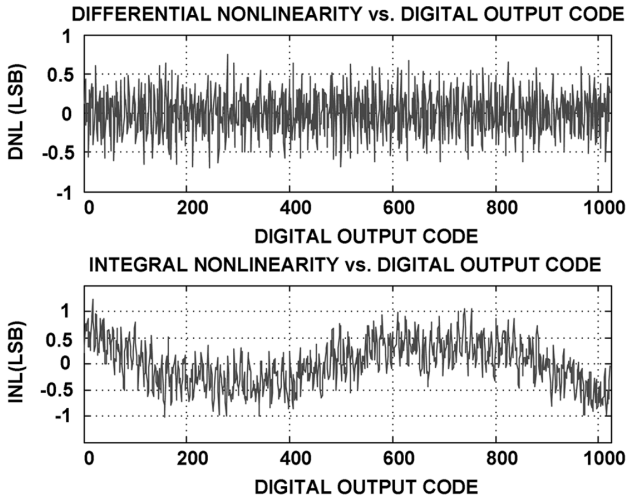

Fig. 17. Measured DNL and INL of the pipelined ADC.

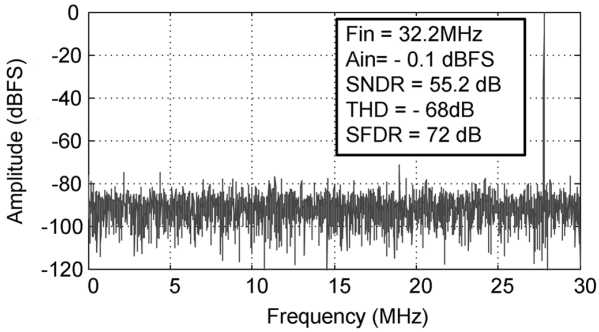

Fig. 18. Measured output spectrum of the pipelined ADC.

with $\mathrm{SNDR} = 55.2$ dB, $\mathrm{THD} = -68$ dB and $\mathrm{SFDR} = 72$ dBc, respectively. Fig. 19 shows a plot of SNDR versus input frequency, which shows that the ADC has an effective resolution bandwidth (ERBW) up to 75 MHz, far higher than the Nyquist frequency. The ADC consumes 85 mW from a 1.2-V supply, and the performance is summarized in Table III.

VII. Conclusion

This paper proposed several LV circuit techniques, summarized together with their advantages in Table IV. They serve as comprehensive solutions to various problems, like CMFB, power-hungry front-end T/R, LS and finite-gain error, in LV, high-speed, power efficient RO and SO circuits. They comprise the VG-CMFB combined with O-CMEC, CCPSI, VCLS,

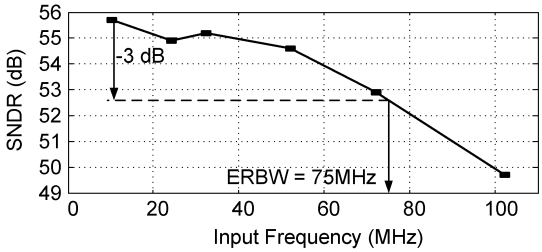

Fig. 19. Plot of SNDR versus input frequency.

and LV-FGC. Finally, a real chip example of a 1.2-V 10-bit 60-MHz pipelined ADC has been designed, integrating all of the proposed techniques, and the measured results are provided to demonstrate their effectiveness. The power consumption is 85 mW with an SNDR of 55.2 dB. Table III summarizes the overall performance of the pipelined ADC, as well as its comparison to the state-of-the-art LV ADC designs.

Appendix

This Appendix provides a detailed mathematical analysis of the operating principle associated with $\mathrm{VG-CMFB+O-CMEC}$ techniques, presented before in Section II, as well as illustrates the derivation of the equation for determining the capacitor ratio selection.

The derivation is based on the VG-CMFB and O-CMEC structures already presented in Fig. 5 plus the external passive network configuration from Fig. 3. Referring to Fig. 5, V_{bias} and $V_{\mathrm{tail,ref}}$ are the nominal values (or zero-CM-error operating point) of the node V_{CMFB} and V_{tail}, respectively, and $V_{G,\mathrm{ref}}$ is the desired value of the VG CM voltage $V_{G,\mathrm{CM}}$. Assuming A_{CM} is the CM gain from the node V_{CMFB} to the output CM level $V_{\mathrm{out,CM}}$, then the following relationship holds for a negative CMFB loop:

$$V_{\mathrm{out,CM}} = -A_{\mathrm{CM}}(V_{\mathrm{CMFB}} - V_{\mathrm{bias}}) \tag{24}$$

or

$$V_{\mathrm{CMFB}} = -\frac{V_{\mathrm{out,CM}}}{A_{\mathrm{CM}}} + V_{\mathrm{bias}} \approx V_{\mathrm{bias}} \tag{25}$$

with the assumption that $A_{\mathrm{CM}} \gg 1$. Considering that the circuit is in the steady-state the O-CMEC should inject no correction charges into the V_{CMFB} node in phase 2 if no output CM error occurs, thus $\Delta q = 0$ which yields

$$2C_3(V_{\mathrm{out,CM}}[\phi 2] - V_{\mathrm{out,CM}}[\phi 1]) + C_4(V_1 - V_2) - (2C_3 + C_4)(V_{\mathrm{CMFB}}[\phi 2] - V_{\mathrm{CMFB}}[\phi 1]) = 0. \tag{26}$$

TABLE III
PERFORMANCE BENCHMARK OF THE ADC

	This Work	TCASI'05 [5]	JSSC'05 [21]	JSSC'07 [7]
Technology	**0.18 μm CMOS (nominal supply = 1.8V)**			
Resolution	10b	12b	12b	8b
Digital Calibration	No	Yes	Yes	No
Supply Voltage	1.2V	0.9V	0.9V	1V
Supply Voltage (% of Nominal)	67%	50%	50%	56%
Full-Scale Input Range	1.2Vpp	0.9Vpp	0.5Vpp	0.5Vpp
Sampling Rate	60MS/s	1MS/s	5MS/s	100MS/s
ADC Core Power	85mW	9mW	12mW	30mW
ADC Core Area	2.2mm^2	1.44mm^2	1.4mm^2	2.04mm^2
DNL	0.7 LSB	0.8 LSB	0.6 LSB	0.5 LSB
INL	1.2 LSB	1.05 LSB	1.4 LSB	1.1 LSB
Effective Resolution Bandwidth	75MHz	N/A	N/A	~8MHz
SNDR	55.2 dB	55 dB	50 dB	41.5 dB
ENOB	8.9	8.9	8	6.6
SFDR	74 dB	75 dB	77 dB	52.6 dB
FOM (Power/[2^{ENOB}*fs] pJ/conversion step)	2.8	18.8	9.4	3.1

TABLE IV
SUMMARY OF THE LV TECHNIQUES

Low-Voltage Techniques	Main Improvements in Low-Voltage Designs
Virtual-Ground CMFB with Output CM Error Correction (VG-CMFB + O-CMEC)	Power Reduction (2 pseudo-diff. opamp to 1 fully-diff. opamp)
Crossed-Coupled Passive Sampling Interface (CCPSI)	Power Reduction (Eliminate the extra T/H)
	Accuracy (Low signal-feedthrough error)
Voltage-Controlled Level Shifting (VCLS)	Speed (increased feedback factor)
Low-Voltage Finite-Gain Compensation (LVFGC)	Improved opamp's speed/power trade-offs (allow the use of high-speed low-gain single-stage opamp

By substituting (25) in (26) it can be simplified to the following design equation:

$$V_{\mathrm{out,CM}}[\phi 2] - V_{\mathrm{out,CM}}[\phi 1] = \frac{C_4}{2C_3}(V_2 - V_1) \tag{27}$$

which defines the relationship between the output CM level in two phases with the capacitor ratio and the reference voltages V_1 and V_2. Notice that by setting $\Delta q = 0$ in phase 1 the same (27) can be derived, implying that the O-CMEC circuit will not inject charges in both phases if there is no CM error in the steady-state.

The derivation is not complete until the VG potential is determined. Referring to Fig. 3 in phase 1 the opamp reset implies that

$$\begin{aligned} V_{\mathrm{tail}}[\phi 1] &= V_{G,\mathrm{CM}}[\phi 1] - V_{\mathrm{GS1,CM}} \\ &= V_{\mathrm{out,CM}}[\phi 1] - V_{\mathrm{GS1}} \end{aligned} \tag{28}$$

where V_{GS1} is the CM gate-source voltage of the differential-pair transistors M1A and M1B from Fig. 4, which remains constant as long as the tail current source does not vary. A charge conservation equation can be written at node V_{CMFB} at phase 1 and rearranged as

$$\begin{aligned} &(C_2 + 2C_3 + C_4)(V_{\mathrm{CMFB}}[\phi 1] - V_{\mathrm{CMFB}}[\phi 2]) \\ &\quad + C_1 V_{\mathrm{CMFB}}[\phi 1] - C_2(V_{\mathrm{tail}}[\phi 1] \\ &\quad - V_{\mathrm{tail}}[\phi 2]) - C_1 V_{\mathrm{tail}}[\phi 1] \\ &\quad - C_1(V_{\mathrm{bias}} - V_{\mathrm{tail,ref}}) - 2C_3(V_{\mathrm{out,CM}}[\phi 1] \\ &\quad - V_{\mathrm{out,CM}}[\phi 2]) + C_4(V_1 - V_2) = 0. \end{aligned} \tag{29}$$

Similarly an equation can be written at node V_{CMFB} at phase 2

$$\begin{aligned} &-(C_2 + 2C_3 + C_4)(V_{\mathrm{CMFB}}[\phi 1] - V_{\mathrm{CMFB}}[\phi 2]) \\ &+C_2(V_{\mathrm{tail}}[\phi 1] - V_{\mathrm{tail}}[\phi 2]) \\ &+2C_3(V_{\mathrm{out,CM}}[\phi 1] - V_{\mathrm{out,CM}}[\phi 2]) - C_4(V_1 - V_2) = 0. \end{aligned} \tag{30}$$

Summing (29) and (30) it yields

$$V_{\mathrm{CMFB}}[\phi 1] - V_{\mathrm{tail}}[\phi 1] = V_{\mathrm{bias}} - V_{\mathrm{tail,ref}}. \tag{31}$$

Substituting (25) and (28) with $V_{\mathrm{tail,ref}} = V_{G,\mathrm{ref}} - V_{\mathrm{GS1}}$ into (9) it will imply

$$V_{G,\mathrm{CM}}[\phi 1] \approx V_{G,\mathrm{ref}} \tag{32}$$

which indicates that the VG CM voltage in phase 1 is stabilized to the reference voltage $V_{G,\mathrm{ref}}$.

The VG CM voltage in phase 2 can be evaluated by subtracting (29) from (30), with substitution of (31) as

$$\begin{aligned} &2(C_2 + 2C_3 + C_4)(V_{\mathrm{CMFB}}[\phi 1] - V_{\mathrm{CMFB}}[\phi 2]) \\ &\quad -2C_2(V_{\mathrm{tail}}[\phi 1] - V_{\mathrm{tail}}[\phi 2]) \\ &\quad -4C_3(V_{\mathrm{out,CM}}[\phi 1] - V_{\mathrm{out,CM}}[\phi 2]) \\ &\quad - 2C_4(V_1 - V_2) = 0. \end{aligned} \tag{33}$$

Also the following equations will hold:

$$V_{\mathrm{CMFB}}[\phi 1] \approx V_{\mathrm{CMFB}}[\phi 2] \approx V_{\mathrm{bias}} \quad (34)$$

$$V_{\mathrm{tail}}[\phi 1] - V_{\mathrm{tail}}[\phi 2] = V_{G,\mathrm{CM}}[\phi 1] - V_{G,\mathrm{CM}}[\phi 2]. \quad (35)$$

Finally by substituting (32), (34), (35) and the design (27) into (33) it yields

$$V_{G,\mathrm{CM}}[\phi 2] \approx V_{G,\mathrm{ref}} \quad (36)$$

which indicates that the VG CM voltage in phase 2 is also stabilized to $V_{G,\mathrm{ref}}$.

APPENDIX

This appendix provides a thermal noise analysis of the front-end S/H with CCPSI circuit, as presented in Fig. 14 and Table I. In Fig. 14 the circuit noise is calculated as follows: In phase 1, the thermal noise sampled in the capacitor $C_1 = C_2 = C_3 = C$ will be transferred to the output in phase 2

$$\overline{v^2_{n,kT/C}[\phi 1]} = 3kT/C. \quad (37)$$

During phase 2, both the opamp input referred noise density and the on-resistance thermal noise density of the switches will be filtered by the closed-loop bandwidth in phase 2, but the contribution from the opamp noise is much dominant and thus it is the only one to be considered. The noise from the opamp in phase 2 can be calculated as

$$\begin{aligned}\overline{v^2_{n,\mathrm{opamp}}[\phi 2]} &= S_{\mathrm{opamp}}(f) \cdot |H_{\phi 2}(0)|^2 \cdot \frac{1}{4}\beta\omega_{\mathrm{GBW}} \\ &= \frac{1}{4\beta} S_{\mathrm{opamp}}(f) \cdot \omega_{\mathrm{GBW}} \end{aligned} \quad (38)$$

where $H_{\phi 2}(0) = 1/\beta$ is the low-frequency noise voltage transfer function from the opamp input referred noise source to the output, β is the feedback factor in phase 2, ω_{GBW} is the gain-bandwidth product of the opamp, and $S_{\mathrm{opamp}}(f)$ is the opamp's input referred noise power spectral density, which depends only on the opamp topology and thus it will be held constant over all the cases from Table I.

Also due to the resetting feature of the RO circuit, opamp noise in phase 1 will be transferred to next stage also

$$\begin{aligned}\overline{v^2_{n,\mathrm{opamp}}[\phi 1]} &= S_{\mathrm{opamp}}(f) \cdot |H_{\phi 1}(0)|^2 \cdot \frac{1}{4}\omega_{\mathrm{GBW}} \\ &= \frac{1}{4} S_{\mathrm{opamp}}(f) \cdot \omega_{\mathrm{GBW}}. \end{aligned} \quad (39)$$

Thus, the total noise power in fully differential mode is the sum of the three parts of noise (with $\beta = 1/3$)

$$\overline{v^2_{n,C_2=C_1}} = 2[3kT/C + S_{\mathrm{opamp}}(f) \cdot \omega_{\mathrm{GBW}}]. \quad (40)$$

Notice that the noise power will be doubled in fully differential operation. Similarly, we can calculate the noise for the case $C_2 = 0 (\beta = 1/2)$

$$\overline{v^2_{n,C_2=0}} = 2[2kT/C + (3/4) \cdot S_{\mathrm{opamp}}(f) \cdot \omega_{\mathrm{GBW}}] \quad (41)$$

The data in Table I are calculated with $S_{\mathrm{opamp}}(f) \cdot \omega_{\mathrm{GBW}} = 30\ \mathrm{nV}^2_{\mathrm{rms}}$ for 10 b cases and $3.75\ \mathrm{nV}^2_{\mathrm{rms}}$ for 12 b cases due to the reduced gain-bandwidth in 12 b (by larger capacitive load), $T = 300$ K and 1.2 V_{pp} differential signal swing.

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