An NMOS-LDO Regulated Switched-Capacitor DC–DC Converter With Fast-Response Adaptive-Phase Digital Control

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***Abstract*—A fully integrated low-dropout-regulated step-down multiphase-switched-capacitor DC–DC converter (a.k.a. charge pump, CP) with a fast-response adaptive-phase (Fast-RAP) digital controller is designed using a 65-nm CMOS process. Different from conventional designs, a low-dropout regulator (LDO) with an NMOS power stage is used without the need for an additional step-up CP for driving. A clock tripler and a pulse divider are proposed to enable the Fast-RAP control. As the Fast-RAP digital controller is designed to be able to respond faster than the cascaded linear regulator, transient response will not be affected by the adaptive scheme. Thus, light-load efficiency is improved without sacrificing the response time. When the CP operates at 90 MHz with 80.3% CP efficiency, only small ripples would appear on the CP output with the 18-phase interleaving scheme, and be further attenuated at $V_{\rm OUT}$ by the 50-mV dropout regulator with only 4.1% efficiency overhead and 6.5% area overhead. The output ripple is less than 2 mV for a load current of 20 mA.**

***Index Terms*—DC–DC converter, digital controller, low-dropout regulator (LDO), power supply rejection (PSR), switched-capacitor power converter (SCPC), voltage regulator.**

I. Introduction

FULLY integrated voltage regulators, including linear regulators and inductive and capacitive dc–dc converters, are in high demands for system-on-chips (SoCs), especially in miniaturized devices [1]–[4], and fully integrated and power-efficient converters with small output ripples are needed for implantable devices [5]. Conventional inductive dc–dc converters need one or more inductors that are hard to be integrated and occupy large chip or printed circuit board area [2], [6]. On the other hand, capacitor density has been significantly increased for advanced processes. Thus, switched-capacitor (capacitive) dc–dc converters (a.k.a. charge pump, CP) are preferred as a fully integrated SoC solution in nanometer processes, while interleaving topology for reducing the output ripple can be easily built into the CP with little power and area overhead [7]–[9]. Moreover, capacitive dc–dc converters could have faster transient response than inductive dc–dc converters. Take the voltage-mode buck converter as an example. In order to change the output voltage, the current of the inductor has to change first, and results in 90° phase delay for the output voltage. In this regard, a capacitive dc–dc converter is more suitable for fast dynamic voltage and frequency scaling applications. However, the output voltage of a CP is a function of input voltage, output current, switching frequency, and values of flying capacitors [10], [11], while the output voltage of an inductive dc–dc converter is only a function of input voltage and duty ratio. As a result, the load and line regulation of a standalone CP is (usually) not good enough for driving noise-sensitive analog circuits. Hybrid power management systems [12] that consist of a CP and linear regulators have been proposed for the following reasons: 1) to improve the efficiency of standalone linear regulators; 2) to improve the line and load regulation of the CP; 3) to realize independent supply voltage domains; 4) to improve transient response; and 5) to reduce output voltage ripple.

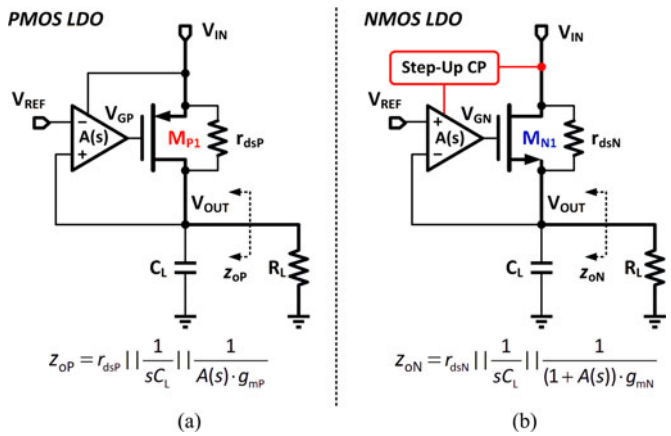

Fig. 1. Generic low-dropout regulators with (a) PMOS power stage or (b) NMOS power stage.

The power supplies of digital loads can be dc–dc converters or LDOs for different voltage domains [13], [14]. On the other hand, the power supply of an analog/RF load should be an LDO so as to suppress the switching noise from the prestage power source. As shown in Fig. 1(a), the power transistor of an LDO is commonly a PMOS transistor as its gate voltage $V_{\rm G}$ can easily be driven by low voltage (LV). The output impedance $z_{\rm oP}$ of an LDO with a common-source PMOS power stage (or PMOS LDO for short) is

$$z_{\rm oP} = \frac{r_{ds\rm P}}{1 + s \cdot r_{ds\rm P} C_L + A(s) \cdot g_{\rm mP} r_{ds\rm P}} \tag{1}$$

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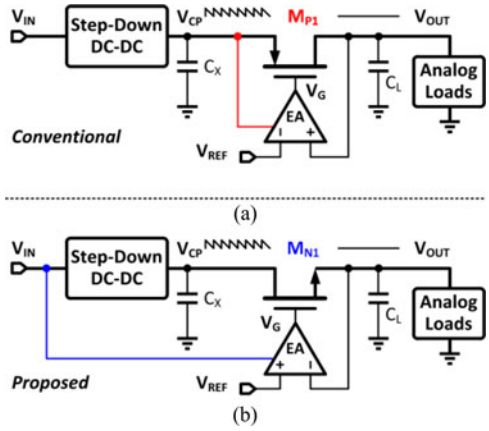

Fig. 2. (a) Conventional dc–dc converter in cascade with PMOS LDO and EA gets power from $V_{\rm CP}$, and (b) the proposed NMOS LDO regulated topology and EA gets power from $V_{\rm IN}$.

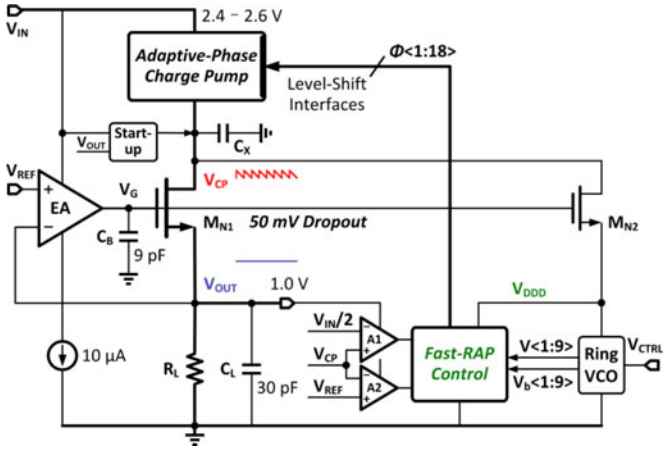

Fig. 3. Block diagram of the fully integrated NMOS-LDO regulated switched-capacitor dc–dc converter with Fast-RAP control.

where $g_{\rm mP}$ and r_{dsP} are the transconductance and the output resistance of the power PMOS transistor, and $A(s)$ is the gain of the error amplifier (EA). Now, the output impedance $z_{\rm oN}$ of an LDO with an NMOS source-follower power stage (or NMOS LDO for short) as shown in Fig. 1(b) is

$$z_{\rm oN} = \frac{r_{dsN}}{1 + s \cdot r_{dsN} C_L + (1 + A(s)) \cdot g_{\rm mN} r_{dsN}} \tag{2}$$

where $g_{\rm mN}$ and r_{dsN} are the transconductance and the output resistance of the power NMOS transistor. Note that the multiplicative factors of $g_{\rm mP}$ and $g_{\rm mN}$ are $A(s)$ and $(1 + A(s))$, respectively. As the low-frequency (LF) gain is very high ($|A(s)| >> 1$ at LF), the above difference is not important, and we have

$$z_{\rm oP,LF} \approx 1/A(s) \cdot g_{\rm mP} \tag{3}$$

$$z_{\rm oN,LF} \approx 1/A(s) \cdot g_{\rm mN}. \tag{4}$$

However, as the EA cannot respond to the out-of-band high-frequency (HF) signal, that is, A(s) ≈ 0 at HF, the HF dependence of the two output impedances are very different

$$z_{\rm oP,HF} \approx 1/sC_L \tag{5}$$

$$z_{\rm oN,HF} \approx 1/(sC_L + g_{\rm mN}). \tag{6}$$

By using a power NMOS and maintaining a low-dropout voltage, a step-up CP is needed to drive the NMOS source-follower power stage [15], [16]. Despite a higher driving voltage is needed, the NMOS LDO is at times preferred because it has low $z_{\rm oN,HF}$ that can intrinsically respond to fast load transients [17].

To drive analog/RF loads, the dc–dc converter should be cascaded with an LDO, as shown in Fig. 2(a), and PMOS LDOs are the common choices [18]–[22]. A fully integrated PMOS LDO suffers from the problem of multipole slow response, and full-spectrum power supply rejection (PSR) is hard to be achieved [23], [24], especially when the dropout voltage is as low as 50 mV, and the power PMOS has to be very large that makes it hard to achieve fast response and good stability.

In this research, an NMOS LDO with fast source-follower response is proposed. As shown in Fig. 2(b), the supply voltage of the LDO EA is $V_{\rm IN}$, and it is high enough such that the output of EA can drive the gate of $\rm M_{N1}$ without the need of a step-up CP as that shown in Fig. 1(b). In addition, to improve the light-load efficiency without sacrificing the response time, a fast-response adaptive-phase (Fast-RAP) digital control loop is proposed to control the multiphase CP. The system-level architecture and control loop design are discussed in Section II. Circuit implementations and design techniques are discussed in Section III. Measurement results and performance comparison are presented in Section IV, and a brief conclusion is drawn in Section V.

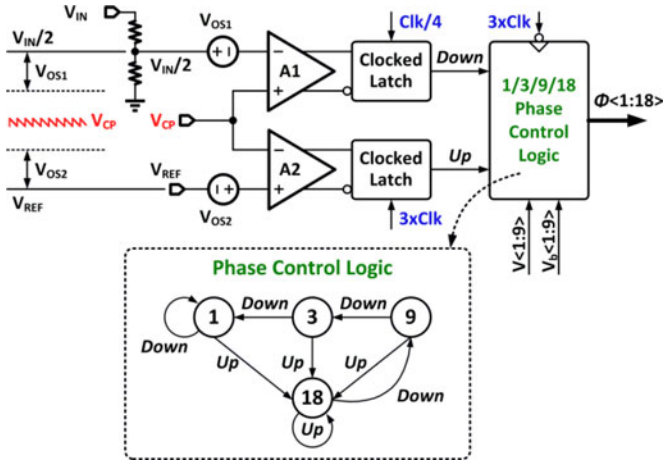

Fig. 4. Fast-RAP control logic with clock frequency tripler (3×Clk) and pulse divider (Clk/4) and up/down signal generated by comparing $V_{\rm CP}$ with $V_{\rm REF}$ and $V_{\rm IN}/2$.

II. System Architecture and Control

Fig. 3 shows the system architecture of the NMOS source-follower-based low-dropout regulator (NMOS-LDO) merged with a step-down multiphase CP with Fast-RAP control. In fact, this Fast-RAP control can suppress the output voltage ripples for both multiphase CPs and inductive dc–dc converters. For the proposed CP + LDO combo, the input voltage range is that of

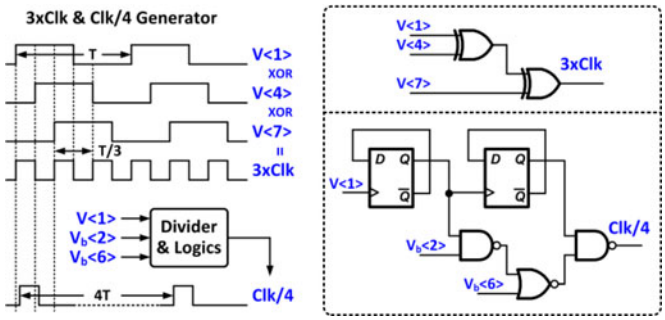

Fig. 5. Clock tripler and pulse divider that use the ring oscillator phases.

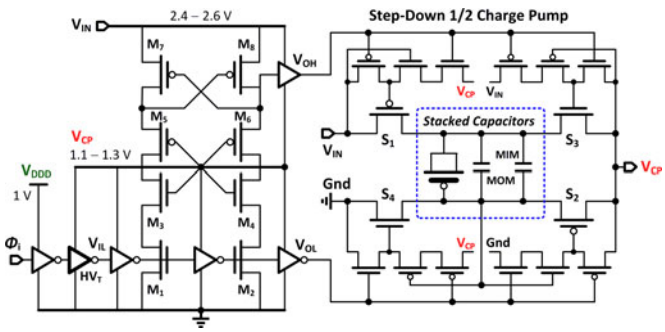

Fig. 6. Unit cell of the 18-phase CP with all LV device stacked LS and a $\mathrm{HV_T}$ inverter at V_{DDD} to V_{CP} interface.

TABLE I
COMPARISON OF LS WITH $V_{\mathrm{IN}} = 2.5$ V AND $V_{\mathrm{CP}} = 1.1$ V AT $f_{\mathrm{SW}} = 100$ MHz

LS V_{IL} to V_{OH}	HV LS	Stacked	Improvement
$T_{D,\mathrm{Rise}}$	120.7 ps	40.2 ps	300.3%
$T_{D,\mathrm{Fall}}$	305.0 ps	93.0 ps	328.0%
Power	13.7 μW	6.05 μW	226.4%

the I/O devices, which is from 2.4 to 2.6 V. The output voltage is set at 1.0 V for low-power RF/analog circuits, and the EA gets power from V_{IN} to drive the gate of $\mathrm{M_{N1}}$. The NMOS power transistor has to deal with two paths of PSR: one path is from V_{IN} to V_{OUT}, and another is from V_{CP} to V_{OUT}. Another power MOS $\mathrm{M_{N2}}$ shares the V_{G} with $\mathrm{M_{N1}}$ and generates an auxiliary V_{DDD} to power up the digital controller and the current-starved nine-inverter ring oscillator (Ring-VCO), isolating the digital circuit noise from affecting V_{OUT}. Indeed, by adding additional power transistors $\mathrm{M_{N}}_n$ $(n = 1, 2, k)$ with gates connected to V_G, many replica voltage islands can be easily generated for noise isolation, and this is another benefit of using the NMOS power stage.

A. Prior Control Loops

Hysteretic control, with single- or multiboundary, is popular due to its fast response and good stability [6]. However, hysteretic or any other ripple-based control methods cannot achieve small output ripple as they need a relatively large output

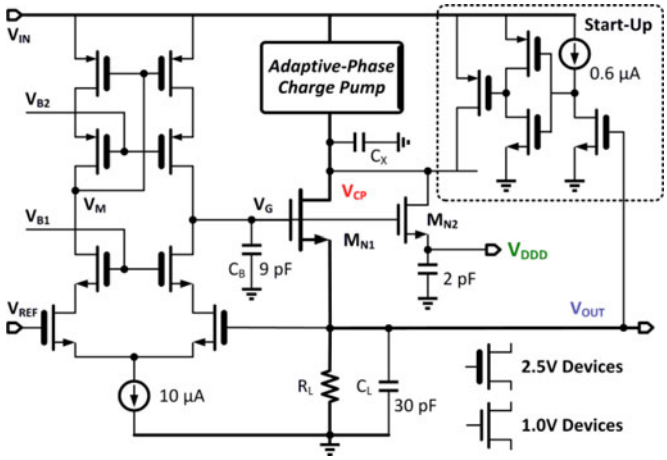

Fig. 7. Schematic of the NMOS-LDO and the start-up circuit.

ripple to define the trip points unambiguously [25]. Voltage-controlled-oscillator (VCO)-based pulse frequency modulation (PFM) with a load-dependent switching frequency is another popular control method with the advantage of high efficiency over a wide load range, but suffers from slow responses and a load-dependent noise spectrum [7], [26]. To achieve fast load response, Breussegem and Steyaert [7] proposed a fast loop triggered by an additional 3.3 GHz clock that bypasses the main integrator loop when the output voltage is lower than its low limit, but such a HF clock may not be available in many low-power applications, such as wireless sensor nodes or implantable medical devices. Besides, the reference tracking speed of a converter that implements dynamic voltage scaling depends on the bandwidth of the main loop, not the fast loop.

Other solutions include regulating the on-resistance of the switches of the CP in both phases to provide a pseudocontinuous output voltage [27]–[29]; however, without using an LDO, these methods have output glitches during phase transitions. In [30], a PMOS LDO was cascaded as the prestage to regulate the output voltage that suppressed both startup inrush surge and steady-state input current. A combined automatic pumping current and frequency control scheme was proposed in [31], which reduced the output ripple to be less than 33.8 mV with a 2-μF off-chip load capacitor.

B. Fast-RAP Control

The proposed Fast-RAP digital control scheme is sketched in Fig. 4. Instead of using a separate clock for fast load-transient response, a frequency tripler (3×Clk) that allows the controller to respond three times faster is implemented by using the interleaving phases of the VCO. The 3×Clk is generated by $\mathrm{V}\langle 1\rangle$ XOR $\mathrm{V}\langle 4\rangle$ XOR $\mathrm{V}\langle 7\rangle$, where $\mathrm{V}\langle k\rangle$ are VCO phases, as shown in Fig. 5. Similarly, a 9×Clk could be generated with a nine-inverter Ring-VCO, but to tradeoff for a lower quiescent current, the 3×Clk is adopted in this design.

One period of the Ring-VCO is T, and one period of the 3×Clk is $T/3$. To avoid phase-number oscillation (to be discussed shortly), a much lower pulse frequency Clk/4 is

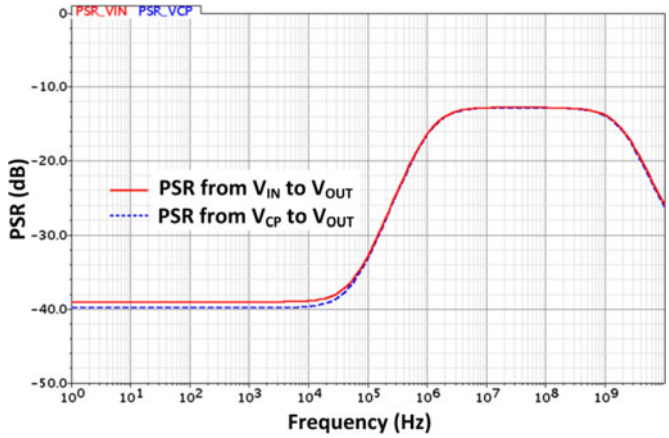

Fig. 8. Simulated PSR from $V_{\rm IN}$ to $V_{\rm OUT}$, and from $V_{\rm CP}$ to $V_{\rm OUT}$, respectively.

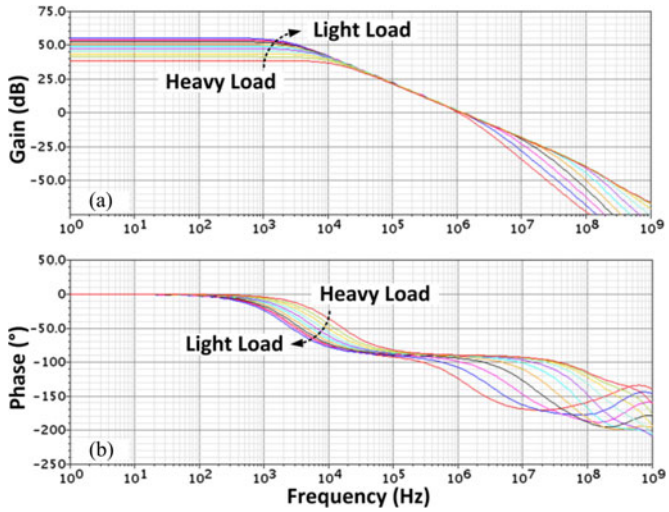

Fig. 9. (a) Open-loop gain and (b) phase of the NMOS-LDO at $I_{\rm Load}$ range from 10 μA to 30 mA.

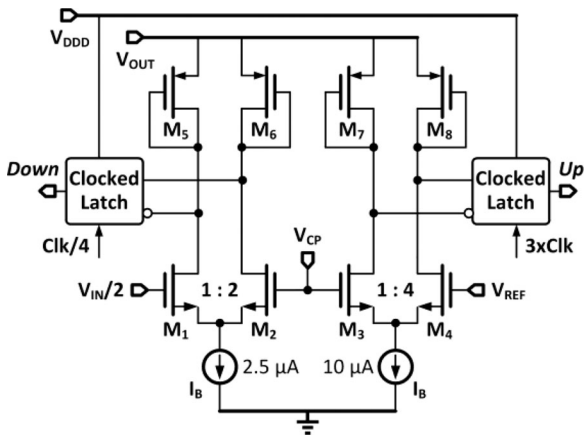

Fig. 10. Schematic of the preamplifiers with built-in offsets.

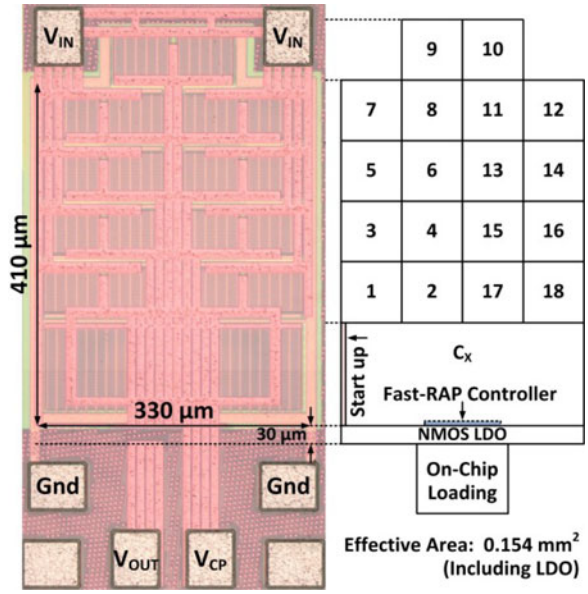

Fig. 11. Chip micrograph of the NMOS-LDO regulated CP.

generated by dividers, logics, and VCO phases, which is also shown in Fig. 5. The period of Clk/4 is 4*T*. The Fast-RAP controller reads its inputs at the falling edge of every 3×Clk period, so the pulse width of one "down" signal should be shorter than *T*/3 to avoid false multiple reading. The rising edge of Clk/4 is designed to be leading the falling edge of the 3×Clk to satisfy the setup time requirement.

The Fast-RAP digital controller sets the phase number of the CP to be used, and tries to keep the output voltage $V_{\rm CP}$ within the upper boundary $V_{\rm IN}/2 - V_{\rm OS1}$ and the lower boundary $V_{\rm REF} + V_{\rm OS2}$. Note that the phase number should not change in the steady state for output noise consideration. When the load current $I_{\rm Load}$ suddenly increases and drives $V_{\rm CP}$ down to be lower than $V_{\rm REF} + V_{\rm OS2}$, "Up" is set to be high, and the Fast-RAP controller will enable all 18 phases within half of 3×Clk period (*T*/6) to drive $V_{\rm CP}$ up fast. If, however, $V_{\rm CP}$ is higher than $V_{\rm IN}/2 - V_{\rm OS1}$ (due to overcharging or decrease in load current), "down" is set to be high, and the phase number will be reduced by only one step (from 18 to 9, or 9 to 3, or 3 to 1) within 4*T* initiated by Clk/4. Hence, in order to avoid phase-number oscillations, the phase number goes up fast to accommodate for fast load transient; and goes down slowly and step by step when $I_{\rm Load}$ decreases. The offset voltages $V_{\rm OS1}$ and $V_{\rm OS2}$ are generated by unbalanced input transistor sizes of the preamplifiers A1 and A2, and are designed to be 30 and 80 mV, respectively. These artificial offset values are a few times larger than the random offsets that can be neglected. In a typical case with $V_{\rm IN} = 2.5$ V, for example, the hysteresis window for phase-number control is from 1.08 to 1.22 V that is large enough to avoid phase-number oscillation at any fixed $I_{\rm Load}$.

This hybrid design has two control loops: the Fast-RAP loop and the LDO loop. The Fast-RAP loop senses the CP output voltage $V_{\rm CP}$, while the LDO loop senses the output voltage $V_{\rm OUT}$. Thus, these two loops will not affect each other in the

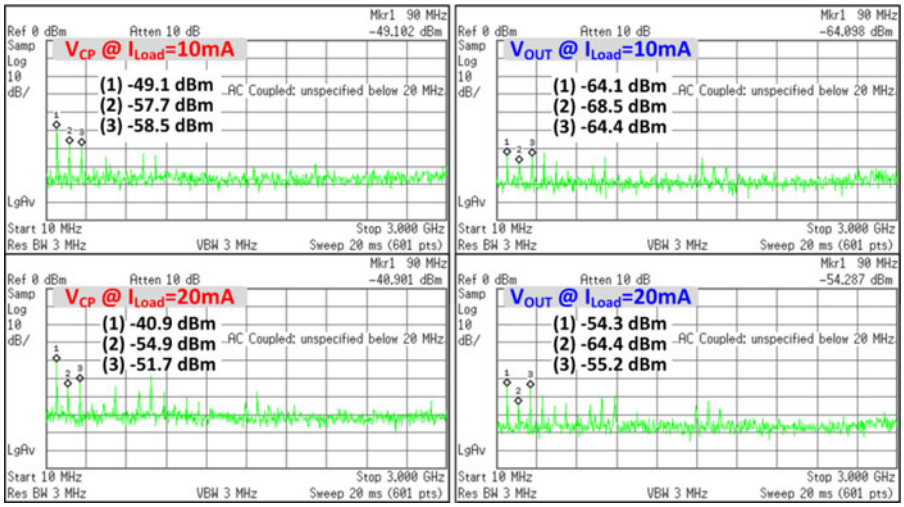

Fig. 12. Measured output spectrum of V_{CP} and V_{OUT} with $I_{\mathrm{Load}} = 10$ and 20 mA, respectively.

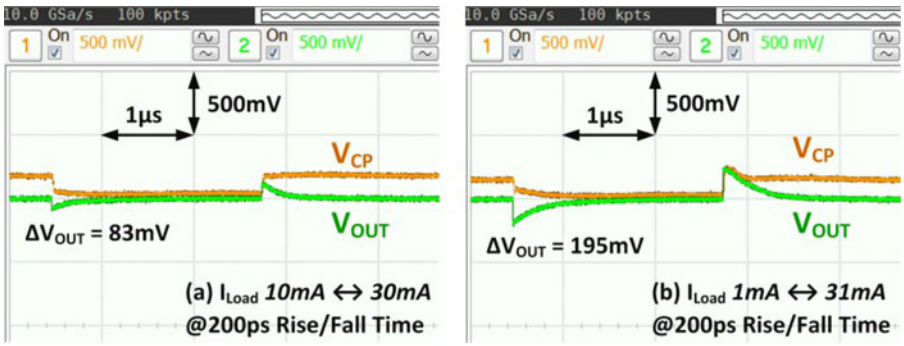

Fig. 13. Measured transient response of V_{CP} and V_{OUT} with on-chip load which has 200-ps load transient edge time.

steady state. During load transient, as long as 1) the adaptive phase loop responds faster than the LDO loop that is guaranteed by the 3×Clk, the speed of a digital circuit is proportional to its clock frequency; and 2) the droop of V_{CP} does not cause the $V_{\mathrm{DS}}(= V_{\mathrm{CP}} - V_{\mathrm{OUT}})$ of the LDO NMOS $\mathrm{M_{N1}}$ to be lower than its dropout voltage V_{DO} (50 mV in this case), then these two loops will not affect each other. Since both V_{OUT} and V_{CP} will vary in the same direction during load transient, and a C_X of 0.26 nF is used to hold V_{CP}; V_{DS} of $\mathrm{M_{N1}}$ will not be lower than V_{DO} when the load current increases. Stability of the LDO loop is discussed in Section III-C.

III. Circuit Implementations

A. Unit Cell of CP

Fig. 6 shows the unit cell of the 18-phase CP implemented with only LV transistors. The clock phases have to be passed from the Fast-RAP controller with the supply voltage $V_{\mathrm{DDD}}(=$ 1.0 V) to the unit cell with the supply voltage V_{CP} (1.1 to 1.3 V), and a level shifter (LS) (an inverter) between V_{DDD} and V_{CP} is needed. As V_{DDD} is lower than V_{CP}, the PMOS of this inverter cannot be completely turned OFF when the inverter input is high, so high-threshold-voltage ($\mathrm{HV_T}$) transistors are used to reduce the subthreshold leakage current in this state. A stacked LS is employed to further convert the phase signal from the (V_{CP}, Gnd) domain to the (V_{IN}, V_{CP}) domain [32]. The improvements of the stacked LV device LS over the conventional high-voltage (HV) device LS are listed in Table I. The delay time and the power consumption are reduced by 3 and 2 times, respectively.

Due to the gate leakage current of LV transistors of the 65-nm CMOS process, the flying capacitor C_{FLY} (30 pF for each phase) is realized by connecting the stacked HV PMOS, MOM, and MIM capacitors in parallel to eliminate leakage current and to increase the capacitance as well as the power density.

To realize nonoverlap timing and consequently eliminate the switch reverse current, three-transistor (3T)-based inverters are utilized to drive the power switches $\mathrm{S_1}$ through $\mathrm{S_4}$. The 3T inverters that drive the PMOS switches $\mathrm{S_1}$ and $\mathrm{S_2}$ consist of two NMOS transistors to turn-on the PMOS switches slowly. Similarly, the 3T inverters that drive the NMOS switches $\mathrm{S_3}$ and $\mathrm{S_4}$ consist of two PMOS transistors. By sensing the negative-plate voltage of the flying capacitor, $\mathrm{S_2}$ will be turned ON after $\mathrm{S_1}$ has been turned ON; and $\mathrm{S_4}$ will be turned ON after $\mathrm{S_3}$ has been turned ON. These switching sequences were designed to avoid the impact of signal mismatch between V_{OH} and V_{OL}.

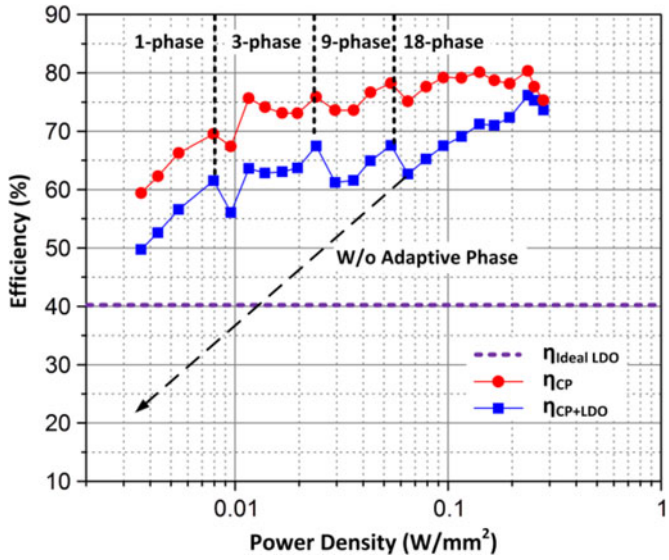

Fig. 14. Measured total efficiency $\eta_{\mathrm{CP+LDO}}$ and derived CP efficiency η_{CP} versus power density with $V_{\mathrm{IN}} = 2.5$ V, $V_{\mathrm{OUT}} = 1$ V, and $f_{\mathrm{SW}} = 90$ MHz.

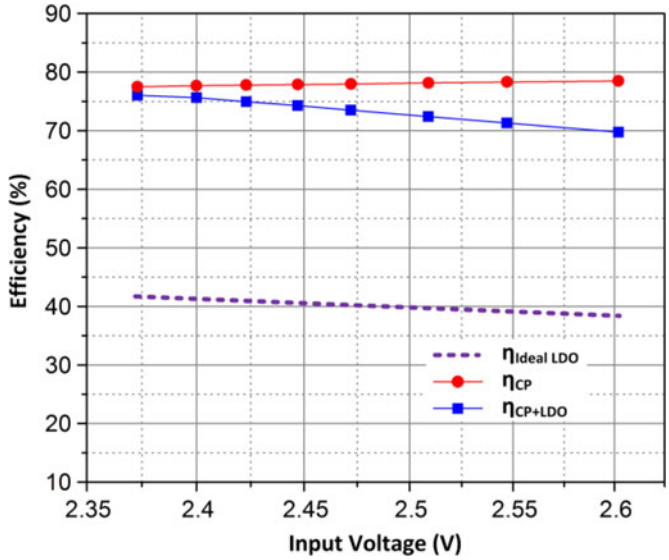

Fig. 15. Measured $\eta_{\mathrm{CP+LDO}}$ and derived η_{CP} with $V_{\mathrm{OUT}} = 1$ V, $I_{\mathrm{Load}} = 30$ mA, $f_{\mathrm{SW}} = 90$ MHz.

TABLE II
POWER LOSS BREAKDOWN OF NMOS-LDO REGULATED CP

Component	SubComponent	Power Loss	Percentage
CP Power Stage	Conduction Loss	5.71 mW	64.3%
	Switching Loss	0.98 mW	11.0%
LDO	Power MOS	1.96 mW	22.1%
	Error Amplifier	25 μW	0.28%
VCO		42 μW	0.47%
Controller	Preamplifiers	12 μW	0.14%
	Fast-RAP Logics	19.5 μW	0.22%
	LSs	109 μW	1.23%
Biases		25 μW	0.28%
Total		8.88 mW	100%

B. Start-Up Circuit

Since the LSs and the gate drivers of the CP are powered up by the voltage V_{CP}, a start-up circuit is needed to charge up V_{CP} before it is ready for use. The schematics of the EA and the start-up circuit are shown in Fig. 7. The start-up circuit, which senses the LDO output V_{OUT} and charges up V_{CP}, consumes less than 1 μA of quiescent current. In fact, if auxiliary intermediate supply rails are available for the CP gate drivers, the start-up circuit will not be needed, and the ripple amplitude can also be reduced.

C. Error Amplifier

A telescopic cascode amplifier powered up by V_{IN} is used to drive both power transistors $\mathrm{M_{N1}}$ and $\mathrm{M_{N2}}$. The voltage drop across the CP output V_{CP} and the LDO output V_{OUT} can be as low as 50 mV to minimize the power loss caused by the LDO. A bypass capacitor $C_{\mathrm{B}} = 9$ pF is added to suppress the noise at V_{G}, and consequently, V_{OUT} has very small voltage ripples. The simulated PSR performances of the LDO from V_{IN} to V_{OUT}, and also from V_{CP} to V_{OUT} at $I_{\mathrm{Load}} = 20$ mA are shown in Fig. 8. The PSR for both paths are –39 and –40 dB at LFs, respectively, and are –12.8 dB in the frequency range of 1 MHz to 1 GHz. Thus, supply noise from both paths can be attenuated by the power MOS $\mathrm{M_{N1}}$.

By using an NMOS as the power transistor, the LDO output pole is designed to be a nondominant pole, while the dominant pole is set by C_{B} and is located at V_{G}. The simulated open-loop Bode plots of the LDO with I_{Load} ranging from 10 μA to 30 mA are presented in Fig. 9. The minimum dc loop gain is 38 dB that occurs at heavy load. The worst-case phase margin of the NMOS LDO is 55° at $I_{\mathrm{Load}} = 10$ μA. This minimum load current requirement is fulfilled by the consumption of the preamplifiers (A1 and A2) to be introduced next.

D. Preamplifiers

Fig. 10 shows the schematic of the preamplifiers (A1 and A2) with built-in offsets generated by unbalanced input transistor sizes. The offset value of A1 can be calculated as

$$V_{\mathrm{OS}} = \sqrt{\frac{2\,(I_B/2)}{k_n\,(W/L)_1}} - \sqrt{\frac{2\,(I_B/2)}{k_n\,(W/L)_2}} = \left(1 - \frac{1}{\sqrt{N}}\right)\sqrt{\frac{I_B}{k_n\,(W/L)_1}} = \left(1 - \frac{1}{\sqrt{N}}\right) V_{\mathrm{OV1}} \quad (7)$$

where $k_n = \mu_n C_{\mathrm{OX}}$, I_B is the bias current of each amplifier, N is the size ratio between the two input transistors, and V_{OV1} is the gate overdrive voltage of $\mathrm{M_1}$. Note that I_B is chosen to fulfill the minimum load current requirement of the NMOS LDO, and the number N is 2 for A1, and 4 for A2 in this prototype. To reduce the noise at V_{OUT}, the digital control circuits are powered up by V_{DDD}, while the amplifiers which consume constant current are powered up by V_{OUT}.

TABLE III
COMPARISON WITH STATE-OF-THE-ART FULLY INTEGRATED CP DESIGNS

CP Work	[7] 2011	[25] 2012	[8] 2013	[33] 2014	[34] 2014	This Paper
Process	90 nm	90 nm	65 nm	22 nm	32 nm SOI	65 nm
Topology	1/2	1/2, 2/3	1/3, 2/5	1/2, 2/3, 4/5, 1	1/2, 2/3	1/2+LDO
Phase No.	10	41	18	8	16	18
$V_{\rm OUT}$	1.3–1.5 V	0.7 V	1 V	0.45–1 V	0.7–1.1 V	1 V
$C_{\rm FLY}$	2 nF	1.148 nF	3.88 nF	1.6 nF	32×1 nF	0.54 nF
C_L or C_X	3.2 nF	84 pF	0	100 pF	0	0.26 nF
$f_{\rm SW}$ at $\eta_{\rm Peak}$	70 MHz	50 MHz	N/A	250 MHz	125 MHz	90 MHz
$I_{\rm IN,\ noload}$	85 μA	N/A	N/A	N/A	N/A	161 μA
$\eta_{\rm CP,Peak}$	77%	81%	74.3%	82.7%	90.0%	80.3%
$\eta_{\rm CP+LDO,Peak}$	N/A	N/A	N/A	N/A	N/A	76.2%
Power Density at $\eta_{\rm Peak}$	0.05 W/mm^2	0.039 W/mm^2	0.19 W/mm^2	0.25 W/mm^2	3.71 W/mm^2	0.24 W/mm^2
$V_{\rm OUT}$ Ripple	N/A	3.8 mV	N/A	43 mV	30 mV	2 mV
$FOM_{\rm Ripple}$	N/A	0.485 n	N/A	2.92 n	3.13 n	0.08 n

TABLE IV
COMPARISON WITH PRIOR DC–DC CONVERTER WORKS WITH SERIES LDO

DC–DC + LDO	[18] 2009	[19] 2010	[20] 2011	[21] 2011	[22] 2013	This Work
Process	130 nm	0.35 μm	0.18 μm	0.35 μm	0.25 μm	65 nm
Topology	CP+LDO	Buck+LDO	Buck+LDO	Boost+LDO	Buck+LDO	CP+LDO
$V_{\rm OUT}$	444 mV	3.3 V	1.8 V	7.7–9.7 V	1.8 V	1 V
$I_{\rm Load}$	285 nA	100 mA	100 mA	110 mA	200 mA	30 mA
$C_{\rm FLY}$ or L	0.6 nF	80 μH	N/A	4.7 μF + 10 μH	1 μH	0.54 nF
C_L or C_X	0.2 nF	10 μF	N/A	10 μF	2 × 2 μF	0.26 nF
$f_{\rm SW}$ at $\eta_{\rm Peak}$	2 kHz	500 kHz	N/A	1.76 MHz	6 MHz	90 MHz
$\eta_{\rm DC-DC}$	N/A	87%	N/A	90%	93.7%	80.3%
$\eta_{\rm DC-DC+LDO}$	56%	79.7%	73%	N/A	86.5%	76.2%
$V_{\rm OUT}$ Ripple	25 mV	∼150 mV	10 mV	N/A	1 mV	2 mV

IV. MEASUREMENT AND SIMULATION RESULTS

The chip micrograph is shown in Fig. 11. The effective area is 0.154 mm^2, including the NMOS-LDO that occupies only 0.01 mm^2. The Fast-RAP digital controller, which dynamically enables the 18 phases, only occupies negligible silicon area. An on-chip load with 2-bit resolution for measurement is implemented by resistors connected in series with switches driven by on-chip inverter buffers. The rising and falling edges of the load current are less than 200 ps to mimic the fast load changes.

Fig. 12 shows the measured output spectrums of $V_{\rm CP}$ and $V_{\rm OUT}$ with $V_{\rm IN} = 2.5$ V, $V_{\rm OUT} = 1.0$ V, and $f_{\rm SW} = 90$ MHz. With an on-chip load current $I_{\rm Load} = 10$ mA, the maximum noise power at $V_{\rm CP}$ (due to the output ripple at $V_{\rm CP}$) is –49.1 dBm, corresponding to 2.2 $\rm mV_{P\text{-}P}$ on a 50-Ω resistor, while the noise power at $V_{\rm OUT}$ is only –64.1 dBm (0.39 $\rm mV_{P\text{-}P}$). Ripple attenuation of 15 dB from $V_{\rm CP}$ to $V_{\rm OUT}$ is measured. With $I_{\rm Load} = 20$ mA, the maximum noise power at $V_{\rm CP}$ is –40.9 dBm (5.7 $\rm mV_{P\text{-}P}$), while the noise power at $V_{\rm OUT}$ is –54.3 dBm (1.22 $\rm mV_{P\text{-}P}$), which gives a ripple attenuation of 13.4 dB. These results matched well with the simulated curves shown in Fig. 8, which means that output voltage ripples are well-attenuated by the merged LDO. Ripples of the light-load cases with fewer phases are smaller than that of the heavy-load cases for two reasons. First, the relatively large load capacitor C_X that occupied 30% of the effective chip area will not be discharged as much for a light-load current. Second, the 50-mV dropout case for the LDO only occurs at the maximum load, and the $V_{\rm DS}$ of $\rm M_{N1}$ is larger at light-load cases; thus, better ripple rejection from $V_{\rm CP}$ to $V_{\rm OUT}$ can be provided by the LDO.

Fig. 13 shows the measured load transient waveforms of $V_{\rm CP}$ and $V_{\rm OUT}$ with fast transient on-chip load. By installing the 3×Clk for the controller, the phase number can quickly be changed from 1/3/9 at light load to 18 at heavy load. Consequently, the voltage droop at $V_{\rm CP}$ is reduced, which guarantees that the $V_{\rm OUT}$ droop will not be deteriorated by $V_{\rm CP}$ variation. The undershoot voltage of $V_{\rm OUT}$ is 83 mV for a 20-mA current step.

The overall efficiency $\eta_{\rm CP+LDO}$ is measured, and the CP efficiency $\eta_{\rm CP}$ is derived as

$$\eta_{\rm CP} = \frac{\eta_{\rm CP+LDO}}{\eta_{\rm LDO}} \approx \frac{V_{\rm CP}}{V_{\rm OUT}} \eta_{\rm CP+LDO} \tag{8}$$

by approximating the LDO efficiency $\eta_{\rm LDO}$ to be equal to $V_{\rm OUT}/V_{\rm CP}$ as the LDO itself consumes a negligible quiescent current. Fig. 14 shows the measured $\eta_{\rm CP+LDO}$ and the derived $\eta_{\rm CP}$ versus power density, with $V_{\rm IN} = 2.5$ V, $V_{\rm OUT} = 1$ V, and $f_{\rm SW} = 90$ MHz. The peak $\eta_{\rm CP}$ is 80.3% when the peak $\eta_{\rm CP+LDO}$ is 76.2%, achieving a power density of 0.24 W/mm^2. Light-load efficiencies are limited by the switching loss and the quiescent current, and are improved by the proposed Fast-RAP scheme. The light-load efficiency could further be improved by adaptive switching frequency and adaptive switch sizing as

TABLE V
COMPARISON WITH STATE-OF-THE-ART LDO DESIGNS

LDO Work	[35] 2005	[36] 2014	[23] 2014	This Paper
Technology	90 nm	21 nm	65 nm	65 nm
$V_{\rm OUT}$	0.9 V	0.6 V	1 V	1 V
$V_{\rm Dropout}$	300 mV	50 mV	150 mV	50 mV
I_Q	6 mA	5 μA	50 μA	10 μA
$I_{\rm MAX}$	100 mA	10 mA	10 mA	30 mA
Total Cap.	600 pF	100 pF	140 pF	39 pF
PSR	N/A	N/A	−15.5 dB at 1 GHz	–12.8 dB @100 MHz
$\Delta V_{\rm OUT}$ at $T_{\rm Edge}$	90 mV at 100 ps	10 mV at 100 ns	82 mV at 200 ps	195 mV at 200 ps
Load Reg.	0.9 mV/mA	0.5 mV/mA	1.1 mV/mA	0.2 mV/mA
T_R	0.54 ns	N/A	1.15 ns	0.254 ns
$FOM_{\rm LDO}$	32 ps	N/A	5.74 ps	0.085 ps

demonstrated in [12] and [26]. Fig. 15 shows the measured $\eta_{\rm CP+LDO}$ and the derived $\eta_{\rm CP}$ with $I_{\rm Load} = 30$ mA, $V_{\rm OUT} = 1$ V, and $V_{\rm IN}$ ranging from 2.37 to 2.6 V. The overall efficiency keeps increasing as $V_{\rm IN}$ decreases because $V_{\rm CP}$ decreases accordingly, and the power dissipated by the NMOS LDO reduces with smaller drain-to-source voltage of $\rm M_{N1}$.

The breakdown of the simulated power loss of the NMOS-LDO regulated CP with $V_{\rm IN} = 2.5$ V, $V_{\rm OUT} = 1.0$ V, $f_{\rm SW} = 90$ MHz, and $I_{\rm Load} = 30$ mA is shown in Table II. In this simulated case, $\eta_{\rm CP}$ is 82.3% and $\eta_{\rm CP+LDO}$ is 77.2%. Over 80% of the power losses are caused by the conduction losses of the CP and the LDO, while the digital logics and LSs only account for less than 2% of the total power losses. Note that when the voltage conversion ratio is 1/2, the maximum achievable efficiency is $2V_{\rm OUT}/V_{\rm IN}$, which is 80% in this case.

Table III summarizes the performance comparison of the proposed CP + LDO combo with state-of-the-art fully integrated CP designs [6], [7], [25], [33], [34]. Our design achieves the smallest output ripple voltage with a power density of 0.24 W/mm^2. Since the output ripple voltage is proportional to the capacitance used and the output power delivered, in this research, a figure-of-merit (FOM) of the output ripple voltage is proposed to be defined as

$$\rm FOM_{Ripple} = \frac{V_{Ripple} \cdot C_T}{P_{MAX}} \tag{9}$$

where $V_{\rm Ripple}$ is the output ripple voltage at heavy load in the steady state, C_T is the total capacitance of $C_{\rm FLY}$ and C_L used in the switched-capacitor dc–dc converter, and $P_{\rm MAX}$ is the output power at which the ripple is measured. Here, smaller $FOM_{\rm Ripple}$ means better performance.

The performance comparison of this paper with prior dc–dc converter + LDO cascaded designs [18]–[22] is listed in Table IV. This hybrid work achieves the smallest efficiency overhead for the additional series LDO because the dropout voltage of the NMOS LDO is only 50 mV, and effectively reduces the ripple down to the level that is comparable to the design of [22] that used large off-chip capacitors.

Many fully integrated LDOs with limited on-chip capacitance (a.k.a. capacitorless LDOs) have been proposed in the past decade [35], [36]. To make a comparison of the fully integrated LDOs, an FOM of LDO is defined in [35] and widely adopted by other researchers. It reads

$$\rm FOM_{LDO} = T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}} \tag{10}$$

where $I_{\rm Q}$ is the quiescent current, and the response time $T_{\rm R}$ is a function of the total on-chip capacitance C of the LDO, load-transient glitches of the output voltage $\Delta V_{\rm OUT}$, and the maximum load current $I_{\rm MAX}$. The performance summary and comparison of the LDOs are listed in Table V. The calculated response time $T_{\rm R}$ and FOM are 0.254 ns and 0.085 ps, respectively, and both are small compared to other designs.

V. CONCLUSION

A fully integrated NMOS source-follower-based low-dropout regulated step-down switched-capacitor dc–dc converter with Fast-RAP control and < 2 mV output voltage ripple is demonstrated in 65-nm CMOS general purpose process. Instead of using an LDO with a PMOS power stage, an NMOS LDO that has the benefits of lower dropout voltage and intrinsic fast transient response is used without the need for an additional step-up CP for driving. When a heavy-load transient is detected, all phases are enabled instantly. Triggered by a proposed clock tripler, the adaptive phase scheme for efficiency optimization is implemented without sacrificing the transient response. The regulator with a dropout voltage of 50 mV only amounts to 4.1% efficiency overhead and 6.5% area overhead. Operating at 90 MHz with the adaptive 18-phase interleaving scheme, the output voltage ripples at the CP output are small, and have been further attenuated at the LDO output. In fact, the smallest output ripple FOM is achieved.

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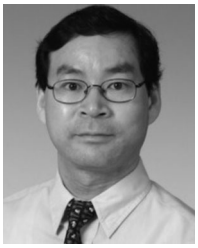

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