A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out}

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***Abstract*— This paper describes a sub-1-V 2.4-GHz ZigBee transmitter (TX) with scalable output power (P_{out}) and system efficiency. It features a function-reuse class-F topology unifying the digital-controlled oscillator (DCO) and power amplifier (PA), designated as DCO-PA. Unlike the existing current-reuse topologies that rely on transistor stacking, here the power consumption of the DCO and PA-driver is absorbed into the DCO-PA without losing the voltage headroom, while allowing a low supply voltage. The DCO-PA also benefits from a six-port transformer with customized coupling coefficients and turn ratios to jointly perform the functions of resonant tank and output matching network, saving the chip area. A fractional-N all-digital phase-locked loop (ADPLL) realizes a two-point data modulation. Its phase-interpolated time-to-digital converter prevents time-consuming calibration. The entire TX fabricated in 65-nm CMOS occupies a 0.39-mm^2 active area. The standalone DCO-PA shows a peak efficiency of 26.2% at a 6-dBm P_{out}, and a back-off efficiency of 17.7% at a −4.3 dBm P_{out} under a scalable supply voltage (0.3–0.7 V). The system efficiency, including the ADPLL, is 22.6% (14.5%) at 6-dBm (0-dBm) P_{out}. The HS-OQPSK modulated output complies with the ZigBee spectral mask with an adequate margin and the error vector magnitude is 2.29%.**

***Index Terms*— Back-off power efficiency, class-F, CMOS, digital-controlled oscillator (DCO), matching network (MN), output power, power amplifier (PA), transformer, transmitter (TX), ultralow-power (ULP), ZigBee.**

I. Introduction

ULTRALOW-POWER (ULP) short-range radios are the key enabler of a wide variety of Internet-of-Things products such as wearables for healthcare [1], [2]. The small physical dimension of those products also significantly limits the size of the battery, pressuring the power budgets of the radios at both architectural and circuit levels. For the common 2.4-GHz short-range wireless standards (e.g., ZigBee or Bluetooth), although research works have demonstrated a sub-1-mW receiver (RX) [3] and 3–5 mW transmitters (TXs) [4]–[6], robust industrial products [7], [8] still consume larger than 6.3 mW for receiving or transmitting. For the ULP TXs, the polar architecture [7] is promising as an ULP ZigBee TX since it can easily embed frequency modulation (FM) inside the phased-locked loop (PLL) [Fig. 1(a)]. To reduce the injection pulling of the voltage-controlled oscillator (VCO) when the power amplifier (PA) starts up, the VCO normally operates at the double of the transmitting frequency (f_{o}), consuming a significant amount of power [4], [7]. For instance, in [7] when transmitting an output power (P_{out}) of 0 dBm, the PA consumes 3.4 mW, while the VCO (1.1 mW), differential-to-single-ended (D2S) converter (0.8 mW) and PA-driver (1.5 mW) together draw another 3.4 mW, lowering the system efficiency to ∼9.9%. If a digital-controlled oscillator (DCO) directly operating at f_{o} is employed, the PLL has to provide a high bandwidth mode for fast recovery from the PA pulling when the PA starts up [5]. An alternative described in [6] stacks the PA atop the VCO for current re-use enhancing system efficiency [Fig. 1(b)]. Yet, it will limit the maximum P_{out} (−1 dBm) due to the reduced voltage headroom. In fact, the power consumption of its VCO is just 41.7% of that of the PA, limiting the system efficiency (17.5%). Also, the need of off-chip passives as the output matching network (MN) raises the system cost.

To save both power and cost, it is worth to explore an ULP TX architecture that allows a high system efficiency, while minimizing the number of external components and on-chip inductors (transformers). This paper proposes a function-reuse class-F DCO-PA [Fig. 1(c)]. This function-reuse technique effectively allows the DCO-PA to absorb the power consumption of the DCO and PA-driver, while preserving the voltage headroom unchanged. Thus, it is promising to achieve a high system efficiency at different values of P_{out} under a scalable supply voltage. Importantly, by merging the DCO and PA, we can architecturally avoid the issue of injection pulling [7] between them when the PA starts up (i.e., no need of high-

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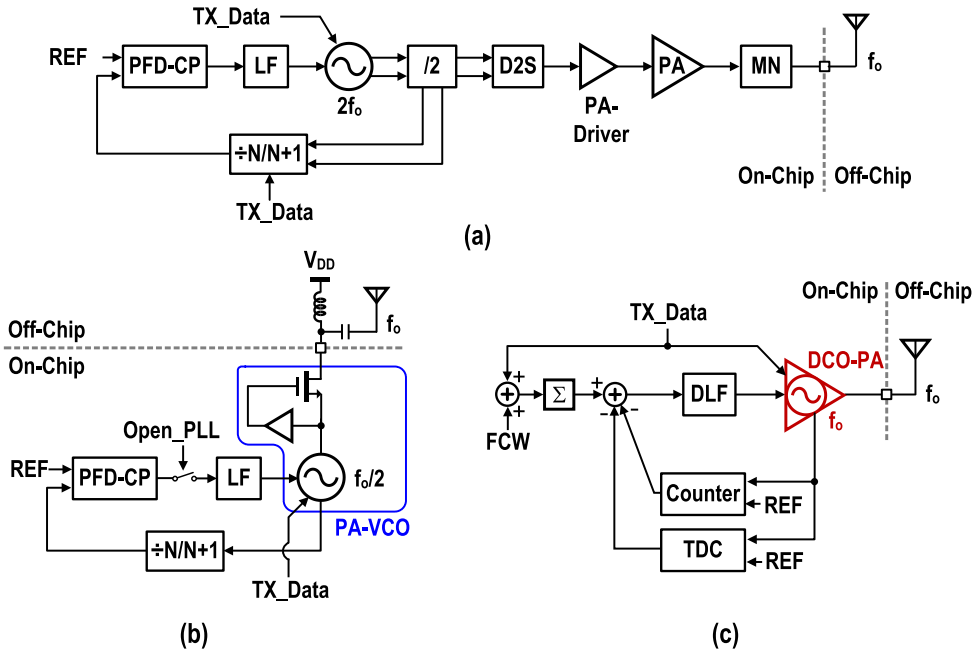

Fig. 1. ULP TXs using (a) separated VCO and PA [7], (b) current re-use PA-VCO [6], and (c) proposed function re-use DCO-PA. f_o is the operating frequency. PFD: phase-frequency detector. CP: charge pump. LF: loop filter. TDC: time-to-digital converter. DLF: digital loop filter.

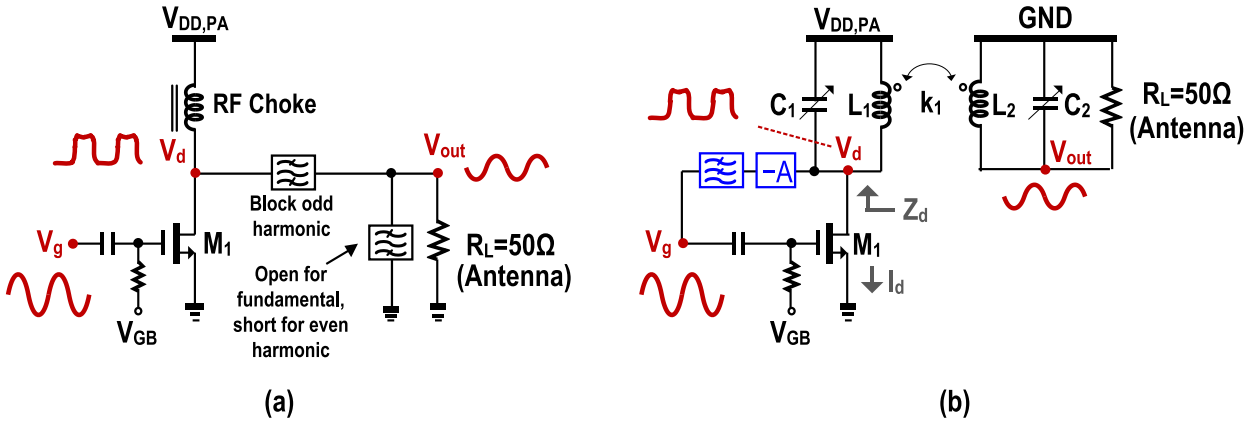

Fig. 2. (a) Typical class-F PA. (b) Conceptual diagram of the proposed class-F DCO-PA using a transformer to boost the third harmonic voltage at V_d.

frequency VCO/DCO and dividers). Finally, instead of using separated inductors (transformers) for the resonant tank and on-chip output MN [4], [7], we propose a six-port transformer to combine both functions, reducing the overall chip area.[1]

Section II describes the principle of the class-F DCO-PA. Section III discusses the circuit implementation including the design of its six-port transformer. Section IV presents the key features of the fractional-N all-digital PLL (ADPLL). Section V reports the experimental results, and finally, Section VI draws the conclusions.

II. Principle of the Class-F DCO-PA

The concept of making the PA act as an oscillator was firstly introduced in [9] to reduce the power of the driving stage of the class-E PA. However, a separate VCO is still necessary to generate the input signal to lock the PA output frequency. In [10], the function of VCO and PA are merged by connecting the antenna across the source terminals of the cross-coupled pair for wireless sensor networks applications, which suffers from a limited maximum output power (−4.4 dBm) and power efficiency (∼13%).

To improve the output power and power efficiency, the DCO-PA based on the class-F PA architecture is introduced in this paper. Fig. 2(a) exhibits the class-F PA that utilizes odd voltage harmonics to resemble a square-wave voltage at the drain node (V_d), thus reducing the voltage across the transistor (M_1) when it is conducting [11], [12]. Theoretically, a maximally flat class-F PA can achieve a power efficiency of ∼88% by simply blocking the third harmonic [13].

Inspired by the class-F PA and class-F oscillator in [14], the proposed class-F DCO-PA [Fig. 2(b)] employs a transformer tank to resemble the filters in Fig. 2(a) that block the third harmonic and short the second harmonic by realizing two drain-impedance peaks located at the fundamental and

[1]The transformer tank has been widely used in the wideband VCO design to cover a wide frequency tuning range without using multiple inductors [15].

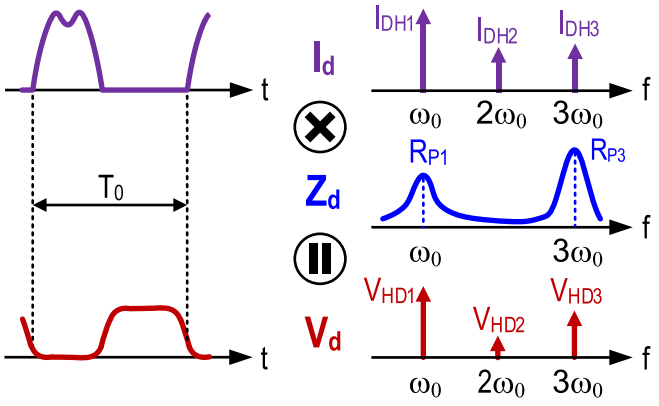

Fig. 3. Current and voltage waveforms of the proposed class-F DCO-PA in the time and frequency domains.

third-harmonic frequencies. The multiplication of the drain impedance (Z_d) by the third harmonic component of the drain current (I_d) generates the third harmonic component at V_d, resulting in a pseudo-square voltage waveform at V_d (Fig. 3). The square voltage waveform of V_d in the class-F DCO-PA (Fig. 3) is similar to that of the class-F oscillator [14], but the current waveform of I_d is no longer a square wave due to the lack of a tail current source in the PA design which results in a small third harmonic component I_{DH3}. To keep a good square waveform of V_d, the gate voltage of the M_1 in Fig. 2(b) is biased well below the V_{TH} to boost the ratio of $I_{\mathrm{HD3}}/I_{\mathrm{DH1}}$. Thus the current waveform deviates from the ideal half sinusoidal wave of a typical class-F PA. Also, the tank impedance peak at the third harmonic is designed much higher than that at the fundamental frequency[2] to compensate the decrease of I_{HD3} and thus still maintain a large V_{HD3}.

To self-oscillate the DCO-PA, the inverted and amplified V_d is fed back to the gate node of M_1 to fulfill the oscillation criteria, i.e., a loop gain >1 and a phase shift of 0°. A lowpass filter (LPF) can be inserted between the drain and gate nodes of M_1 to suppress the third harmonic component of the gate voltage (V_g), so that M_1 can operate as a transconductance amplifier, and the waveform of I_d can be determined. From the oscillator's perspective, a pseudo-square voltage waveform at the drain node is desirable since it can reduce the output phase sensitivity to the noise sources (i.e., the transistors and tank resistors), improving the output phase noise [14].

The locations of the two resonant frequencies are related to the sizing of the transformer, efficiency of the output MN, and load impedance R_L of the PA. Since the PA is expected to directly drive the antenna, the output secondary coil L_2 is connected to $R_L = 50\ \Omega$ [Fig. 2(b)]. Fig. 4(a) depicts the schematic of a transformer tank considering the losses from the primary (L_1) and secondary (L_2) coils, where r_{L1} and r_{L2} model the equivalent series resistance of L_1 and L_2, respectively. k_1 is the magnetic coupling coefficient between the two coils. Substituting the transformer by its T-model leads to the equivalent circuit for the MN shown in Fig. 4(b). By further assuming that $Q_{L1} = \omega L_1/r_{L1}$ and $Q_{L2} = \omega L_2/r_{L2}$ are high (i.e., $Q_{L1} \to \infty$ and $Q_{L2} \to \infty$), the drain impedance Z_d becomes

$$Z_d = \omega L_1 \frac{-(1-k_1^2)+j\,Q_{\mathrm{load}}\omega_1^2\left[\omega_2^2-\omega^2(1-k_1^2)\right]}{Q_{\mathrm{load}}\left[\omega^4(1-k_1^2)-\omega^2(\omega_1^2+\omega_2^2)+\omega_1^2\omega_2^2\right]+j\omega_2^2\left[\omega_1^2-\omega^2(1-k_1^2)\right]} \tag{1}$$

where $\omega_1 = 1/(L_1C_1)^{1/2}$, $\omega_2 = 1/(L_2C_2)^{1/2}$, and $Q_{\mathrm{load}} = R_L/\omega L_2$. The resonant frequencies of the transformer tank can be obtained by satisfying the condition where the phase of Z_d equals to zero. For the case that Q_{load} is extremely high (i.e., $Q_{\mathrm{load}} \to \infty$), the tank is reduced to that in a transformer-based dual-mode VCO and two possible resonant frequencies ω_L and ω_H would exist [15]. On the other hand, if Q_{load} is extremely low (i.e., $Q_{\mathrm{load}} \to 0$), the tank will have only one resonant frequency

$$\omega_{\mathrm{osc}} = \frac{\omega_1}{\sqrt{1-k_1^2}}. \tag{2}$$

For other practical values of Q_{load}, two resonant frequencies are generated which only depend on $\omega_{1,2}$, k_1, and Q_{load} according to (1). To realize a pseudo-square waveform across the tank, it is preferable that the DCO-PA oscillates at the lower resonant frequency ω_L, and ω_H is set as $3\times$ of ω_L. Fig. 5(a) plots the simulated contour curves of $\omega_H/\omega_L = 3$ as a function of $X = (\omega_1/\omega_2)^2$ and k_1 for different values of Q_{load}. Differing from the case that $Q_{\mathrm{load}} \to \infty$ where two possible values of X exist to guarantee $\omega_H/\omega_L = 3$ when $k_1 < 0.8$, only one solution of X exists for a particular k_1 when Q_{load} is small. As expected, the range of k_1 and X that guarantees $\omega_H/\omega_L = 3$ becomes narrower with the decreasing of Q_{load}, since only one resonant frequency exists when $Q_{\mathrm{load}} \to 0$.

The transformer tank also serves as the MN of the PA, and its loss would inevitably degrade the overall PA efficiency

$$\begin{aligned}\eta_{\mathrm{PA}} &= \frac{P_{\mathrm{dc}} - P_{\mathrm{loss},T} - P_{\mathrm{loss},M}}{P_{\mathrm{dc}}} \\ &= \frac{P_{\mathrm{dc}} - P_{\mathrm{loss},T}}{P_{\mathrm{dc}}} \cdot \frac{P_{\mathrm{dc}} - P_{\mathrm{loss},T} - P_{\mathrm{loss},M}}{P_{\mathrm{dc}} - P_{\mathrm{loss},T}} \\ &= \eta_{\mathrm{PA},T} \cdot \eta_M\end{aligned} \tag{3}$$

where P_{dc}, $P_{\mathrm{loss},T}$, and $P_{\mathrm{loss},M}$ are the dc power consumption, power losses on the transistors and MN, respectively. $\eta_{\mathrm{PA},T} = (P_{\mathrm{dc}} - P_{\mathrm{loss},T})/P_{\mathrm{dc}}$ is the PA efficiency without considering the loss from the MN, and $\eta_M = (P_{\mathrm{dc}} - P_{\mathrm{loss},T} - P_{\mathrm{loss},M})/(P_{\mathrm{dc}} - P_{\mathrm{loss},T})$ is the power efficiency of the MN. Typically, the maximum efficiency of a PA is achieved when its output reaches rail-to-rail [6]. Thus assuming the square wave for the drain voltage, the output power P_{out} of the PA can be given by

$$P_{\mathrm{out}} = \eta_M \cdot \frac{32V_{\mathrm{DD,PA}}^2}{\pi^2 R_{P1}} \tag{4}$$

where $R_{P1} = Z_d(\omega_0)$ is the impedance of the transformer tank at the resonant frequency ω_0, and $V_{\mathrm{DD,PA}}$ is the supply

[2]In the class-F VCO [14], the tank impedance peak at the 3rd harmonic is lower than that at the fundamental frequency since a large I_{HD3} is available in the square wave I_d waveform.

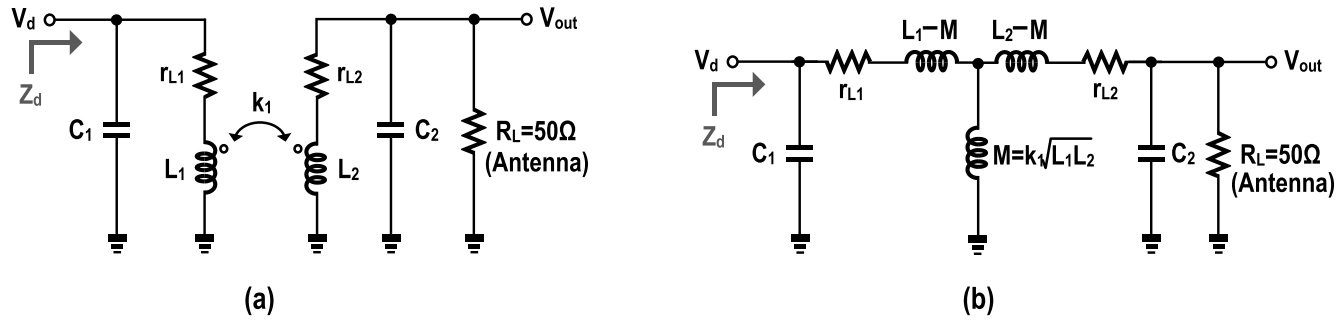

Fig. 4. (a) Schematic and (b) equivalent circuit of the transformer tank when considering the loss from the coils L_1 and L_2.

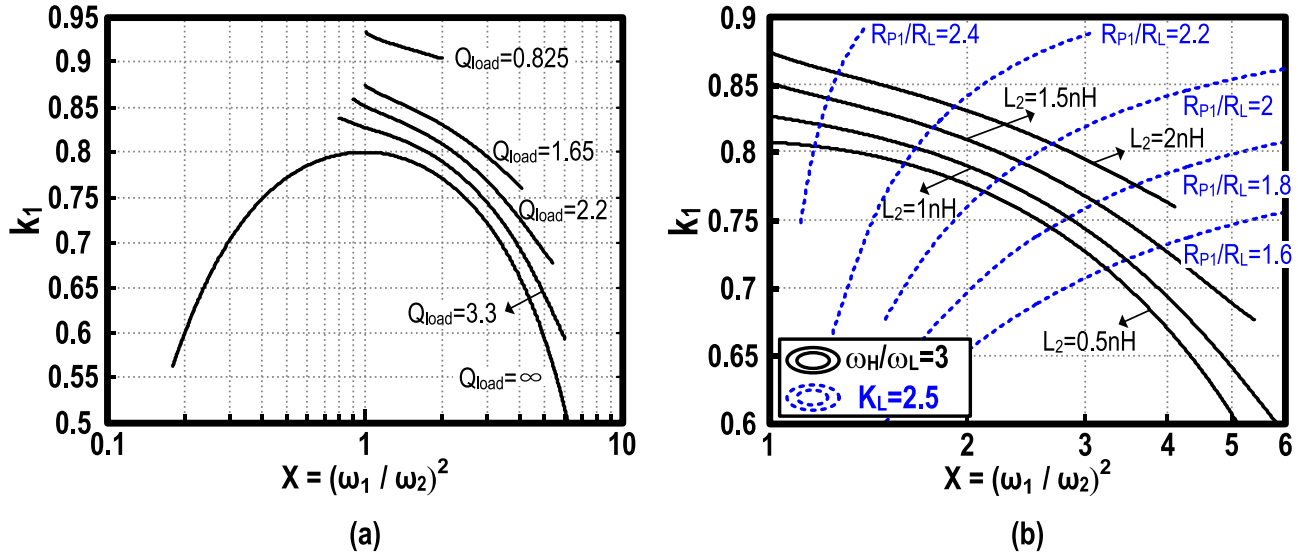

Fig. 5. (a) Contour plot of $\omega_H/\omega_L = 3$ as a function of $X = (\omega_1/\omega_2)^2$ and k_1 for different values of Q_{load}. (b) Contour plot of $\omega_H/\omega_L = 3$ and $K_L = 2.5$ as a function of $X = (\omega_1/\omega_2)^2$ and k_1 for different values of L_2 and R_{P1}/R_L.

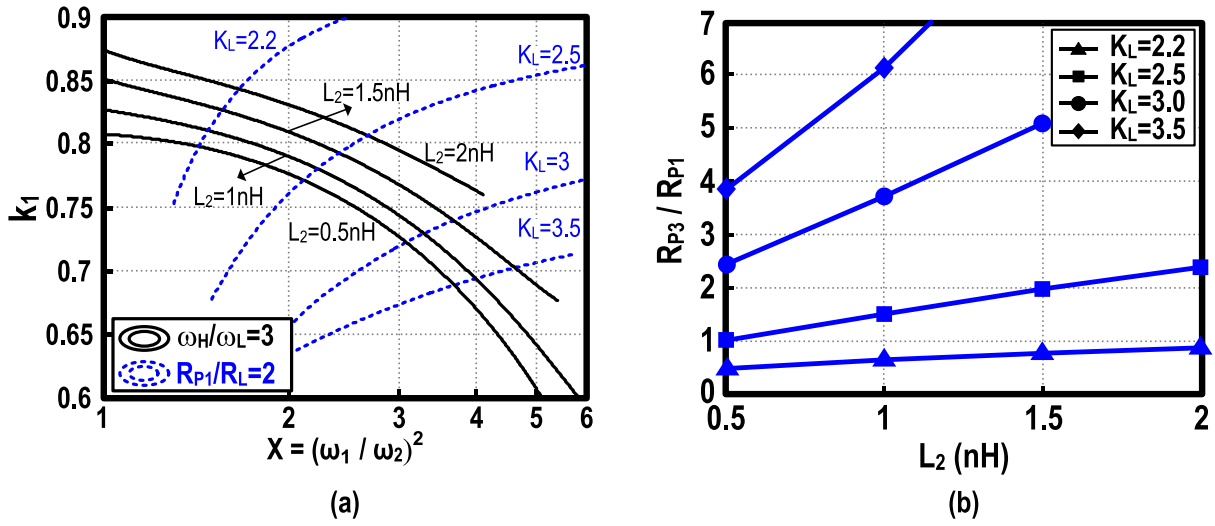

Fig. 6. (a) Contour plot of $\omega_H/\omega_L = 3$ and $R_{P1}/R_L = 2$ as a function of $X = (\omega_1/\omega_2)^2$ and k_1 for different values of L_2 and K_L. (b) Ratio between the impedances at third harmonic and fundamental frequencies as a function of L_2 ($Q_{L1} = Q_{L2} = 10$).

of the PA. By choosing $R_{P1} = 2R_L = 100\ \Omega$ and assuming $\eta_M \approx 55\%$, a $V_{\text{DD,PA}}$ of 0.53 V (0.265 V) will be adequate to generate a P_{out} of 7 dBm (1 dBm).[3] The required $V_{\text{DD,PA}}$ can be halved by using the differential topology[4] that employed in this paper. Since the minimum supply voltage for the ADPLL is 0.7 V, $R_{P1} = 100\ \Omega$ can guarantee a maximum output

[3]The simulation excluded the loss from the bondwires and capacitors, thus P_{out} is set 1 dB higher than the target of 6 dBm.

[4]Assuming the differential and single-ended structures employ the same transformer tank and thus achieve the same R_{P1}. Since the voltage swing across R_{P1} can be doubled in the differential structure, the required V_{DD} for delivering the same maximum output power can be halved.

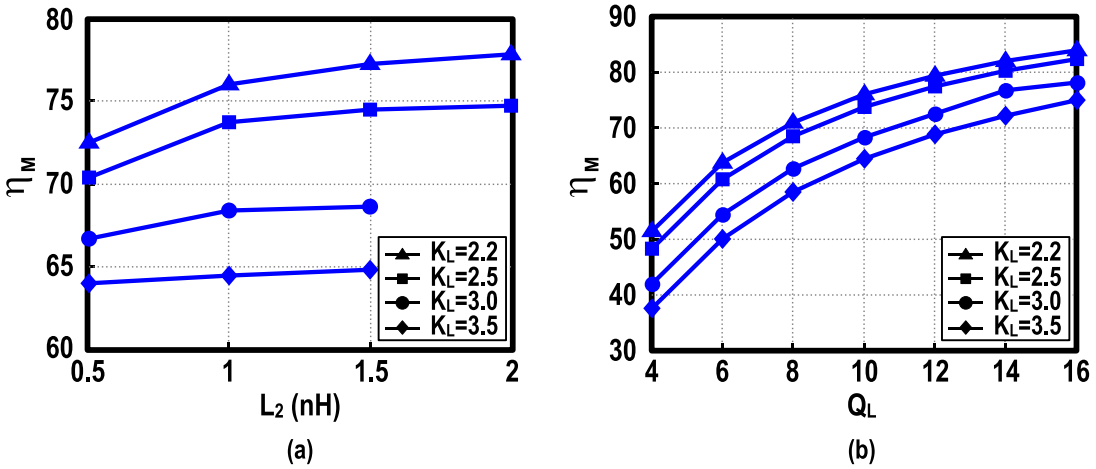

Fig. 7. Efficiency η_M of the MN as a function of (a) L_2 ($Q_{L1} = Q_{L2} = 10$) and (b) $Q_L = Q_{L1} = Q_{L2}$ ($L_2 = 1$ nH).

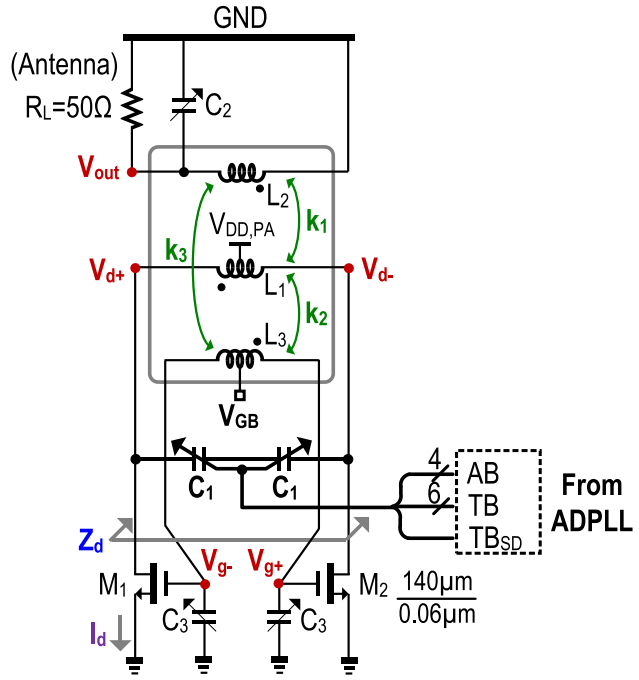

Fig. 8. Schematic of the proposed class-F DCO-PA.

TABLE I

COMBINATIONS OF L_3 AND k_2 TO KEEP A CONSTANT $P_{out} = 7$ dBm ($L_1 = 2.5$ nH, $L_2 = 1$ nH, AND $k_1 = 0.7$)

L_3 (nH)	10	8	2.8	0.7	0.55
k_2	0.25	0.35	0.45	0.55	0.65

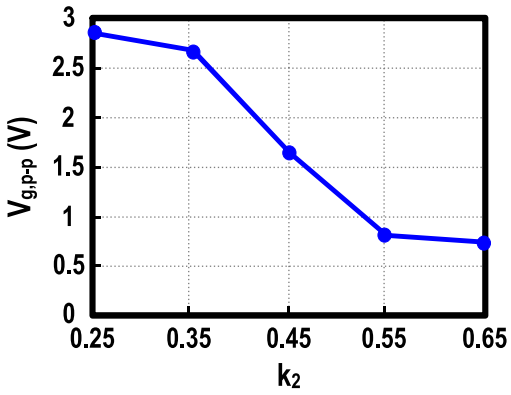

Fig. 9. Simulated voltage swing of the gate voltage $V_{g,p-p}$ versus k_2 at $P_{out} = 7$ dBm and $V_{GB} = 0.24$ V.

power of 7 dBm at $V_{DD} = 0.7$ V when considering non-ideal square-wave voltage waveform and reduced voltage swing at the drain node as will be shown in Section III-B.

From simulations, the tank impedance at the fundamental frequency, i.e., R_{P1}, and thus the transformer gain defined as R_{P1}/R_L strongly depends on the inductance ratio $K_L = L_1/L_2$ rather than the absolute values of L_1 and L_2. A large K_L would result in a large R_{P1}/R_L if k_1 and X are kept the same. For a certain R_L, the relationship between R_{P1}/R_L and k_1 (X) can be studied through the contour plots as shown in Fig. 5(b). A large k_1 (X) would result in a large R_{P1}/R_L if X (k_1) is kept constant. To study tank impedance at the third harmonic frequency, i.e., R_{P3}, $\omega_H/\omega_L = 3$ must be guaranteed. Fig. 6(a) plots the simulated contour curves of $R_{P1}/R_L = 2$ along with the contour curves of $\omega_H/\omega_L = 3$ as functions of X and k_1 for different values of K_L by assuming Q_{L1} and Q_{L2} are high. The intersection points between the contour curves of ω_H/ω_L and R_{P1}/R_L give the possible values of k_1, X, L_2, and K_L that meet the requirements of $\omega_H/\omega_L = 3$ and $R_{P1}/R_L = 2$ at the same time. By using the k_1 and X values obtained from Fig. 6(a) and assuming $Q_{L1} = Q_{L2} = 10$, we can obtain the relationship between R_{P3}/R_{P1} and K_L, which indicates that a large K_L which requires a small k_1 and a large X to maintain $\omega_H/\omega_L = 3$ also helps to boost the R_{P3}/R_{P1}.

By using the k_1 and X values obtained from the intersection points between the contour curves of ω_H/ω_L and R_{P1}/R_L in Fig. 6(a) again, we can obtain the relationship between η_M and L_2 (and the inductor Q_L) under the same voltage swing of V_d as shown in Fig. 7(a) and (b). As expected,

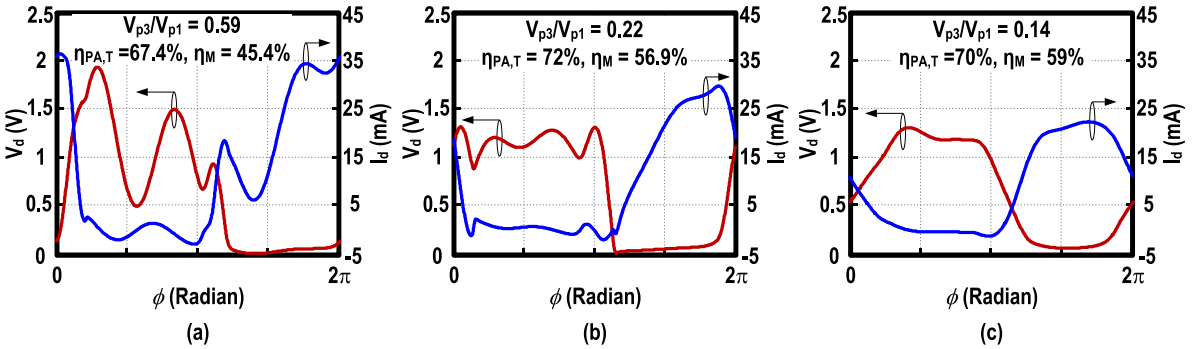

Fig. 10. Simulated drain voltage and current waveforms of M_1 at $V_{GB} = 0.24$ V and (a) $k_2 = 0.25$, (b) $k_2 = 0.45$, and (c) $k_2 = 0.65$.

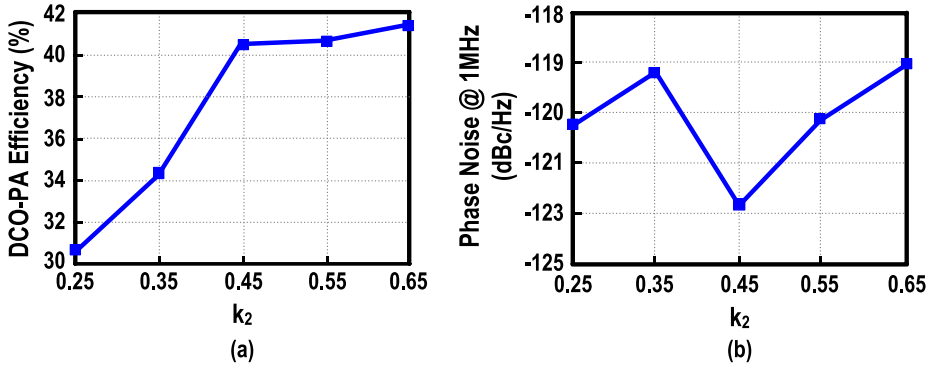

Fig. 11. Simulated (a) efficiency and (b) phase noise of DCO-PA versus k_2 at $P_{out} = 7$ dBm and $V_{GB} = 0.24$ V.

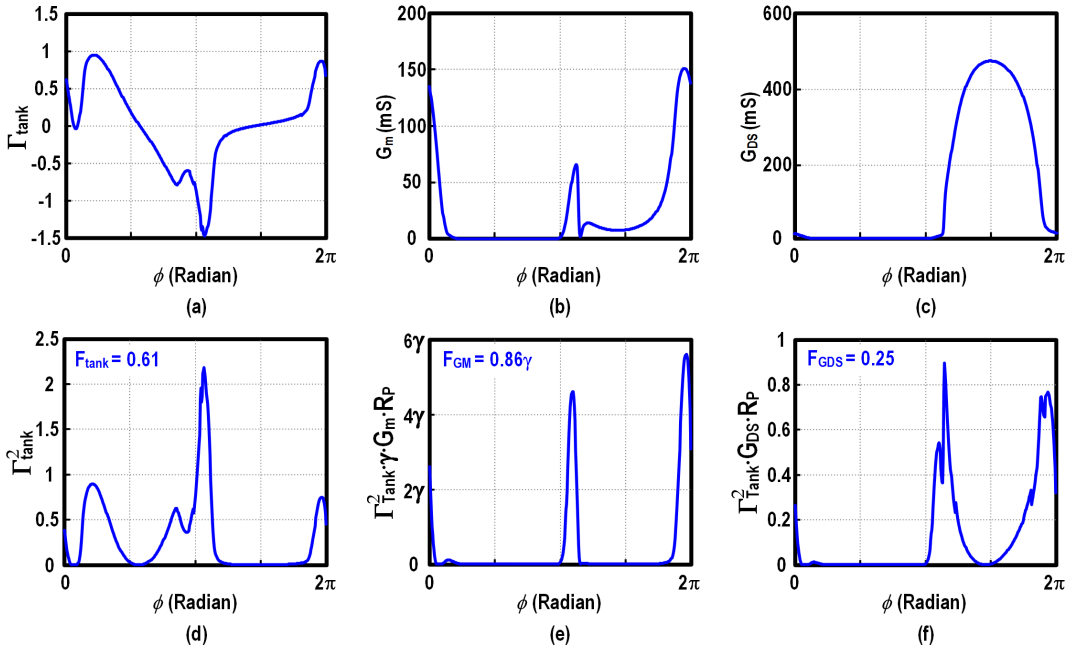

Fig. 12. Simulated (a) tank ISF, (b) Gm of M1/M2, (c) G_{DS} of M1/M2, (d) tank effective noise factor, (e) G_m effective noise factor and (f) G_{DS} effective noise factor of the DCO-PA at $k_2 = 0.45$, $P_{out} = 7$ dBm and $V_{GB} = 0.24$ V.

η_M increases with the Q_{L1} and Q_{L2} as shown in Fig. 7(b). Generally, to boost η_M implies to have larger Q_{L1} and Q_{L2}. Thus, both the primary and secondary coils of the planar transformer should be realized with maximum Q_{L1} and Q_{L2}. According to Fig. 7(a), we can also improve η_M by choosing a small K_L and a large k_1. On the other hand, the transformer's geometry must be well considered because it restricts the values of K_L and k_1. Typically, a tightly coupled transformer

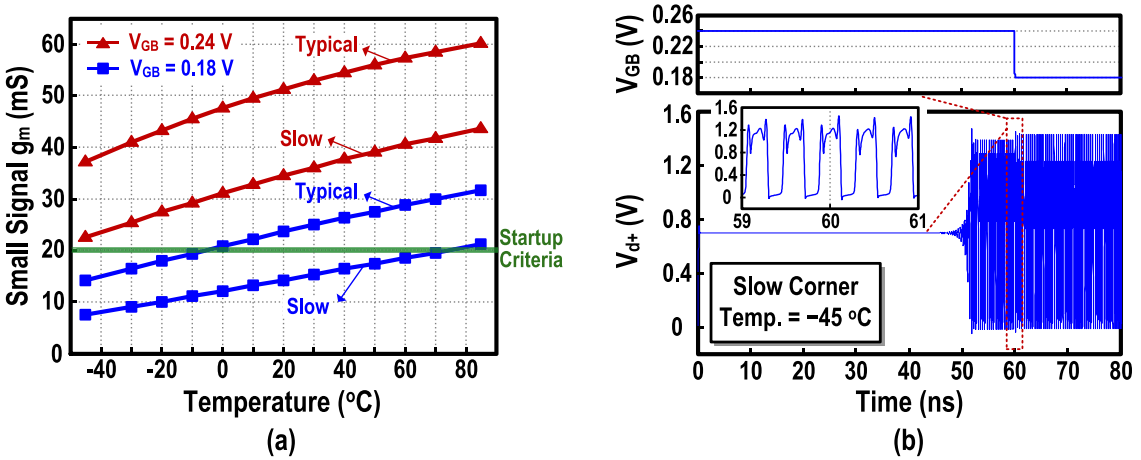

Fig. 13. Simulated (a) small signal g_m of M_1/M_2 versus temperature at different process corners and (b) voltage waveforms during startup under the slow corner and the temperature of −45 °C.

with a turn ratio of 2:1 can provide a $K_L \approx 2.5$ and a high k_1 of 0.7–0.8. For $K_L = 2.5$, η_M can be improved with L_2 but will saturate when $L_2 \geq 1$ nH. A large L_2 is not favored since it increases the transformer size and thus the chip area. As a result, $L_2 = 1$ nH is chosen, which results in a η_M of 73% when $Q_{L1} = Q_{L2} = 10$. Thus, for a maximally flat class-F PA with $\eta_{PA,T} = 88\%$, the maximum overall PA efficiency by using the transformer tank is 64.2% according to (4). By choosing $K_L = 2.5$ and $L_2 = 1$ nH, a $k_1 = 0.78$ is required to guarantee $\omega_H/\omega_L = 3$ [Fig. 6(a)] and a high $R_{P3} = 1.5R_{P1}$ can also be achieved [Fig. 6(b)].

III. Implementation of the Class-F DCO-PA

A. Circuit Implementation

Fig. 8 illustrates the structure of the proposed Class-F DCO-PA implemented differentially, with its output transformer serving as a D2S voltage converter, suppressing the emission of all even harmonics at V_{out}. When compared with its single-ended counterpart, the differential topology also helps to reduce by half the required supply voltage for a given output power. The implementation of the inverting amplifier and LPF from Fig. 2(b) uses another inductor L_3 magnetically coupled to L_1. Although the schematic of the class-F DCO-PA looks similar to that of the class-F VCO [14] by removing the coil L_2 and the output loading, the proposed class-F DCO-PA mainly relies on the tightly coupled coils L_1 and L_2 at drain and output nodes to generate the tank impedance peaks at the fundamental and third harmonic frequencies and the coil L_3 is loosely coupled to L_1 and L_2 as discussed later, while the class-F VCO relies on the tightly coupled coils L_1 and L_3 to generate the tank impedance peaks. The simulated voltage gain from V_d to V_g at the fundamental frequency ($\omega_0 = 2.4$ GHz) is ~1.5 dB, and the rejection ratio for third harmonic is ~14 dB. In the simulations $K_L = 2.5$ and $L_2 = 1$ nH are kept unchanged, but $k_1 = 0.7$ is chosen which is smaller than the value ($k_1 = 0.78$) obtained in Section II since it is the maximum value of the coupling coefficient that can be achieved for a 2:1 transformer confirmed by the electromagnetic (EM) simulation. The coupling through k_3 can compensate the decrease of k_1 and still guarantee $\omega_H/\omega_L = 3$

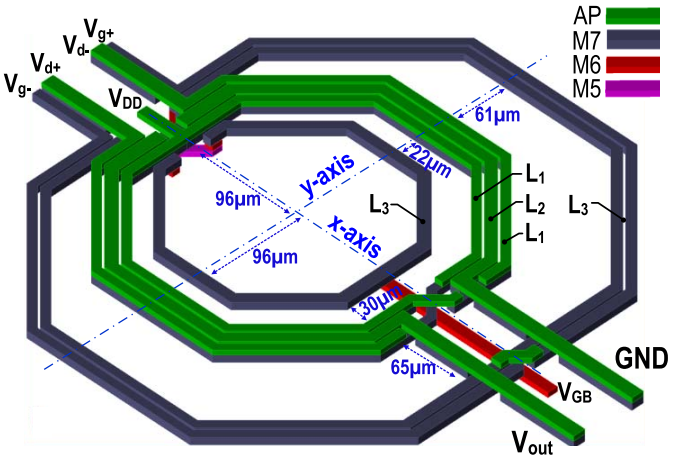

Fig. 14. Layout of the six-port transformer in the employed seven-metal 65-nm CMOS process.

and $R_{P1} = 100\ \Omega$. Furthermore, EM simulations confirm the practical quality factors $Q_{L1} = 8.2$, $Q_{L2} = 5.6$, and $Q_{L3} = 5.9$. Another reason why the inverted V_d is not directly fed back to the gate node (i.e., connecting $V_{d+/-}$ to $V_{g-/+}$ without adding L_3) is to guarantee a unique oscillation frequency at ω_L. As explained in [14] and [16], the oscillation condition is met at both ω_L and ω_H with the negative transconductance directly connected to the drain nodes, which indicates the DCO-PA may oscillate at either ω_L and ω_H during the startup. The circuit topology that feeds back the inverted V_d to the gate node in Fig. 8 avoids the multi-oscillation problem since Z_{31} (defined as V_g/I_d) fulfills the phase condition only at the frequency ω_L.

The DCO-PA has three sets of variable capacitors. For frequency acquisition and tracking the ADPLL controls the 10 bits of C_1 at the drain node. To withstand process variations and correct the antenna impedance mismatch (i.e., VSWR) we utilize the C_2 (5 bits) and C_3 (4 bits).

When integrating the TX into a transceiver, one possible solution to avoid adding a separate VCO and PLL for the RX is to insert a switch between the DCO-PA output and

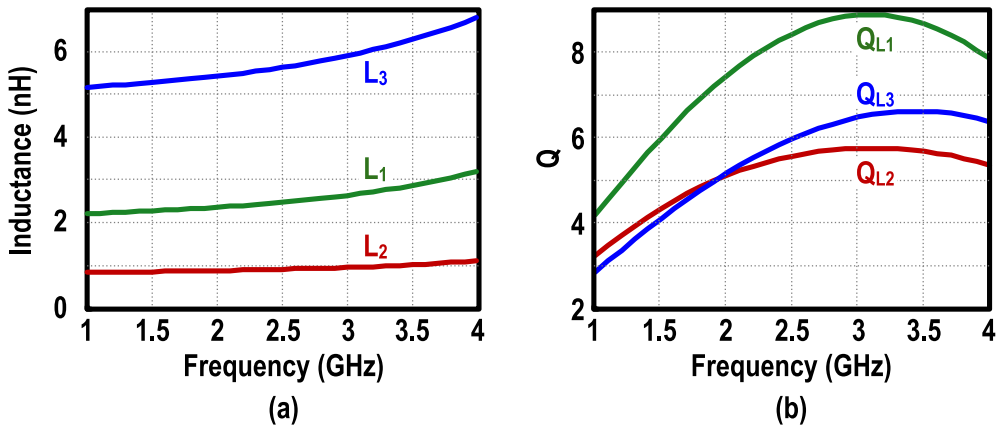

Fig. 15. EM-simulated (a) inductances and (b) *Qs* of the six-port transformer.

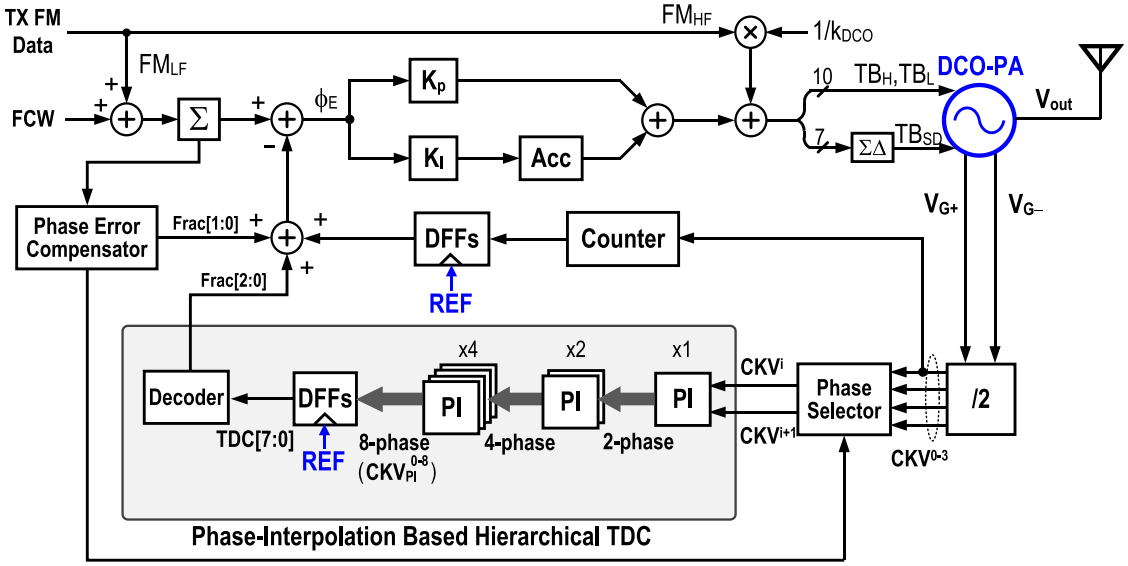

Fig. 16. Block diagram of the fraction-N ADPLL for locking the DCO-PA and two-point modulation.

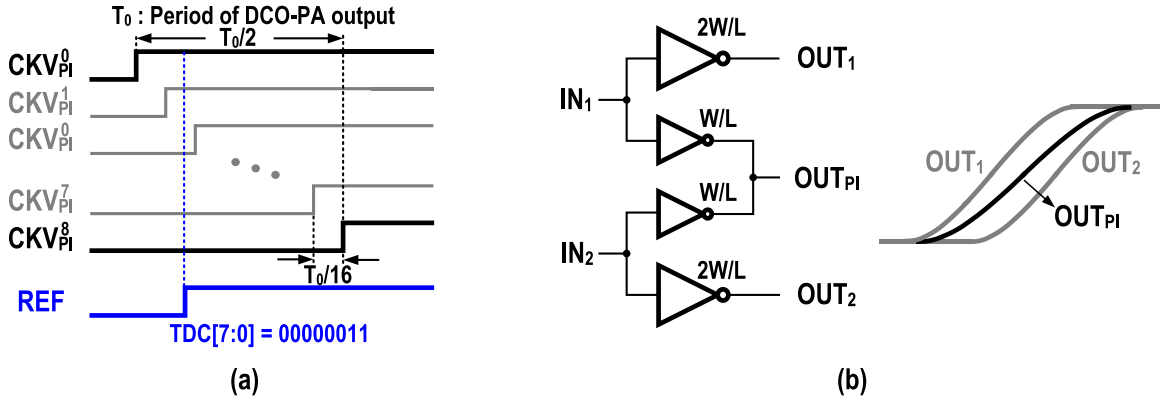

Fig. 17. (a) Timing diagram of the phase-interpolation based hierarchical TDC. (b) Inverter-based phase interpolator [19].

the antenna. During the RX operation, the antenna can be disconnected from the transformer and the cross-coupled pair M_1/M_2 of the DCO-PA are shut down by setting $V_{GB} = 0$. Thus we can add another small cross-coupled pair with tail-current source at the drain node V_{d+}/V_{d-} and realize a low-power VCO by turning on the tail-current source. The same ADPLL that controls the C_1 at the drain node can be re-used to lock the low-power VCO for RX operation.

B. Design of the Six-Port Transformer

To design the six-port transformer, we initially choose $L_1 = 2.5$ nH, $L_2 = 1$ nH, and $k_1 = 0.7$ based on the

analysis in Section II. Then, we can determine C_1 and C_2 to achieve $\omega_H/\omega_L = 3$. The choices of L_3, k_2, and k_3 can affect the power efficiency and phase noise performance of the DCO-PA. Ideally, the DCO-PA should work well without the coupling between L_2 and L_3 (k_3). Yet, since L_1 and L_2 have to be tightly coupled to maximize k_1, we cannot avoid k_3 in the practical transformer layout. Here, it is reasonable to assume k_3 is a fraction of k_2 when k_2 changes (i.e., $k_3 = 0.82k_2$). Table I lists the combinations of k_2 and L_3 values which guarantee $\omega_H = 3\omega_L$ for the Z_d, while preserving a constant output power of 7 dBm.[5]

Fig. 9 shows the simulated voltage swing of the gate voltage (V_g) for different values of k_2 at $V_{\rm GB} = 0.24$ V while we obtain the corresponding value of L_3 from Table I. When we choose a small k_2 and a large L_3, V_g achieves a large swing. Fig. 10 displays the simulated waveforms of V_d and I_d for different values of k_2. The ratio of the third harmonic to the fundamental voltage (V_{p3}/V_{p1}) increases when k_2 goes down because the large swing of V_g boosts the third harmonic current by imposing M_1 and M_2 to operate like a switch. For $k_2 = 0.25$, a large V_{p3}/V_{p1} of 0.59 induces a deep valley in the voltage waveform forcing it to deviate significantly from a square wave. The large amplitude of the overlapped current and voltage raises the power loss on M_1/M_2. Fig. 11(a) reveals that the DCO-PA efficiency grows with k_2, but saturates when $k_2 > 0.45$. Thus, a large k_2 is preferable to improve the power efficiency and reduce the voltage swing at the gate of M_1/M_2 for better reliability.

The phase noise performance of the DCO-PA can be evaluated by using the linear time-variant model [17]. According to [14], phase-noise equation of the DCO-PA at an offset frequency $\Delta\omega$ can be expressed as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{kTR_{P1,\rm se}}{2Q_t^2V_P^2}\cdot F\cdot\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{5}$$

where $R_{P1,\rm se} = R_{P1}/2$ and Q_t are the single-ended equivalent tank resistance at resonant frequency and the quality factor of the transformer tank when looked into the coil L_1. V_p is the maximum voltage amplitude of V_{d+}/V_{d-} (Fig. 8). The effective noise factor F can be expressed as [14]

$$F = \sum_i \frac{1}{2\pi}\int_0^{2\pi}\Gamma_i^2(\phi)\overline{i_{n,i}^2(\phi)}\frac{R_{P1,\rm se}}{4KT}dt \tag{6}$$

where $\overline{i_{n,i}^2(\phi)}$ and $\Gamma_i(\phi)$ are the white noise power density and the corresponding impulse sensitivity function (ISF) of the ith noise source. In the proposed DCO-PA, F consists of three terms from the equivalent tank impedance $R_{P1,\rm se}$ ($F_{\rm tank}$), the channel thermal noise ($F_{\rm GM}$) and the output resistance ($F_{\rm GDS}$) of M_1/M_2. According to the simulation results in Fig. 11(b), a k_2 of 0.45 would result in an optimized phase noise performance. After all, we choose a moderate k_2 of 0.45 to balance the power efficiency and phase-noise performance. The simulated tank ISF, G_m, and $G_{\rm DS}$ of M_1/M_2 and effective noise factors $F_{\rm tank}$, $F_{\rm GM}$, and $F_{\rm GDS}$ at $k_2 = 0.45$ are plotted in Fig. 12. Since the $G_{\rm DS}$ peak [Fig. 12(c)] coincides with the zero-crossing point of the ISF [Fig. 12(a)], $F_{\rm GDS}$ is relatively small and the total F is dominated by $F_{\rm tank}$ and $F_{\rm GM}$. The maximum $V_{\rm GS}$ for M_1/M_2 is ~1 V, which is within the breakdown voltage of the MOS transistor in the CMOS technology employed.

[5]To obtain the value of L_3 for a certain k_2, both L_3 and C_3 are changed while L_1, L_2, C_1, C_2, and k_1 are fixed in the simulation to find the right combination that guarantee $\omega_H = 3\omega_L$ and the desired output power of 7 dBm.

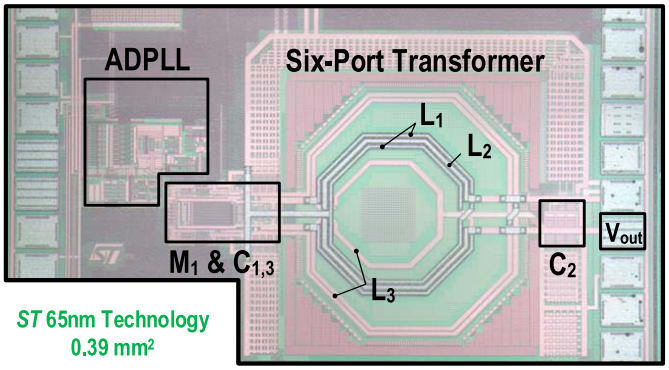

Fig. 18. Chip micrograph of the fabricated ULP TX.

Since $R_{P1,\rm se} = 50\ \Omega$ is chosen for the DCO-PA to deliver enough power to the antenna, the Q_t of the DCO-PA is only 2.6 which is lower than that of the oscillator with a high tank parallel impedance. Fortunately, a high output amplitude V_p can still be kept since the oscillator function reuses the large current required by the PA function in the proposed DCO-PA, which relieves the degradation of the phase noise. Compared with an oscillator that has a Q_t of 15 and the same values of V_p, F, and tank equivalent inductance, the phase noise degradation of the DCO-PA can be estimated to be 7.6 dB according to (5).

The power efficiency can be further increased from 41% to 42.3% due to the reduced overlap time between the V_d and I_d waveforms when the $V_{\rm GB}$ is reduced from 0.24 to 0.18 V. Fig. 13(a) shows the small signal transconductance g_m of M_1/M_2 at different process corners and temperatures. The DCO-PA can robustly startup at $V_{\rm GB} = 0.24$ V under the process and temperature variations since the g_m is always larger than the startup criteria of 20 mS for $R_{P1,\rm se} = 50\ \Omega$. At $V_{\rm GB} = 0.18$ V, a dynamic voltage biasing scheme that applies a high $V_{\rm GB}$ (e.g., 0.24 V) at first and then decreases it to 0.18 V after the setup of a stable oscillation can be employed to guarantee the robust startup. As shown in Fig. 13(b), the effective large signal transconductance of M_1/M_2 is large enough to sustain the oscillation at $V_{\rm GB} = 0.18$ V even under a slow corner and a temperature of −45 °C.

C. Layout of the Six-Port Transformer

Fig. 14 elucidates the layout of the six-port transformer is non-trivial since it has to balance a number of parameters, $L_{1\text{-}3}$, and $k_{1\text{-}3}$. To achieve a large coupling coefficient k_1 between L_1 and L_2, we have to interleave the two coils in the layout with a minimum space of 2 μm between the adjunct metal traces. Then, we pick a turn ratio of 2:1 to realize a K_L of ~2.5 and a k_1 of ~0.7. To improve the η_M, we route in parallel both the 1.2 μm Alucap (AP) layer and the 0.9 μm top metal (M7) for coils L_1 and L_2 to enhance

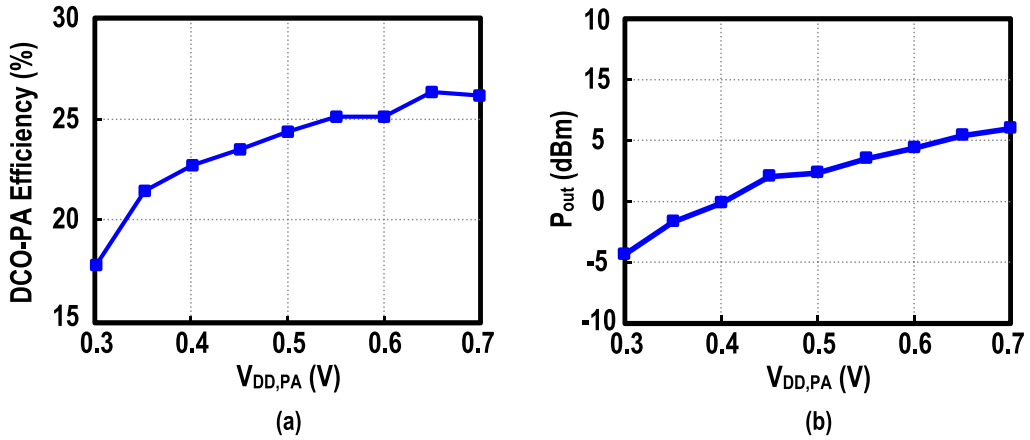

Fig. 19. Measured (a) DCO-PA efficiency and (b) P_{out} versus $V_{\text{DD,PA}}$.

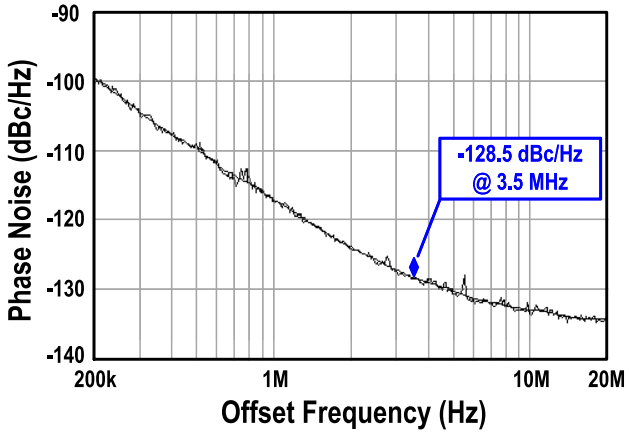

Fig. 20. Measured phase noise of the DCO-PA at the carrier frequency of 2.4 GHz ($P_{\text{out}} = 6$ dBm).

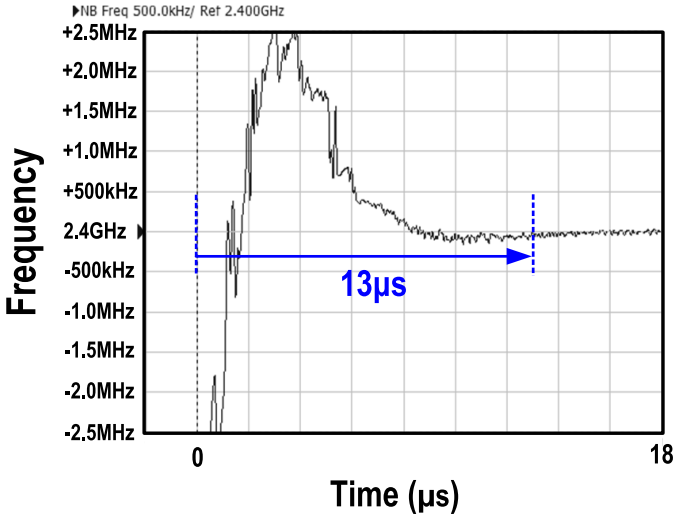

Fig. 21. Measured settling time of the ADPLL down to ±98 kHz frequency error.

Q_{L1} and Q_{L2}. Due to the limited contact area between the AP layer and M7 allowed by the technology, we use only M7 for the coil L_3. To realize a large inductance of 5.6 nH and a moderate coupling coefficient k_2 of 0.45, we draw L_3 in three turns: placing one at the inner side of L_1 and L_2 and the other at the outer side of L_1 and L_2. Since k_2 mainly depends on the space between L_1 and the two large outer turns of L_3, the diameter of the inner turn of L_3 represents a degree of freedom to obtain the size of L_3. The inter-winding capacitance between coils L_1 and L_2 would cause phase and amplitude imbalances during the D2S voltage conversion, thus degrading the oscillation frequency and the power efficiency. With two 100 fF inter-winding capacitors connected between V_{d+} and V_{out} and between V_{d-} and GND ports of coils L_1 and L_2, the simulation results indicate that the oscillation frequency and power efficiency will drop by 19 MHz and 1%, respectively.

Fig. 15(a) and (b) shows the EM-simulated inductances and Qs of the six-port transformer, respectively. At 2.4 GHz, $L_1 = 2.46$ nH, $L_2 = 0.92$ nH, and $L_3 = 5.62$ nH, with $Q_{L1} = 8.2$, $Q_{L2} = 5.6$, and $Q_{L3} = 5.9$. For the coupling coefficients, k_1, k_2, and k_3 are 0.7, 0.45, and 0.37, respectively, which should be insensitive to the process variation due to the lithography that precisely sets the layout dimensions [14].

IV. Fast-Settling Fractional-N ADPLL

Fig. 16 exhibits the ULP TX that employs a fractional-N ADPLL for channel selection and FM. The differential outputs ($V_{G+/-}$) at the gates of the DCO-PA are divided by 2 to generate the four phase signals ($\text{CKV}^{0\text{-}3}$) as the inputs to the phase selector and the counter. Operating at half of the DCO-PA's output frequency, the power consumption of the counter and TDC can be reduced by half. Since the phase relationship between the reference clock (REF) and $\text{CKV}^{0\text{-}3}$ can be predicted by the accumulation of the fractional part of the frequency control word (FCW), the CKV^{i} and CKV^{i+1}, with their rising edges closer to that of the REF, are selected as the inputs to the time-to-digital converter (TDC), as shown in Fig. 16. This phase selection scheme can reduce the input range of the TDC by 4× [18].

To operate under a low supply voltage, we utilize a phase-interpolation-based hierarchical TDC [19] to achieve a time resolution of 26 ps. Since the TDC input range (208 ps) is only one quarter of the CKV period (832 ps) we use a three-stage phase interpolator to generate 8-phase signals that have a time space of 26 ps between the two adjacent phases [Fig. 17(a)]. The inverter-based phase interpolator [Fig. 17(b)] is insensitive

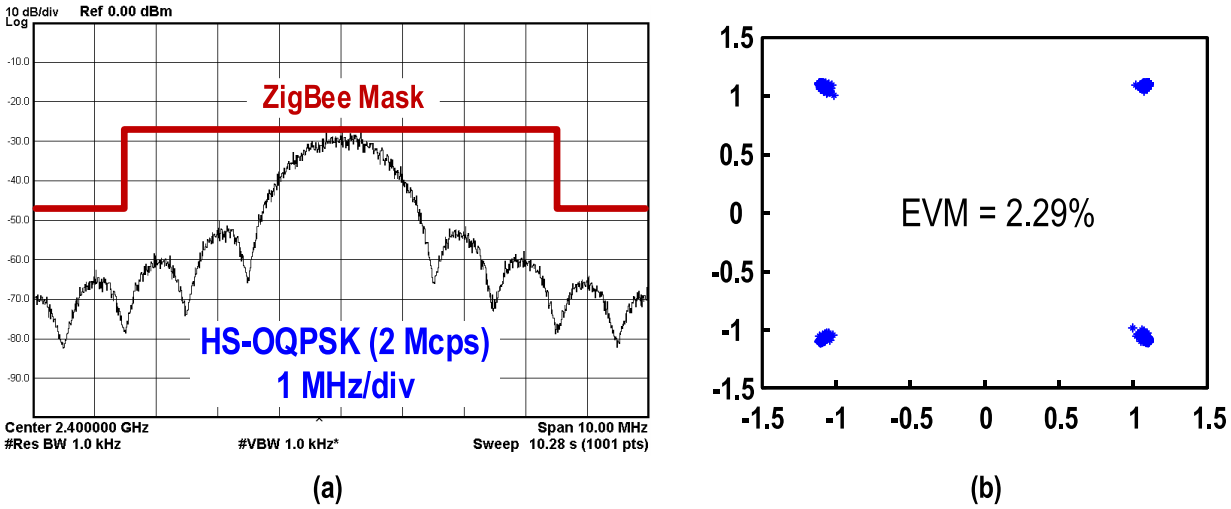

Fig. 22. Measured (a) ZigBee HS-OQPSK modulation spectrum at 2.4 GHz and (b) EVM.

to the PVT variation under a low supply voltage of 0.7 V, which allows calibration-free operation and, subsequently, reducing the frequency locking time. As a result, we can reduce the TX startup and turn-around times (i.e., energy loss). The added phase noise from the phase-interpolator chain is −135.7 dBc/Hz at 1 MHz offset at the carrier frequency of 1.2 GHz which is well below the phase noise of its input signal.

The ADPLL controls the acquisition bank (AB) and tracking bank (TB) varactors at the drain of the DCO-PA. As shown in Fig. 8, the TB is segmented with 6-bit (LSBs) unit-weights varactors and the AB is segmented with 4-bit (MSBs) binary-weights varactors. The step size and frequency range of the AB + TB are 125 kHz and 128 MHz, respectively. We utilize a third-order MASH-type $\Sigma\Delta$ modulator to further reduce the frequency resolution of the DCO to 125 kHz/2^7 = 977 Hz. We utilize a third-order MASH-type modulator to further reduce the frequency resolution of the DCO to 125 kHz/2^7 = 977 Hz. To obtain the FM we use a two-point modulation scheme by controlling the same varactor bank for frequency tracking. Finally, we add the TX FM to both the FCW and the control word of the DCO to achieve an all-pass characteristic from the TX FM Data to the output frequency.

V. Experimental Results

The ULP TX prototype, fabricated in 65-nm CMOS, includes a Class-F DCO-PA and a fractional-N ADPLL. Fig. 18 shows the chip photo occupying a 0.39-mm^2 active area. Fig. 19 shows the measured DCO-PA efficiency and P_{out} versus $V_{\text{DD,PA}}$ under V_{GB} = 0.18 V. The cable and board losses of ∼2 dB is de-embedded when obtaining the output power. The system efficiency reaches 26.2% at 6-dBm P_{out}. A scalable $V_{\text{DD,PA}}$ for the DCO-PA can keep high the back-off efficiency (>17.7%), while offering a wide P_{out} range from −4.3 to 6 dBm. With the carrier at 2.4 GHz, the phase noise measures −128.5 dBc/Hz at 3.5-MHz offset as shown in Fig. 20, which is well below the −103 dBc/Hz requirement of the ZigBee standard.

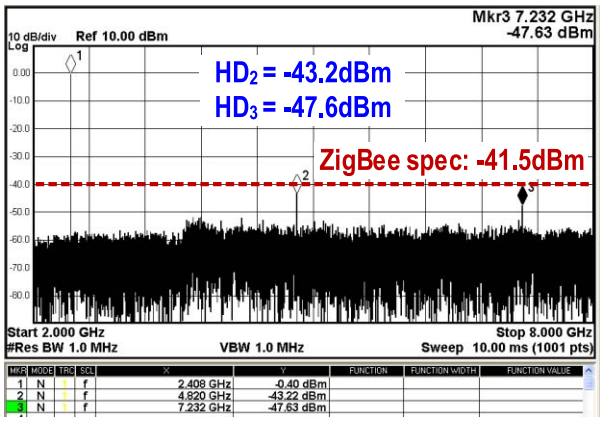

Fig. 23. Measured output spectrum when delivering a single tone at 0 dBm (cable and PCB losses included).

The ADPLL consumes 2.4 mW when we use a reference frequency of 32 MHz. As shown in Fig. 21, it takes 13 μs for the ADPLL output to settle down to a frequency error of ±40 ppm (±98 kHz) of the desired 2.4 GHz frequency. When operating at another channel frequency, such as 2.402 GHz, the measured reference and fractional spurs are −72.5 and −41.9 dBc, respectively, at FCW = 75.0625. The fractional spurs are mainly induced by the TDC non-linearity.

Fig. 22 shows the measured spectra for HS-OQPSK modulation, which complies with the ZigBee spectral mask with adequate margin. The achieved EVM (2.29%) is well below the specification (35%). Fig. 23 shows the measured output spectrum when delivering a single tone at 0 dBm (cable and PCB losses included), the HD_2 and HD_3 are −43.2 and −47.6 dBm, respectively, after adding an external 0.5-pF capacitor for harmonic filtering. The TX using the class-F DCO-PA and two-point modulation scheme is also possible to be applied for other short-range radio standards using constant envelope modulation, e.g., bluetooth low-energy (BLE), if the ADPLL can provide sufficient fractional frequency resolution.

Antenna impedance mismatch can potentially pull the oscillation frequency of the DCO-PA, but it should be a slow process induced by humans or other means. Thus, the ADPLL

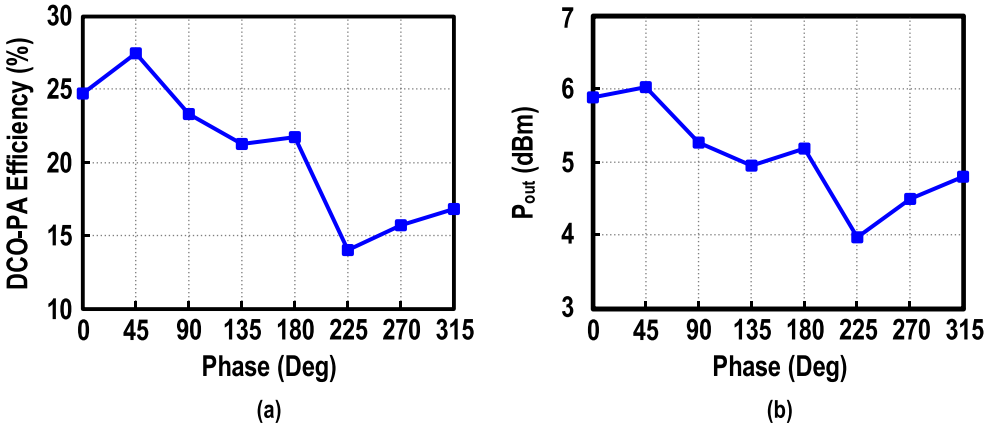

Fig. 24. Measured (a) DCO-PA efficiency and (b) P_{out} under VSWR 1.5:1.

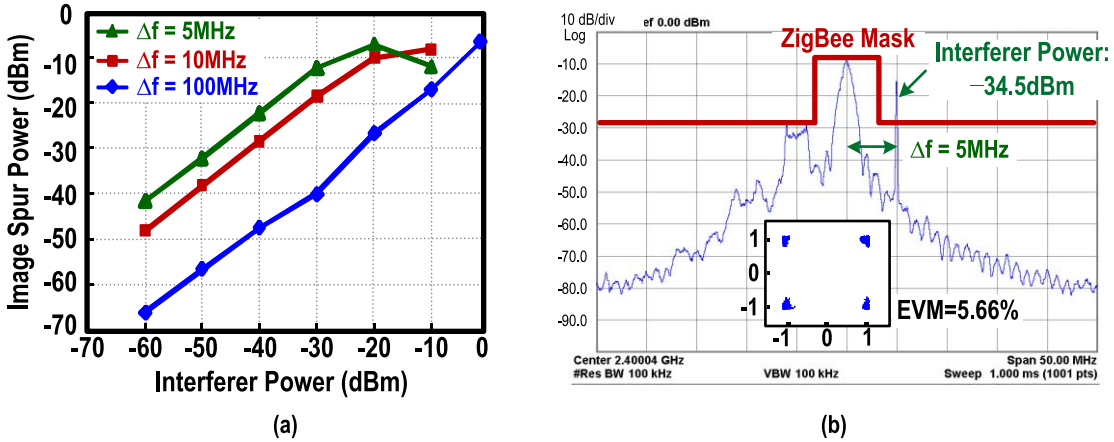

Fig. 25. Measured (a) image spur power versus the interferer power and (b) ZigBee modulation spectrum and its EVM at 2.4 GHz in the presence of a −34.5 dBm interferer at 2.405 GHz. (The single tone located at 2.405 GHz exceeding the ZigBee mask are due to interferer power reflected back from the DCO-PA output to the spectrum analyzer.)

should be able to correct it swiftly if the variation of the oscillation frequency is within the frequency range covered by the AB and TB varactors of the DCO-PA. Here, we measured the DCO-PA and TX under VSWR 1.5:1 as a static impedance mismatch. The free-running oscillation frequency of the DCO-PA changes from 2.376 to 2.408 GHz. The ADPLL successfully locks the DCO-PA at all angles, while keeping reasonable DCO-PA efficiency (>14%) and P_{out} (>4 dBm), as shown in Fig. 24. The insufficient isolation between the antenna and the oscillator would make the carrier frequency of the DCO-PA sensitive to the interferers. To measure the DCO-PA performance due to the presence of interferers, the signal generator, DCO-PA output and spectrum analyzer are connected to a circulator which allows the signal to travel in the direction of signal generator → DCO-PA output → spectrum analyzer. The blocking performance of the DCO-PA is tested firstly without data modulation. Under a low interferer power at the upper sideband, the output frequency can still be locked by the ADPLL, but an image spur is induced at the lower sideband of the carrier [20]. Fig. 25(a) shows the measured image spur power when the interferer is applied at an offset frequency of 2.4 GHz + Δf. When the interferer power reaches −8.5, −7.5, and 1.5 dBm at Δf = 5, 10, and 100 MHz, the DCO-PA will eventually be locked to the interferer frequency. When the data is transmitted, the image spur should be below the transmission spectral mask required by the ZigBee standard. As shown in Fig. 25(b), the maximum interferer power at Δf = 5 MHz that still meets the ZigBee mask requirement is −34.5 dBm and the corresponding EVM is degraded to 5.66%. When Δf increases to 10 MHz, the maximum interferer power is relaxed to −29.5 dBm with an EVM of 4.59%.

Table II compares the performance of the proposed DCO-PA and ULP TX with the state-of-the-art. In a comparison with the existing solutions using separated VCO and PA or current re-use VCO–PA, the proposed function-reuse Class-F DCO-PA achieves a competitive power efficiency of 22.6% at a 0-dBm P_{out}. Our chip area is the smallest (0.39 mm^2) among all the TXs with on-chip MNs, and the TX efficiency can be further improved by reducing the REF frequency of the ADPLL, or by powering down the ADPLL during transmission as in [4], [6], and [21].

VI. Conclusion

This paper demonstrated a sub-1-V 2.4-GHz ZigBee TX with an on-chip MN in 65-nm CMOS. By exploiting a function-reuse class-F DCO-PA plus a six-port transformer, and a fractional-N ADPLL for two-point data modulation, the

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Parameters	This Work	M. Babaie et al. JSSC'16 [4]	C. Li et al. JSSC'16 [6]	J. Prummel et al. JSSC'15 [7]	Y. -H. Liu et al. ISSCC'15 [5]
Applications	2.4 GHz ZigBee	2.4 GHz BLE	2.4 GHz BLE	2.4 GHz BLE	2.4 GHz BLE/ ZigBee/ 2M Proprietary
Architectures	**Function-Reuse Class-F DCO-PA + ADPLL**	Class-E/F_2 PA + LC-DCO + ADPLL	PA-VCO+ Analog PLL	Class-D PA + LC-VCO + Analog PLL	Class-D PA + LC-DCO + ADPLL
On-chip inductors Or transformers	**1 (Shared by DCO, PA and MN)**	2 (1 for LC-VCO, 1 for MN)	1 (1 for LC-VCO)	3 (1 for LC-VCO, 2 for MN)	2 (1 for LC-DCO, 1 for MN)
On-Chip MN	**Yes**	Yes	No	Yes	Yes
Active Area (mm^2)	**0.39**	0.65	0.35*	0.53*	0.8*
Supply Voltage (V)	**0.3 to 0.7 (DCO-PA) 0.7 (ADPLL)**	0.5 (DCO) 1 (ADPLL+PA)	1.2	1.2	1
Power Consumption @ P_{out} (DCO/VCO + PA + PA Driver)	**4.4 @ 0 dBm 15.3 @ 6 dBm**	3.6 @ 0 dBm 5.5 @ 3 dBm	4.46 @ −1 dBm	6.8 @ 0 dBm	3.45 @ −2 dBm
Power Efficiency @ P_{out} (DCO/VCO + PA + PA Driver)	**22.6% @ 0 dBm 26.1% @ 6 dBm**	28% @ 0 dBm 36% @ 3 dBm	17.9% @ −1 dBm	14.7% @ 0 dBm	18.3% @ −2 dBm
TX Power Consumption (mW) @ P_{out}	6.8 @ 0 dBm 17.7 @ 6 dBm	4.4 @ 0 dBm 6.3 @ 3 dBm	4.56 @ −1 dBm	10.1 @ 0 dBm	4.2 @ −2 dBm
System Efficiency @ P_{out}	14.5% @ 0 dBm 22.6% @ 6 dBm	23% @ 0 dBm 32% @ 3 dBm	17.5% @ −1 dBm #	9.9% @ 0 dBm	15% @ −2 dBm
Settling Time (μS)	13	15	N/A	N/A	15
HD_2/HD_3 @ P_{out} (dBm)	−43.2 / −47.6 & @ 0 dBm P_{out}	−50 / −47 @ 0 dBm P_{out}	< −40 / −40 @ −1.6 dBm P_{out}	<−54 / −52 @ 0 dBm P_{out}	−50.9 / −54.5 @ −2 dBm P_{out}
VCO Phase Noise @ 3.5 MHz (dBc/Hz)	−128.5	−126.9 to −127.9 ^	−131.9 ^	−122.3 ^	N/A
Technology	65 nm CMOS	28 nm CMOS	130 nm CMOS	55 nm CMOS	40 nm CMOS

* Estimated from die photo & With a 0.5 pF external capacitor # PLL is off during transmission

^ Normalized from phase noise @ 1-MHz [4], @ 2-MHz [6] and @ 2.5-MHz [7] offset frequency.

system efficiency attains 22.6% at a peak P_{out} of 6 dBm, and 8.2% at a back-off P_{out} of −4.3 dBm. The problem of injection pulling between the DCO and PA when the PA starts up is architecturally addressed. The HS-OQPSK modulated output complies with the ZigBee spectral mask with an adequate margin and the EVM is 2.29%. The active area is 0.39 mm^2.

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