An Integrated DC–DC Converter With Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery

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***Abstract*— This paper presents a fully integrated voltage-controlled oscillator (VCO)-based switched-capacitor (SC) 15-phase dc–dc converter in 65-nm CMOS. We propose two transient-enhancement techniques: segmented frequency modulation (SFM) and multiphase co-work (MCW) control to reduce the latency of the VCO-based control loop and shorten the SC dc–dc converter's transient response time. The SFM can improve the heavy-to-light load transient by dynamically increasing the charge pump discharge current by nine times, while the MCW can enhance the light-to-heavy load recovery by synchronously combining three interleaved flying capacitors together during the transient state. We designed the 15-phase interleaved converter to support an output voltage of 1 V from a 2.4-V input supply, delivering up to 138 mA of load current, which takes only 25/29 ns for output voltage recovering to the steady state from heavy-to-light/light-to-heavy load transients, respectively. It obtains a peak efficiency of 82.8% and maintains the efficiency above 80% from 31 mA to the maximum load current. The SC dc–dc converter chip occupies 0.61 mm^2, and its output power density is 240 mW/mm^2.**

***Index Terms*— Fully integrated, SC dc–dc converter, switched capacitor (SC), voltage-controlled oscillator (VCO).**

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I. Introduction

THE minimization of the overall package size of a portable device requires a built-in system-on-a-chip (SoC) solution instead of a chip with external discrete components. DC–DC power converters are also necessary to be fully integrated with the SoC together [1]–[3]. Besides, the multi-function-SoC draws large and frequently varying current from power supplies, leading to undershoot and overshoot in the supply voltages. The long recovery time and large voltage droop will degrade the SoC performance, or even cause malfunction. Therefore, a fully integrated and fast transient response dc–dc converter is mandatory to provide reliable power supplies to the SoCs. To compare with the inductive topology [4], the capacitive dc–dc converter [5] can achieve lower cost, a more compact area and higher compatibility in a single chip integration [6]–[8]. Furthermore, it allows a simpler compensation scheme for stability due to the first-order system behavior of the power stage [9]–[11], when compared with its inductive counterpart.

Currently, multiphase interleaving technique is widely used to enhance the transient speed of the dc–dc converters [9], [12]–[15], and recently has been applied for generating continuously scalable voltage conversion ratios [16]. Multiple phases allow the control loop to respond at every phase that is a fraction of the switching period, exhibiting a strong ability to achieve a fast load transient response. However, to employ multiphase interleaving alone for improving the transient response is not sufficient to satisfy the increasingly stringent requirements of SoC power supplies. To further accelerate the load transient recovery speed, it is essential to improve the control loop itself.

Traditionally, a linear compensator or a charge pump integrator can be used to control the ring oscillator or the voltage-controlled oscillator (VCO) [13], [15], but the response speed is limited by gain-bandwidth product, which is a tradeoff for stability with a wide range of load current. A hysteretic control loop is another popular choice in the design of capacitive dc–dc converters [12], [14]. It exhibits fast load regulation and is inherently stable [12]. However, this approach employs one comparator for each interleaving channel. In other words, it needs n comparators for n interleaving phases [12], or a

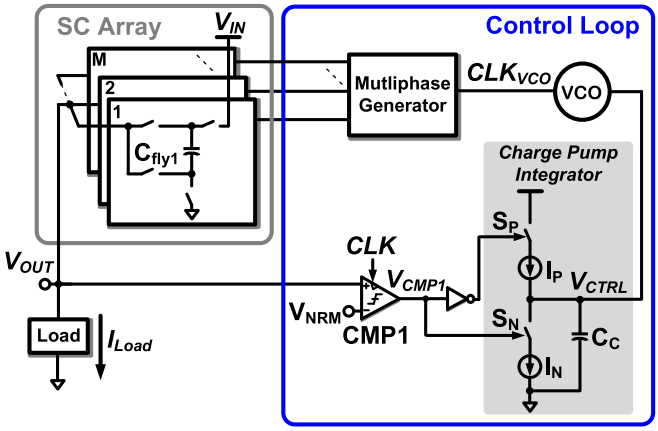


Fig. 1. Typical VCO-based SC multi-phase dc–dc converter.

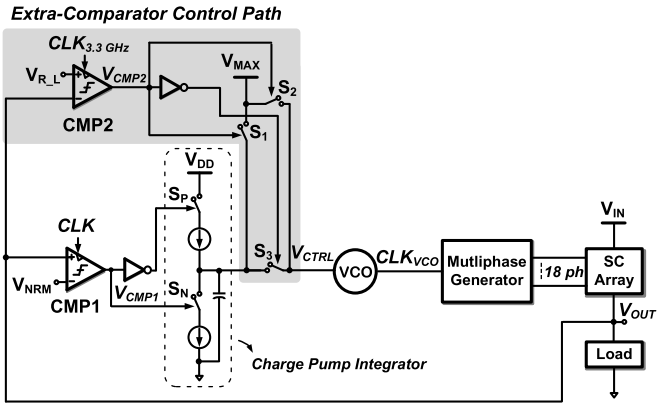


Fig. 2. Circuitry of the VCO-based SC dc–dc converter in [13].

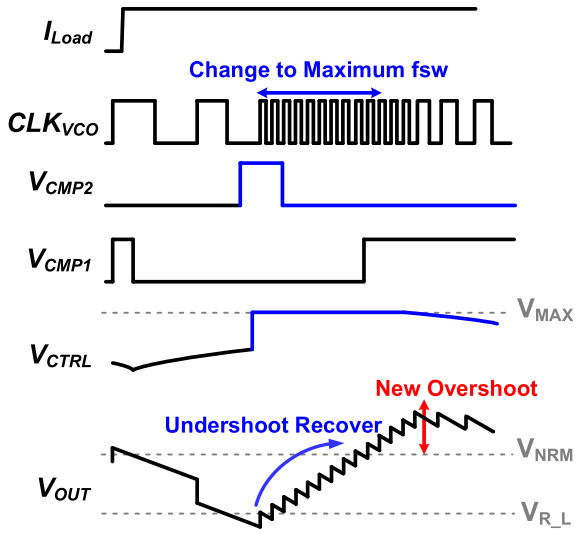


Fig. 3. Waveform diagrams of the VCO-based SC dc–dc converter with the excessively high VCO frequency during the moderate light-to-heavy load transition.

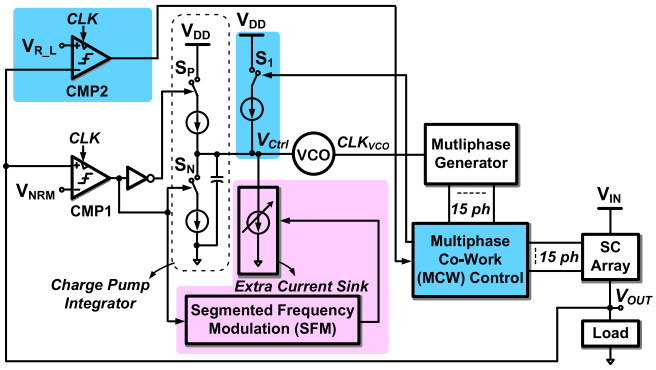


Fig. 4. Simplified circuitry of the VCO-based SC dc–dc converter with the proposed load transient enhancement control techniques.

shared comparator that works at n times higher clock frequency [14], which is power hungry. To achieve a high unity-gain frequency, the dominant pole is designed at the output node in [9]. But it suffers from dc regulation accuracy because it is a proportional-control only.

Fig. 1 shows the typical block diagram of a VCO-based switched-capacitor (SC) dc–dc converter. The comparator CMP1 with nominal voltage $V_{\rm NRM}$ tracks the variation of the converter output voltage and then adjusts $V_{\rm CTRL}$ through the charging of the charge pump integrator up or down. The VCO frequency of $\rm CLK_{VCO}$ is proportional to the charge pump integrator voltage $V_{\rm CTRL}$, revealing the load current is heavy or light. In the steady state, the charging and discharging of $V_{\rm CTRL}$ are smooth and robust. During load transition, such scheme is very slow to pull up or push down $V_{\rm CTRL}$, due to the fixed source current I_P or sink current I_N to charge/discharge the capacitor C_C cycle-by-cycle. Consequently, the load transient recovery is very sluggish. To accomplish both the rapid detection and fast recovery, Le *et al.* [13] used an additional controlled path to deal with the load transition specifically. Fig. 2 depicts the circuitry of the VCO-based SC dc–dc converter from [13]. The frequency of the VCO-based clock generator is set to the maximum immediately after the detection of undershoot caused by light-to-heavy load transition, i.e., when the extra comparator CMP2 detects $V_{\rm OUT}$ falling below the lower boundary voltage $V_{\rm R\_L}$. However, for moderate light-to-heavy load transition, this solution results in the over-switching of the SC array which exceeds the steady-state frequency required by the load current. Consequently, there is an overshoot due to the overcharged $V_{\rm CTRL}$ from the integrator which prolongs the total transient recovery time, as illustrated in Fig. 3. Finally, Le *et al.* [13] did not provide the enhancement of the transient recovery during heavy-to-light load conditions.

In this work, we propose segmented frequency modulation (SFM) and multiphase co-work (MCW) scheme techniques for a multi-phase SC dc–dc converter to improve the transient recovery speed during light-to-heavy and heavy-to-light load transients. Fig. 4 depicts the simplified block diagram of the VCO-based SC dc–dc converter with the proposed techniques, reported in [18]. It optimizes and speeds up the VCO-based control loop for improving the load transient response of the converter. The SFM circuit reduces the recovery time during heavy-to-light load transition (detected by CMP1), by improving the discharge mechanism and speed of the charge pump integrator. The MCW circuit reduces the

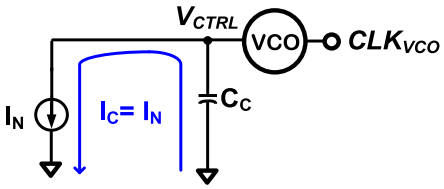


Fig. 5. Circuitry of the typical VCO generator in discharging mode.

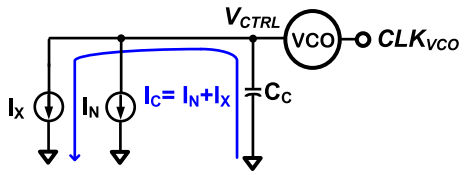


Fig. 6. Circuitry of the VCO generator with an extra sink current I_X.

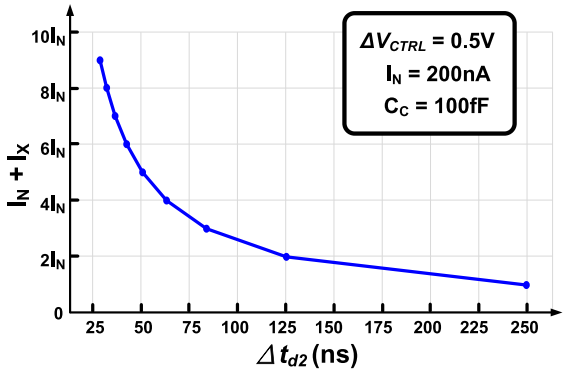


Fig. 7. Discharging time Δt_{d2} and corresponding discharging current $I_N + I_X$ (based on typical corner calculation).

recovery time during light-to-heavy load transition (detected by CMP2). This additional block, as discussed in detail shortly, relaxes the limitation outlined in [13].

The organization of this paper is as follows: Section II presents the control loop analysis of the VCO-based SC dc–dc converter. Sections III and IV introduce the operation principle and the circuitries associated with the proposed SFM and MCW schemes. Section V exhibits the implementation and measurement results, and, finally, Section VI concludes this paper.

II. VCO-Based Control Loop Analysis

This section analyzes the working scheme of a VCO-based control loop and, thus, paves the way for the basic principle of the proposed load transient enhancement control techniques in Sections III and IV. As illustrated in Fig. 1, if the dc–dc converter output voltage $V_{\rm OUT}$ is higher than the nominal voltage $V_{\rm NRM}$, the sink current I_N will be turned on to discharge the VCO voltage $V_{\rm CTRL}$. Fig. 5 shows the equivalent circuitry of the typical VCO generator in the discharging mode. The discharging time can be expressed as

$$\Delta t_{\rm d1} = \frac{C_{\rm C}\Delta V_{\rm CTRL}}{I_{\rm N}} \tag{1}$$

where $\Delta V_{\rm CTRL}$ is the voltage difference of $V_{\rm CTRL}$ from a heavy load to a light load. Once a step-down load transition happens, a big difference, $\Delta V_{\rm CTRL}$, must be cut down to meet the appropriate lower frequency of the VCO. Then, the discharging time, Δt_{d1}, will be very long if I_N does not increase. It directly reflects the slow recovery speed of the dc–dc converter during load transition. Fig. 6 shows the circuitry of the VCO generator with an extra sink current I_X, whose discharging time can be expressed as

$$\Delta t_{\rm d2} = \frac{C_{\rm C}\Delta V_{\rm CTRL}}{I_{\rm N} + I_{\rm X}}. \tag{2}$$

After the extra sink current I_X is employed, the discharging time can be reduced and adjusted by different amounts of I_X. Fig. 7 illustrates the relationship between the discharging time Δt_{d2} and the corresponding discharging current $I_N + I_X$.

In this work, we design the VCO switching frequency range from 1 to 250 MHz with $V_{\rm CTRL}$ scaling from 0.3 to 0.8 V, for the entire load range of 10–150 mA. While the load current changes from the heaviest to the lightest, $\Delta V_{\rm CTRL}$ is equal to 0.5 V in the typical corner. If I_N is given as 200 nA, C_C is 100 fF, and I_X is given as 0, Δt_{d2} is equal to 250 ns. If I_X is given as $8I_N$, Δt_{d2} is shortened to only 27.8 ns. Therefore, the extra sink current can accelerate the discharging speed of $V_{\rm CTRL}$ at the VCO generator at the load step-down transition. Likewise, using the extra source current can accelerate the charging speed of $V_{\rm CTRL}$ during the load stepup transition.

Using the extra current can speed up the transient response of the VCO generator, but the amount of the additional current is a design consideration. Because the step of load change is related to $\Delta V_{\rm CTRL}$, very small extra current diminishes the recovery effect. On the contrary, overshoot or undershoot will be generated due to the over-large extra current, prolonging the recovery time. Next, we will propose an SFM scheme to deal with the extra current adaptively.

III. Segmented Frequency Modulation

The aim of the proposed SFM scheme is the reduction of the recovery time during the load step-down transition. The operation principle of SFM is to increase the corresponding amount of the discharging current in the charge pump of the VCO generator, depending on the magnitude of the load current change. Fig. 8 shows the circuitry of the segmented frequency modulator. It consists of a pulse counter, a 2-bit decoder, three switches S_{X0}, S_{X1}, $S_{\rm OV}$, and three binary weighted extra sink current branches. The pulse counter accumulates the output states of the CMP1 in each comparison cycle. If the load current changes from heavy to light, it generates an overshoot at the output of dc–dc ($V_{\rm OUT}$) that switches the CMP1 output to "1." When the sum of "1" counts is larger than a given threshold (i.e., detection of a prolonged overshoot transient), an overshoot detection signal $V_{\rm SIG}$ changes from "0" to "1," turning on the switch $S_{\rm OV}$ which subsequently increases the sink current of the charge pump integrator. Therefore, the discharging speed of the charge pump integrator increases, and the clock frequency of the VCO generator can be quickly reduced to the value

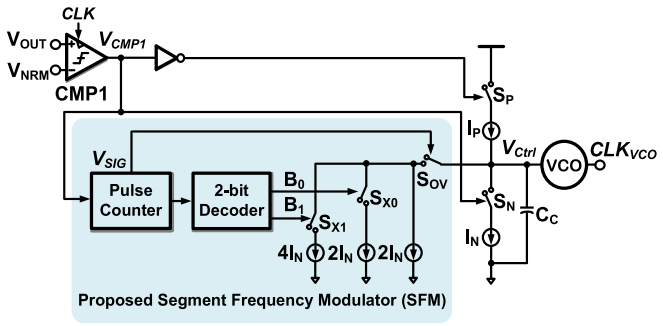


Fig. 8. Circuitry of the proposed SFM technique.

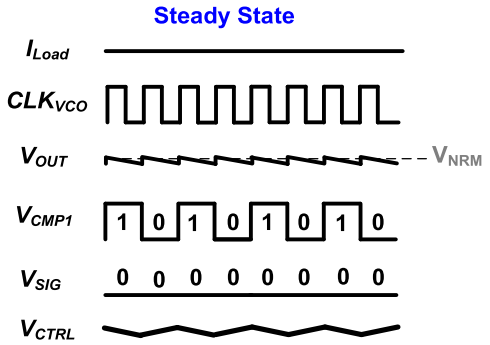


Fig. 9. Waveform diagrams of the VCO-based SC dc–dc converter with SFM at steady state.

for the lighter load state. Consequently, the load transition recovery time shrinks.

A. Steady State Operation

Fig. 9 sketches the waveform diagram of the VCO-based SC dc–dc converter with the SFM during the steady state. In the steady state, the output voltage $V_{\rm OUT}$ of the dc–dc converter swings up and down regularly around the nominal voltage $V_{\rm NRM}$. The output pattern of the CMP1 is "101010…." The pulse counter identifies this output pattern, then the overshoot detection signal $V_{\rm SIG}$ is always "0" and the SFM scheme does not turn on. The VCO voltage $V_{\rm CTRL}$ changes with the normal charging and discharging by the source current I_P and sink current I_N in the charge pump integrator. Therefore, maintaining the VCO frequency of the $\rm CLK_{VCO}$ constant.

B. Step-Down Load Transition and Segmented Sink Current

Fig. 10 plots the waveform diagram of the proposed VCO-based SC dc–dc converter with extra sink current enabled during the load step-down transient state. During the load step-down, an overshoot appears at the output of the dc–dc converter. Since $V_{\rm OUT}$ is larger than $V_{\rm NRM}$, the output pattern of the comparator CMP1 becomes "11" after several comparisons. Then, the overshoot detection signal $V_{\rm SIG}$ of the pulse counter output changes from "0" to "1." In order to avoid misjudgment, it starts when the third consecutive "1" occurs at $V_{\rm CMP1}$, i.e., "111." The extra sink current, initially set to twice the discharging current I_N, brings the total sink current to $3I_N$. The discharging slew rate of the VCO control

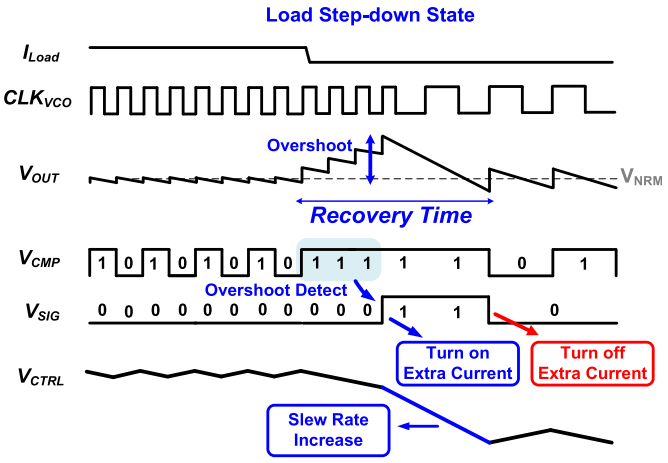
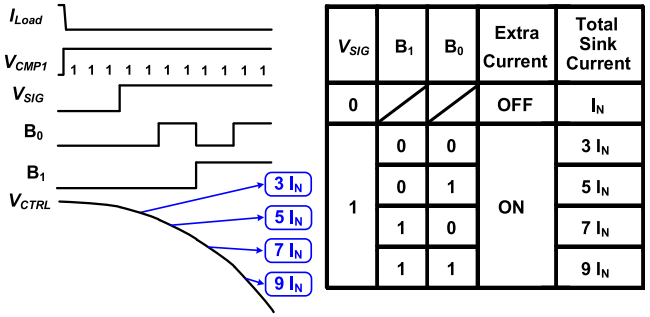


Fig. 10. Waveform diagrams of the SFM scheme with extra sink current enabled at load step-down transient state.



V_{SIG}	B_1	B_0	Extra Current	Total Sink Current
0			OFF	I_N
1	0	0	ON	$3\,I_N$
	0	1		$5\,I_N$
	1	0		$7\,I_N$
	1	1		$9\,I_N$

Fig. 11. Waveform diagrams of the SFM scheme with segmented increasing sink current enabled and the mapping table of the 2-bit decoder.

voltage, $V_{\rm CTRL}$, increases by three times until the output voltage becomes lower than the nominal level $V_{\rm NRM}$. The output pattern of the comparator then goes back to the steady state "10." At this point, $V_{\rm SIG}$ switches back and disconnects the extra discharging current.

When the frequency of the VCO is not low enough to match the heavy-to-light load transition, the overshoot persists. It indicates that the transition step is very large and loading current changes a lot. The recovery is still slow since the enabled sink current is too small to discharge the charge pump integrator. In this case, the output pattern of the comparator always keeps the value "11," like in the case shown in Fig. 11. The pulse counter computes the value of "11" and recognizes it through the 2-bit decoder. Consequently, the segmented increased sink currents will be enabled to speed up the discharging of the charge pump integrator.

Fig. 11 displays the mapping table used to switch ON/OFF the sink current branches under the control of the 2-bit decoder. The sink current branches operate as a 2-bit digital-to-analog converter (DAC) with the LSB always on. The output code B_1B_0 of the 2-bit decoder determines how much extra discharging current should be connected to the discharging loop of the charge pump integrator.

Therefore, when heavy load changes to a very light load, the decoder turns on more extra discharging currents

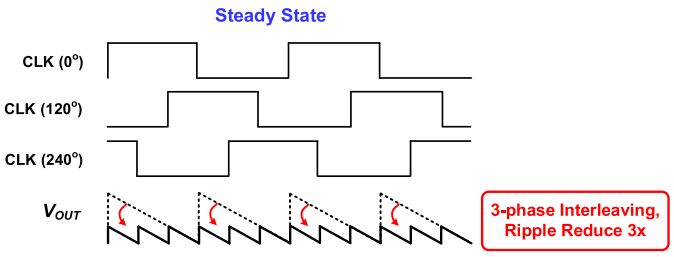


Fig. 12. Effective output voltage of a three-phase interleaved SC dc–dc converter as an illustrative example.

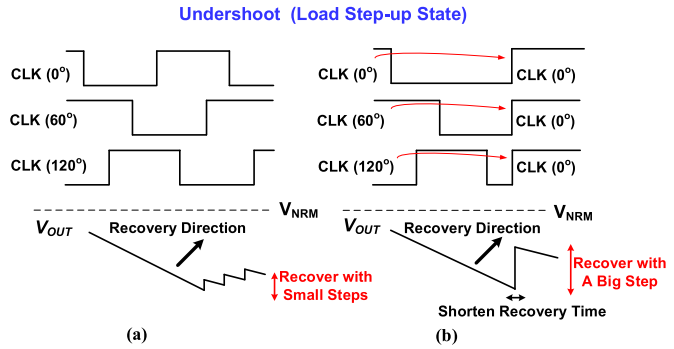


Fig. 13. Effective output voltages of a three-phase interleaved SC dc–dc converter during load step-up transient state with (a) normal phase interleaving and (b) MCW control schemes.

$(2I_N, 4I_N)$ to speed up the reduction of V_{CTRL}. Since the total sink current can go from I_N to $9I_N$, the discharging slew rate of the control voltage V_{CTRL} can be very large, and thus, a fast heavy-to-light load transient recovery can be achieved.

The same SFM technique can be potentially applied to improve the light-to-heavy transient, by injecting extra current sources to supplement I_P. Nonetheless, in this work, we propose the MCW technique (in Section IV), which can improve the light-to-heavy transient recovery. As a result, the SFM only needs to implement the extra adapted sink current to improve the heavy-to-light load transient.

IV. Multi-Phase Co-Work Scheme

As it is known, the multi-phase interleaving technique can reduce the output voltage ripples of the dc–dc converter while avoiding a dedicated output decoupling capacitor [19]. Fig. 12 shows an example of the output voltage of a three-phase interleaved SC dc–dc converter. The ripple of V_{OUT} decreases by a factor of 3 due to the interleaving of the three channels. This work uses a modified version of the multi-phase technique. It allows reducing the ripple and the transient recovery time during light-to-heavy load transition.

Fig. 13(a) exhibits the effective output voltage of a three-phase interleaved SC dc–dc converter during a step-up load transition. However, a limitation of multi-phase interleaving is the reduction of the step size in the load transient recovery. Thus, it requires many small steps to recover the output voltage back to its nominal level, even if the switching frequency increases with heavier loading. In fact, the undershoot phenomenon already implies that the SC network should provide

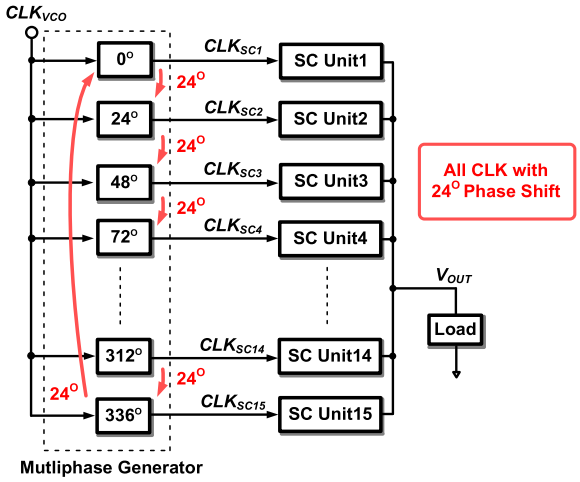


Fig. 14. 15-phase interleaved SC dc–dc converter with the conventional scheme.

a higher energy supply. However, the multi-phase interleaving technique also reduces the transient supply-to-load current, and it conflicts with the goals of compensating the energy during light-to-heavy load transient in a very short time. Therefore, the concept of increasing the energy supply of the multi-phase SC network over time can enhance the load transient recovery speed. The solution is here the MCW control technique, which aims to synchronize the selected interleaving multiple-phase SC channels to provide an immediate larger energy step to the load, thus reducing the load transient recovery time. Fig. 13(b) shows the effective output voltage of a three-phase interleaved SC dc–dc converter during light-to-heavy load transient with the proposed MCW scheme. For example, the interleaving three-phase SC channels have 120° phase shift with each other. Once the light-to-heavy load transient is detected, the three channels are synchronized to provide more energy to the load and at the same time to reduce the recovery time.

Fig. 14 presents the conventional scheme of the 15-phase interleaved SC dc–dc converter [19], which is partitioned into 15-phase interleaved small SC units/channels. A multiphase generator produces the clock pulse of each SC unit, whose phase is always consistent in the interleaving loop. Each SC unit has a clock phase shift of 24° with its adjacent.

Fig. 15 illustrates the structure of the 15-phase interleaved SC dc–dc converter with the proposed MCW control scheme. Different from the conventional structure, the proposed scheme determines the connection between the clock phases, i.e., 0°, 24°, 48°, . . . , 312°, 336° blocks and the small SC units. In the steady state, the value of the CMP2 output is "0." Thus, each SC unit is interleaved by 24° phase shift. When the large undershoot during the light-to-heavy (step-up) load transient is detected, the CMP2 output changes to "1." And then, the extra source current I_Y given as $4I_P$ will be enabled to speed up the charging of V_{CTRL}. The total charge current flowing through the charge pump integrator is then $5I_P$. At the same time, the MCW scheme will be triggered to synchronize the selected SC units to switch on together and enhance the load transient recovery speed, which will be discussed below.

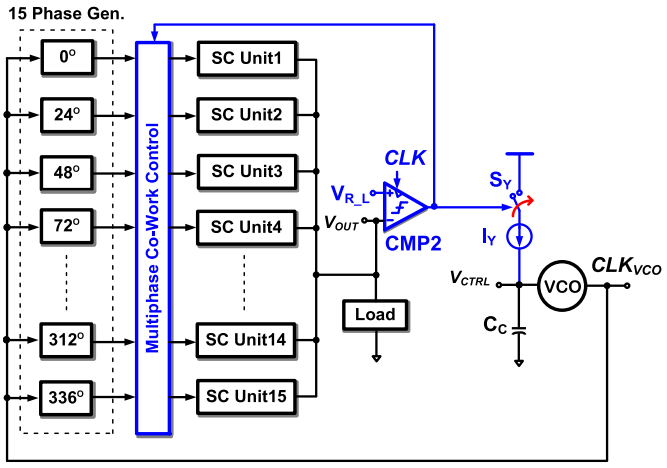


Fig. 15. 15-phase interleaved SC dc–dc converter with the proposed MCW scheme.

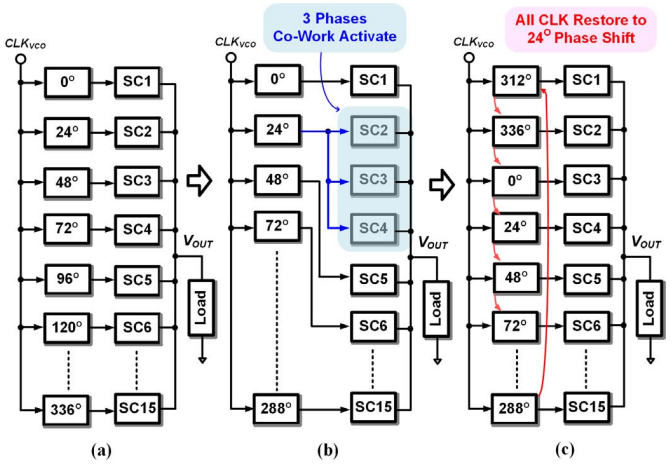


Fig. 16. Equivalent circuits of a 15-phase interleaved SC dc–dc converter with the MCW scheme during operation of (a) steady state, (b) MCW state (undershoot detected), and (c) recovery state.

Fig. 16 shows the simplified diagrams of a 15-phase interleaved SC dc–dc converter with the MCW during operations of (a) steady state, (b) MCW state, and (c) recovery state. Once the MCW control is triggered at the SC unit 1 (SC1), the next three adjacent SC units with SC2, SC3, and SC4 are switched on simultaneously. Then, SC5, SC6, . . . , SC15 are continuously switched with 24° phase shift among each other. Consequently, the load transient-recovery step and recovery speed increase by threefold when compared with that in the steady state. With this control scheme, the converter can transmit more energy to the load in a very short period, and therefore, reduce the light-to-heavy load transient recovery time, which will be verified in Section V. Afterward, the converter entered the recovery state, and the SC unit one is no longer connecting to 0° clock phase. However, the clock phase shift between $\mathrm{CLK_{SC1}}$ to $\mathrm{CLK_{SC15}}$ is always kept at 24°, as shown in Fig. 16(c), and the normal steady state can be continued.

If a larger step-up load transition happens and the recovery is not enough, i.e., V_{OUT} is still lower than $V_{\mathrm{R\_L}}$, MCW can activate again with three clock phases of "waiting time" as exemplified in Fig. 17, and then the integrator voltage V_{CTRL} continues to pull up faster until recovering the undershoot. Otherwise, MCW will be finished, and V_{CTRL} stops the charging. The three phases of waiting time (instead of 0) are set to avoid overshooting the V_{OUT}. When compared to [12], the VCO frequency of $\mathrm{CLK_{VCO}}$ will just be pulled up to an appropriate steady-state frequency for the corresponding load current, and then avoids inducing an extra overshoot due to the excessively high VCO frequency. As a result, we obtain, simultaneously, a smooth and fast response VCO-based loop controller and fast recovery SC network. Fig. 18 displays the overall timing diagram of a 15-phase interleaved SC dc–dc converter with the MCW control scheme. With the MCW turned on three times within a single cycle, the equivalent clock period of 15 phases can be reduced from T_S to 0.6 T_S. Therefore, the power throughput of the converter also increases, even with the flying capacitor fixed in the design.

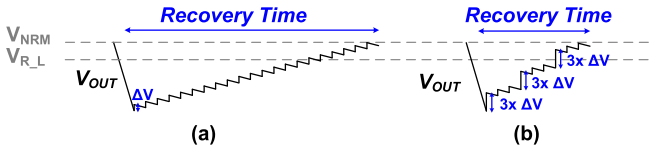


Fig. 17. Effective output voltages of a 15-phase interleaved SC dc–dc converter during light-to-heavy load transient with (a) normal phase interleaving and (b) MCW scheme with three-phase "waiting time."

Finally, while MCW can improve the light-to-heavy load transient by supplying more flying capacitors simultaneously, it cannot help to improve the heavy-to-light load transient due to its nature, which is instead improved by the proposed SFM technique.

V. Implementation and Measurement Results

We utilized a 65-nm standard CMOS process for the implementation of the proposed dc–dc converter which occupies an effective chip area of 0.61 $\mathrm{mm^2}$ (0.78 mm × 0.78 mm), as shown in Fig. 19. An on-chip load current generator implemented with a programmable PMOS array can adjust the equivalent width of the PMOS devices [19] by off-chip clock gating to obtain correct I–V measurements during the load transient. In this design, we choose to implement the capacitors by means of standard available MOS capacitors. The flying capacitors are constructed by the PMOS with flying well approach [20], in order to shrink the bottom-plate parasitic capacitance and, thus, reduce the power loss. The implemented circuit, switch sizing and optimization of the power switches and drivers followed the methodology discussed in [19], with conversion ratios of 1/2.

As shown in Fig. 20, the circuit implementation of the SC unit and its driver is depicted. The structure consists of four switches and a flying capacitor. The voltage domain stacking technique [12] is utilized in this design to reduce the switching losses and avoid all the switches exposed to a voltage higher than the breakdown voltage. The power switches M1 and M3 operate in the upper voltage domain (voltage domain 1), while M2 and M4 operate in the lower

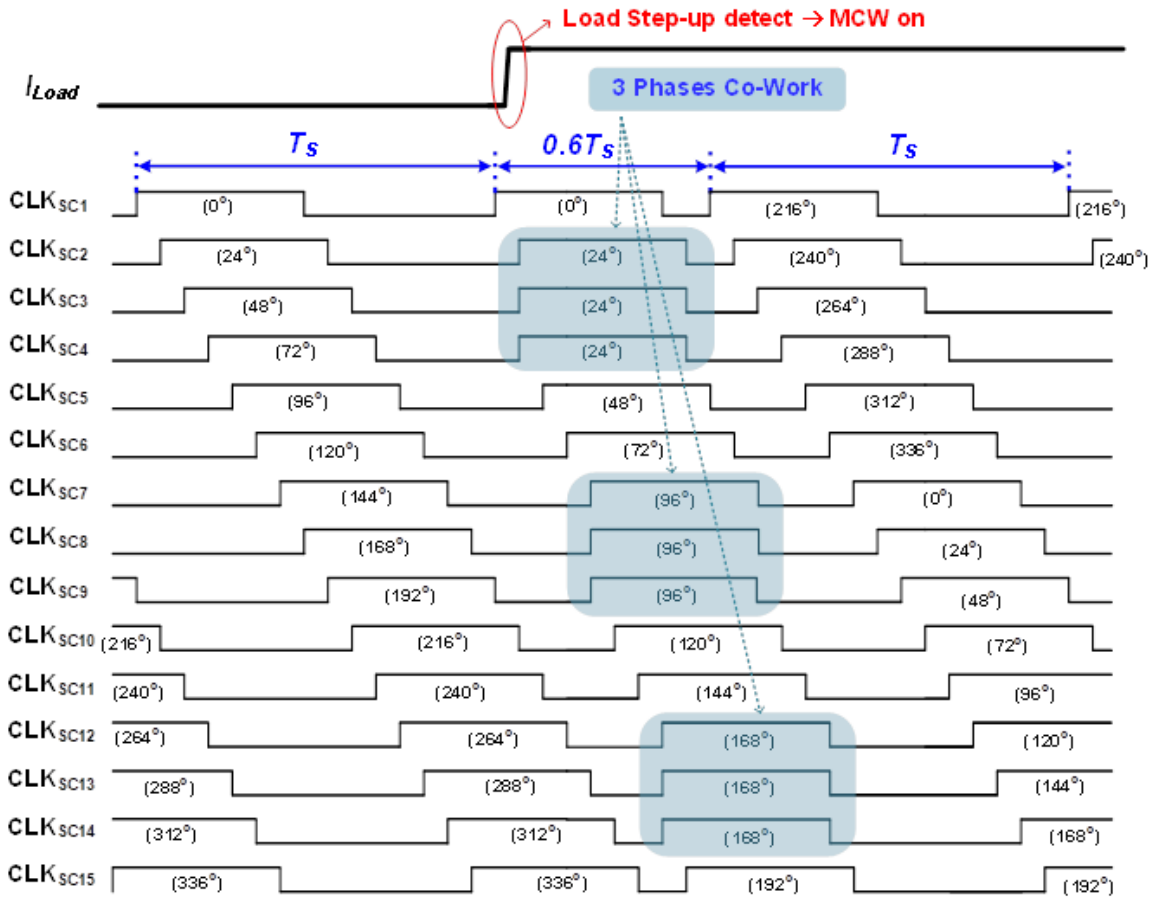


Fig. 18. Overall clock diagram of a 15-phase interleaved SC dc–dc converter with the MCW scheme.

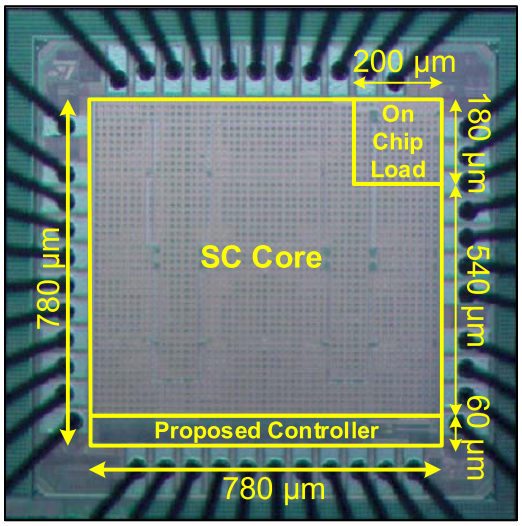


Fig. 19. Chip micrograph.

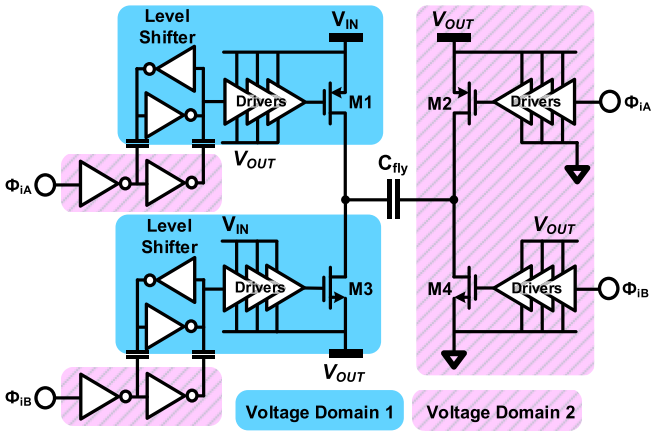


Fig. 20. Circuit implementation of the SC unit.

voltage domain (voltage domain 2). Capacitive level shifters are employed to translate the control signals Φ_{iA} and Φ_{iB} from the lower voltage domain to the upper voltage domain. The drivers are implemented by the cascaded inverters, and their sizes increase until the last stages are sufficient to drive the switches. Each SC unit operates in two nonoverlapping clocks Φ_{iA} and Φ_{iB}, which is translated from the output phase Φ_i $(i = 1, 2, \ldots, 15)$ of the 15-phase generator with MCW control. The circuit and waveform of the nonoverlapping clock generator are shown as in Fig. 21. Because the minimum-size bypassing gates are employed inside the MCW, and each SC unit only has one set of the clock drivers associated with it. There is only small parasitic capacitance imposed between the SC blocks, which does not degrade the power efficiency significantly due to MCW implementation.

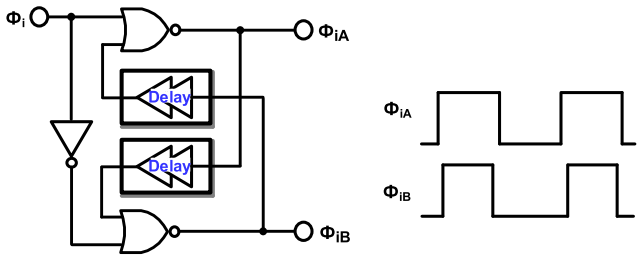


Fig. 21. Nonoverlapping clock generator.

TABLE I
CHIP AREA SUMMARY

Circuit	Area (mm^2)	Occupied Ratio
SC Core	0.527	86.4%
Proposed Controller, Comparators, Multiphase Generator	0.047	7.7%
On Chip Load Current Generator	0.036	5.9%
Total	0.61	100.0%

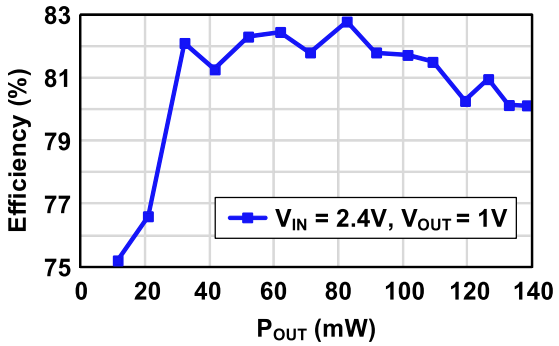


Fig. 22. Measured converter efficiency as a function of output power for $V_{IN} = 2.4$ V and $V_{OUT} = 1$ V.

Table I presents the chip area summary. The SC core occupies 86.4% of the total area. The proposed controller, comparators, and multiphase generator occupy 7.7% of the area, and we use the remaining 5.9% for on-chip load current testing.

In this work, the phase number of 15 is chosen to interleave the SC units. If the number of interleaved channel is even, there is always a pair of clock phases just in exactly 180° out of phase. Then, 2X current ripple appears on the output load current since the two charging clock edges overlap at the same time. If the interleaved channel number is odd, the charging clock edges do not overlap. Consequently, the current ripple is smaller.

Fig. 22 exhibits the measured efficiency of the converter with an input voltage $V_{IN} = 2.4$ V and a constant output voltage $V_{OUT} = 1$ V delivered to the load. We conducted this measurement by sweeping the load current, with a wide loading range from 11 to 138 mA. The power efficiency is higher than 75% at light load. We also observe >80% efficiency from 31 to 138 mA, with a peak efficiency of 82.8% at a current of 80 mA.

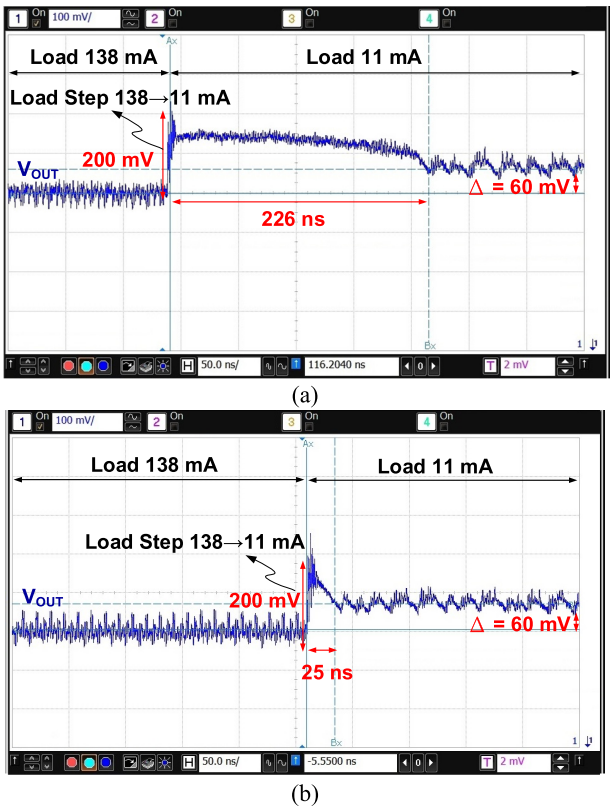


Fig. 23. Measured output voltage waveforms during heavy-to-light load transition from 138 to 11 mA while (a) SFM turns off and (b) SFM turns on.

Fig. 23(a) and (b) shows the measured output voltage waveforms during heavy-to-light load transient under the condition of the load current changing from 138 to 11 mA while SFM turns off and on, respectively. As plotted in Fig. 23(a), when a load current step changes from heavy to light, it generates an overshoot phenomenon. Without the SFM technique, the output voltage takes about 226 ns to recover to its steady-state value. When the SFM turns on, it takes only 25 ns for the output voltage to recover to its steady-state value as depicted in Fig. 23(b). The experimental results confirm that the proposed SFM control technique can assist the VCO-based control loop to obtain faster load transient response during the heavy-to-light load transient situation.

Fig. 24(a) and (b) displays the measured output voltage waveforms during light-to-heavy load transient under the condition of the load current changing from 11 to 138 mA while MCW turns off and on, respectively. From Fig. 22(a), when a load current step changes from light to heavy, it generates an undershoot phenomenon. It takes 100 ns for the output voltage to recover to its steady-state value while MCW does not turn on. On the other hand, from Fig. 24(b), it takes only 29 ns for the output voltage to recover to its steady-state value when the MCW turns on. This demonstrates that the MCW control can significantly improve the recovery speed during the light-to-heavy load transient case.

TABLE II
PERFORMANCE COMPARISON WITH STATE OF THE ART

		[12] JSSC 2011	[13] ISSCC 2013	[14] ISSCC 2014	[15] TPE 2016	[9] JSSC 2017	This Work
Technology		90 nm	65 nm	32 nm SOI	28 nm FD-SOI	65 nm	65 nm
Topology		1/2 SC	1/3, 2/5 SC	1/2, 1/3 SC	1/3, 1/2, 2/3, 3/4 SC	1/2, 2/3, 3/4 SC	1/2 SC
Interleave Phase		10	18	16	8	123	15
Capacitor Type		MOS & MIM	MOS	Deep Trench	MIM	MOS, MOM & MIM	MOS
C_{fly} / C_{out}		2 nF / 3.2 nF	3.88 nF / 0	1 nF / 0	8.3 nF	4.8 nF / 0	2.56 nF / 0
SC Frequency		70 MHz	1 - 300MHz	125MHz	NA	0.25 - 50MHz	1 - 250 MHz
V_{IN}		3 - 3.6 V	3 - 4 V	1.8 V	1.8 V	1.6 - 2.2 V	2.4 V
V_{OUT}		1.3 - 1.5 V	1 V	0.7-1.1 V	0.2-1.1 V	0.6 - 1.2 V	1 V
$P_{OUT, MAX}$		150 mW	162 mW	840 mW	250 mW	152 mW	138 mW
Active Area		3.24 mm^2	0.64 mm^2	0.15mm^2	0.52 mm^2	0.84 mm^2	0.61 mm^2
Power Density		50 mW/mm^2	253 mW/mm^2	2.17 W/mm^2	310 mW/mm^2	180 mW/mm^2	240 mW/mm^2
η_{peak}		77%	74.3%	90%	72.5%	78.3%	82.8%
Load Transient Step		42 <->72 mA	0<->162 mA	30<->365 mA	50<->130 mA	10<->110 mA	11<->138 mA
Heavy-to-Light Recovery	Time	N/A	700 ns*	250 ns*	200 ns	25 ns*	25 ns
	FOM	N/A	0.23 mA/ns	1.3 mA/ns	0.4 mA/ns	4 mA/ns	5.1 mA/ns
Light-to-Heavy Recovery	Time	25 ns	80 ns*	200 ns*	200 ns	25 ns*	29 ns
	FOM	1.2 mA/ns	2 mA/ns	1.68 mA/ns	0.4 mA/ns	4 mA/ns	4.38 mA/ns
Controller Area Overhead		N/A	8 %	11.1 %	11.5 %	< 10 %	7.7 %

* Estimated by the presented measurement results

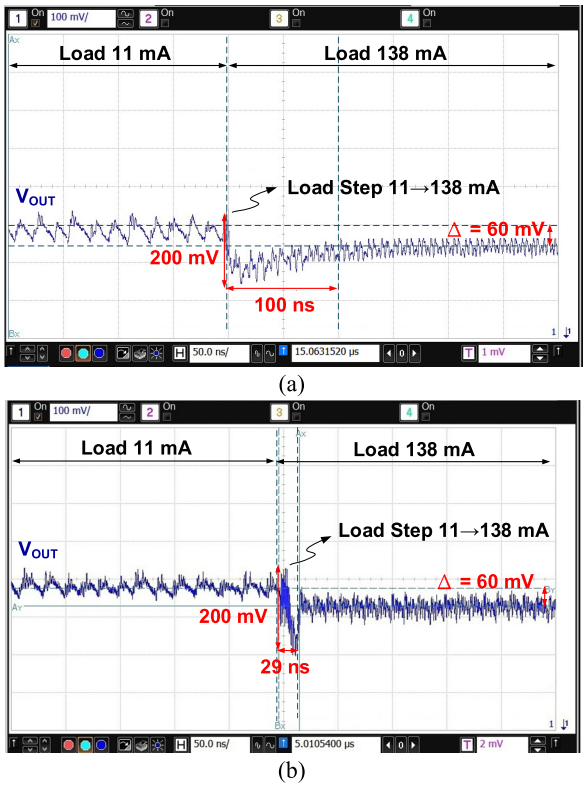


Fig. 24. Measured output voltage waveforms during light-to-heavy load transition from 11 to 138 mA while (a) MCW turns off and (b) MCW turns on.

As noted from Figs. 23 and 24, the overshoot and undershoot are around 200 mV, and there is about 60 mV drop (6% of V_{OUT}) between 11 and 138 mA at steady state. The measured ripple voltages are about 60 mV in full load condition. In the measurement, we set V_{DD} as 1.2 V, the nominal voltage V_{NRM} as 1.06 V with V_{R_L} set as 0.96 V. The loop response time is within 5 ns, with the VCO switching frequency ranging from 1 to 250 MHz for the entire load range, while the clock frequency of the comparators is 1.5 GHz. A fully dynamic latch-type voltage sense amplifier [21] is chosen to implement the circuit of comparators, which can operate at high speed with low power consumption.

Table II presents the performance comparison of the proposed work with other designs of fully integrated switched capacitor dc–dc converters [9], [12]–[15]. These works revolved around the improvement of the multiphase feedback control loop, thus approaching the faster transient dynamic response of the converters. The test chip of [13] employs a current-starved VCO controller to distribute 18 interleaving phases and occupies 0.64 mm^2 by using MOS flying capacitors in 65 nm. The design chip of [14] using the deep-trench capacitor in 32-nm silicon-on-insulator (SOI) achieves remarkable efficiency and power density performances. For comparison with recovery speeds between the converters, we define the figure of merit (FOM), as

$$\text{FOM} = \frac{\Delta I_{\text{Load}}}{t_{\text{R}}} \tag{3}$$

where ΔI_{Load} is the load step current during the load transient, and t_{R} is the recovery time. The larger FOM reveals the better load transient recovery capability. When compared with previous designs, this work exhibits a competitive efficiency at comparable power densities, revealing also a superior recovery speed at the load transients.

VI. Conclusion

This paper proposed two load transient enhancement control techniques: segmented frequency modulator (SFM) and MCW to reduce the recovery time during heavy-to-light and light-to-heavy load transients. We verified these two methods through a proof-of-concept converter prototype implemented in 65-nm CMOS. The 15-phase interleaved converter implementation supports output voltages of 1 V from a 2.4-V input supply attaining 82.8% peak efficiency at an output power density of 240 mW/mm^2. From light-to-heavy and heavy-to-light load transients, the converter can also reach a fast recovery speed of 5.1 and 4.38 mA/ns, respectively, reflecting a state-of-the-art transient recovery performance.

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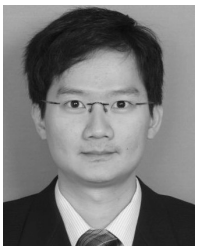

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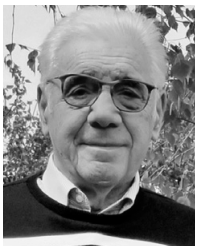

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Dr. Martins was a member of IEEE CASS Fellow Evaluation Committee (2013, 2014, 2018—Chair, and 2019). In 2010, he was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia. He was a recipient of the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He received two Macao Government Decorations: the Medal of Professional Merit (Portuguese 1999) and the Honorary Title of Value (Chinese 2001). He was the Founding Chair of IEEE Macau Section from 2003 to 2005 and IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)], and the General Chair IEEE Asia–Pacific Conference on CAS—APCCAS'2008. He was the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) (2014) and the IEEE CASS Nominations Committee from 2016 to 2017. He was the General Chair of ACM/IEEE Asia South Pacific Design Automation Conference—ASP-digital-to-analog converter (DAC)'2016. He was the Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013 and nominated as the Best Associate Editor from 2012 to 2013. He was the Vice President (VP) from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities (AULP). He was the VP Region 10 (Asia, Australia, and Pacific) from 2009 to 2011, and VP-World Regional Activities and Membership of IEEE CASS from 2012 to 2013.