A Single-Chip Solar Energy Harvesting IC Using Integrated Photodiodes for Biomedical Implant Applications

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***Abstract*—In this paper, an ultra-compact single-chip solar energy harvesting IC using on-chip solar cell for biomedical implant applications is presented. By employing an on-chip charge pump with parallel connected photodiodes, a 3.5× efficiency improvement can be achieved when compared with the conventional stacked photodiode approach to boost the harvested voltage while preserving a single-chip solution. A photodiode-assisted dual startup circuit (PDSC) is also proposed to improve the area efficiency and increase the startup speed by 77%. By employing an auxiliary charge pump (AQP) using zero threshold voltage (ZVT) devices in parallel with the main charge pump, a low startup voltage of 0.25 V is obtained while minimizing the reversion loss. A $4\,V_{in}$ gate drive voltage is utilized to reduce the conduction loss. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency. The proposed system is implemented in a standard 0.18-μm CMOS technology and occupies an active area of 1.54 mm^2. Measurement results show that the on-chip charge pump can achieve a maximum efficiency of 67%. With an incident power of 1.22 mW/cm^2 from a halogen light source, the proposed energy harvesting IC can deliver an output power of 1.65 μW at 64% charge pump efficiency. The chip prototype is also verified using *in-vitro* experiment.**

***Index Terms*—Auxiliary charge pump, charge pump/solar cell area optimization, photodiode-assisted dual startup circuit, single-chip solar energy harvesting.**

I. Introduction

THE emerging eHealthcare system is patient-driven, where patients can continuously monitor their own health status even at home. Their physiological data, such as breathing, electrocardiogram (ECG), heart beat, glucose level and so on, can be sent back to dedicated medical data servers wirelessly for further analysis. Existing research on implantable/wearable systems include retinal prosthesis [1], intraocular pressure monitoring [2], wearable ECG [3], and many others. In order to achieve minimal invasiveness for implantable devices, such systems should be miniaturized as much as possible, leading to a stringent size and energy bottleneck. As a result, energy harvesting becomes a favorable alternative to achieve system autonomy or even battery replacement in various implantable systems.

Solar energy harvesting has been recently demonstrated as a viable solution in applications including intraocular pressure monitoring [2] and subdermal implant applications [4]. In [5] and [6], the feasibility of powering CMOS circuitry using different types of photodiodes built on the substrate in standard CMOS is demonstrated. By integrating the CMOS circuitry and solar energy harvester on the same chip, the associated difficulty during the system assembly can be much relaxed, improving the system reliability and reducing the cost. However, the low voltage generated by integrated photodiodes (typically ranging from 0.3 V to 0.5 V) can result in significant circuit performance degradation. Even though a complete sensor readout circuit directly powered by on-chip solar cells in the same substrate is demonstrated in [4], the achieved sensing accuracy is limited. Various attempts to passively boost the voltage generated by integrated photodiodes have been reported. In [7], the property of Silicon-on-Insulator (SOI) is exploited to serially connect photodiodes with separate substrates, but with the tradeoff of increased cost. In [8] and [9], different approaches to stack photodiodes in a standard CMOS process are studied. Nevertheless, due to the single substrate limitation, the total photosensitive area cannot be optimized, sacrificing the overall energy harvesting efficiency.

Instead of passively stacking integrated photodiodes, a more efficient approach is to employ DC-DC converters to boost the low voltage generated. Even though an inductor-based boost converter solution can be employed to boost up the voltage harvested by on-chip solar cells as demonstrated in [10], the requirement for large off-chip components can jeopardize its applicability in implantable applications. To solve this problem, charge pumps using integrated capacitors while preserving ultra-low voltage operations can be employed. In [11], a solar energy harvesting charge pump with a startup voltage of 0.27 V is introduced. However, the ZVT switches and the non-uniform gate drive voltages can lead to increased reversion

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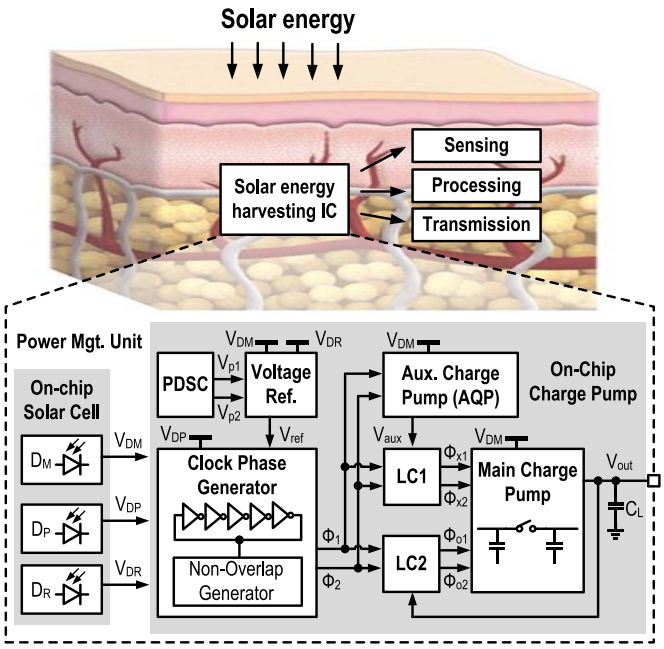

Fig. 1. System overview of the proposed single chip solar energy harvesting system in subdermal implant applications.

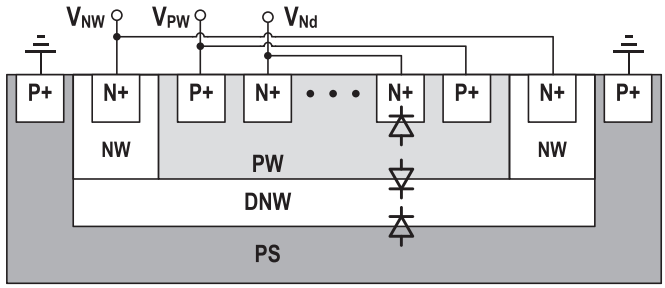

Fig. 2. Illustrative diagram showing the PN junctions available in a standard triple-well CMOS process.

TABLE I
MEASURED PHOTODIODE PERFORMANCE WITH PARALLEL AND STACK CONNECTIONS UNDER AN INCIDENT POWER OF 1.13 mW/mm^2 FROM A HALOGEN LIGHT SOURCE

Parameter	Diode Type			Connection	
	N+/PW	PW/DNW	DNW/PS	Parallel	Stacked
I_{sc}(pA/μm^2)	74.3	69.6	433	577	74.7
V_{oc}(V)	0.55	0.527	0.526	0.53	1.05
Max. Eff.(%)	2.8	2.6	16.7	21.9	5.9

I_{sc}: Short-Circuit Current V_{oc}: Open-Circuit Voltage

and conduction losses, sacrificing the efficiency. In [12], an ultra-low input voltage energy harvesting charge pump that can operate down to 0.15 V using dynamic body biasing is proposed. But it requires 6 off-chip capacitors that can lead to significant packaging complexity and overhead. In [13], a complete die-stacked sensing platform using integrated solar energy harvesting is reported. Nevertheless, the feasibility and co-optimization of a single-chip solar energy harvesting solution, that can boost the harvested voltage while achieving a high efficiency suitable for implantable applications, is yet to be demonstrated.

In this paper, we propose a single-chip solar energy harvesting system using a 3-stage integrated charge pump with on-chip photodiodes. An output power in the μW level is targeted for subdermal implant applications, where the key challenge is to achieve high energy efficiency at ultra-low power levels and in a small volume [14]. By preserving a single-chip solution, a complete highly efficient energy harvesting system with a high output voltage as well as an ultra-compact form factor can be accomplished while fulfilling the system dynamic range requirement [15].

II. SYSTEM ARCHITECTURE

Fig. 1 shows the application scenario of a typical subdermal implant, which is responsible for harvesting the incoming solar energy, retrieving the physiological data from miniaturized sensors, processing the collected data and transmitting the acquired information wirelessly. This work focuses on the power management unit, where on-chip charge pump and integrated photodiodes are utilized to provide an ultra-compact highly efficient energy harvesting solution.

The proposed single-chip solar energy harvesting system is comprised of an on-chip solar cell, a voltage reference with a photodiode-assisted dual startup circuit (PDSC), a clock phase generator, an auxiliary charge pump (AQP), two level converters (LCs) and a main charge pump. The solar cell harvests the incoming solar energy and provides power to the other building blocks as well as to the load. To prevent noise coupling between modules, the solar cell is divided into three sub-blocks D_M, D_P, and D_R to provide energy to the main/auxiliary charge pump, clock phase generator and voltage reference, respectively. The voltage reference generates a reference voltage $V_{\rm ref}$ for biasing the clock phase generator. PDSC is proposed to improve the voltage reference startup time while imposing minimum overhead. The clock phase generator provides a two-phase non-overlapping clock Φ_1 and Φ_2 to the AQP and LCs using a 5-stage ring oscillator with body-biasing optimized for on-chip solar energy harvesting. Instead of implementing the main charge pump with zero threshold devices as in [11], an AQP is utilized to generate an auxiliary supply voltage $V_{\rm aux}$ to LC1 to ensure a low startup voltage while minimizing the reversion loss. High swing clock phases Φ_{x1}/Φ_{x2} and Φ_{o1}/Φ_{o2} are utilized for improved conduction loss in the main charge pump. Descriptions of individual building blocks are outlined as follows.

A. On-Chip Photodiode

Fig. 2 shows the PN junctions available for serving as on-chip photodiodes in a standard triple-well CMOS process, including: (i) N+/PW; (ii) PW/DNW; and (iii) DNW/PS. In order to characterize the photodiode performance using the selected 0.18-μm CMOS process, test structures are fabricated and measured under direct illumination using a halogen light source with an incident power of 1.13 mW/mm^2. The corresponding measurement results are shown in Table I. It can be observed

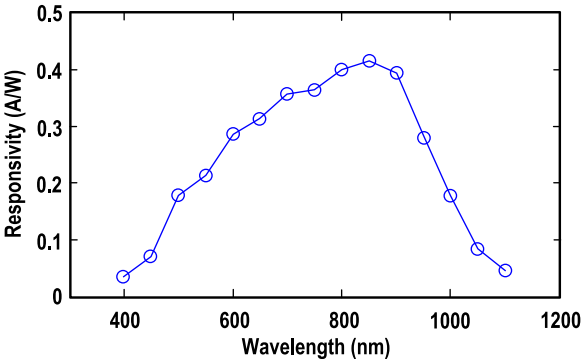

Fig. 3. Measured responsivity of the proposed parallel photodiode configuration.

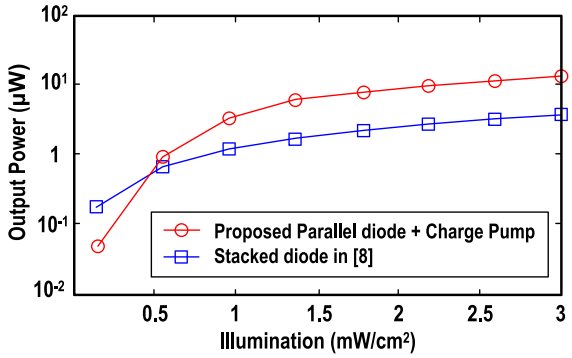

Fig. 4. Simulation results showing the achieved output power of the proposed photodiode with charge pump and the stacked photodiode approach in [8] under the same area budget.

that the normalized short-circuit current density from DNW/PS is almost 6 times larger than that obtained from N+/PW and PW/NW, which is consistent with [9]. As a consequence, unlike [4] that shorts DNW/PS for generating a positive output voltage, the DNW/PS photodiode is utilized to improve the energy harvesting efficiency at the expense of an extra inversion stage. Apart from that, the harvested low voltage should be further boosted for system use. Even though passive stacking on photodiodes as in [8] (by shorting the PW/DNW photodiode) can be employed to increase the output voltage, the incurred efficiency loss due to the shorting of PW/DNW and the mismatch between N+/PW and DNW/PS can be significant as shown in Table I. To address the above issues while improving the energy harvesting efficiency and maintaining a compact solution, we propose to utilize all the available on-chip photodiodes through parallel connections and subsequently boost the harvested voltage using an on-chip charge pump built on the same substrate.

Fig. 3 shows the measured responsivity of the proposed parallel photodiode configuration. The maximum responsivity is achieved at a wavelength of 850 nm. Fig. 4 shows the simulated results of the proposed parallel photodiode together with our designed on-chip charge pump as well as the solar energy harvesting system using stacked photodiodes from [8] with the same technology and active area of 1.54 mm^2. The incident power is expected to be within 3 mW/cm^2 for harvesting power in the order of few μW. It can be observed that almost 3.5$\times$ more output power can be extracted using our proposed approach with an incident power of approximately 1.22 mW/cm^2. The loss in efficiency at very low illumination levels is mainly due to the overhead of the on-chip charge pump as expected.

B. Voltage Reference

The voltage reference serves as an important module to generate the required biasing and wake up the entire system. As the open-circuit voltage generated by on-chip photodiodes is small, the voltage reference should be designed to operate at a low supply voltage. In this work, we implemented the voltage reference based on [16], which can achieve ultra-low voltage/power operation and is therefore suitable to be powered using on-chip photodiodes with nA power consumption. However, the slow startup problem due to the use of a conventional startup circuit under a low supply voltage still remains unresolved. Apart from that, the large energy surge during the startup period can lead to system instability or even startup failure for the proposed system where the available energy can be limited. To resolve the above issues, PDSC is proposed to ensure a robust startup process with minimal overhead while improving the startup time.

Fig. 5(b) shows the proposed voltage reference with PDSC. The voltage reference operation can be found in [16]. The PDSC is composed of a light induced startup signal V_R, and two photo-delay generators ($\mathrm{PDG}_{1,2}$) for controlling M_{st1} and M_{st2}, respectively. The schematic of the PDG is shown in Fig. 5(a). To improve the startup time, locally self-stacked photodiodes are utilized to generate a local high voltage to reduce the switch on-resistance for improved startup speed while imposing minimal overhead. The capacitor C_x is utilized to generate different delays from the two PDGs during the startup sequence. V_R is employed to discharge C_x of the two PDGs to prevent possible startup failure during a fast incident power transient. As mentioned before, the startup circuit consumes a transient power which can be much larger than the nominal power consumption of the voltage reference during the startup period. This can limit the startup speed or even lead to startup failure. Instead of increasing the size of D_R to cater for the extra energy required during system startup, PDG_2 is employed to temporarily connect D_R and D_M to support the extra energy required during the startup process, improving the system area efficiency.

Fig. 5(c) shows the illustrative timing diagram of a typical startup sequence. In the beginning of the startup period, the incoming solar energy triggers V_R, and two pulses V_{p1} and V_{p2} with different pulse widths are generated by $\mathrm{PDG}_{1,2}$, respectively. D_M is connected to D_R through M_{st2} to provide the extra startup energy, and is disconnected at the end of V_{p2}. Fig. 6(a) shows the transient simulation results of the voltage reference using the conventional startup as in [16] and our proposed PDSC with an incident power of 1.22 mW/cm^2, and the startup time comparison is shown in Fig. 6(b). It can be concluded that a startup time improvement by 77% with an incident power of 1.22 mW/cm^2 can be achieved. Notice that the peaking of V_{ref}, which is contributed by the large shoot-through current during the startup process, can be alleviated by optimizing the sizing of Mst1 while ensuring robust startup operation under process variations.

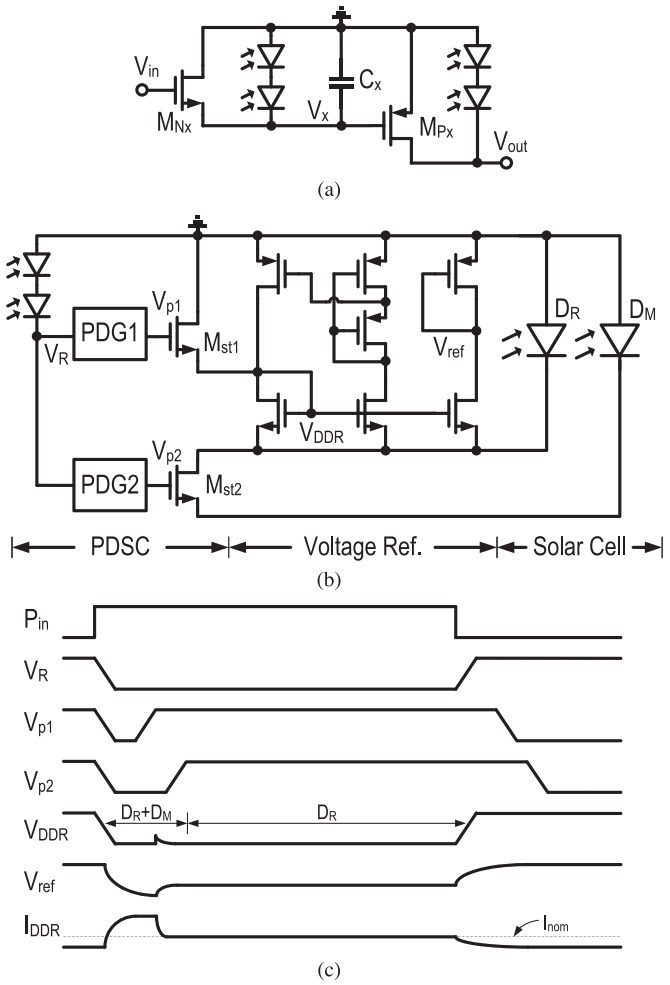

Fig. 5. Simplified schematic showing (a) the photo-delay generator (PDG), (b) the proposed voltage reference with PDSC, and (c) the corresponding timing diagram.

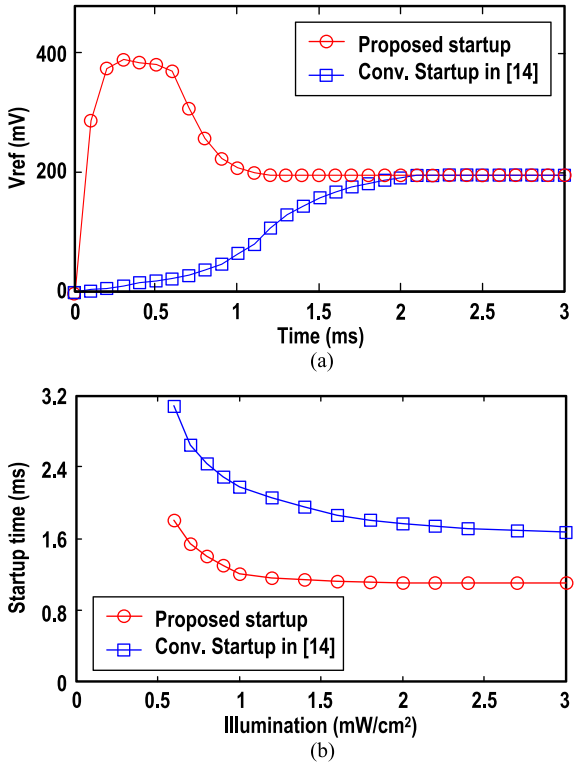

Fig. 6. Simulation results of the voltage reference showing (a) the transient waveform of the proposed PDSC and the conventional startup in [16] at an incident power of 1.22 mW/cm^2, and (b) the startup time comparison under different illumination levels.

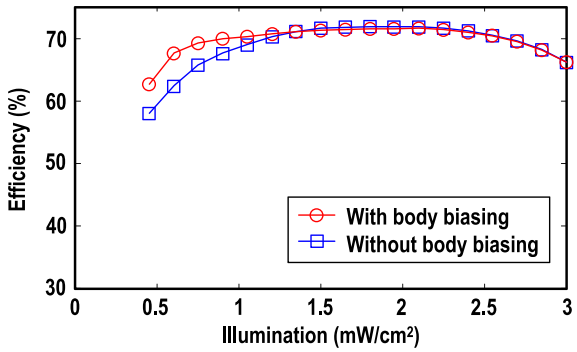

Fig. 7. Simulation results of the proposed charge pump with and without using body biasing for the clock phase generator.

C. Clock Phase Generator

The on-chip charge pump should operate at a frequency in the order of MHz to reduce the output impedance as a result of the limited size of the flying capacitors. Nevertheless, due to the low voltage generated by the on-chip solar cell, the operating frequency of the ring oscillator and the non-overlap clock generator can be sacrificed. As a result, forward biasing both the PMOS and NMOS body [17] is utilized to increase the operating frequency. Fig. 7 shows the simulated efficiency of the on-chip energy harvesting charge pump both with and without body biasing at different illumination levels. It can be observed that body biasing can significantly increase in efficiency by up to 5% at low light conditions, while resulting in only an approximate 0.5% efficiency reduction at high illumination levels due to parasitic loss.

D. On-Chip Charge Pump

Conventionally, bootstrapping and ZVT switches are utilized for solar energy harvesting applications due to the low input voltage $V_{\rm in}$. This will inevitably lead to significant reversion loss due to the increased leakage as in [11], sacrificing the overall efficiency. The non-uniform gate drive voltages in [11] can also increase the conduction loss. Fig. 8(a) and (b) shows the simplified schematics of the proposed auxiliary and main charge pump based on the linear charge pump topology, respectively. In order to minimize the reversion loss while maintaining a low startup voltage, ZVT switches [shown as shaded in Fig. 8(a)] are only utilized in the AQP. The AQP, which is preceded by an inversion stage and followed by two boosting stages, generates an output voltage $V_{\rm aux}$ at $3V_{\rm in}$ to obtain a pair of high swing clock $\Phi_{x1,2}$ through LC1 for controlling the cold start switches in the main charge pump, to charge up $V_{\rm out}$. $V_{\rm out}$ is then utilized to power up LC2 to generate $\Phi_{o1,2}$ for driving

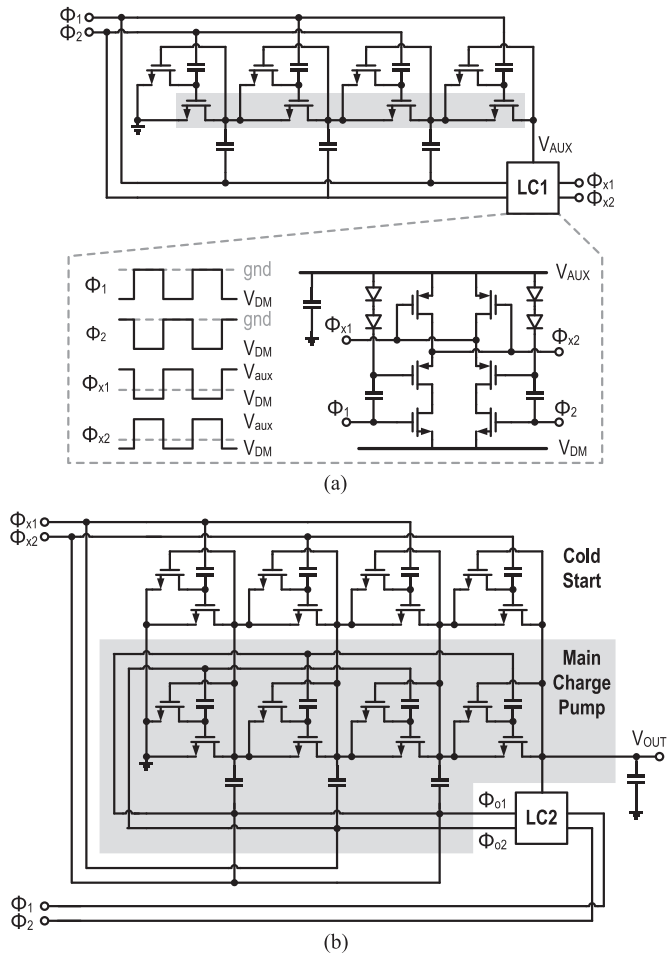

Fig. 8. Simplified schematic showing the (a) AQP and LC, and (b) main charge pump with cold start switches in parallel.

the main switches and work cooperatively with $\Phi_{x1,2}$ in the steady state to further improve the efficiency. The main charge pump switches are controlled with a $4V_{\rm in}$ gate drive voltage to reduce the conduction loss. The structure of LC1 (LC2 is similar) is shown in Fig. 8(a). To balance the pull up/down speed of the LC, the turn on voltage of the pull up PMOS is buffered by a 50 fF capacitor. Notice that the AQP is also turned on during normal operations to improve the heavy load efficiency.

III. System Analysis and Optimization

To maximize the energy harvesting efficiency of the on-chip solar cell, all the available photodiodes are utilized and connected in parallel, as discussed in Section II-A. A 3-stage linear charge pump (one inversion stage + two boosting stages) is utilized to convert the negative voltage into a high output voltage.

A. Switching Loss Optimization

For a N-stage linear charge pump within an input voltage $V_{\rm in}$ (i.e., the harvested voltage from on-chip photodiodes in the proposed system), the corresponding output voltage $V_{\rm out}$ can be approximated as

$$V_{\rm out} = N\left(V_{\rm in}\frac{C_{\rm fly}}{C_{\rm fly}+C_P} - R_{\rm eq,on}I_{\rm out}\right) \tag{1}$$

where $C_{\rm fly}$ is the flying capacitance, C_P is the parasitic capacitance, $R_{\rm eq,on}$ is the equivalent switch on-resistance, and $I_{\rm out}$ is the load, respectively. The equivalent on-resistance of a switch can be approximated as [18]

$$R_{\rm eq,on} = \sqrt{\sum R_{\rm on}^2 + \frac{1}{fC_{\rm fly}}^2} \tag{2}$$

where $R_{\rm on}$ is the on-resistance of a switch and f is the frequency. To achieve a high charge pump efficiency, $R_{\rm eq,on}$ should be much smaller than R_L to minimize conduction loss, where R_L is the equivalent load resistance. For a micro-power charge pump, the reversion loss, which is characterized by the switch off-resistance $R_{\rm off}$, can become significant and hence cannot be neglected. As a result, both the switch on- and off-resistance should be optimized, leading to

$$R_{\rm off} \gg R_L \gg R_{\rm eq,on}. \tag{3}$$

From [19], when the drain-source voltage $V_{\rm ds}$ is much smaller than the overdrive voltage $V_{\rm gs}-V_{\rm th}$, where $V_{\rm gs}$ is the gate-source voltage and $V_{\rm th}$ is its threshold voltage, respectively. $R_{\rm on}$ can be expressed as

$$R_{\rm on} = \frac{1}{\mu C_{\rm ox}\left(\frac{W}{L}\right)\left((V_{\rm gs}-V_{\rm th}\right)} \tag{4}$$

μ is the electron mobility, $C_{\rm ox}$ is the unit oxide capacitance and W/L is the aspect ratio. Similarly, when $V_{\rm ds}$ is much larger than $4V_T$ (V_T is the thermal voltage) when the switch is turned off, $R_{\rm off}$ can be expressed as

$$R_{\rm off} = \frac{V_{\rm ds}}{Se^{\frac{V_{\rm gs}-V_{\rm th}}{mV_T}}} \tag{5}$$

where S is a proportional factor. From (4) and (5), it can be observed that a lower $V_{\rm th}$ reduces $R_{\rm off}$ more rapidly than $R_{\rm on}$. As a result, the charge pump efficiency is sacrificed especially when R_L is large, rendering the use of low $V_{\rm th}$ devices or body biasing technique [17] as the charge pump switches unsuitable. Even though the switching body biasing technique [12] can extend the ratio between $R_{\rm on}$ and $R_{\rm off}$, the increase in design overhead under a variable input condition for micro-power energy harvesting applications can be undesirable. Comparatively, a better solution should be to increase the switch driving voltage $V_{\rm gs}$.

To determine the optimal switch driving voltage $V_{\rm gs}$, we first determine the associated switching power loss $(P_{\rm sw})$ of a charge pump, expressed as

$$P_{\rm sw} = \frac{N}{2}fC_0\sum W_iL_iV_{{\rm gs},i}^2 \tag{6}$$

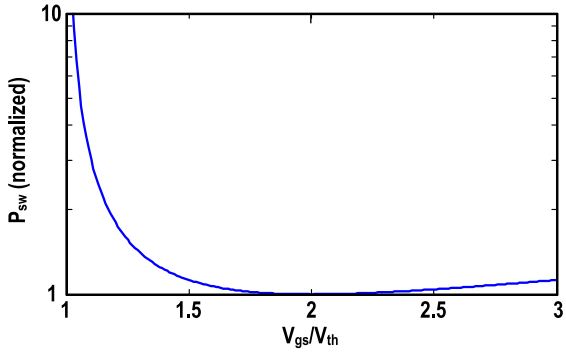

Fig. 9. Normalized switching loss $P_{\rm sw}$ versus different $V_{\rm gs}/V_{\rm th}$ ratios.

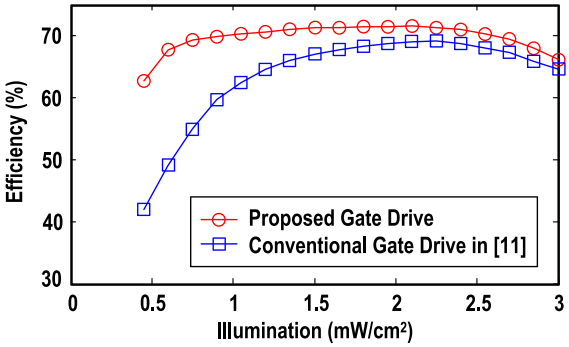

Fig. 10. Simulation results showing the efficiency of the proposed $4V_{\rm in}$ gate drive and the conventional approach in [11].

where n is the number of stage for the charge pump, f is the switching frequency, C_0 is the gate capacitance per unit area, and W_i, L_i and $V_{{\rm gs},i}$ are the switch width, switch length and gate driving voltage of the i-th switch, respectively. Due to the limited $C_{\rm fly}$, a high switching frequency f is required to suppress the series loss. This will inevitably increase the gate switching loss $P_{\rm sw}$ which can be significant for micro-power energy harvesting. As shown in (4) and (5), $R_{\rm on}$ varies significantly when $V_{\rm gs}$ is close to $V_{\rm th}$. As a result, an increase in switch driving voltage $V_{\rm gs}$ should be ensured instead of enlarging the switch width W when the input voltage is low. From (4) and (6), it can be observed that an increase in $V_{\rm gs}$ can reduce the loss through $R_{\rm on}$ while increasing $P_{\rm sw}$. By substituting (4) into (6), the optimal $V_{\rm gs}$ can be deduced as

$$V_{\rm gs} = 2V_{\rm th}. \tag{7}$$

Fig. 9 shows the charge pump efficiency with respect to different ratios of $V_{\rm gs}/V_{\rm th}$ in a standard 0.18 μm CMOS process. It can be observed that the minimum normalized $P_{\rm sw}$ is achieved when $V_{\rm gs} \sim 2V_{\rm th}$ as expected. With a $V_{\rm th}$ of approximately 0.49 V (without body effect) and an expected worst case photodiode voltage of roughly 0.3 V, $V_{\rm gs}$ is therefore designed to be $4V_{\rm in}$. Fig. 10 shows the simulated efficiency by using the proposed AQP with the proposed $4V_{\rm in}$ gate drive and the one in [11] using the same area budget. It can be observed that our proposed scheme can achieve better efficiency over the targeted illumination power levels.

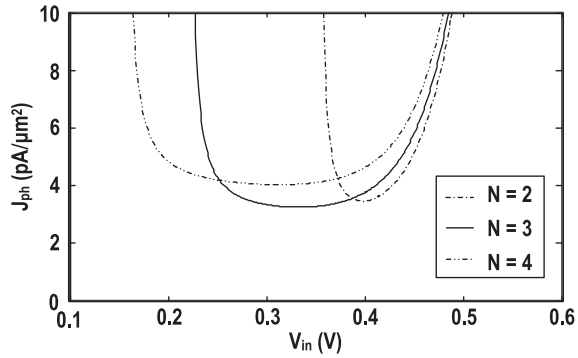

Fig. 11. Optimization of the photocurrent density versus photodiode voltage $V_{\rm in}$ using numerical method.

B. Solar Cell Area Optimization

To optimize the area of the proposed single-chip solar energy harvesting system, both the solar cell and the charge pump should be considered. As stated in [11], the charge pump current consumption $I_{\rm cp}$ can be expressed as

$$I_{\rm cp} = I_{\rm out}\left(N + \alpha\frac{N^2V_{\rm in}}{NV_{\rm in} - V_{\rm out}}\right) \tag{8}$$

where α is the ratio between the bottom plate parasitic and the nominal capacitance of the on-chip capacitor. The on-chip photodiode should be able to provide this charge pump current together with its intrinsic loss, and can be defined as

$$I_{\rm ph} = I_S e^{\frac{V_{\rm in}}{\eta V_T}} + I_{\rm cp} \tag{9}$$

where η and I_S are the non-ideality factor and the saturation current of the on-chip photodiode, respectively. To minimize the area of the on-chip solar cell, the photocurrent density $J_{\rm ph}$ for driving a particular charge pump load $I_{\rm out}$ should be minimized. The total capacitance $C_{\rm total}$ for a N-stage linear charge pump can be expressed as

$$C_{\rm total} = \frac{I_{\rm out}}{f}\frac{N^2}{NV_{\rm in} - V_{\rm out}}. \tag{10}$$

For a total chip area $A_{\rm total}$, the photocurrent is defined as

$$I_{\rm ph} = \left(A_{\rm total} - \frac{C_{\rm total}}{C_0}\right)J_{\rm ph} \tag{11}$$

where C_0 is the capacitance per unit area of the on-chip capacitor. By using (8)–(11), the optimized $J_{\rm ph}$ under different N and $V_{\rm in}$ can be obtained numerically, as shown in Fig. 11. It can be observed that the minimum $J_{\rm ph}$ of 3.3 pA/μm^2 can be achieved with $N = 3$. The optimized $C_{\rm total}$ can be deduced to be approximately 15% of $A_{\rm total}$.

IV. Measurement Results

The complete single-chip solar energy harvesting system is designed and fabricated in a standard 0.18-μm CMOS process. Fig. 12 shows the corresponding chip micrograph with key building blocks indicated. The on-chip photodiode, main flying capacitors, auxiliary flying capacitors and voltage reference

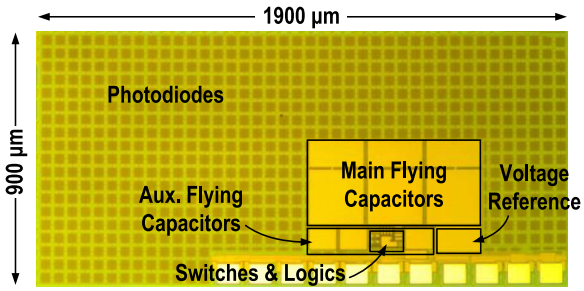

Fig. 12. Chip micrograph of the proposed single-chip solar energy harvesting IC with test pads for verifications only.

TABLE II
POWER DISTRIBUTION OF THE PROPOSED SYSTEM WITH AN INCIDENT POWER OF 1.22 mW/cm^2

	Simulated	Measured
Power Harvested	2.6 μW	2.58 μW
Power Consumed		
Ring Oscillator	3.3 nW	523 nW
Clock Phase generator	38.2 nW	
Voltage reference	0.9 nW	
Level converters	439 nW	
Power Delivered	1.8 μW	1.65 μW

occupy 1.3, 0.2, 0.04, and 0.02 mm^2, respectively. The total area is 1.54 mm^2 (excluding test pads which are utilized for verifications of different building blocks only). The charge pump to solar cell area ratio is approximately 18%, which is kept to be close to the value deduced in Section III-B. Storage capacitors are constructed underneath the flying (MIM) capacitors to save area. Circuits are shielded from incoming light using metal shielding on top.

The chip prototype is characterized with the halogen light source (Newport model no. 66885) using a light guide. The incident power is measured using the Newport Power Meter model 2936-C. Table II summarizes the simulated and measured power of the chip prototype under an incident power of 1.22 mW/cm^2. The harvested power is measured by using equivalent loads under the same illumination condition. The difference between the simulated and measured results is mainly due to process variations as verified by the corner models provided by the foundry. With a harvested power of 2.58 μW, a measured output power of 1.65 μW can be achieved. Fig. 13 shows the measured efficiency with respect to I_{out} under different illuminations (from 0.6 to 2.43 mW/cm^2). The on-chip clock frequency is fixed at 800 kHz. It can be seen that the proposed system achieves a maximum efficiency of 67% at $P_{\text{in}} = 0.6$ mW/cm^2, which is close to the simulated value. At higher illumination levels, the maximum efficiency slightly drops as a result of the reduction in the photodiode efficiency due to increased chip temperature during the measurement. Fig. 14 shows the measured transient waveform of the charge pump start up sequence with a loading of 10 MΩ (oscilloscope probe loading). The auxiliary charge pump controls the cold start switches to charge the loading capacitor when incoming light power is available. When V_{out} exceeds the predefined threshold, the main charge pump starts to operate. The voltage

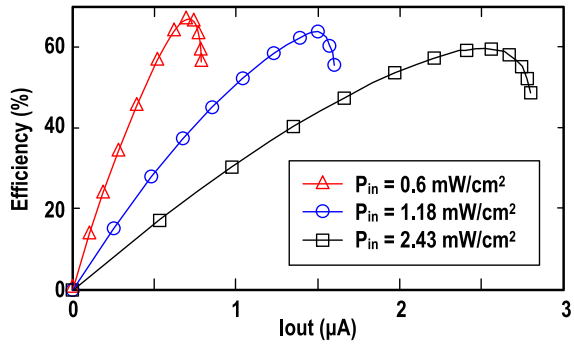

Fig. 13. Measured efficiency under different incident power levels.

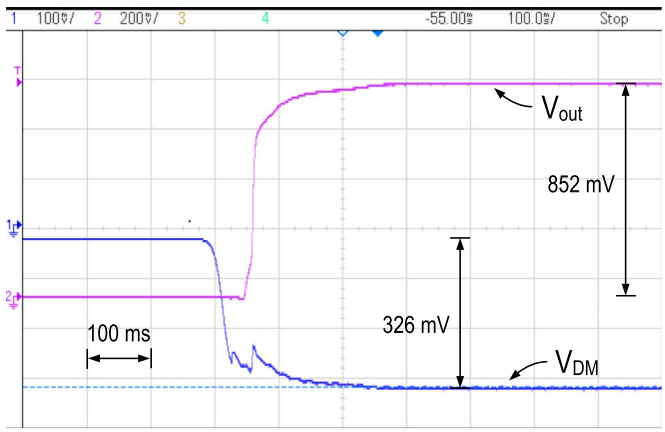

Fig. 14. Measured system startup waveform with an incident power of 0.6 mW/cm^2.

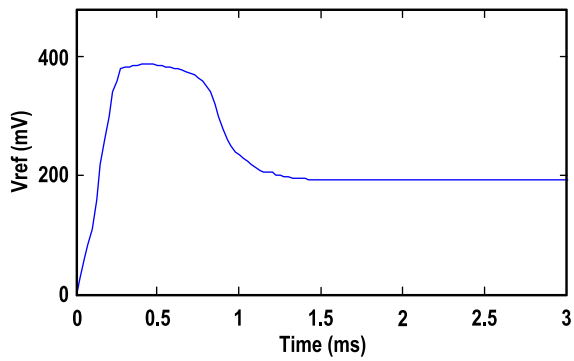

Fig. 15. Measured V_{ref} during startup with an incident power of 1.22 mW/cm^2.

droop at V_{DM} is due to the disconnection between D_R and D_M during the PDSC operation. An output voltage of 852 mV is achieved when the photodiode voltage V_{DM} is 326 mV. Fig. 15 shows the measured V_{ref} during the system startup with an incident power of 1.22 mW/cm^2, and the result is consistent with the simulated one. Fig. 16 shows the test setup for *in-vitro* system verification. A piece of pork skin with fat and muscle (1 mm + 2 mm + 1.5 mm) is utilized to mimic the situation for subdermal implant applications. It can be concluded that the proposed energy harvesting IC can successfully harvest the incoming solar energy. With an output power close to 1.6 μW, the measured source power is roughly 110 mW/cm^2, corresponding to an incident power loss of approximately 20 dB.

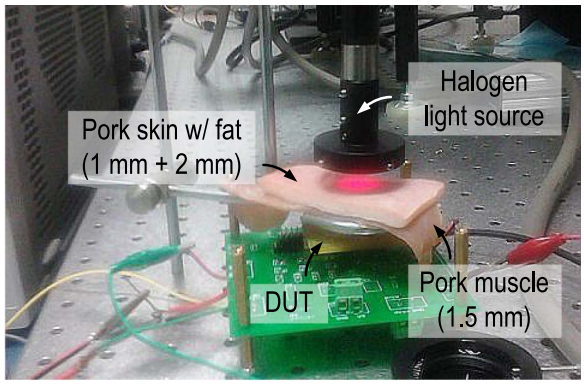

Fig. 16. *In-vitro* measurement setup using a pork skin + fat + muscle (1 mm + 2 mm + 1.5 mm).

TABLE III
PERFORMANCE COMPARISON WITH EXISTING INTEGRATED CHARGE PUMPS FOR ENERGY HARVESTING

	JSSC'13 [13]	TCAS-II'11 [11]	JSSC'15 [12]	This work
Process (μm)	0.18	0.13	0.13	0.18
Charge pump area (mm^2)	0.95	0.42	0.066	0.24
Capacitors	On-chip	On-chip	Off-chip	On-chip
Solar cell	External $1.62mm^2$	External $1.21mm^2$	–	**Integrated $1.3mm^2$**
Extra pads and packaging cost	Yes	Yes	Yes	**No**
No. of stages	6	3	3	3*
freq. (kHz)	335	800	250	800
Gate Drive	$3V_{in}$	$2 \sim 3V_{in}$	$2 \sim 3V_{in}$	$4V_{in}$
Min. V_{in}(V)	–	0.27	0.15	0.25
Max. Eff. (%) @V_{in} (V)	26.9^	61@0.35†‡	62@0.3†‡	**67@0.31**‡§

* One inversion + two boosting stages
^ Overall energy harvesting efficiency
† Extracted from the corresponding literature
‡ Without regulation
§ Corresponding to $P_{in} = 0.6$ mW/cm^2

Table III compares the performance of our work with state-of-the-art energy harvesting systems using on-chip charge pumps. Our work realizes a single-chip solar energy harvesting solution without the overhead of extra pads and packaging cost. The on-chip charge pump achieves the highest efficiency of 67% at low incident power levels (with an input voltage close to 0.3 V) which is expected in subdermal implant applications. Even though [12] can achieve a low input voltage down to 0.15 V, the requirement of 6 off-chip capacitors can induce significant overhead both in size and cost. The proposed PDSC also enables a fast voltage reference startup time of 1.4 ms with an incident power of 1.22 mW/cm^2, corresponding to a 77% improvement when compared to the conventional startup circuit. Table IV summarizes the performance comparison with existing single-chip solar energy harvesting solutions. It can be observed that our work results in the highest energy harvesting efficiency ($\sim$3.5$\times$ improvement when compared with [8]

TABLE IV
PERFORMANCE COMPARISON WITH EXISTING SINGLE-CHIP SOLAR ENERGY HARVESTING SOLUTIONS

	TED'12 [8]	TVLSI'11 [6]	This work
Process (μm)	0.35	0.35	0.18
Light source	White LED	Green laser (532 nm)	Halogen lamp
Incident light intensity	31 klx	34.2 μW	1.13 mW/mm^2
Area	0.69* mm^2 1.38^ mm^2	338 μm^2	1.3 + 0.24 mm^2
V_{oc} (V)	0.52*	0.533	0.53
I_{sc} (μA)	17.5*	680	750
P_{out} (μW)	7.14*	225	322
Eff. (%)	9.5*‡	24	21.9*
Voltage boosting	Stacked	–	On-chip charge pump
$V_{out,boosted}$ (V)	0.97^†	–	**1.08**§
$Eff_{boosted}$ (%)	3.5^	–	**12.1**§

* Single photodiode configuration only
^ Two-photodiode stacked configuration
† Estimated using the open-circuit voltage
‡ Extracted using a luminous efficacy of 285 lm/W
§ Corresponding to $P_{in} = 1.22$ mW/cm^2

while generating a boosted output voltage for system use. Simulation result shows that close-loop regulation using pulse skipping modulation similar to [11] can be achieved with a controller power overhead of 69.7 nW. The ultra-compact form factor and high efficiency at a low input voltage demonstrates that our proposed system is especially suitable for subdermal implant applications.

V. CONCLUSION

In this paper, an ultra-compact single-chip solar energy harvesting IC using on-chip photodiodes is introduced. The proposed system employs an on-chip charge pump to extract energy from an integrated photodiode and to generate a high output voltage while preserving a single substrate solution. Based on the photodiode measurement results, the proposed system achieves a 3.5$\times$ improvement in energy harvesting efficiency when compared to the conventional stacked photodiode for boosting the harvested voltage with no external components. The proposed PDSC achieves a 77% startup speed improvement when compared with the conventional startup circuit. The charge pump reversion and conduction loss are improved by employing an auxiliary charge pump (AQP) and a $4V_{in}$ gate drive voltage, respectively. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency. Our proposed solar energy harvesting system achieves high efficiency without extra pads and packaging cost, making it suitable for low-cost ultra-compact robust subdermal implant applications. The future work includes the development of a reconfigurable charge pump with close loop maximum power point tracking (MPPT) capability.

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