Analysis of Reference Error in High-Speed SAR ADCs With Capacitive DAC

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***Abstract*— The high-speed successive-approximation-register (SAR) analog-to-digital converters (ADCs) rely on the switched capacitive digital-to-analog converter (CDAC) to perform the fast transition, which causes voltage ripples at the output of the reference circuits. Such ripples lead to the reference error that eventually prolongs the time for DAC settling. To minimize such error with a short available time, it either demands a power-hungry reference buffer or large die area for the decoupling. In this paper, we offer a comprehensive analysis of the reference errors in SAR ADCs with a practical reference network circuit (RNC) in consideration. A circuit model is developed in order to quantify the error amplitude for the critical DAC settling condition. Based on the proposed model, the settling behavior of the DAC with reference buffer can be precisely characterized, leading to a better understanding about the design tradeoff of the RNC. Finally, the developed model is verified by both circuit level simulations and measurement results.**

***Index Terms*— Reference error, reference buffer, successive-approximation-register (SAR), analog-to-digital converter (ADC), reference ripple.**

I. Introduction

SAR architecture has been widely adopted in the ADCs with high-resolution (>10b) and hundreds of MS/s sampling rate due to its excellent energy efficiency [1]–[7]. The *capacitive DAC* (CDAC) is often employed for both sampling and residue generation purposes due to its good matching characteristic and low switching energy. In practice, the reference voltage of the DAC requires a low-dropout (LDO) regulator to provide a supplies interference isolation. However, the switch transitions in high-speed SAR ADCs generate large voltage ripples, while the LDO is not able to recover the error on time due to its slow transient response. To support such a stringent requirement, a reference network circuit (RNC), including decoupling capacitance and reference buffer, is often necessary [5], [8], [9]. The RNC not only can isolate the switching noises from the CDAC to the LDO but simultaneously provides a low impedance for the reference voltage output. In general, the insufficient DAC settling time can lead to a wrong comparison, eventually resulting in a large conversion error, while the essential time for the DAC settling can limit the overall conversion speed in high-resolution SAR ADCs. Previous works [7], [10], [11] focus on the DAC bottom-plate switches and its capacitive load but neglect the reference circuit when considering the DAC settling; however, such reference settling often becomes the dominating factor in the high speed scenario, where a large load is driven by the RNC in a short time with large transient current. While with finite output impedance in the RNC, it leads to a reference voltage ripple that can induce reference error if it fails to recover before the next comparison. To alleviate this reference error, either utilizing the reference buffers with sufficient low output impedance [5], [8] or adding a large number of decoupling capacitors [9] in the RNC is indispensable. However, both solutions introduce a significant design tradeoff on power or die area which makes the SAR ADCs become a less attractive choice in high -speed and -resolution scenario.

This particle design issue has obtained more attentions in the recently years, while various techniques [3], [4], [7], [12] are presented to relax the power and area tradeoff. However, very few studies can be found in the literature that analyzes such tradeoffs based on a close-loop mathematical model. Under the consideration of the worst DAC settling case, existing works [3], [13] have simplified the problem and modeled the settling scenario as a first-order RC circuit settling, that neglects the on-resistance of the bottom-plate switches and shorts the bottom-plate of the DAC to the reference. However, such models fail to characterize the DAC settling in high speed conditions. In high -speed and -resolution scenario, the required output impedance of the reference buffer could be as small as the on-resistance (R_{on}) of the switches which makes it becomes unneglectable [3]. To better characterize the DAC settling behavior for this scenario, a more complete model which considers the reference ripple as well as R_{on} is highly desirable.

In this paper, we present a comprehensive analysis of the reference induced error in SAR ADCs employing the CDAC. Its error characteristics are identified and error amplitude are quantified based on our developed model. Unlike the conventional approach, the presented model considers the ripple and

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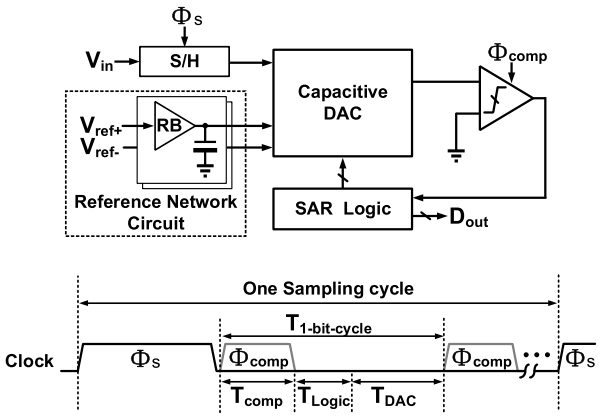

Fig. 1. Generic structure of a SAR ADC.

settling characteristic not only on the DAC but also on its reference voltage, which provides a precise prediction for the reference error even with the reference buffer scenario. Based on the developed model, we study the tradeoffs of the reference circuit in term of power and area aspects. It is worth noting that the scope of the paper is to give a general analysis on the reference error of the CDAC in SAR ADCs but not aiming for any specific correction techniques scenario. Reference errors with these techniques will be a topic of interest in future studies. While the proposed method is still compatible with SAR ADCs with those techniques but a new critical DAC settling case needs to be explored individually. Besides, even though we develop and verify the model based on a particular SAR switching scheme, the model can be easily modified to fit other high speed switching methods that usually contain 2-3 reference voltages.

The rest of the paper is organized as follows. Section II introduces the background, including two different reference error mechanisms in SAR ADCs employing the capacitive DAC. Section III describes the proposed circuit model. Section IV studies the design tradeoffs on the reference network circuit. Finally, the experimental results and comparison are presented in Section V.

II. Background

In this section, the basic architecture and operation of the SAR ADC will be briefly reviewed. In addition, two types of error caused by the reference ripple/non-settled as well as their characteristics will be discussed.

A. ADC Architecture

Fig.1 illustrates the generic structure of the SAR ADC in single-end configuration, which consists of a sampling-and-hold (S/H), CDAC, RNC, comparator and SA control logic. Its basic operation can be described as follows. The input (V_{in}) is first sampled on the CDAC through the S/H. Then the comparator makes the decisions according to the top-plate residual voltage of the CDAC and controls it to successively approximate toward the threshold through the SA logic. The RNC provides a reference voltage for the CDAC to perform a fast and accurate SA operation at high speed.

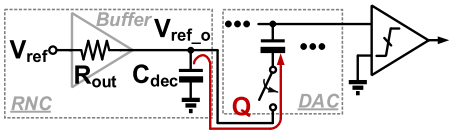

Fig. 2. The RNC provides charges for the DAC during each bit cycle.

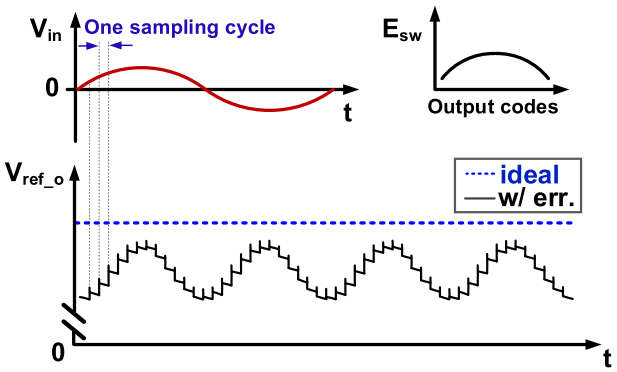

Fig. 3. Signal behavior of the output of the RNC vs. different input signal V_{in} and switching energy.

The time allocation for each bit conversion cycling can be divided into 3 parts which consist of T_{comp}, T_{Logic} and T_{DAC}, referring to time allocation for comparison, SA logic and DAC settling, respectively. For high-speed and -resolution, the SAR loop leaves only a small timing margin for each part, which may cause a metastability type of error [14] due to insufficient time for comparison and logic processing. The incomplete settling of the DAC results in a different error characteristic. Besides, the stringent DAC settling requirement leads to a power/area-hungry reference network which can dominate the total power/area of the ADC. These issues will be discussed next.

B. Reference Errors Mechanisms

Fig. 2 illustrates the RNC that drives the CDAC during each bit cycle. During the conversion, the top-plate voltage of the DAC performs the successive approximation based on the decisions of the comparator with the reference voltage provided by the RNC. When the DAC array are switched for the SA operation, the decoupling capacitor (C_{dec}) at the output of the RNC provides charges (Q) initially, but the buffer with finite output impedance (R_{out}) fails to fully recover the loss, leading to a voltage droop at the output of RNC (V_{ref_o}). If such droop cannot recover within the required accuracy before the upcoming comparison, it leads to a conversion error. Next, we will introduce two types of reference error mechanism, designated by sample-by-sample and bit-by-bit error related to the value of C_{dec} and target speed.

One of the possible reference error scenario is depicted in Fig 3. This reference error occurs when the design targets for low speed and a large C_{dec} is used at the output of the reference buffer which has insufficient low output impedance. The output of the RNC is not able to recover back to its initial value before the next incoming conversion, which is correlated with the previous conversion implying the signal-dependent

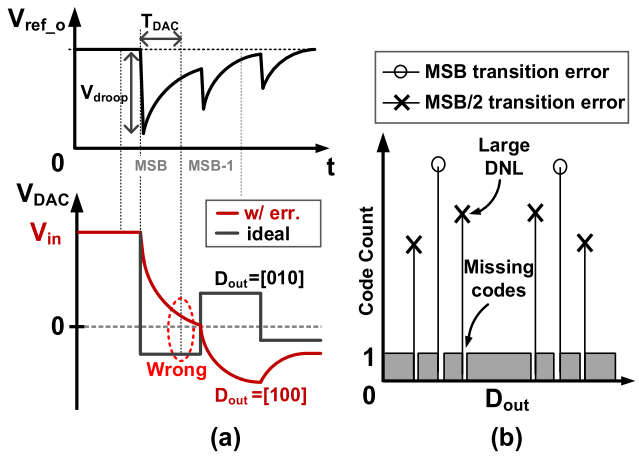

Fig. 4. (a) signal behavior of the output of the RNC and DAC with reference error (b) the corresponding output code histogram.

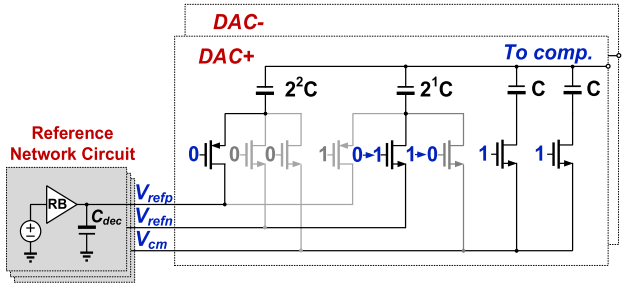

Fig. 5. Worst settling case of the differential DAC switching.

feature of RNC. As illustrated in Fig. 3, the V_{ref_o} is not an expected constant value but varies sample-by-sample, whose variation depends on the total switching energy E_{sw} drawn by the DAC in each sample and alters under different switching approaches [1], [15]. Consequently, such reference error affects the linearity of the ADC and gives rise to the 3rd harmonic at the ADC's output spectrum. It is worth noting that this error rises inversely proportional to the input frequency as the large C_{dec} would decouple the high frequency ripple but passing the low frequency one.

Except the global sample-by-sample error, there is another local bit-by-bit error scenario occurs at bit cycling. During the DAC switching, a large voltage droop (ΔV_{droop}) is generated at the output of the RNC (V_{ref_o}) due to its insufficient low impedance, eventually leading to a wrong switching operation for the next bit cycling. Fig. 4 (a) shows the signal behavior of $V_{ref,o}$ and corresponding DAC output in a 3-bit example. The ΔV_{droop} at the output of the RNC is caused by the MSB transition that cannot recover before the next comparison. As a result, V_{DAC} is now above the comparison threshold "0", leading to the decision of MSB/2 to be "1", which is contrary to the ideal scenario. The amplitude of the reference ripple is code-dependent as it is correlated with switching energy in each bit cycling [1], [3], [13]. As depicted in Fig. 4 (a) the wrong transition results in the final residue error at the DAC output that is larger than $\pm 1/2$ least significant bit (LSB). Such bit-by-bit reference error only occurs once among the n-bit cycling in the design without redundancy. Fig. 4 (b) shows the corresponding error characteristic at the output histogram. Such error can lead to a large DNL and missing codes as well as spurs at the ADC spectrum output [2], [3].

In this study, we focus on the model development for the bit-by-bit reference error which is more critical in high speed SAR ADC designs. A small C_{dec} often demands much lower output impedance from the reference buffer to avoid the bit-by-bit reference error rather than its counterpart (sample-by-sample reference error) as the available settling time of the bit-by-bit reference error is much shorter than the sample-by-sample in the SAR architecture. A large C_{dec} requires only a short time for bit-by-bit reference error to settle; therefore, the ADC must be running in a high speed. In that case, the corner frequency of the sample-by-sample error ($1/2\pi R_{out}C_{dec}$) is much lower than the Nyquist rate, thus the sample-by-sample error is not visible in the normal high frequency inputs. In the following session, we develop a circuit model that can characterize the bit-by-bit reference error based on the critical case, which reveals the design tradeoffs in term of area and power consumption of the RNC.

III. Circuit Model for DAC Settling

In order to quantify the bit-by-bit reference error in a manner that obtains insightful and designer-friendly results, a simplified model of the DAC circuitry is developed in this section. In this study, the proposed analytical model is applied in a SAR ADC with V_{cm}-based switching method [1], which is one of the advanced power-efficient DAC switching scheme for high speed. Nevertheless, it also is worth nothing that our approach is applicable to other kinds of switching methods and will eventually lead to similar conclusions in Section IV.

From previous studies [1], [2] of V_{cm}-based switching, it can be noted that it consumes the largest energy when the first two leading bits (B_1B_2) are switched to a complementary logic "10" or "01". Fig. 5 demonstrates this critical case in a 3 bit differential DAC with V_{cm}-based switching. In order to obtain a quantitative analysis of reference errors with close-loop formula, a transfer function (TF) from the reference input to the DAC output needs to be obtained. However, it is too complicated to directly derive such DAC settling TF based on the circuit shown in Fig. 5, where it involves multiple different reference sources with a complex RC networks and instantaneous complementary switching. Instead, we found that the transfer function of the RNC can be easily obtained by the Y-Δ transform; then, we manage to refer the RNC's results to the DAC's one. In order to derive the RNC TF, we firstly simplify the switching model in Fig. 5 to a single reference source network (sub-section A); Then, we explore the relationship between the DAC's output and the RNC's one (sub-section B); Thirdly, we attempt to convert the circuit model to the s-domain where we can attain the transfer function with a step-response input (sub-section C); Finally, by applying the inverse Laplace transform, a time domain expression for the DAC settling with RNC can be obtained that allows us to characterize the reference error amplitude (sub-section D).

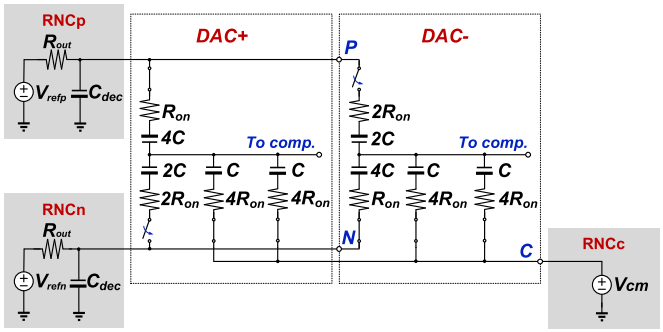

Fig. 6. Simplified RC equivalent circuit of the model in Fig. 4.

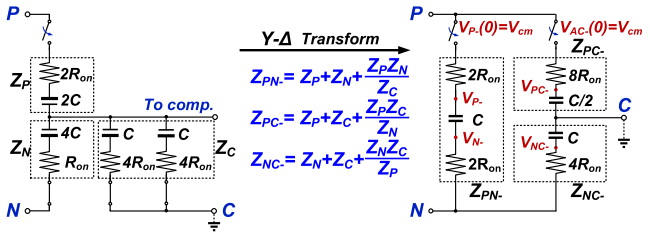

Fig. 7. Y-Δ circuit transform of the DAC.

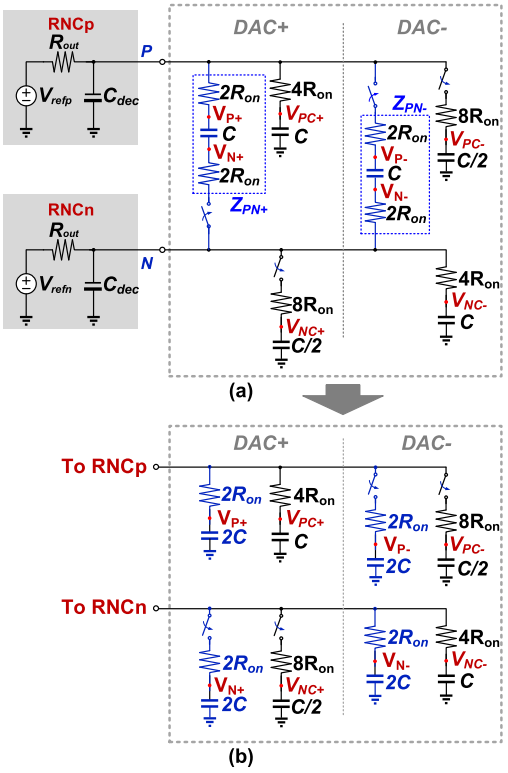

Fig. 8. Simplified RC circuit model (a) after Y-Δ transformation; (b) with Miller theorem.

A. Simplification of DAC Switching Model

In order to simplify the model, several assumptions are made. Firstly, the DAC performs a differential switching according to the nature of the V_{cm}-based switching method. The RNC of the V_{cm} voltage provides charges for the DAC_+ while it also absorbs the same amount of charges from the DAC_- simultaneously, which theoretically leads to zero energy consumption on the RNC of the V_{cm} [1] generation. Therefore, we ignore its effect in the analysis where the V_{cm} node is connected to an AC ground in the simplified model. Secondly, we assume both RNCp and RNCn (for the reference voltages V_{refp} and V_{refn}, respectively) being designed with the same output impedance and C_{dec}. Thirdly, a simplified DAC switch model [16] is adopted. It characterizes its turn-on behavior as an abrupt but delayed jump, and models the R_{on} of the MOSFET switch with its resistance in the maximum overdrive voltage condition. Besides, the size of DAC switches is scaled down according to the bit-weighted of the capacitor which keeps the time constant being the same in each bit cycling. Fig. 6 depicts the simplified model, where R_{out} and C_{dec} denote the output impedance and capacitance of the reference buffer, respectively. R_{on} represents the on-resistance of the MSB switches and C is the unit capacitance.

The model in Fig. 6 can be further simplified with the Y-Δ circuit transform as illustrated in Fig. 7. The nodes A, B and C refer to the different reference inputs of the DAC, V_{refp}, V_{refn} and V_{cm}, respectively. For DAC-, the equivalent impedance from nodes P to N (P-N), N-C and P-C can be expressed as:

$$Z_{\text{PN-}} = 4\text{R}_{ON} + \frac{1}{sC}, \quad Z_{\text{NC-}} = 4\text{R}_{ON} + \frac{1}{sC},$$
$$Z_{\text{PC-}} = 8\text{R}_{ON} + \frac{2}{sC} \tag{1}$$

where Z_{PN-}, Z_{NC-} and Z_{PC-} are the equivalent impedance of the reference network between nodes P and N, N and C, and P and C, respectively. Similarly, the corresponding equivalent impedance can be obtained in DAC_+ as:

$$Z_{\text{PN+}} = 4\text{R}_{ON} + \frac{1}{sC}, \quad Z_{\text{NC+}} = 8\text{R}_{ON} + \frac{2}{sC},$$
$$Z_{\text{PC+}} = 4\text{R}_{ON} + \frac{1}{sC}. \tag{2}$$

Fig. 8(a) depicts the final equivalent RC circuit model after the Y-Δ circuit transformation according to (1) (2). It worth nothing that Z_{PN-} and Z_{PN+} can be equivalent to two series RC circuits in separated branches (highlighted in blue in node P and N) according to the Miller theorem [17], as depicted in Fig. 8(b). Hence, the transfer function from the reference input to the RNC's output can be found with this simplified model. Next, we manage to obtain the relationship between the RNC's and DAC's output.

B. Equivalent the Output of RNC to the DAC

Fig. 9 illustrates that the settling characteristic at the output voltage (ΔV_{out+}) of the DAC_+ can be equivalent to the sum of the voltage droops from ΔV_P and ΔV_N. By applying Kirchhoff's circuit law (KCL) in Fig.9, it can be obtained that

$$\frac{\Delta V_{\text{P}} - \Delta V_{out+}}{Z_P} + \frac{\Delta V_N - \Delta V_{out+}}{Z_N} + \frac{\Delta V_C - \Delta V_{out+}}{Z_C} = 0. \tag{3}$$

Based on abovementioned models, it can be assumed that $Z_P = Z_N/2 = Z_C/2 = R_{on} + 1/4sC$, and $\Delta V_C = 0$ for

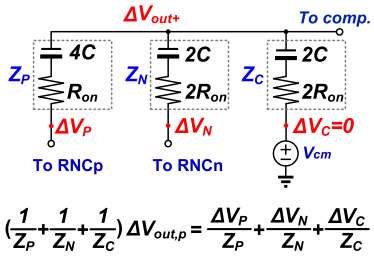

Fig. 9. RC equivalent circuit for relationship between the settling behavior of DAC+ output and the RNC output.

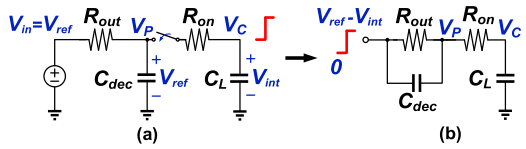

Fig. 10. (a) Circuit network for second-order RC settling model; (b) equivalent circuit model for the transfer function.

Z_C connecting to the ac ground. In addition, as node P is symmetrical with node N in Fig. 8, it is also assumed that $\Delta V_P = -\Delta V_N$. Therefore, by substituting these assumptions into (3), we can obtain that $\Delta V_{out+} = \Delta V_P/4$. Therefore, for the differential DAC, its settling characteristic can be equivalent to that of RNC's output. Such relationship allows us to simply derive the transfer function of the RNC to obtain the DAC one.

C. Transfer Function and Time Domain Response

In order to better illustrate how to obtain the transfer function based on the circuit model in Fig. 8(b), we first adopt a simple second-order RC settling network as an example. Fig. 10 (a) depicts a second-order RC circuit, which consists of a DC voltage source with finite output impedance R_{out}, decoupling capacitor C_{dec}, switch with on-resistance R_{on} and load capacitor C_L, where C_{dec} has an initial voltage V_{ref}. When the switch is close, C_L is charged by the DC voltage source and the voltage V_C is changed from 0 to V_{ref}. In order to characterize this switching activity with a transfer function under a step respond input, it is necessary to obtain its equivalent s-domain model. When converting the circuit model, the initial conditions on each node must be taken into account as they can affect the respond in their corresponding node. By using the KCL in each node of the model with the initial condition of C_{dec}, it can be obtained that

$$\frac{V_{in}(s) - V_{\rm P}(s)}{R_{out}} = C_{\rm dec}(sV_P(s) - V_P(0)) + \frac{V_P(s) - V_{\rm C}(s)}{R_{\rm on}} \tag{4}$$

$$\frac{V_{\rm P}(s) - V_C(s)}{R_{\rm on}} = sC_{\rm L}V_C(s) \tag{5}$$

where $V_P(0)$ denotes the initial condition of C_{dec} and $V_P(0) = V_{ref}$. As the input of the model is a step response, $V_{in}(s) = V_{ref}/s$, so that $V_P(0) = sV_{in}(s)$. By substitute this into (4),

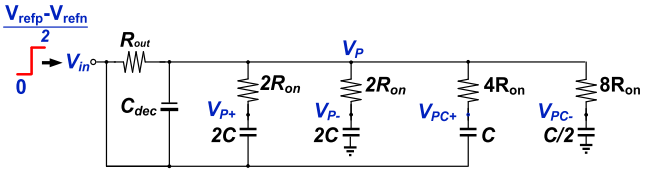

Fig. 11. Equivalent circuit model with step-function response input for the transfer function.

we obtain

$$\frac{V_{in}(s) - V_{\rm P}(s)}{\frac{1}{sC_{\rm dec}} // R_{out}} = \frac{V_P(s) - V_C(s)}{R_{on}}. \tag{6}$$

From (4) and (6), the corresponding equivalent circuit model based on a step response input ($V_{in}(s) = V_{ref}/s$) is depicted in Fig. 10(b) where its transfer function for the voltage droop at node P can be derived as:

$$\frac{V_{\rm P}(s)}{V_{in}(s)} = \frac{(sR_{out}C_{dec}+1)(sR_{on}C_L+1)}{(sR_{out}C_{dec}+1)(sR_{on}C_L+1)+sR_{out}C_L}. \tag{7}$$

The transfer function in (7) is still valid if C_L has an initial voltage V_{int} ($V_{int} =< V_{ref}$) which can be equivalently considered in a step-response input with a modified swing. In such a scenario, we can set V_{int} to be 0 and use the step function $V_{in}(s) = (V_{ref}\text{-}V_{int})/s$ as its input instead. Similarly, the equivalent circuit model with step function response input for the circuit in Fig. 8 can be found in a similar manner, where the final complete model is depicted in Fig. 11 and its transfer function is (detailed derivation steps are in the Appendix):

$$\frac{V_{\rm P}(s)}{V_{in}(s)} = \frac{1+s(4R_{on}C+3R_{out}C+R_{out}C_{dec})+4s^2R_{out}R_{on}C_{dec}C}{(sR_{out}C_{dec}+1)(4sR_{on}C+1)+\frac{11}{2}sR_{out}C}. \tag{8}$$

Equation (7) contains two poles, which are

$$\omega_{p1} = \left[\frac{1}{2}\left(R_{out}C_{dec}+4R_{on}C+\frac{11}{2}R_{out}C + \sqrt{\left(R_{out}C_{dec}+4R_{on}C+\frac{11}{2}R_{out}C\right)^2 - 16R_{out}R_{on}C_{dec}C}\right)\right]^{-1}$$

$$\omega_{p2} = \left[\frac{1}{2}\left(R_{out}C_{dec}+4R_{on}C+\frac{11}{2}R_{out}C - \sqrt{\left(R_{out}C_{dec}+4R_{on}C+\frac{11}{2}R_{out}C\right)^2 - 16R_{out}R_{on}C_{dec}C}\right)\right]^{-1}. \tag{9}$$

As $\omega_{p1} < \omega_{p2}$, ω_{p1} is the dominate pole. Since our analysis aims for moderate to high resolution designs, the required time for the DAC settling is several folds of the time constant, thus the effect of other non-dominate poles on the time response can be neglected. By applying the step response

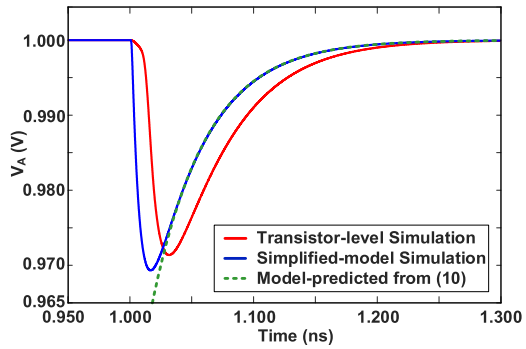

Fig. 12. The settling behavior of the V_P obtained by the transistor-level simulation, simplified RC circuit model simulation and simplified model-prediction from (10).

input $V_{in} = (V_{refp}\text{-}V_{refn})/2/s$ to (8) and taking inverse laplace transform, the time-domain response expression of the differential reference voltage V_P can be simplified as shown in (10), as shown at the bottom of this page.

In order to check the soundness of our proposed model, we compare our model-predicted result with simulations. Fig. 12 depicts the settling behavior of V_P from three results: (a) simulation of the transistor-level circuit in Fig. 4, (b) simulation of the simplified model in Fig. 11, and (c) the developed model from (10). Initially, the developed model (dotted curve) starts at an initial value different from the others that is due to the simplification on (10) by ignoring those non-dominated poles. However, all of them reach a good agreement in the fine settling region, where the comparisons are made. Due to the parasitic capacitance of MOS switches that are ignored in our model, the transistor-level simulation result shows a smaller amplitude of the voltage droop and a delay time shift; however, its trend and characteristic match well with our model. These verify the accuracy of our developed model which can estimate the DAC settling behavior in high resolution designs. Indeed, without any simplification, our modeling can fit in different resolution applications. Our choice here neglecting the non-dominant poles targets mainly high resolution >10b and high speed designs.

D. Reference Error and DAC Settling Time

Based on the time-domain expression of the DAC settling in (10), we can obtain the reference error in a given DAC settling time. With the DAC settling time set to be T_{DAC}, since the DAC output variation $\Delta V_{out+} = 1/4 V_P$, the corresponding reference error can be calculated from (10) as

$$\begin{aligned}\Delta V_{\text{out+}}(t = T_{DAC}) &= \frac{1}{4} \times \left[V_{\text{refp}} - V_P(t = T_{DAC})\right] \\ &= \frac{(V_{refp} - V_{refn})}{8} \times exp\left(-\omega_{p1} T_{DAC}\right) \\ &\times \left[\frac{\frac{5}{2} R_{out} C}{\sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}}\right].\end{aligned} \tag{11}$$

For the SAR ADC without redundancy, the residue error at the output of the DAC is required to be suppressed less than half *LSB* before the next upcoming comparison. In this scenario, T_{DAC} is required to be large enough to satisfy $\Delta V_{out+} \leq$ ½ *LSB*. According to (11), the critical DAC settling time should be, T_{DAC}, as shown at the bottom of this page, where $V_{ref} = V_{refp} - V_{refn}$, $LSB = V_{FS}/2^n$ for n-bit resolution and the input signal with full scale amplitude of V_{FS}. If $V_{ref} = V_{FS}$, according to (12) we can rewrite T_{DAC} as following:

$$T_{DAC} = \tau \times Nt \tag{13}$$

where τ is the time constant which is

$$\begin{aligned}\tau = \frac{1}{\omega_{p1}} = \frac{1}{2}\Bigg(&R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C \\ &+ \sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}\Bigg).\end{aligned} \tag{14}$$

and Nt is the number of time constant which is, Nt, as shown at the bottom of this page, From (12), it can be recognized that T_{DAC} is a function of R_{out}, C_{dec}, R_{on}, C, and *LSB* size.

$$V_P(t) \approx V_{refp} - \frac{(V_{refp} - V_{refn})}{2} \times \left[\frac{\frac{5}{2} R_{out} C}{\sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}}\right] \times exp\left(-\omega_{p1} t\right) \tag{10}$$

$$\begin{aligned}T_{DAC} = \frac{1}{2}\Bigg(&R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C + \sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}\Bigg) \\ &\times \ln\left[\frac{V_{ref}}{4LSB} \frac{\frac{5}{2} R_{out} C}{\sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}}\right],\end{aligned} \tag{12}$$

$$Nt = (n-2)\ln(2) + \ln\left[\frac{\frac{5}{2} R_{out} C}{\sqrt{\left(R_{out} C_{dec} + 4R_{on} C + \frac{11}{2} R_{out} C\right)^2 - 16 R_{out} R_{on} C_{dec} C}}\right]. \tag{15}$$

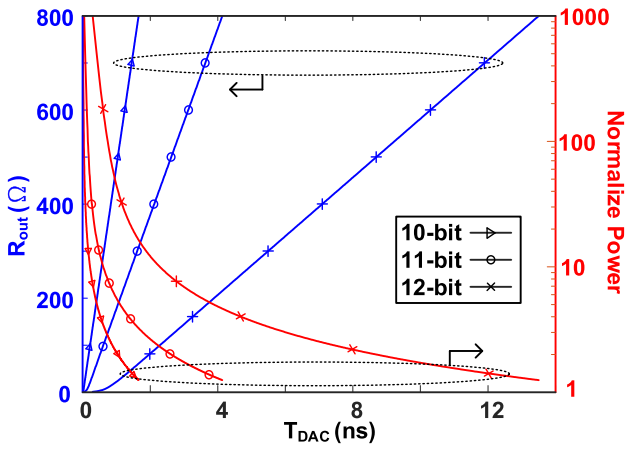

Fig. 13. R_{out} (left) and normalized power (right) against T_{DAC} with different resolution requirements.

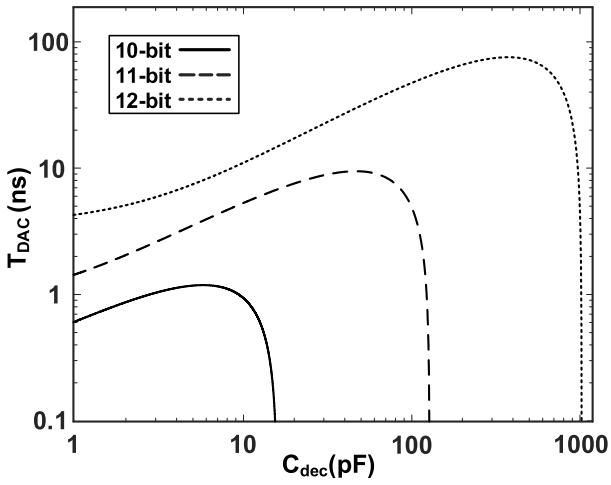

Fig. 14. T_{DAC} against C_{dec} with different resolution requirements.

While the DAC unit capacitance C is determined by the ADC requirements, such as noise and matching, we will explore the relationship among R_{out}, C_{dec} and R_{on} based on our developed model.

IV. Design Guide With the Proposed Model

The trade-off between the design of R_{out} (power) and C_{dec} (area) under finite DAC settling time T_{DAC} will be studied in this section by utilizing our developed model.

A. R_{out} Versus DAC Settling Time T_{DAC}

Firstly, it is assumed the recovery of the reference voltage mainly supported by the buffer circuit and the C_{dec}, including the self-load and the routing parasitics, is 0.5 pF for high -speed and -resolution designs. The total capacitances of the DAC are set to be 0.2, 0.8 and 3.2 pF to meet the *kT/C* noise requirement for the target ADC resolutions (10b, 11b and 12b, respectively) with a full swing of 1.6 V. [18], while R_{on} is designed with 100Ω for high speed purpose. Fig. 13 plots the required output impedance of the reference buffer (R_{out}) versus different T_{DAC} based on (13)-(15) for the half LSB DAC settling accuracy criteria. With shorter T_{DAC}, it places a more restrict requirement on R_{out} that needs to be reduced for faster settling. Based on the R_{out}, the required power from the reference buffers can be easily obtained to study its tradeoff with expected T_{DAC}. Without losing the generality, considering that the buffers are based on a simple source follower topology [4] whose power is inversely proportional to R_{out} ($R_{out} \propto 1/P_{ower}$). Fig. 13 also plots the normalized power from the buffer versus the T_{DAC} based on (13)-(15). According to Fig. 13, it can be observed that there is a steep tradeoff between power and T_{DAC} for high –speed and -resolution designs. For instance, when $T_{DAC} = 2$ ns, an extra bit settling requirement calls for >2.3 times additional power from the reference buffer; while reducing T_{DAC} to 1ns, 3.6 folds of power needs to be budgeted.

For a practical case study, when considering an 11-bit 100 MS/s SAR ADC with state-of-the-art performance, its power consumption is ∼1.6 mW in 65nm CMOS technology [3]. While targeting for such specifications in a reasonable decoupling area overhead, the R_{out} of the reference buffer should be less than 42.7Ω according to our modeling with $R_{on} = 100\Omega$ and minimum C_{dec}. That means a 2.81 mW power needs to be budgeted from the reference buffer [3], [19] and which is more than 1.75 folds of the ADC. For higher resolution and speed specifications with small area, the power of the reference buffer becomes dominant in the whole design.

B. C_{dec} v.s. DAC Settling Time

In this sub-section, we will study the relationship between C_{dec} and T_{DAC}. Several assumptions for this case study are made as below. Similar to previous section, R_{on} is set to 100Ω while R_{out} is assigned to be 200Ω for relatively low power consideration. The initial value of C_{dec} is set to be 0.5 pF as explained before due to the buffer's self-load and parasitic of the routing. Fig. 13-(a) depicts the relationship between the T_{DAC} and C_{dec} based on our developed model, where the solid, dash and dot line referring to the resolution of 10, 11 and 12 -bit cases, respectively. Not surprisingly, adding small amount of decoupling capacitance C_{dec} significantly deteriorates the settling speed, leading to a longer required T_{DAC}. However, improvements on the DAC settling can be observed when C_{dec} rises to a relatively large value (like >1nF in 12b case). With a large C_{dec}, the T_{DAC} is able to improve to ∼100 ps which is more than 6-fold better than those with $C_{dec} = 0.5$ pF in various resolutions. From (13)-(14), it can be recognized that C_{dec} can affect both τ and Nt. While τ is linearly proportional related to C_{dec}, Nt has an inversely exponential relationship with C_{dec}. The overall variation of T_{DAC} is dominated by τ with a small grown on C_{dec}, but mainly depends on Nt with much larger C_{dec}. Therefore, adding just a small C_{dec} will not reduce T_{DAC}, instead it induces extra burden with the additional load from the decoupling capacitance. Such additional load indeed prevents the reference voltage to recover from the ripple as a large amount of charge on C_{dec} is taken by the DAC, and the reference buffer with large R_{out} cannot provide sufficient

support on time. On the other hand, with enough large C_{dec}, the charge taken by the DAC becomes relatively small, in other words the reference voltage become closer to an ideal source with low impedance. The support requested by the buffer becomes less important in the transient condition where only its DC output value is a concern as it affects the initial value on C_{dec}. For 10, 11 and 12b cases, the improvements start when C_{dec} is >50, 150 and 310 -fold of the total capacitance of the DAC, respectively.

In conclusion, using a large C_{dec} can achieve high speed without dissipating much power to the reference buffer but that significantly increases the die cost. For instant, in order to reduce T_{DAC} to be 100 ps, additional capacitance of more than 31, 127 and 1022 pF are desired for 10, 11 and 12 -bit resolution, respectively. While considering a MOS decoupling capacitor with 5 μm $\times$ 5 μm in 65nm CMOS technology, the capacitance is only around 300 fF at 1V supply. For 11-bit resolution, C_{dec} costs at least 0.0i1mm^2 chip-area without considering other overheads, which is almost same size of the state-of-the-art ADC core area [3]. Moreover, for $T_{DAC} = 100$ ps, increasing 1b resolution leads to about 8-fold of additional decoupling capacitance (0.08 mm^2). Therefore, when targeting for a high -speed and -resolution ADC with low power, the required decoupling capacitance can occupy a considerable chip-area.

C. Design Guidelines

Based on the previous analysis and discussions, several considerations and guidelines are provided for the reference network circuits of high speed SAR ADC designs.

1) For the reference network with power-hungry reference buffer but a small decoupling capacitor, T_{DAC} mainly depends on the value of the time constant τ in (13). As we keep reducing R_{out} to push T_{DAC} to the speed limitation, the on-resistance of the switches R_{on} can dominate τ. On the other hand, for the low-power reference network with a large C_{dec}, the reduction of T_{DAC} is dominated by the number of time constant Nt. From (14), it can be recognized that $T_{DAC} \propto$-$ln[C_{dec}]$. This accounts for large area budget to achieve a short T_{DAC} in high- speed and resolution designs.
2) To achieve a short T_{DAC}, our developed model indicates that either a power-hungry reference buffer or a large decoupling capacitance is necessary in the RNC. For low power and small area consideration, one can reduce the power/area of RNC by allocating more time for those more critical settling cases, such as in the first few MSBs' switching [20]. In addition, time-interleaved (TI) technique can be utilized to relax power/area overhead of the RNC. By adopting the TI technique, the demanded power of reference buffers increases linearly with T_{DAC} as individual reference buffer is often used for each channel [22], [23]. On the other hand, for the single-channel scenario, the power often rises more rapidly due to other overheads, such as parasitic and limited on resistance of the DAC switches.

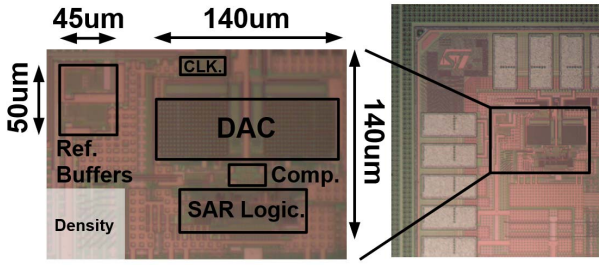

Fig. 15. Microphotograph of the SAR ADC with reference buffer.

3) Rather than allocating more time for T_{DAC}, the critical settling case can be eased by the various approaches. One can add redundancies [6], [7] during the SA conversion which can provide certain error tolerance range for the reference errors. On the other hand, its efficiency is also degraded as the redundancy bits also suffer with the reference error. Besides, the threshold reconfigurable reference error calibration [3] enables a large error calibration range. The data driven charge compensation [12] use reservoir capacitors to relax the RNC requirement. Last but not least, digital calibration methods [21], [24] can also correct the error from the RNC. Although these approaches can correct the reference errors to some extents, there still exists a critical settling condition for the DAC where our developed scheme is still applicable to analyze the design tradeoffs.

V. Experimental Comparison

To verify the correctness of the proposed model and analysis, we compare our model result with the measured one. Fig. 15 depicts the microphotograph of the ADC. The measured SAR ADC is fabricated in 65nm CMOS process with 11b resolution and running at 30 MS/s. The ADC uses Vcm-based switching method for the SA switching. On-chip reference buffers are adopted to provide the reference voltage whose topology is similar as [25]. The bottom-plate switches of the DAC are scaled proportionally according to the binary weight of the capacitor in the first few bits. During the measurement, we intentionally reduce the available DAC settling time in the first 4b to stimulate the reference error, which is accomplished through a voltage control delay time-loop designed in the SAR ADC. Fig. 16 (a) and (b) illustrate the measured output code histogram of the SAR ADC with and without reference error in the first three switchings, respectively. The locations of the 1st, 2nd, 3rd and 4th correspond to reference error in the 1st, 2nd and 3rd and 4th switching, respectively. While recalling that no switching is necessary before the MSB comparison in the V_{CM}-based switching scheme, the 1st reference error occurs in the 2nd MSB comparison. It can be observed that there are large hits and gaps near the locations of first three switchings when we allocate less available time for DAC settling in Fig. 16 (a). From the remarks of the location of the 1st switching, it also can be recognized that the largest hit and gap occurs near the 2nd switching that matches well with our analysis in Section III. Fig. 17 (a) and (b) show the differential nonlinearity (DNL)

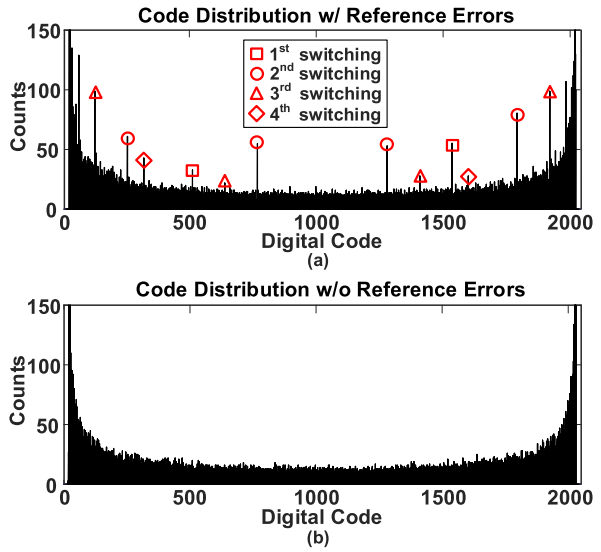

Fig. 16. Code histogram of SAR ADC (a) with reference errors and (b) without reference errors.

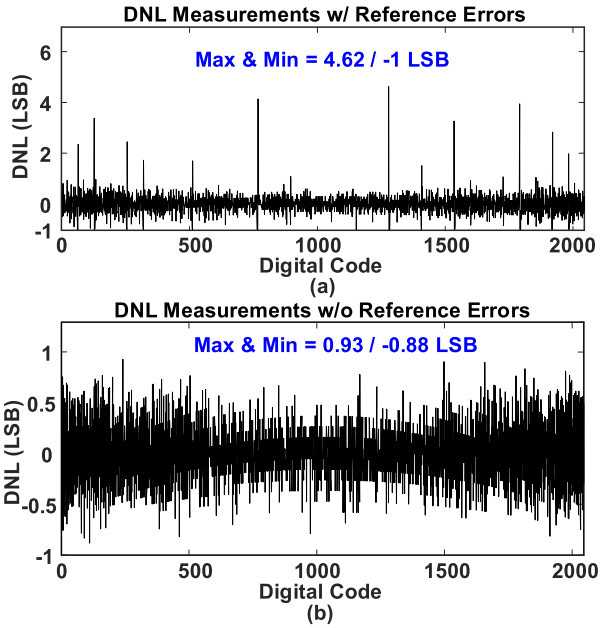

Fig. 17. Measured DNL of SAR ADC (a) with reference errors and (b) without reference errors.

of the SAR ADCs with and without the reference errors, respectively. The measured DNL are 4.62/-1 LSB for SAR ADC with reference errors, while giving more time for DAC settling, the DNL is suppressed ∼1 LSB without missing code. Such results indicate the effectiveness of the tunable delay and less available DAC settling does give rise reference error.

We also compare the modeled results with the simulation and measured ones by substituting the design parameters of this prototype in (10). In this design, the RNC consists of reference buffers with output impedance of ∼25 Ω and output capacitor of ∼3 pF. The MSB capacitance of the binary DAC is ∼384 fF and the on-resistance of MSB MOSFET switch is ∼200Ω at TT corner. Fig.18 depicts the voltage-controlled

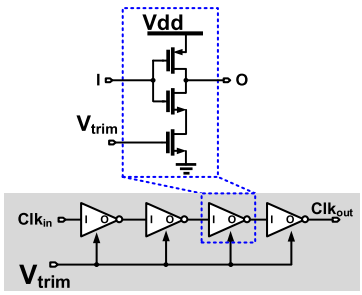

Fig. 18. Voltage-control delay circuit to trim the DAC settling time T_{DAC}.

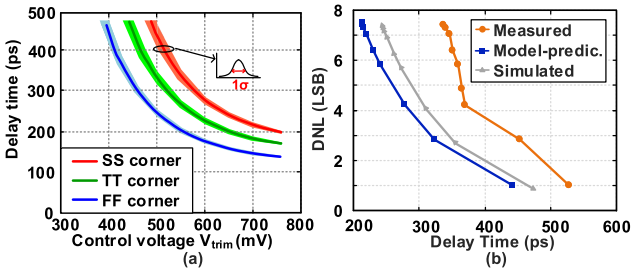

Fig. 19. (a) Delay time against control voltages of the tunable delay circuit at TT, SS and FF corners with 1 sigma mismatch variation; (b) Model-predicted, simulated and measured DNL against settling time for 2nd MSB transition.

delay circuit to control the time T_{DAC} for DAC settling. It consists of 4 inverters with pull-down path voltage-controlled delay. By trimming different control voltages V_{trim} of the delay circuit, we can obtain the measured DNL. Fig. 19 (a) shows the relationship between the control voltage and delay time of the trimming circuit from the post-layout simulation at TT, FF and SS corners. Since we cannot directly obtain the available DAC settling time through the measurement, we estimate such time from the applied trimming voltage and the results in Fig. 19 (a) typical condition. Fig. 19 (b) plots the measured DNL along with the model-prediction and simulation one from (10). The measured results illustrate the same trend with a reasonable agreement to our model as well as to the simulation. While there exists a constant shift in the time axis, it is mainly due to the 3 following reasons. 1) The delay time in the measurement is estimated from Fig. 19 (a) where we are not able to measure the exact delay on-chip, and where we can observe as well that the delay time varies under different corners with device mismatch. Such variations alter the voltage-to-time gain and induces error in the estimation. 2) We simplified the switch turn-on behavior as an abrupt but delayed jump that induces a constant delay error between the result of the model and the realistic transistor operation (Fig. 12). 3) The model and simulation results do not consider the routing parasitic in the layout. However, such consideration is too specific and will be different in various designs. Adding those parasitics into consideration will imply loss of generality of the model and a significant increase in the complexity while failing to provide any additional theoretical information. Also, they only affect the curve shifting in the time-axis but not the trend (shape of the curve) in Fig. 19 (b).

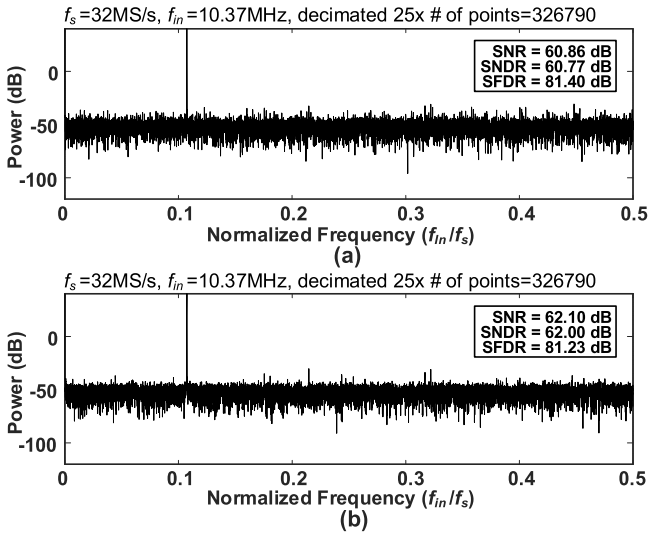

Fig. 20. Output spectrum at 10MHz input for SAR ADC (a) with reference errors and without reference errors.

Fig. 20 also compares the FFTs plots of the SAR ADC with and without reference errors. Patten spurs can be observed at the output spectrum of the SAR ADC with reference errors. Even though the SNDR only degrades less than 1 dB, the ADC suffers from the miss code issue which limits its usage on some specific applications.

VI. Conclusion

This paper presents a model to precisely characterize the reference error in SAR ADCs with consideration of reference ripples at the reference circuits. The proposed model can quantify the error amplitude across different design parameters, such as on-resistance of switches, decoupling capacitance as well as output impedance of reference buffers. It also helps to investigate the design limitations and tradeoffs of the reference circuit in SAR ADCs, providing guidelines for design optimization. We verified the model both through simulation and experimental results which revealed a reasonable agreement.

Appendix
Equivalent Circuit Model With Step Response Input

In order to obtain the equivalent circuit model with step response input, the initial conditions on each capacitor need to be converted into a step-function input. Considering the circuit branch connecting to RNC for V_{refp} in the model from Fig. 8(b), the initial voltage $V_A(0)$, $V_{A,p}(0)$, $V_{AC,p}(0)$ are equal to V_{refp}, and the step function for the RNC input is $V_{in,p} = V_{refp}/s$. Therefore, similar to the example in Fig. 10, we have $V_A(0) = V_{A,p}(0) = V_{AC,p}(0) = sV_{in,p}$. In additional, since the initial voltage at the switching output node $V_{A,n}(0) = V_{AC,n}(0) = (V_{refp}+V_{refn})/2 \neq 0$, in order to avoid complex calculation, we need to modify this model to be the one similar to the case in Fig. 11. We first assume that the initial voltage of all the capacitors in this system are shift down by $(V_{refp}+V_{refn})/2$ so that the initial voltage at the switching output node $V_{A,n}(0)$ and $V_{AC,n}(0)$ are equal to 0, then use the similar approach to obtain the time-domain expression $V_A(t)$. By setting $V_{A,n}(0) = V_{AC,n}(0) = 0$, the step-function input is modified to be $V_{in,p} = (V_{refp} - V_{refn})/2/s$, and the initial conditions for the other capacitors are changed to be $V_A(0) = V_{A,p}(0) = V_{AC,p}(0) = (V_{refp}-V_{refn})/2$. Therefore, by using the KCL in each node with the above conditions, we can be obtained:

$$\begin{aligned}
\frac{V_{in,p}(s) - V_A(s)}{R_{out}} &= sC_{\text{dec}}\left[V_A(s) - V_{in,p}(s)\right] \\
&\quad + \frac{V_A(s) - V_{A,p}(s)}{2R_{on}} \\
&\quad + \frac{V_A(s) - V_{A,n}(s)}{2R_{on}} \\
&\quad + \frac{V_A(s) - V_{AC,p}(s)}{4R_{on}} \\
&\quad + \frac{V_A(s) - V_{AC,n}(s)}{8R_{on}} \\
\frac{V_A(s) - V_{A,p}(s)}{2R_{on}} &= 2sC\left[V_{A,p}(s) - V_{in,p}(s)\right] \\
\frac{V_A(s) - V_{A,n}(s)}{2R_{on}} &= 2sCV_{A,n}(s) \\
\frac{V_A(s) - V_{AC,p}(s)}{4R_{on}} &= s\text{C}\left[V_{AC,p}(s) - V_{in,p}(s)\right] \\
\frac{V_A(s) - V_{AC,n}(s)}{8R_{on}} &= \frac{1}{2}sCV_{AC,n}(s). \qquad (16)
\end{aligned}$$

From (15), the corresponding equivalent circuit model based on the step function $V_{in} = (V_{refp}\text{-}V_{refn})/2/s$ as input is depicted in Fig. 9, and its transfer function is

$$\frac{V_A(s)}{V_{in}(s)} = \frac{1+s\left(4R_{on}C+3R_{out}C+R_{out}C_{dec}\right)+4s^2R_{out}R_{on}C_{dec}C}{\left(sR_{out}C_{dec}+1\right)\left(4sR_{on}C+1\right)+\frac{11}{2}sR_{out}C}. \qquad (17)$$

By taking inverse Laplace transform to (16) with the step input $V_{in}(s) = (V_{refp} - V_{refn})/2/s$, the time-domain response expression of V_A' can be derived as

$$\begin{aligned}
V_A'(t) &= \frac{\left(V_{refp} - V_{refn}\right)}{2} \\
&\quad \times \left\{1 - \left[exp\left(-\omega_{p1}t\right) - exp\left(-\omega_{p2}t\right)\right]\right. \\
&\quad \left. \times \left[\frac{\frac{5}{2}R_{out}C}{\sqrt{\left(R_{out}C_{dec}+4R_{on}C+\frac{11}{2}R_{out}C\right)^2 - 16R_{out}R_{on}C_{dec}C}}\right]\right\}, \qquad (18)
\end{aligned}$$

where $\omega_{\text{p1}}, \omega_{\text{p2}}$ are the two poles in (9).

The above derivations simply compute variation (difference) of the voltage $V_A(t)$ responses to the step input of $V_{in,p} = (V_{refp} - V_{refn})/2/s$, since we remove all the DC components in the initial condition. To match the model and simulation results with a correct DC value, a common-mode voltage of $(V_{refp} + V_{refn})/2$ can be added to (17), thus eventually obtained the final expression as (10).

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