A 10-MHz Bandwidth Two-Path Third-Order ΣΔ Modulator With Cross-Coupling Branches

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***Abstract*—This brief presents a two-path discrete-time third-order sigma-delta (ΣΔ) modulator with an extra zero in the noise transfer function (NTF) located at $z = -1$, reducing the NTF coefficients of intermediate terms for optimal design. Applying polyphase decomposition of the NTF, the proposed ΣΔ modulator is implemented by a two-path architecture with cross-coupling branches. The 65-nm CMOS experimental chip running at a sampling rate of 340 MHz achieves a DR of 68.8 dB and a SNDR of 65.4 dB for a 10-MHz signal bandwidth, occupying an active area of 0.2257 mm^2 and consuming 19.47 mW from a 1.2-V supply.**

***Index Terms*—ΣΔ modulator, two-path, cross-coupling, noise transfer function, polyphase decomposition.**

I. Introduction

THE INCREASE in the speed of modern wireless communication systems, including software-defined radio (SDR), demands more and more wideband and high-resolution analog-to-digital converters (ADCs) as well as low power dissipation to allow longer battery life in portable devices [1]–[5]. Meanwhile, nanometer CMOS technologies (≤65 nm) with scaled-down supply voltage impose new challenges for circuit design because of augmented sensitivity to noise and mismatch.

It is well known that sigma-delta (ΣΔ) modulators achieve a high degree of insensitivity to analog circuit imperfections due to oversampling and noise-shaping. This important advantage makes ΣΔ modulators more suitable for the increased scaling in CMOS processes.

A conventional third-order DT ΣΔ modulator uses three operational amplifiers (op-amps). Two-path or multi-path (N-path) architectures reduce the channel speed [6], [7], but the high values of the coefficients of intermediate terms penalise the feedback factor of the op-amps to 1/8 [6]. The implementation can be sampled-data or continuous-time (CT). However, for very high speed, very low clock jitter requirement of CT implementation possibly hampers the achievable SNR.

This brief optimises the modulator architecture with a topological transformation of the basic scheme, by adding an extra zero in the NTF to reduce the coefficients of the intermediate terms, resulting in an improved feedback factor of the op-amps. The method ensures that, by applying the NTF polyphase decomposition technique, the proposed ΣΔ modulator can be efficiently implemented by a two-path architecture with cross-coupling branches. Multi-path solution is attractive for increasing the sampling frequency without requiring to speed up the analog blocks. As a result, an operating speed that can exceed the maximum allowed by the single-path counterpart with the same CMOS technology used is obtained.

II. Proposed ΣΔ Modulator Architecture

The NTF of a third-order ΣΔ modulator is

$$NTF = (1 - z^{-1})^3 = 1 - 3z^{-1} + 3z^{-2} - z^{-3} \tag{1}$$

By supposing to add an extra zero at $z = -1$, it becomes

$$NTF' = (1 - z^{-1})^3(1 + z^{-1}) = 1 - 2z^{-1} + 2z^{-3} - z^{-4} \tag{2}$$

The z^2 polyphase decomposition of NTF′ [8], leads to

$$N_0(z^2) = 1 - z^{-4}; \quad N_1(z^2) = -2(1 - z^{-2}) \tag{3}$$

Fig. 1 shows the corresponding block diagram. It uses a two-path cross-coupling architecture. Each path cascades two basic blocks [8], with the following transfer functions

$$H_1(z) = \frac{z^{-2}}{1 - z^{-2}}; \quad H_2(z) = \frac{1}{1 + z^{-2}} \tag{4}$$

The signal and noise transfer functions of each path are

$$STF = z^{-2}; \quad NTF = 1 - z^{-4} \tag{5}$$

Note that the two cascaded basic blocks exactly realise the required $N_0(z^2)$. Besides, the transfer function from the auxiliary input of the second block to the output, $H_{aux} = 1 - z^{-2}$, has a convenient expression for achieving $N_1(z^2)$, only missing a multiple of $-2z^{-1}$. The observation leads to the cross-coupling branch, $-2z^{-1}$ multiplying the quantization error from the other path, to obtain the intermediate terms of the NTF in (2).

Since each path operates at $f_s/2$ (being f_s the sampling frequency), interleaving the input signal makes the even and

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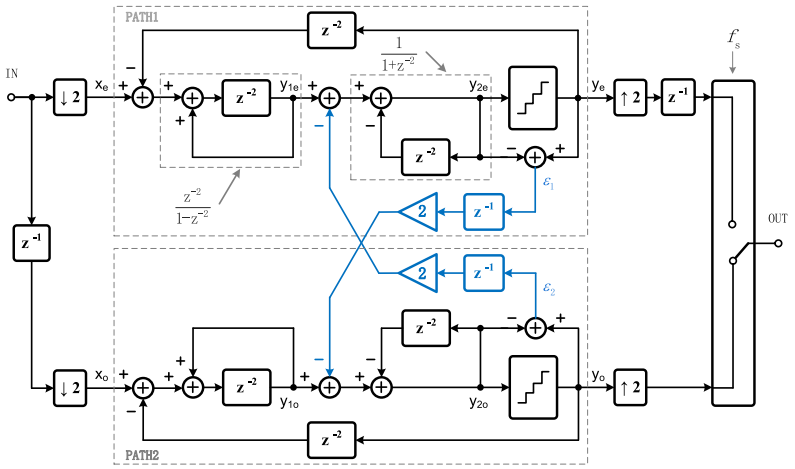

Fig. 1. Block diagram of the proposed third-order ΣΔ modulator using a two-path architecture with cross-coupling branches ($z = e^{s/f_s}$, $z^2 = e^{2s/f_s}$).

odd inputs, x_e and x_o, respectively. By inspection of the circuit, for the first path, it holds

$$[(x_e - z^{-2}y_e)\frac{z^{-2}}{1-z^{-2}} - 2z^{-1}\epsilon_2]\frac{1}{1+z^{-2}} + \epsilon_1 = y_e \quad (6)$$

yielding, after rearrangement,

$$y_e = x_e z^{-2} + (1-z^{-4})\epsilon_1 - 2z^{-1}(1-z^{-2})\epsilon_2 \quad (7)$$

Similar equation results can be achieved for the second path

$$y_o = x_o z^{-2} + (1-z^{-4})\epsilon_2 - 2z^{-1}(1-z^{-2})\epsilon_1 \quad (8)$$

Combining the even and odd outputs yields the expected result

$$y = xz^{-2} + \epsilon(1 - 2z^{-1} + 2z^{-3} - z^{-4}) \quad (9)$$

where $\epsilon = \sqrt{(\epsilon_1^2 + \epsilon_2^2)/2}$ is the quadratic superposition of the quantization noises and their interpolation by a factor of 2.

The extra zero at $z = -1$ worsens the signal-to-noise ratio (SNR) by 6 dB as its low-frequency gain is 2 (when $z = 1$, $1 + z^{-1} = 2$). The 1-bit loss in resolution is certainly a disadvantage, but the above simplification of the NTF is such to permit a straightforward implementation of a two-path architecture with the 2x speed increase, making the overall sampling speed of this brief faster. Moreover, the extra zero reduces the intermediate terms′ coefficients of the NTF from 3 to 2 compared to the traditional 3rd-order ΣΔ case. The resulting improved feedback factor, β, requires op-amps with a lower f_T.

III. Architectural Optimisation

A conventional switched-capacitor (SC) integrator with delay is used to implement the first basic block $z^{-2}/(1-z^{-2})$ in Fig. 1. For the second integrator, modulating both the input and output of the conventional integrator by ±1 at half of the path operating frequency leads to $1/(1+z^{-2})$ [7]. This second block is hereinafter referred to as chopper integrator.

The lack of a delay in the chopper integrator is problematic, as conceptually illustrated in Fig. 2. Indeed, sampling occurs during the injection phase (ϕ_2) of the preceding conventional integrator with delay and this can give rise to an error or to the demand for a much higher op-amp speed.

Adding a clock period of delay to the chopper integrator largely relaxes the op-amp specifications. This is made

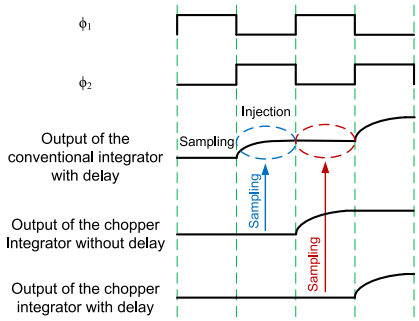

Fig. 2. The problem of the chopper integrator without delay.

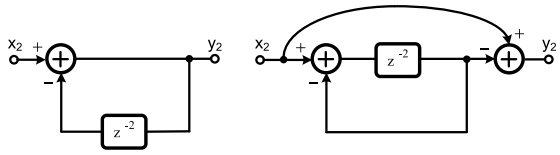

Fig. 3. The transformation from $1/(1+z^{-2})$ to $1-[z^{-2}/(1+z^{-2})]$.

possible by the transformation

$$\frac{1}{1+z^{-2}} = 1 - \frac{z^{-2}}{1+z^{-2}} \quad (10)$$

leading to the diagram of Fig. 3. The cost is an extra summation node in front of the quantizer, whose implementation can be, however, passive, thus without requiring extra power.

The optimal structure, illustrated in Fig. 4, separates the analog and digital parts of the cross-coupling branches. The scheme incorporates the use of scaling techniques to optimise the dynamic ranges of the op-amps and their linear settling times. As commonly done, an attenuation coefficient of 0.5, compensated for by halving the reference voltages of the quantizer, is employed at the input of the first integrator. In this way, the output swings of the two op-amps are reduced by a factor of 2. Concerning the scheme of Fig. 1, thanks to the adopted scaling, the feedback factor of the conventional integrator is increased from 1/3 to 1/2. In addition, notice that the feedback coefficient of the digital cross-coupling goes from 2 to 1: this enables sharing a single capacitor (used in different phases) between the digital cross-coupling branch and the

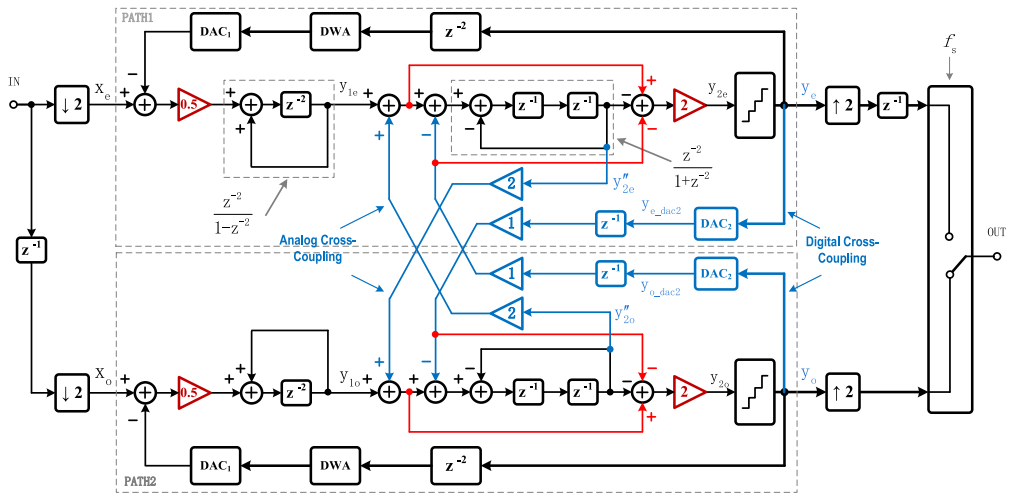

Fig. 4. Improved block diagram of the proposed third-order two-path ΣΔ modulator with cross-coupling branches.

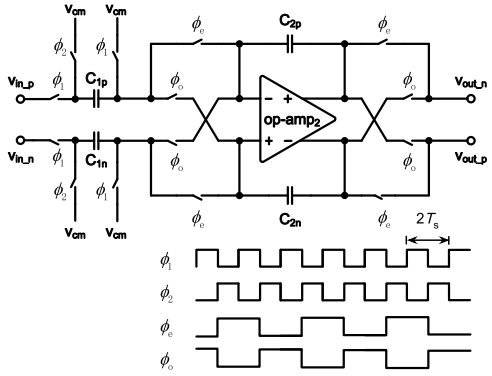

Fig. 5. The conventional circuit implementation of the chopper integrator with delay together with phases timing.

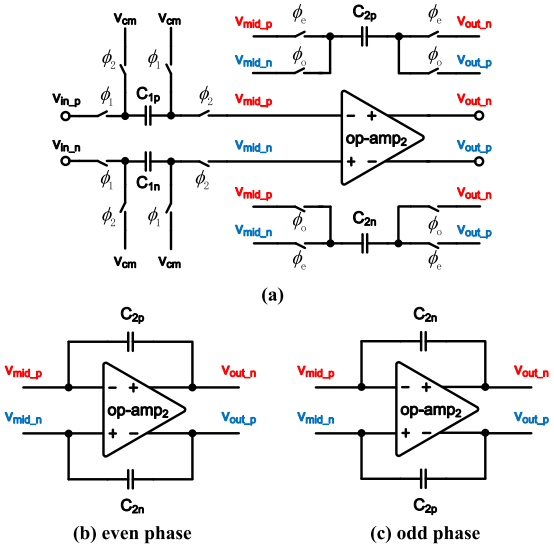

Fig. 6. The improved circuit implementation of the chopper integrator with delay: (a) the scheme, (b) and (c) the simplified circuit in the even and in the odd phase, respectively.

output of the first integrator. As a result, the feedback factor for the used scheme of Fig. 6 is 1/3. The linear settling time of the chopper integrator in Fig. 4 is, hence, reduced by 33.3% (supposing to keep unchanged the op-amp GBW).

IV. Circuit Design

A. Chopper Integrator

The conventional implementation of the chopper integrator $z^{-2}/(1+z^{-2})$ uses two square wave modulators, one in front and the other at the output terminals of an integrator [7], as shown in Fig. 5. Since the scheme chops both the inputs and the outputs of the fully differential op-amp, in case a two-stage op-amp is used to accommodate the required output swing, exactly as in this design, the Miller compensation capacitors, C_c, are also chopped. As a result, the op-amp output voltages vary over a wide range while the actual output v_{out_n} changes in a relatively small range. A large output swing would require high-performance op-amps for fully charging and discharging the C_c used.

The limit is resolved by incorporating the two choppers in the feedback capacitors. Fig. 6 shows the adopted solution. The timing is the same as the one reported in Fig. 5. The connections in the even phase, ϕ_e, and in the odd phase, ϕ_o, are shown in Fig. 6(b) and Fig. 6(c), respectively. When chopping from ϕ_e to ϕ_o, only the feedback capacitor is chopped.

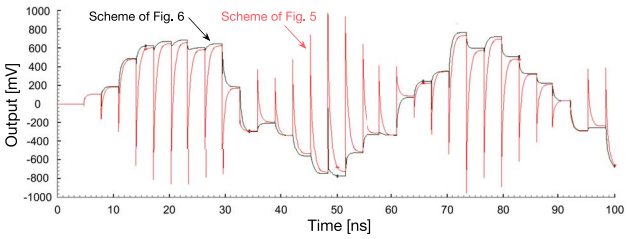

Fig. 7. Simulated output voltages of the chopper integrator, implemented with the schemes of Fig. 5 and Fig. 6.

Simulation results at the transistor level with the used technology show that the proposed chopping method ensures an optimal settling, as shown in Fig. 7.

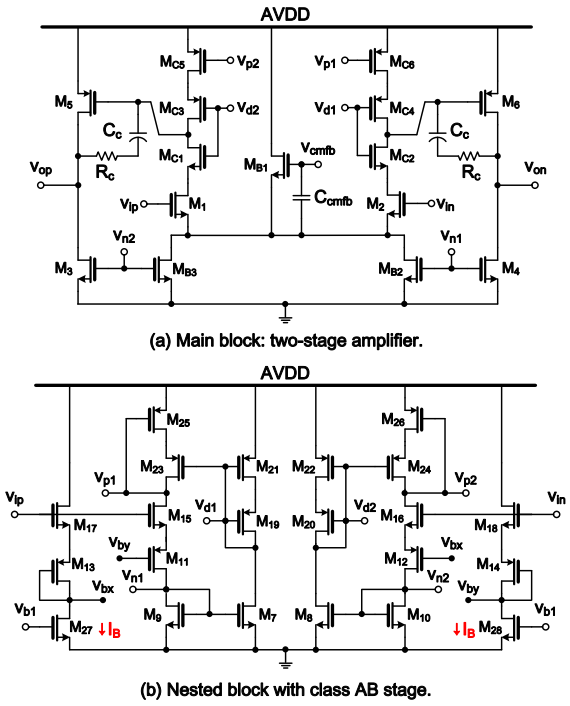

Fig. 8. Schematic diagram of the op-amp used in the conventional integrator: (a) two-stage amplifier and (b) nested block with class AB stage.

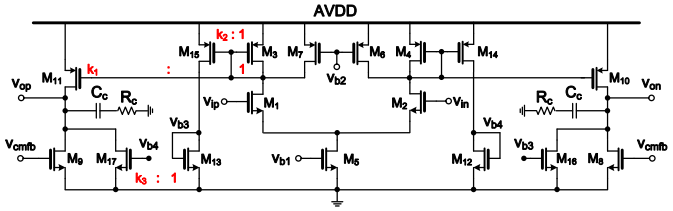

Fig. 9. Schematic diagram of the current-mirror op-amp in the chopper integrator.

B. Operational Amplifiers

Each path of the architecture uses two op-amps. One is for the conventional integrator, the other is for the chopper integrator.

Simulation results show that the minimum required gain for the first op-amp is about 60 dB. This design uses a two-stage configuration: the first stage is a telescopic scheme while a common-source configuration with active load makes the second stage, as shown in Fig. 8(a). A general issue for high-speed sampled-data circuits is the slew-rate. It is addressed here by the use of an extra nested block with class AB stage, as depicted in Fig. 8(b) [9]. It generates four output voltages (V_{p1}, V_{p2}, V_{n1}, and V_{n2}) that boost the currents in the main block when slewing occurs.

Simulations show that the gain of the op-amp used for the chopper integrator can be as low as 40 dB, but its bandwidth must be large. The current-mirror scheme depicted in Fig. 9, where current mirrors M_3-M_{11} and M_4-M_{10}; M_4-M_{14} & M_{12}-M_{17} and M_3-M_{15} & M_{13}-M_{16} fold the signal currents to the output stage, fulfils the request. The simulated GBW of this design is 3.25 GHz, adequate for the application.

C. Summation Circuit and 4-Bit Quantizer

The diagram of Fig. 4 outlines the need in each path of a linear combination of analog signals before the 4-bit quantizer.

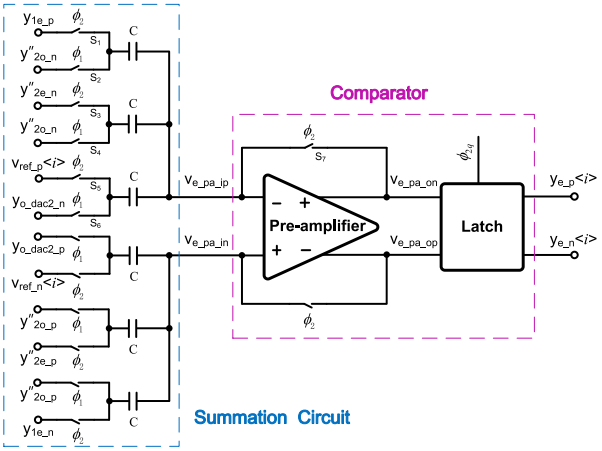

Fig. 10. Schematic diagram of a comparator of the 4-bit quantizer used in the even path together with the passive summation circuit (C = 5 fF).

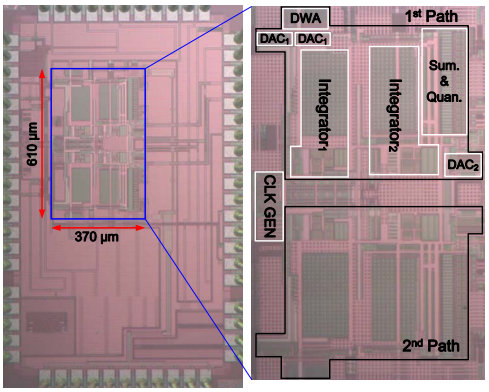

Fig. 11. Chip micrograph.

For the even and the odd path, they are

$$y_{1e} + 2y''_{2o} - y''_{2e} - y_{o\_dac2}; \quad y_{1o} + 2y''_{2e} - y''_{2o} - y_{e\_dac2} \tag{11}$$

where signals y_{e_dac2} and y_{o_dac2} are the outputs of two resistive-based digital-to-analog converters (DAC_2 in Fig. 4).

Fig. 10 shows the schematic diagram (differential version) of one of the 16 comparators used in the 4-bit quantizer of the even path together with its passive summation circuit. It makes full use of the differential features and only employs three equal capacitors to carry out the summation of the five unity terms in (11) with the threshold. The capacitive network attenuates the signal by a factor of 3, but the sign does not change. A conventional preamplifier, whose gain is about 20 dB, drives a latch followed by a SR flip-flop [10].

V. Measurement Results

The proposed modulator has been designed and fabricated in a standard 65-nm 1P7M CMOS process. Fig. 11 shows the chip microphotograph. The two paths are symmetrical. The figure outlines the two integrators with the capacitor array, in which multiple unit metal-to-metal (MOM) capacitors with n-well shielding are used. Data weighted averaging (DWA) circuits [11], located on the top and bottom of the chip, occupy a minimal area and reduce the nonlinearity errors in the signal band caused by the mismatch in the feedback DACs (DAC_1 in Fig. 4). The clock generator, placed in left-middle,

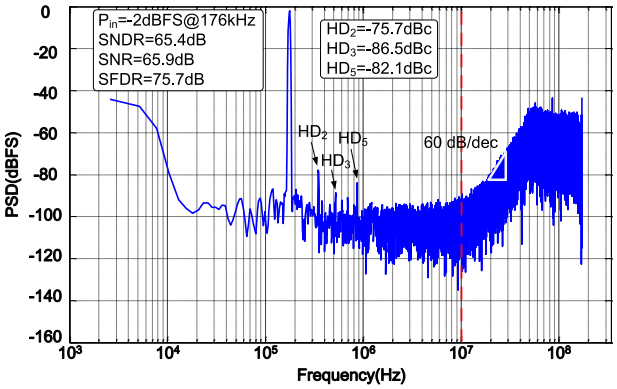

Fig. 12. Measured output spectrum.

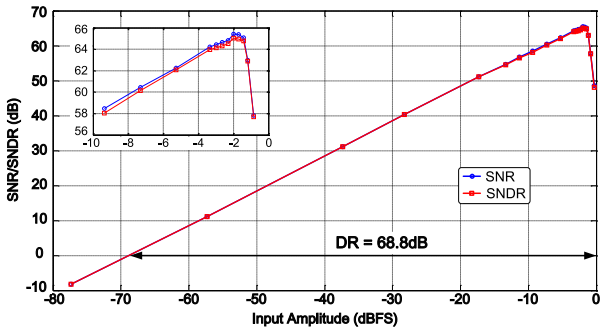

Fig. 13. Measured SNR and SNDR as a function of the input signal amplitude for a 176-kHz input.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work	[1]	[2]	[3]	[4]	[5]
Achitecture	**DT**	DT	DT	DT	CT	CT
Process(nm)	**65**	130	65	65	28	65
Supply(V)	**1.2**	1.2	1.25	1.2	1.2/1.5	1.0
$\mathbf{F_S}$ (MHz)	**340**	240	240	240	640	1000
BW(MHz)	**10**	10	15	15	18	10
DR (dB)	**68.8**	67.0	-	-	78.1	77
SNDR(dB)	**65.4**	63.0	67.0	67.0	73.6	72.2
Power(mW)	**19.74**	20.5	37.0	46.0	3.9	1.57
Area(mm^2)	**0.2257**	0.4	0.28	0.28	0.08	0.027
$\mathbf{FoM_W}^*$ (fJ/conv.-step)	**648.6**	888.0	674.1	838.1	27.7	23.6
$\mathbf{FoM_S}^{**}$(dB)	**152.4**	149.9	153.1	152.1	174.7	170.2

$^*\text{FoM}_\text{W} = \dfrac{\text{Power}}{2\cdot\text{BW}\cdot 2^{[(\text{SNDR}-1.76)/6.02]}}$ $^{**}\text{FoM}_\text{S} = \text{SNDR}+10\cdot\lg\left(\dfrac{\text{BW}}{\text{Power}}\right)$

serves both paths of the architecture. The active area is 0.2257 mm^2.

Each path operates with a clock frequency of 170 MHz, so that the overall sampling frequency of the modulator is 340 MHz. Fig. 12 shows the measured output spectrum with -2 dB_{FS} input signal at a frequency of 176 kHz. The FFT has been obtained with 131072 points. The measured SNDR and SNR are 65.4 dB and 65.9 dB, respectively. The spurious-free dynamic range (SFDR) of 75.7dB is dominated by HD_2 caused by the residue nonlinearity in the DACs and the op-amps. The signal bandwidth is 10 MHz and the OSR is 17. The 60-dB/decade spectral slope validates the desired third-order noise-shaping function. In addition, the output spectrum of Fig. 12 at high frequency sharply falls down, so a side benefit of adding the extra zero at $z = -1$ is that the design of the digital filter cascaded to the modulator can be relaxed with respect to the conventional implementations.

Fig. 13 shows the measured SNR and SNDR as a function of the input signal amplitude for a 176-kHz input. The measured dynamic range (DR) is 68.8 dB.

The measured overall power consumption is 19.74 mW (the analog and digital consumptions are 12.38 mW and 7.36 mW, respectively) with a 1.2-V supply voltage. Table I summarises the measured performances of this design and compares them with published $\Sigma\Delta$ modulators with similar bandwidth. With a lower FoM_W and a smaller active area, the sampling frequency is about 40% higher than that of the conventional discrete-time implementations with the same CMOS technology.

VI. CONCLUSION

A third-order two-path $\Sigma\Delta$ modulator with cross-coupling branches doubles the OSR for a given sampling frequency. The result is an increase of 3.5 bit in the resolution and a reduction of the power consumption. The techniques proposed in this brief allow using only two op-amps in each path at the cost of 1-bit of resolution. The experimental verification validates the proposed techniques with good overall performance.

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