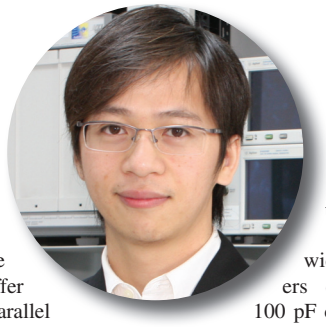
interview

Pui-In Mak

"Creating multi-stage amplifiers with a wide range of output-current drivability and capacitive-load drivability is still very challenging"



Pui-In Mak from the University of Macau talks about the research behind his Letter 'Ultra-area-efficient three-stage amplifier using current buffer Miller compensation and parallel compensation' on Page 624.

What are your main research interests?

I work on radiofrequency, analogue and mixed-signal VLSI circuits and systems for wireless and biomedical applications in mainstream CMOS technologies. Examples of circuits that I am involved in are: active-decoupling techniques, balun amplifiers, low-noise amplifiers, mixers, channel-selection filters, oscillators, data converters and power amplifiers. Systems examples are: adaptive/multimode/multiband transceivers, software-defined radio, cognitive radio, ultrasound circuits, a bio-potential (ECG/EEG/EMG) readout front-end and digital microfluidics. We have a cross-disciplinary research team at the University of Macau in the State Key Laboratory of Analog and Mixed-Signal VLSI to address the development of next-generation microsystems for emerging applications.

What are the advantages of the three-stage amplifier presented in your *Electronics Letters* paper?

We strategically merged Miller and parallel compensations, while shifting up the pole-zero cancellation to a higher frequency value so that the amplifier area efficiency can be significantly improved without penalising the speed and power of the amplifier. We fabricated a CMOS prototype that verified the concepts experimentally.

What did you do differently in designing your amplifier?

Miller and parallel compensations are the two most common techniques for the design of two-stage amplifiers. The former uses a small compensation capacitor and brings a no pole-zero doublet to the passband, but at the expense of the speed. The latter, on the other hand, relies on pole-zero cancellation to maximise the speed. The key pitfalls are the pole-zero doublet and the large compensation capacitance impacting the die area. In our design of three-stage amplifiers, merging the Miller and parallel compensations appears to be more advantageous because their merits can be combined while leveraging their drawbacks. Moreover, by shifting the pole-zero cancellation up to a high frequency, the area efficiency can be significantly improved.

In which applications will this amplifier be most useful?

Low-power, compact and wideband three-stage amplifiers capable of driving over 100 pF capacitive load have found productive applications in capacitorless low-dropout regulators that are widely utilised in modern mixed-signal microsystems, such as wireless transceivers in cellular and WiFi devices. A low-dropout regulator can significantly improve the power-supply rejection ratio of sensitivity circuits, such as an oscillator, to the supply variation. Our amplifier can also be designed with a big output current drivability to fit audio applications, such as in headphone drivers.

What other projects are you working on?

In the amplifier research area, one of our related projects is also on three-stage amplifiers, which are specifically designed to drive a wide range of heavy capacitive load in nF range, without penalising stability. Such an amplifier can be applied in the driving unit of large-scale LCD displays. A second project is to apply a current-recycling technique to maximise the speed-power efficiency of single-stage amplifier under a low-voltage supply. It can be considered as a general improvement of the amplifier such that it can be used in different applications. A third project is to use an elevated supply voltage to leverage the speed-gain trade-off of the amplifier in ultra-deep-submicron CMOS technologies. The key consideration is the reliability of all devices, which must be guaranteed under transient and steady states.

What do you see as the biggest future challenges in your field?

In the amplifier research area, creating multi-stage amplifiers with a wide range of output-current drivability and capacitive-load drivability is still very challenging, especially under a low-voltage supply in advanced CMOS technologies. Reconsidering the ways to generate the transconductance and to create a large output impedance are both essential. Selecting an optimum supply voltage can also create more design headroom. The final goal is a set of amplifier design techniques more in tune with the advantageous features (e.g. speed and area) of ultra-scaled CMOS technologies. With such techniques, the technologies will be able to cope more easily with the many different emerging applications in the years to come.

doi: 10.1049/el.2012.1609