Low-Power CMOS Laser Doppler Imaging Using Non-CDS Pixel Readout and 13.6-bit SAR ADC

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***Abstract*—Laser Doppler imaging (LDI) measures particle flows such as blood perfusion by sensing their Doppler shift. This paper is the first of its kind in analyzing the effect of circuit noise on LDI precision which is distinctively different from conventional imaging. Based on this result, it presents a non-correlated-double-sampling (non-CDS) pixel readout scheme along with a high-resolution successive-approximation-register (SAR) analog-to-digital-converter (ADC) with 13.6b effective resolution (ER). Measurement results from the prototype chip in 0.18 μm technology confirm the theoretical analysis and show that the two techniques improve LDI sensing precision by 6.9 dB and 4.4 dB (compared to a 10b ADC) respectively without analog pre-amplification. The sensor's ADC occupies $518\ \mu\mathrm{m} \times 84\ \mu\mathrm{m}$ and is suitable for fast column parallel readout. Its differential non-linearity (DNL), integral non-linearity (INL), and input referred noise are +3.0/-2.8 LSB, +24/-17 LSB, and 110 $\mu\mathrm{V}_{rms}$ respectively, leading to a Figure-of-Merit (FoM) of 23 fJ/state which makes it one of the most energy efficient image sensor ADCs and an order of magnitude better than the best reported LDI system using commercial high-speed image sensors.**

***Index Terms*—CMOS image sensor, correlated double sampling (CDS), flowmetry, laser Doppler imaging (LDI), perfusion, successive-approximation-register analog-to-digital-converter (SAR ADC), time-domain comparator.**

I. Introduction

THE laser Doppler (LD) effect describes the difference in frequency—the Doppler Shift—between the incident light and its scattered parts from moving particles. The particle's velocity can be estimated by measuring the heterodyne in its back-scattered light. This technique, known as laser Doppler flowmetry (LDF), is used in a large number of industrial and biomedical instruments purposed to study liquid and gas dynamics [1], [2].

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LDF in biomedicine can provide accurate, non-invasive, non-contact, and instantaneous measurements of bodily fluid flow including blood perfusion and microcapillaries circulation [3], [4]. When combined with modeling and calibration, LDF can be extended to other monitoring applications such as blood pressure sensing [5]. The basic LDF apparatus consists of a laser source illuminating the blood vessel and a photo-detector to collect the back-scattered photons. This random back-scatter will create a time-varying interference pattern with a bandwidth on the order of 20 kHz. The first moment of this spectrum is an estimator of the flow-rate. Most research efforts on LDF to date including body tissue models, circuit, and device integration [6], [7] have focused on the single photo-detector configuration.

Laser Doppler imaging (LDI) is the 2D extension of LDF parallelized over an array of photo-detectors. It poses formidable new challenges due to its exponential increase in bandwidth [8]. Owing to the lack of suitable hardware platforms other than general-purpose high-speed image sensors [9], [10], most of the research on LDI has been confined to the system and algorithm level [1], [2], [11]. Standard video-rate charge-coupled-device (CCD) or complementary-metal-oxide-semiconductor (CMOS) image sensors can be used in laser speckle contrast analysis (LASCA) where the optical beating is sensed as speckles in the spatial domain instead of the temporal domain [12], its precision and image quality is inferior to LDI unless it is complemented by sophisticated modeling and costly imaging equipment [13].

Much of the current discussion in the literatures on LDI is focused on its system-level implementation. This paper aims to provide a circuit-level analysis on how LDI imposes a distinctively different set of noise requirements compared to general purpose imaging. Quantitative conclusions will be drawn on how ADC resolution and correlated-double-sampling (CDS) impact LDI instrumentation precision. A number of circuit and sensing techniques are described in this paper to enable faster and more precise LDI on a low-cost CMOS device at very low power consumption. A compact body-biased PMOS reset pixel structure is put forward to improve LDI precision by reducing reset-noise without CDS. A compact time-domain noise-averaging comparator is presented to satisfy the ADC resolution requirements of LDI while enjoying the energy efficiency of the SAR architecture. It also eliminates the need for a separate analog pre-amplifier which would otherwise add noise to the readout chain.

The relationship between LDI precision and circuit noise is discussed in Section II. The prototype LDI sensor and its operation is described in Section III. Measurement results are presented in Section IV before final conclusions are made in Section V.

II. LDI Considerations

A. Principle of Operation

The velocity induced laser Doppler shift of particle flow is calculated from the power spectral density (PSD) of the back-scattered light intensity signal

$$S(v) = |\mathbb{F}\left(V_{sig}(i)\right)|^2 + N_{tot}(v) \tag{1}$$

where $\mathbb{F}$ is the discrete Fourier transform (DFT) of the sampled light intensity signal $V_{sig}(i)$ over the time instances $T, 2T, \ldots, iT, \ldots, NT$, and $N_{tot}(v)$ is the noise PSD. The moments of $S(v)$, M_n, are

$$M_n = \sum_{v>0}^{F_s/2} v^n S(v). \tag{2}$$

It is well known [1], [8], [12] that the particle concentration, c, and their perfusion, p, can be calculated from the zeroth, M_0, and first, M_1, moments respectively. The particle concentration, c, is proportional to the zeroth moment

$$c \propto M_0/S(0) \tag{3}$$

and the perfusion, p, is proportional to the first moment

$$p \propto M_1/S(0). \tag{4}$$

For most biomedical applications, a sampling rate of 40 kSa/s per pixel and $N = 256$ (256 FFT bins) has been shown to provide sufficient spectral resolution [8].

B. Noise Behavior

This section provides an analysis on the effect that the noise PSD, $N_{tot}(v)$, has on perfusion, p. Only circuit noise is considered here since LDI is always performed under controlled laser illumination. Changes in M_1 only reflects a change in the spectral bandwidth of $S(v)$ and does not shift its base illumination level, so the pixel noise can be characterized from one set of illumination condition consistent with the LDI experiments. Additionally, it allows the noise analysis to be performed in the absence of a noise-free ideal LDI response which would otherwise be difficult to derive in closed form. The standard deviation of p, σ_p, is a function of

$$\overline{v^2_{rms,tot}} = \int_0^\infty N_{tot}(v)\mathrm{d}v = (1-\alpha)\overline{v^2_{N,w}} + \alpha\overline{v^2_{N,1/f}} \tag{5}$$

where $\overline{v^2_{rms,tot}}$ is the total noise at the input of the LDI function, $\overline{v^2_{N,1/f}}$ is the $1/f$ noise power weighted by α, and $\overline{v^2_{N,w}}$ is the white noise power (flat spectrum up to the Nyquist rate). If $\alpha = 0$, $\overline{v^2_{rms,tot}}$ is entirely white. It is difficult to directly simulate σ_p because $S(0)$ itself is also a random variable. Fortunately, for large N (N is typically >128 for LDI, see Table III), $S(0)$ can be considered to have very little variation (subject to only $1/N$th of $\overline{v^2_{rms,tot}}$'s noise power), and the behavior of σ_p can be estimated from the standard deviation of M_1, σ_{M1}. Fig. 1 shows the simulated gain in σ_{M1} as a function of increasing total noise power, $\overline{v^2_{rms,tot}}$, at different ratios of α [17]. The range of $\overline{v^2_{rms,tot}}$ is chosen based on Table I. There are two important features in Fig. 1. Firstly, the value of σ_{M1} increases at 40 dB/decade because σ^2_{M1} is the 4th moment of the RMS noise voltage. Secondly, white noise has a much bigger impact on σ_{M1} than $1/f$ noise. To achieve the same σ_{M1}, $\overline{v^2_{rms,tot}}$ must be approximately 3.39 times bigger for $\alpha = 1$ than for $\alpha = 0$. From this, the LDI process' white equivalent (WEQ) noise power, $\overline{v^2_{weq}}$, can be estimated as

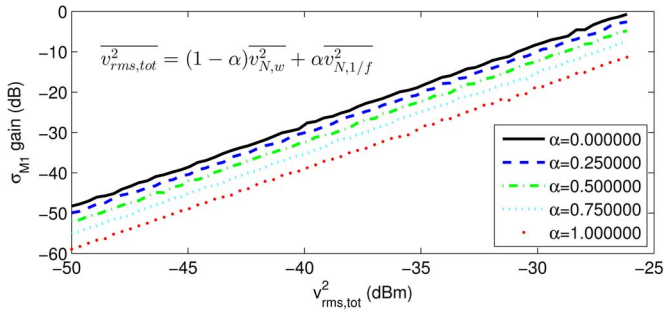


Fig. 1. The standard deviation of the first moment, σ_{M1}, as a function of input noise power. The variable α represents the ratio of $1/f$ noise to the total noise power, $P_{N,tot}$. If $\alpha = 0$, the noise PSD is white.

TABLE I
RMS Voltage Noise, $\sqrt{\overline{v^2_{rms,tot}}}$, and α Measured From On-Chip Test-Structures Under 256 Lux Illumination and 22 μs Exposure

	$\sqrt{\overline{v^2_{rms,tot}}}$ (uV)	α	$\sqrt{\overline{v^2_{weq}}}$ (uV)
Pixel pitch = 5.3 μm	1030	0.62	775
Pixel pitch = 10.6 μm	538	0.66	393

$$\overline{v^2_{weq}} = \overline{v^2_{N,w}} + \left(\overline{v^2_{N,1/f}}\right)/w \tag{6}$$

where the WEQ factor, w, is estimated to be 3.39 in this simulation. In other words, σ_{M1} is significantly more sensitive to white noise sources such as thermal noise and ADC quantization noise. Table I shows the measured $\overline{v^2_{rms,tot}}$ and the estimated $\overline{v^2_{weq}}$ and α values from on-chip test-pixels. The 5.3 μm pixel is identical to the one described in Section III-A and the 10.6 μm pixel is simply a scaled version of the 5.3 μm pixel. The values of α are estimated by taking two noise measurements for each test pixel: one with CDS ($\overline{v^2_{N,CDS}}$) and one without CDS ($\overline{v^2_{N,nCDS}}$), and applying

$$\overline{v^2_{N,w}} = \overline{v^2_{N,CDS}}/2 \tag{7}$$

$$\overline{v^2_{N,1/f}} = \overline{v^2_{N,nCDS}} - \overline{v^2_{N,w}} \tag{8}$$

$$\alpha = \overline{v^2_{N,1/f}}/\overline{v^2_{rms,tot}}. \tag{9}$$

C. ADC Resolution

Table II estimates the degradation in LDI precision after quantization noise (modeled as white) is added to the pixel's own noise power (from Table I). For simplicity, LDI input signal is assumed to be evenly distributed and the quantization noise power, $\overline{v^2_{N,Q}}$, is modeled as white noise with the equivalent noise power of $\overline{v^2_{N,Q}} = \delta_v^2/12$ where δ_v is the quantization interval. The pixel noise power is the $\overline{v^2_{weq}}$ value of the 5.3

TABLE II
DEGRADATION OF LDI PRECISION AT DIFFERENT ADC RESOLUTIONS FOR THE 5.3 μm PIXEL. THE WHITE EQUIVALENT RMS NOISE, $\sqrt{\overline{v'^2_{weq}}}$, IS THE SUM OF BOTH THE PIXEL'S NOISE POWER AND ALSO THE ADC'S QUANTIZATION NOISE POWER

ADC resolution (b)	$\sqrt{\overline{v'^2_{weq}}}$ (uV)	gain on σ_{M1} (dB)
14	775	0.00
13	777	0.04
12	785	0.22
11	815	0.87
10	926	3.09
9	1277	8.66
8	2173	17.90

μm pixel (pitch chosen to match the ADC layout pitch) from Table I. The gain on σ_{M1} is calculated for increasingly large δ_v under lowering ADC resolutions. These data show that an ADC resolution of $> 12b$ should be used in order to avoid any appreciable precision loss. If ADC resolution is reduced from 14b to 10b, the LDI precision is estimated to suffer a loss of more than 3.1 dB in this case. ADCs of even higher resolutions should be used for larger pixels with lower noise power.

D. Effect of CDS

CDS is routinely used in image sensors with 4T pixels [18]–[20], but it is also used in certain high-speed image sensors that employ 3T-styled pixels [21]. The impact of CDS on the first moment of LDI, M_1, will be briefly summarized in this section. The detailed analysis can be found in Appendix A. The digital CDS process is depicted in Fig. 2. The input signal from the photo-diode (PD) is sampled at the Nyquist rate, F_s, and stored on the sample-and-hold (SAH) capacitor. Zeroth order interpolation is then performed on the stored $X(\omega)$ to double its sampling rate to $2F_s$. This signal is modulated by a repeating sequence of $0.5, -0.5, 0.5, -0.5, \ldots$, or $0.5cos(\pi n)$. The pixel reset-noise (sum of image lag noise and thermal noise), $\overline{v_n^2}$, is modelled in Fig. 2 on a separate path. It is also sampled at the Nyquist rate, F_s, and stored on the SAH capacitor, but since it is correlated between reset and pixel readout it is simply zeroth order interpolated without going through the modulator. Both the $1/f$ noise component, $\overline{v_{N,1/f}^2}$, and the white noise component, $\overline{v_{N,w}^2}$, are superimposed in the noise PSD, $N(\omega)$, and ADC quantization noise is lumped into $\overline{v_{N,w}^2}$. The signal part of the quantized output of this modulator, $Y(\omega)$, is the sequence of CDS signal pairs representing the reset voltage followed by the integration voltage. In this model, $2F_s$ is the ADC sampling rate. In other words, the correlated samples are only separated by the ADC quantization time, which is the most general case [18]–[21]. The subtraction in CDS is modeled by a single tap finite impulse response (FIR) filter with one delay element followed by decimation by 2. The sampled reset-noise PSD (including image lag noise), $V_{rst}(\omega)$, is completely cancelled by the CDS filter. Without CDS, it will essentially appear as an additional white noise component in $N'(\omega)$ superimposed on the digital pixel value $Z(\omega)$. Section III-A will describe an alternative method where a PMOS reset transistor is used to remove this reset-noise without the aid of CDS. Since the pixel circuit in LDI sensors must operate with a much larger bandwidth than compared to conventional video-rate image sensors, its noise power contribution to $N(\omega)$, especially the $\overline{v_{N,w}^2}$ part, can be comparable or larger than $\overline{v_n^2}$.

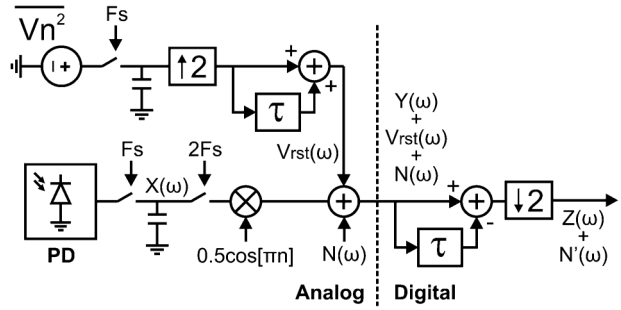


Fig. 2. The pixel CDS process.

Conventional wisdom suggests that the $1/f$ noise component in $N(\omega)$ should be largely eliminated by the CDS subtraction, but this is not quite true when considering the spectral weighting of the first moment, M_1. Numerical evaluation of the closed-form solution in Appendix A shows that when compared to the non-CDS case, CDS has a noise power gain of approximately 0.91 for $1/f$ noise (compared to 2 for white noise). This is because M_1 places higher weight on the high-frequency part of the spectrum. After repeating the noise simulation in Fig. 1 with the CDS filter, the WEQ factor, w, is evaluated to be 2.72 which is close to $2/0.91 = 2.2$ from the analytical results. The total equivalent noise power gain of CDS in determining M_1 should be between 0.91 and 2. Consequently, the worst-case total SNR degradation of the first moment, M_1, is 2. Since M_1 is calculated directly from the PSD, its variance, σ_{M1}^2, is the 4th moment of the RMS voltage noise. The deterioration of precision in M_1 in terms of σ_{M1}^2 should be $< 2^2$, or 6 dB. Since CDS does not significantly mitigate the effect of $1/f$ noise on σ_{M1} but it doubles the white noise contribution which σ_{M1} is sensitive to, it should be avoided in LDI.

E. Comparison of Current Systems

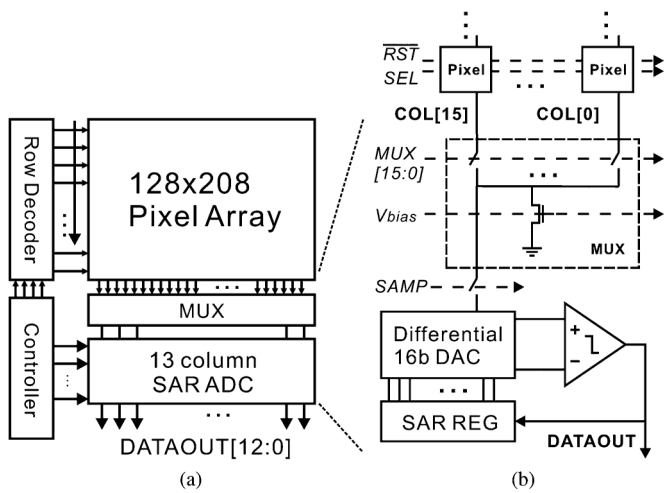
Table III summarizes the current state-of-the-art LDI systems found in the literatures. It can be seen that most of them are based on off-the-shelf high-speed image sensors which typically resort to using ADCs with limited resolution. Another important observation is that they typically use pixels larger than the 5.3 μm pixel pitch in this study (a compromise between prototyping cost and imaging resolution). This is a necessary measure when limited laser source power is spread over a large imaging area. Interpreting this together with the noise trends in Table I and Table II suggests that the ADC resolutions in these LDI sensors are not high enough to avoid losses in sensing precision. The effects of quantization noise due to low ADC resolution can be mitigated by introducing high SNR analog amplification prior to the ADC stage. However, this approach basically shifts the design challenge from the ADC to the analog pre-amplifier, which still needs to pay the necessary costs in circuit area and power consumption to meet the same noise requirements. Another important consideration here is the ADC's sampling speed. It sets a fundamental limit on a LDI sensor's frame-rate, and also to

TABLE III
COMPARISON OF LDI SYSTEMS

Year	2013	2011	2005	2009	2006	2014
Ref	[14]	[8]	[10]	[15]	[16]	This work
Custom chip	Yes	No	No	No	-	Yes
Technology (μm)	0.35	-	-	-	-	0.18
Resolution (pixel)	64 × 64	480 × 480	256 × 256	128 × 128	256 × 64	128 × 208
FFT points	1024	128	256	1024	256	256
Sampling frequency (kSa/s)	40	12.4-14.9	14	27	45	44.6
Frame-rate (fps)	1	14.6-59.2	0.18	0.2	0.25	**1.4**
ADC area (μm^2)	586 × 586	-	-	-	-	**518 × 84**
ADC resolution (b)	10	9	8	10	12	**13.6**
ADC rate (MHz)	1.28	-	40	-	-	0.714
Pixel throughput (MSa/s)	4.2	430.6	3.1	3.4	0.3	**8.9**
Pixel pitch (μm)	55	14	7	17	-	**5.3**
Sensor area (mm^2)	12.4	45.2	3.2	4.7	-	**0.7**
Imaging area (mm^2)	25 × 25	80 × 80	55 × 55	70 × 70	200 × 150	11 × 18
Laser wavelength (nm)	780	808	671	671	780	638
Sensor power (mW)	-	-	39	-	-	**4.75**
LDI precision (dB)	20.3	6-14	-	-	>26	**21.2**

some extent its sensing accuracy (related to the number of FFT points). It is challenging to design an ADC with both high-speed and high-resolution at the same time. It is even harder to do so within a reasonable power budget. Therefore the paramount need for ADC parallelization favors small ADCs with limited chip area.

In summary, good LDI performance in terms of sensing precision, speed, and accuracy requires the sensor to use the largest possible pixel size (assuming same or better fill-factor) and avoid CDS, and its ADCs must be high-resolution $(> 12b)$, small (for parallelization), and fast. Compared to other entries in Table III, this work is the first attempt to systematically optimize the circuit-level design trade-offs for custom LDI sensors. It has the smallest pixel pitch, the smallest ADC, the highest ADC resolution, and the second highest pixel throughput rate. Yet its power consumption is more than an order of magnitude smaller than the best reported system based on a commercial high-speed image sensor.



(a) (b)

Fig. 3. The (a) block diagram of the LDI sensor chip and (b) its column circuit from pixel to source follower to SAR ADC.

III. IMAGE SENSOR

Recent advances in CMOS fabrication have made it possible to build low power, small, and inexpensive single-chip cameras offering comparable imaging performance to CCD [22]–[26]. In state-of-the-art CMOS image sensors (CIS), column parallel successive-approximation-register (SAR) analog-to-digital-converters (ADC) have become popular for reasons of speed and power consumption [19], [27]–[32], but SAR ADCs face immense challenges for resolutions beyond the 7b to 10b [33]–[40] due to device mismatch, comparator noise, and circuit area. This section describes a number of circuit techniques useful in overcoming these challenges.

The CMOS LDI sensor depicted in Fig. 3(a) is composed of a 128 × 128 pixel array and 13 column parallel high-resolution SAR ADCs. Each ADC is shared between 16 neighboring pixel columns via transfer-gate multiplexers. The source-follower circuit from the pixel column selected by $MUX[15:0]$ is completed by the single-NMOS current source. Each current source is biased with 10 μA to balance between power consumption and speed. The output of this source follower is sampled by the 16b SAR ADC which generates 19 bits of data (including redundancy) for each sample. The ADC's resolution is chosen to be as high as possible in order to study the impact of quantization noise on LDI precision. The sensor can operate in both standard imaging mode where each pixel is exposed once and LDI mode where each pixel is exposed 256 times at a rate of 40 kSa/s. CDS can be enable or disabled for both modes. In CDS mode, the pixel is sampled once immediately after pixel reset and once at the end of exposure. If CDS is disabled, the pixel is only sampled at the end of exposure.

A. Body-Biased Pixel

The complete column circuit starting from the pixel is shown in Fig. 3(b). Each pixel has a large NWELL-Psub photo-diode (PD) for high sensitivity and Signal-to-Noise Ratio (SNR) photo-detection. The PMOS reset transistor, $MP1$, is placed

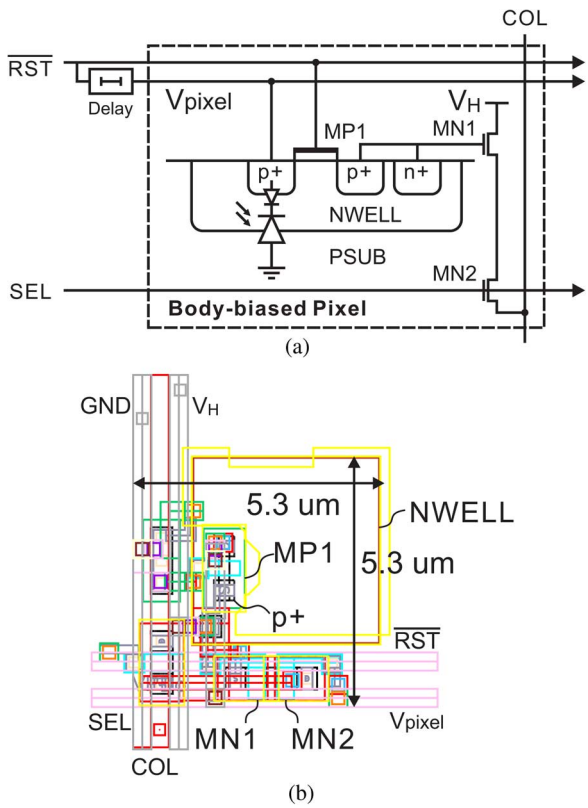


Fig. 4. The (a) schematic and (b) layout of the body-biased PMOS reset pixel.

inside this PD [Fig. 4(a)] to avoid the need for a separate NWELL. It is evident in Fig. 4(b) that this choice leads to a very compact pixel layout. The advantage of using a PMOS reset transistor is twofold: firstly, it eliminates image lag between samples and ensures all PDs are operating at the same bias point with similar charge-to-voltage gains; secondly, it can increase the nodal capacitance during reset and reduce the thermal reset-noise, $\overline{v_{nt}^2}$, of each pixel. The total pixel reset-noise ($\overline{v_n^2}$ in Fig. 2) is the sum of image lag noise and $\overline{v_{nt}^2}$.

The thermal noise sources ($\overline{v_{ns}^2}$ and $\overline{v_{nr}^2}$) contributing to the total thermal reset-noise of each individual pixel, $\overline{v_{nt}^2}$, from a N pixel array are illustrated in Fig. 5. The ratio of the source impedance, R_s, to the reset transistor's drain-to-source impedance, R_{ds}, play a critical role in determining the value of $\overline{v_{nt}^2}$. It can be shown that

$$\overline{v_{nt}^2} = \frac{kT}{C_{ph}} \left(\frac{R_s + R_{ds}}{NR_s + R_{ds}} \right). \tag{10}$$

If $R_{ds} \ll NR_s$, the source impedance, R_s, effectively sees N capacitors ($C_{tot} = NC_{ph}$) connected in parallel and the kT/C_{tot} term is reduced by a factor of N when compared to the case of kT/C_{ph} of a single PD. If $R_{ds} \gg NR_s$ then each pixel sees an independent noise source dominated by R_{ds}. In conventional pixels with NMOS reset, where $MP1$ is replaced with a NMOS transistor, the NMOS reset transistor spends most of the reset phase in cut-off region, and the reset-noise can be shown by temporal analysis to be approximately $kT/2C_{ph}$ [41].

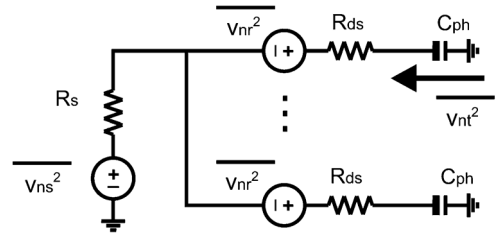


Fig. 5. Model of pixel reset-noise.

The PMOS reset will have an advantage when $R_{ds} < NR_s$. A 0.22 μm wide and 0.3 μm long 3.3 V PMOS transistor in Global Foundries 0.18 μm process has a R_{ds} of 14.6 kΩ. If $R_s = 100\ \Omega$, then $\overline{v_{nt}^2} < kT/2C_{ph}$ when $N > 146$. This is not difficult to achieve in modern mega-pixel CIS. Additional low-frequency noise sources are not considered here because M_1 in (2) inherently discriminates against them [see (6) in Section II-B].

The main drawback of the described topology lies in the parasitic diode between the source and body of the PMOS reset transistor. This parasitic diode becomes forward biased when the PD voltage is discharged beyond its on-voltage. The solution to this problem is shown in Fig. 4(a). A time delay is inserted to ensure that the reset voltage V_{pixel} is pulled to ground after $MP1$ is turned off by $\overline{RST}$. This is implemented by an inverter delay chain in the row decoder outside of the pixel array.

B. SAR ADC

The schematic of the 16b SAR ADC is shown in Fig. 6. Its sub-radix-2 digital-to-analog converter (DAC) with 19 weights is split into 3 sections. The MSB array is sized so $kT/C \approx 1LSB_{rms}$. The unit capacitor is a 5 $um \times 5$ um 28 fF MIM capacitor. Fig. 7 illustrates the operation of this ADC on a simplified 4b DAC. During the sampling phase [Fig. 7(a)], the bottom-plates of all capacitors in the negative DAC, DAC_n, except for the MSB capacitor is connected to GND while their top-plates sample the input signal, V_{sig}. Meanwhile, the top-plates of all capacitors in the positive DAC, DAC_p, except for the MSB capacitor is connected to V_{ref} while their bottom-plates sample the input signal, V_{sig}.

When the DAC is settled after the sampling phase in Fig. 7(b), the DAC output, V_{DAC}, as the difference between the DAC_n output, $V_x[0]$, and the DAC_p output, $V_x[1]$, becomes

$$\begin{aligned} V_{DAC} &= V_x[0] - V_x[1] \\ &= (KV_{ref} + V_{sig}) - (KV_{ref} - V_{sig}) \\ &= 2V_{sig} \end{aligned} \tag{11}$$

where the DAC offset factor, K, is

$$K = \frac{\sum_{i \neq 2, j \neq 8} C_{ij}}{\sum_{i,j} C_{ij}}. \tag{12}$$

The DAC settling voltage as a function of V_{sig} is plotted in Fig. 8. The differential DAC output to the SAR comparator,

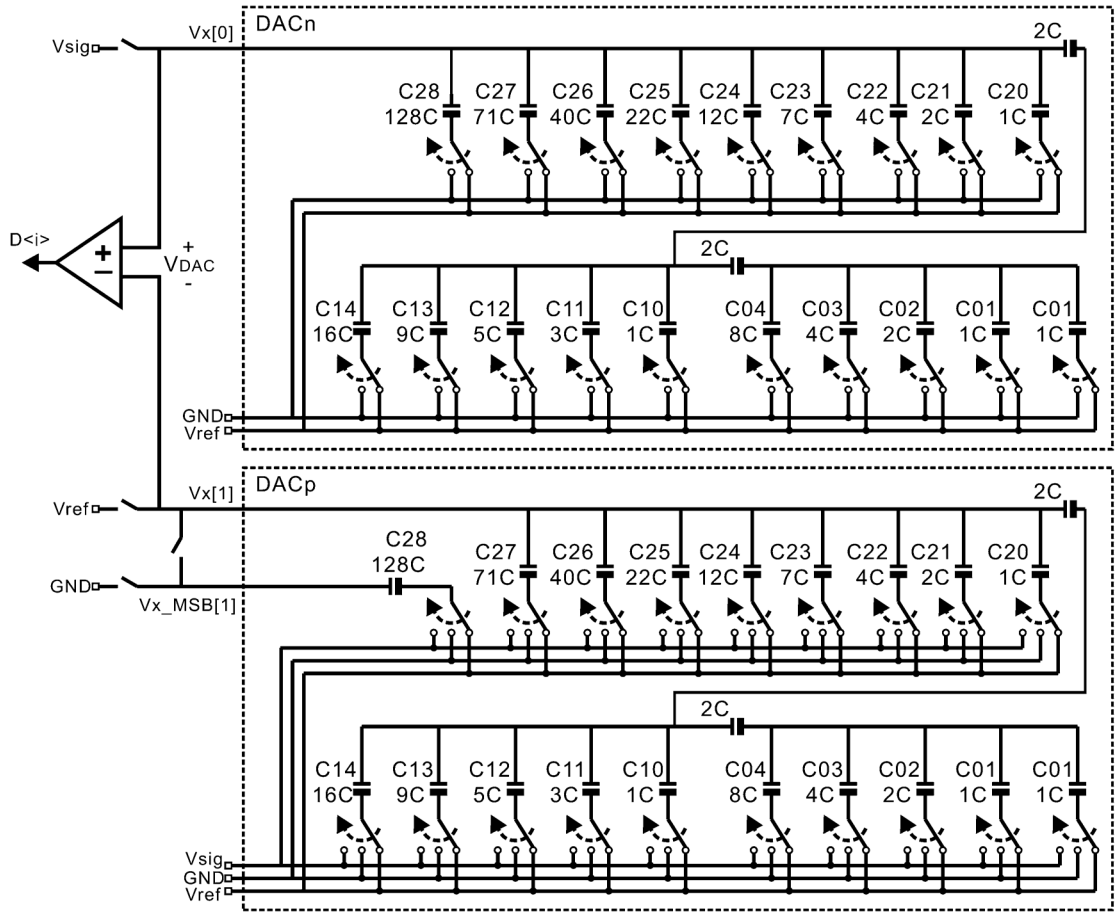


Fig. 6. Schematic of the sub-radix-2 16b SAR ADC.

V_{DAC} is $2V_{sig}$. There are two main benefits to this sampling scheme. Firstly, the DC bias of the comparator input is determined by K. This simplifies comparator design complexity because it only needs to work for one common-mode input voltage instead of a wide range. Secondly, V_{sig} enjoys an inherent voltage gain of $\times 2$ through the sampling process. Since both DAC_n and DAC_p are connected to V_{sig} during sampling, the kT/C thermal noise requirement is satisfied by the sum of C_{ij} from both DACs. During successive approximation, the capacitance at each comparator input is halved, but because of the DAC's gain in the voltage domain, the comparator's effective input referred noise is still attenuated by 3 dB.

C. DAC Calibration

The redundant sub-radix-2 DAC in Fig. 6 is calibrated against an off-chip commercial 18b DAC. Because the SAR ADC uses a much lower reference voltage (1.8 V) when compared to the commercial DAC (5 V), the actual usable resolution of the commercial DAC is close to 16b. The commercial DAC claims to have an INL and DNL of 0.2 LSB and 0.15 LSB respectively. This means that given enough noise averaging samples, the DAC's differential steps can be used as a reliable means of calibrating the SAR ADC's weights. The detailed calibration procedure based on matrix projection is detailed in Appendix B. This calibration scheme prioritizes the minimization of the ADC's Differential Non-Linearity (DNL) error in the absence of an accurate reference for INL. It can be integrated on-chip by adding a high-resolution thermal coded single-slope reference to be shared among the ADC array. This can be in the form of a large (2900 μm $\times$ 2900 μm for 18b) capacitive DAC, or a smaller but very slow $\Delta\Sigma$ DAC. A popular alternative would be self-calibration schemes. They are often faster and much more compact [28], [42].

D. Low-Noise Time-Domain Comparator

The resolution of a SAR ADC is largely limited by the input referred noise of its comparator, especially from a power consumption's point of view. This SAR ADC overcomes this limitation by using a noise-averaging time-domain comparator. The core of this comparator, as shown in Fig. 9, is formed by two voltage controlled delay lines (VCDL). The transistors $M4$, $M5$, $M6$, and $M7$ form an inverter chain for the V_{CLK} pulse to propagate through. During reset, V_{CLK} is low and the transistors $M4$ and $M7$ are turned on to reset all internal nodes of the inverter chain while $M5$ and $M6$ are off. The common source node of $M6$ is reset to the supply voltage by $M1$, $M2$, and $M3$ and the common source node of $M5$ is reset to ground by $M8$, $M9$, and $M10$. During the evaluation phase, V_{CLK} is asserted high to create a step pulse which turns on $M5$ and $M6$ from stage to stage. Their current supplies are starved by $M3$ and

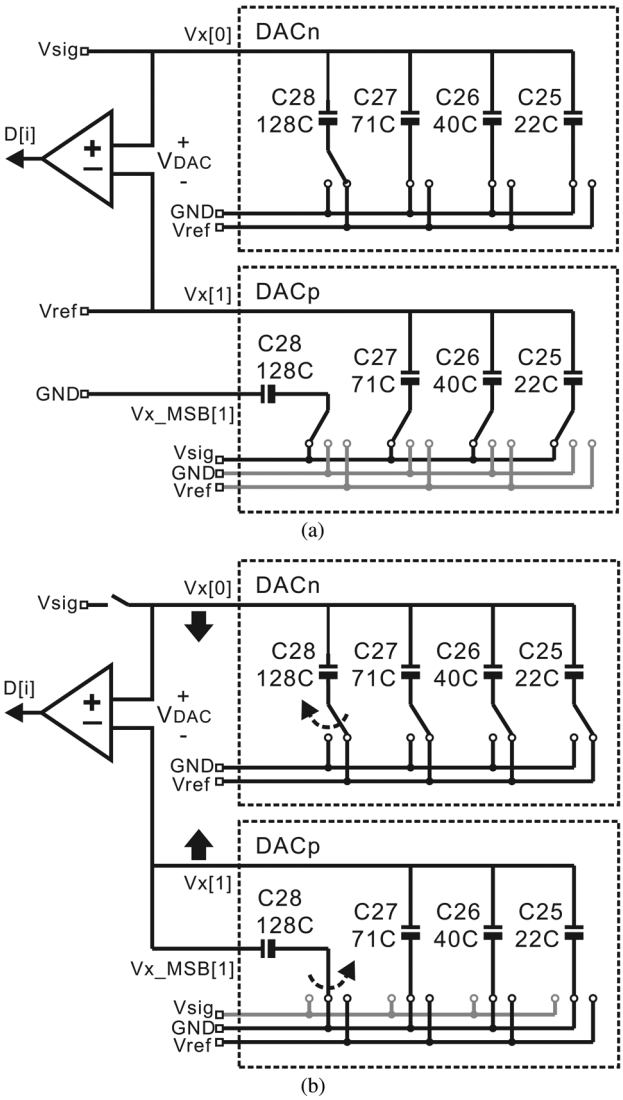


Fig. 7. Operation of a 4b SAR ADC during (a) sampling phase and (b) MSB evaluation.

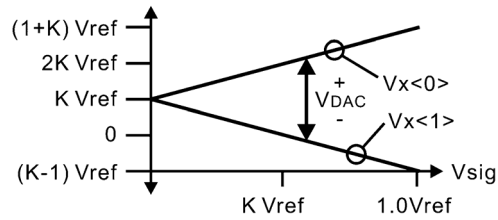


Fig. 8. DAC post-sample settling voltage for different input voltages, V_{sig}.

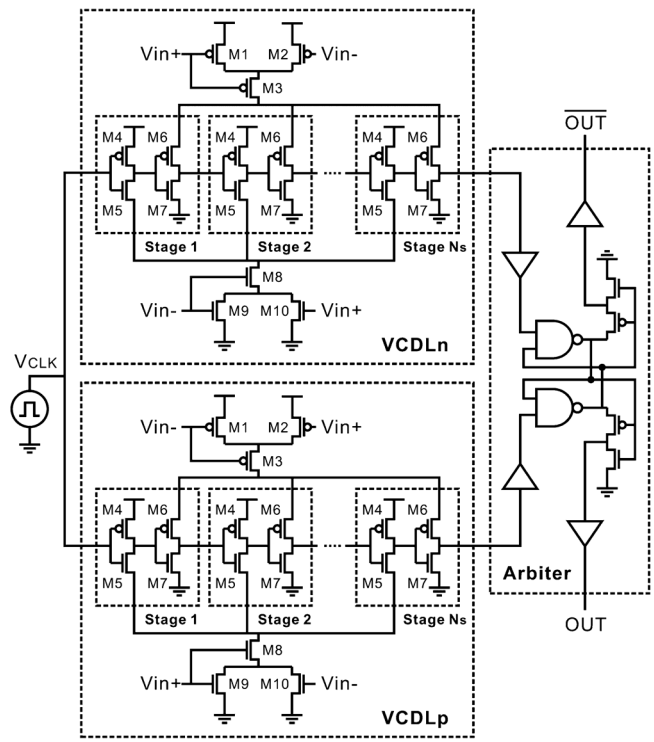


Fig. 9. Schematic of the time-domain noise-averaging comparator.

$M8$ (biased in the saturation region). Consequently, the difference in the gate voltages of $M3$ and $M8$ between the two VCDL determines the difference of their delay time. The absolute delay time of each VCDL determines their respective noise bandwidth because the noise current of $M3$ and $M8$ are integrated over the time it takes for V_{CLK} to propagate from one end of the delay line to the other. This leads to an averaging effect on the comparator noise. The difference in delay time between the two VCDL is then arbitrated by the arbiter to produce the final comparator output.

The transistors $M5$ and $M6$ are sized to be much bigger than $M3$ and $M8$ (approximately eight times), so they operate in the linear region and have low gain. The above configuration is fundamentally different from the VCDL in [43] where an independent transistor is used to control the current of each inverter stage. In certain sizing conditions, it can become a multi-stage amplifier while the circuit described here is always a single-stage amplifier. The inverters formed by $M4$ and $M5$ see a common noise source, $M8$, and similarly the inverters formed by $M6$ and $M7$ see a common noise source, $M3$. This ensures that the phase noise, $\overline{n_T^2}$, of each inverter-pair stage is added equally and does not experience the cascaded gain in [43] where the first inverter stage will have the largest noise contribution. The net effect, as the V_{CLK} pulse propagates through the inverter chain, is that N_s observations of $\overline{n_T^2}$ is added to the total inverter chain delay power (T_{delay}^2)

$$T_{delay}^2 = (N_s A_T V_{in})^2 + N_s \overline{n_T^2} \tag{13}$$

where A_T is the voltage-to-time gain of a single inverter-pair stage comprising $M4$, $M5$, $M6$, and $M7$. The first term of (13), $N_s A_T V_{in}$, is the voltage-to-time conversion gain of the entire VCDL. Its second term, $N_s \overline{n_T^2}$, is the time-domain noise power summed from the N_s inverter-pair stages. The output SNR is estimated by

$$SNR = \frac{N_s (A_T V_{in})^2}{\overline{n_T^2}}. \tag{14}$$

The noise power term, $\overline{n_T^2}$, is attenuated by a factor of N_s, which is the noise-averaging factor of the comparator. Intuitively, this is the result of the output noise current of $M3$ and $M8$ being integrated over the time period of T_{delay}.

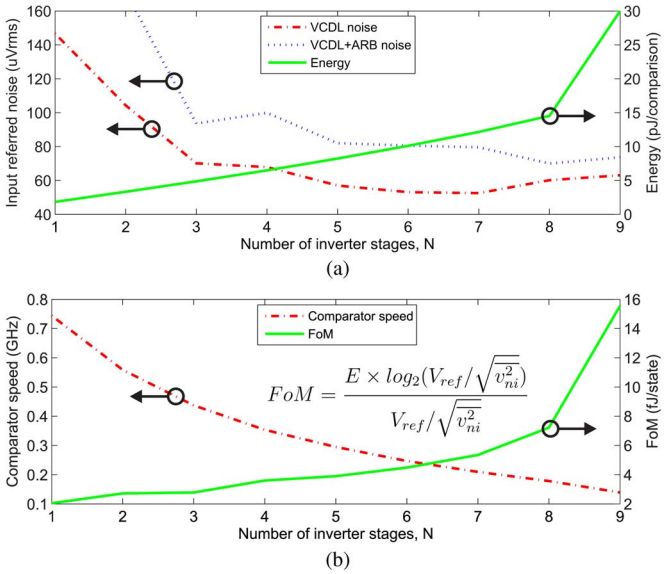


Fig. 10. The comparator's (a) input referred noise, energy consumption, (b) speed, and FoM as a function of the number of VCDL inverter-pair stages. The corresponding vertical axis of each curve is indicated by its associated arrow.

The transistors $M1$, $M2$, $M9$, and $M10$ are biased by the common-mode input voltage. They serve the purpose of tuning the bias conditions of $M3$ and $M8$ to minimize $\overline{v_{ni}^2}$ and enlarge A_T. A larger A_T reduces noise contributions from the arbiter.

The comparator's input referred noise, $\sqrt{\overline{v_{ni}^2}}$, and energy consumption per comparison, E, is plotted in Fig. 10(a) against an increasing number of inverter-pair stages. The supply and reference voltage, V_{ref}, are set to 1.8 V, and the load capacitance, C_L, is 15 fF. The lower bound of $\sqrt{\overline{v_{ni}^2}}$ observed in Fig. 10(a) is due to the noise contributions from the inverter-pair themselves which follows the conventional noise model of cascaded amplifier chains. In Fig. 10(b), the comparator speed is inversely related to the number of inverter stages. In this design, $N_s = 8$ is chosen as a conservative choice. For aggressive high-speed designs, 5 or 6 stage inverter-pairs offer good performance trade-offs.

IV. Prototype and Experimental Results

A. Prototype Chip

The prototype LDI sensor in Fig. 11 is fabricated in Global Foundry 1P6M 0.18 μm mixed-signal technology. The imager and ADC specifications are summarized in Table IV. The DNL and INL reported in Table IV are measured from the first ADC channel in the array. The Figure-of-Merit (FoM) calculated for each imaging mode and also the ADC itself (without CDS) is based on the effective resolution, ER. This definition is appropriate for image sensors since the output from the pixel array can be considered to be a DC signal [20], [45], [47], [48] as opposed to a full-range sinusoid.

Evident from entries in Table III, only a limited number of LDI sensors use custom chips, and an even smaller number of them disclose their circuit details. In order to better assess

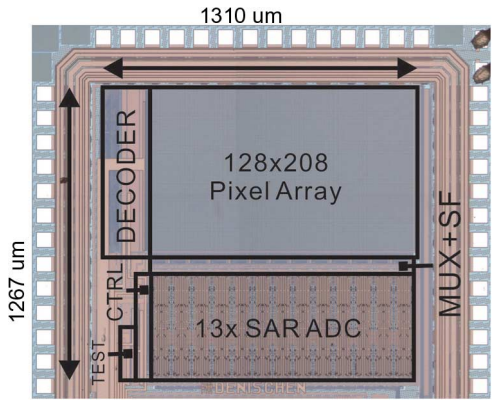


Fig. 11. Prototype LDI sensor (MONAVALE).

TABLE IV
Summary of the Prototype Chip

	Standard Image		LDI Image	
	no CDS	CDS	no CDS	CDS
Process	0.18 μm 1P6M CMOS			
Supply voltage (V)	3.3, 1.8			
ADC Area (μm^2)	518 × 84			
Clock frequency (MHz)	20			
Pixel resolution	128 × 208			
Frame rate (fps)	340	167	1.4	0.67
Pixel rate (kSa/s)	0.340	0.167	44.6	43.1
Pixel size (μm^2)	5.3× 5.3			
Fill factor	45%			
Dark current (e^-/sec)	<4688			
Sensitivity (e^-/Lux.sec)	269000 @ 201 Lux			
Dynamic range (dB)	74			
ADC rate (kSa/s)	683	335	714	345
ADC noise (μV_{rms})	110 (4 LSB)			
DNL (LSB)	+3.0/-2.8			
INL (LSB)	+24/-17			
column FPN (μV)	22700	138	-	-
Pixel noise@256Lux (μV_{rms})	509	449	-	-
Pixel noise@dark (μV_{rms})	477	427	-	-
SF noise (μV_{rms})	812	873	812	873
ER (b)	13.6			
Imager power (mW)	4.46	4.75	4.75	4.73
Energy (nJ/pixel)	0.50	1.09	131	270
Imager FoM (fJ/step)[a]	31	66	31	64
ADC FoM (fJ/step)[a]	23			

[a] The Figure-of-Merit (FoM) is defined as $FoM = P/(F_s \times 2^{ER})$. Here, P is the power consumption, F_s is the sampling frequency, and ER is the effective resolution ($ER = log_2(V_{ADC}/n)$ where V_{ADC} is the ADC's input range and n is the average input referred noise of the ADC).

the performance merit of this design, a comparison is made in Table V against general-purpose image sensors especially in terms of energy efficiency. The FoM of the prototype chip is calculated from its effective resolution, ER, and it includes energy contributions from digital CDS (two ADC samples), pixel source-follower, and additional shutter-related digital control. For the other entries in Table V, because image sensors typically do not quote their standalone ADC noise, their FoMs are calculated directly from their nominal resolution assuming zero

TABLE V
COMPARISON OF ADCS FOR IMAGE SENSORS

Year	2009	2009	2011	2011	2009	2012	2012	2013
Ref	[44]	[18]	[20]	[45]	[19]	[27]	[46]	This work
ADC architecture	2-step SS	Cyclic	$\Delta\Sigma$	Cyclic	SAR	SAR	SAR	SAR
Technology (μm)	0.35	0.18	0.13	0.13	0.18	0.13	0.18	0.18
Supply (V)	2.8	1.8, 3.3	2.8, 1.2	2.8, 1.5	3.3, 1.8	2.8, 1.5	-	1.8, 3.3
Column area (μm^2)	11.2×484	5.6×1112	4.5×600	18×240	8.4×1320	9×425	15×700	518 × 84
Resolution	320×240	640×428	1692×1212	1696×1212	4112×2168	1600×1200	256×256	128 × 208
Pixel pitch (μm)	5.6	5.6	2.25	2.25	4.2	2.25	15	5.3
Pixel structure	4T APS	4T APS	2.5T APS	2.5T APS	4T APS	2.5T APS	CTIA	BB 3T APS
Sensitivity (V/lux.s)	0.52	7.1	-	0.11	-	1.6	68.5	2.0
Conv. gain ($\mu V/e^-$)	46	61	80	80	45	-	-	7.6
Saturation level (e^-)	18500	-	11000	11000	27800	-	-	68115
Read noise (μV_{rms})	490	336	152	1000	17.6	2400	3202	909 (**110** [a])
Dynamic Range (dB)	64.8	71	75	59	84	52	56.5	74
Clock (MHz)	25	-	48	25	41.25	7	25	20
Frame rate (fps)	700	390	120	250	50	150	1500	167
Analog gain	No	No	No	No	Yes	No	Yes	No
CDS	Analog	Digital	Digital	Analog	Digital	Analog	Analog	Digital
ADC resolution (b)	11	13	12	10	14	10	10	**13.6**
DNL(LSB)	+0.53/-0.78	0.5	+0.55/-0.63	+0.59/-0.83	1	-	0.34	+3.0/-2.8
INL(LSB)	+1.42/-1.61	3.2	+3.7/-0.8	+2.8/-3.6	+2/-15	-	0.6	+24/-17
column FPN	0.10%	0.06 LSB	0.01%	0.10%	$0.38e^-$	0.4 LSB	0.52%	**0.026** %
Power (mW)	36	297	180	300	1085	220	390	**4.46**
Energy (nJ/pixel)	0.670	2.780	0.731	0.584	2.434	0.764	3.967	**1.09**
FoM (fJ/step)	327	339	179	570	149	746	3874	**66**

[a] noise contribution from ADC.

noise and non-linearity. Despite this, the SAR ADC in this paper still has the lowest FoM among the published works.

B. Non-Linearity and FPN

The ADC's differential non-linearity (DNL) and integral non-linearity (INL) are characterized from the calibration data generated by the method in Section III-C. The measured DNL of the first 4 ADC channels in the ADC array is plotted in Fig. 12(a). Out of the 13 ADCs on-chip, 11 have a maximum DNL value [half of the peak-to-peak span in Fig. 12(a)] less than 4 LSBs. This indicates that the sub-radix-2 DAC has provided enough redundancy to accommodate process variation within the die. The INL in Fig. 12(b) has a large common-mode component across all channels. This INL error profile changes from measurement to measurement. It may be the result of limitations in the test setup where the ADC's reference voltage is directed connected to an Agilent E3646A power supply causing low-frequency drifts in the reference. Fortunately, in most imaging applications INL is less critical than DNL because large INL does not lead to missing codes; linearity is either not critical or can be corrected during post-processing. The LDI perfusion calculated by (4) inherently discriminates against low-frequency components in the signal.

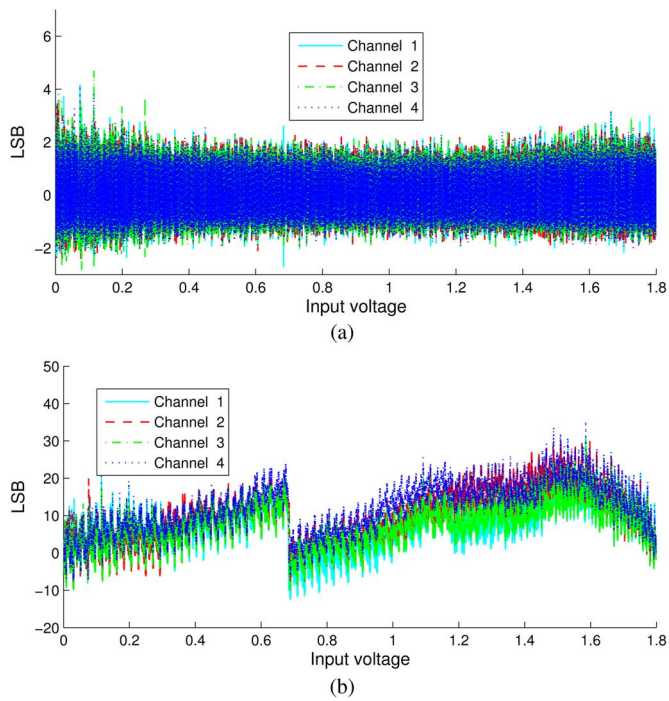


Fig. 12. (a) DNL and (b) INL (normalized to the LSB) of the first four columns of 16b SAR ADC array.

C. Noise

The ADC input referred noise in Table IV is measured by calculating the power spectrum of the ADC output when the ADC input is clamped to a heavily low-pass filtered DC input. Similarly, the source-follower (SF) noise is measured from the power spectrum of the ADC output when all the photo-diodes (PD) are biased at a constant voltage by turning on the in-pixel reset PMOS transistor. The PD noise can be calculated by illuminating the sensor array with constant and uniform illumination from an integrating sphere and subtracting from its ADC output power spectrum the SF noise power characterized earlier. Two sets of pixel noise measurements are reported in Table IV: one under 256 Lux illumination and one in dark conditions. The

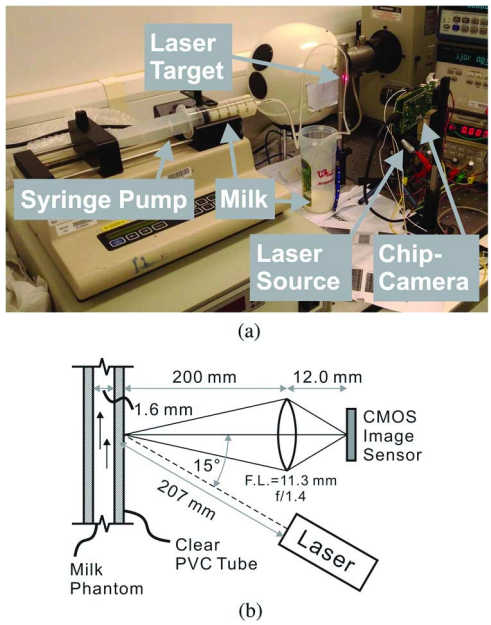


Fig. 13. The (a) photo and (b) schematic of LDI flowmetry experiment apparatus.

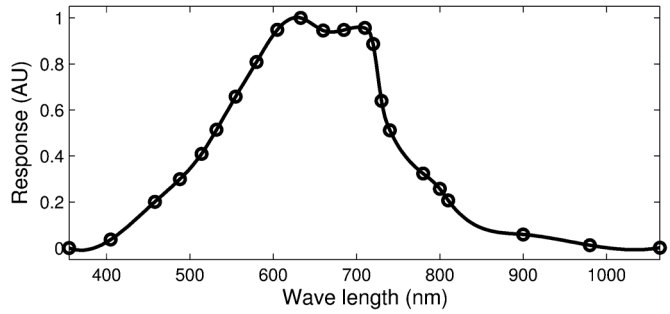


Fig. 14. Spectral response of the pixel's NWELL photo-diode.

pixel reset-noise without CDS is back calculated to be 212 μV which is smaller than the 355 μV noise level expected from kT/C_{ph} of a single pixel where $C_{ph} = 33$ fF. Among dark shot noise, optical shot noise and reset-noise, dark shot noise is rendered negligible here due to the short exposure time, and reset-noise is alleviated by the PMOS reset switch. So the PD noise is mainly contributed by optical shot noise, and a constant illumination source is a valid means to characterize this. The results in Table IV confirm that the PD and its SF are the dominant noise sources. The SF here has the same noise bandwidth in standard imaging mode as it does in LDI mode. Its noise power when compared to the PD's own contribution can therefore be higher than certain video-rate image sensors whose SF is low-pass filtered to much smaller bandwidths.

D. Power Consumption

The total sensor power consumption reported in Table IV is composed of 12% from the ADC reference, 60% from the analog circuits (predominantly ADC comparators and pixel source-followers), 4% from digital circuits, and 24% from pixel circuits. These ratios are consistent across all imaging modes. The contribution of digital circuits is low because image processing is performed off-chip.

E. Laser Doppler Imaging

The LDI algorithm ((4)) is implemented off-chip using Matlab's fast Fourier transform (FFT) function. For future on-chip LDI processing, M_0 and M_1 can be approximated by simple digital filters [49]. The LDI experimental set-up is shown in Fig. 13. Skimmed milk with 3.4% protein content (human blood has a 7% protein content) is used as the phantom serum because there were no blood samples or alternative optical phantoms available at the time of this experiment. Milk has been used as the test phantom in a number of studies due to its optical properties [50]–[53]. In this experiment, it is pumped through a clear 1.6 mm PVC tube (1.6 mm wall thickness) by a 3 ml syringe pump from KD Scientific. A section of the PVC tube and its content is illuminated by a 1 mW 638 nm laser. This wavelength is chosen to match the spectral response of the pixel's NWELL photo-diode as shown in Fig. 14. The illuminated section of the PVC tube is imaged by the LDI sensor chip in Fig. 15. While a number of earlier LDI experiments [8]–[11], [14] on biological tissues have provided important insights into LDI's biomedical application, the above setup is useful for subjectively measuring LDI precision against a known flow reference.

The effects of CDS and quantization noise on LDI quality are compared in Fig. 15. Fig. 15(a) shows the light intensity image (with CDS) captured by the prototype camera. Fig. 15(b) shows the flow-image [first moment, M_1, (2)] without CDS. Fig. 15(c) shows the same flow-image with CDS, and finally Fig. 15(d) recalculates Fig. 15(b) with 10b quantization error. The laser dots in Fig. 15(b), Fig. 15(c), and Fig. 15(d) is much smaller than that in Fig. 15(a) because LDI only generates a response in areas where there is particle flow. In Fig. 15(c), the image quality is significantly deteriorated by the noise gain of the CDS process. Similarly, the background noise in Fig. 15(d) is increased by 2.3 dB because of higher quantization noise as shown by the corresponding reduction in its PSNR (maximum LDI response divided by background RMS noise).

Similar noise performance trends are also observed in perfusion (4) measurements. In Fig. 16, Fig. 17, and Fig. 18, the measured LDI response in arbitrary units (AU) is plotted over a range of flow-rates set by the syringe pump. Ten measurements are repeated over the same LDI pixel for each chosen flow-rate. The confidence interval deteriorates from 16b without CDS to 10b without CDS to 16b with CDS. Due to the large noise in the single pixel measurements, the underlying linearity of the LDI response is more easily seen by averaging across 49 neighboring pixels centered around the laser spot. This is appended to Fig. 16 and Fig. 18.

The LDI sensing precision, Ψ, is defined as

$$\Psi = \frac{\overline{p}}{\sigma_p} \tag{15}$$

where $\overline{p}$ is the average perfusion as defined by (4) over the 10 measurements and σ_p is its standard deviation. This Ψ is plotted in Fig. 19 using data from Fig. 16, Fig. 17, and Fig. 18. Averaging across the 49 pixel patch increased the Ψ by 15 dB when

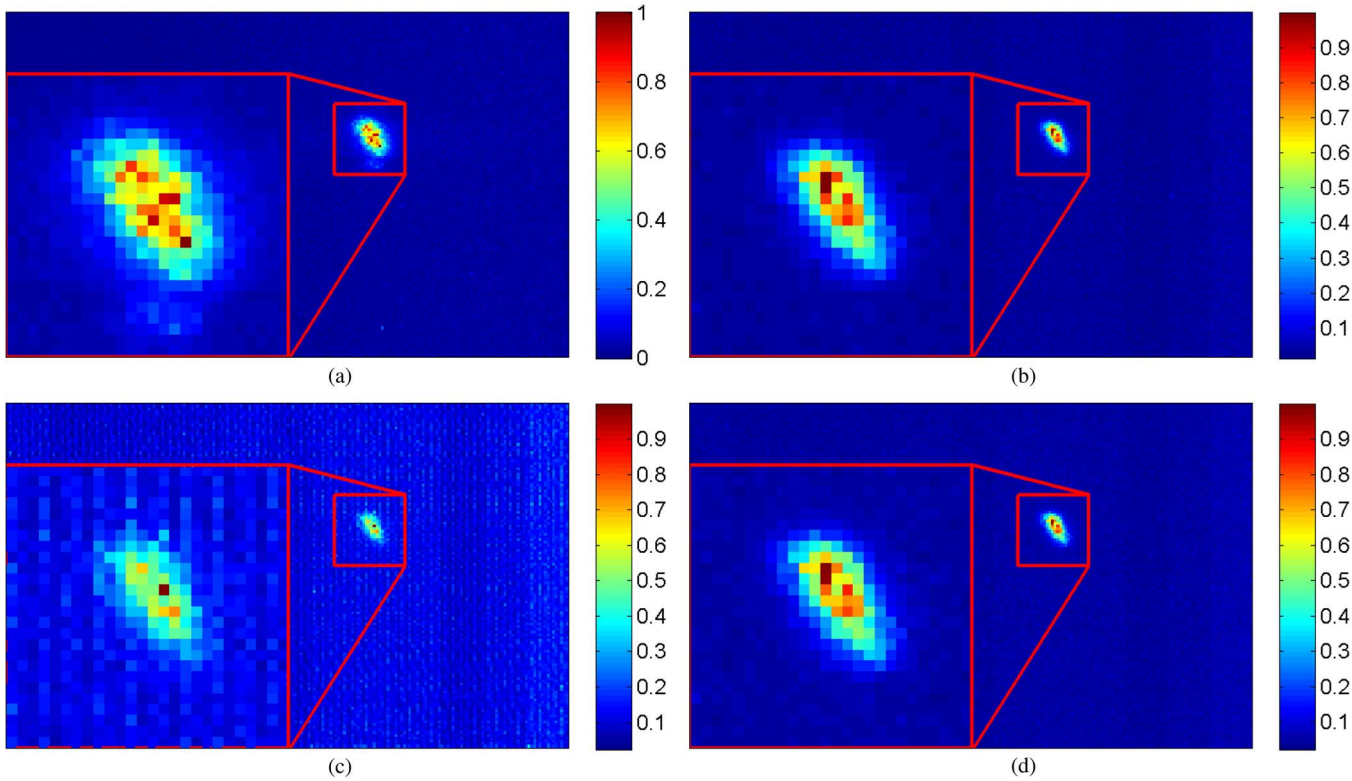


Fig. 15. The (a) light intensity image (PSNR = 40.6 dB) against LDI images (12 mm/s flow-rate) in (b) 16b resolution without CDS (PSNR = 40.5 dB), (c) 16b resolution with CDS (PSNR = 27.8 dB), and (d) 10b resolution without CDS (PSNR = 38.2 dB).

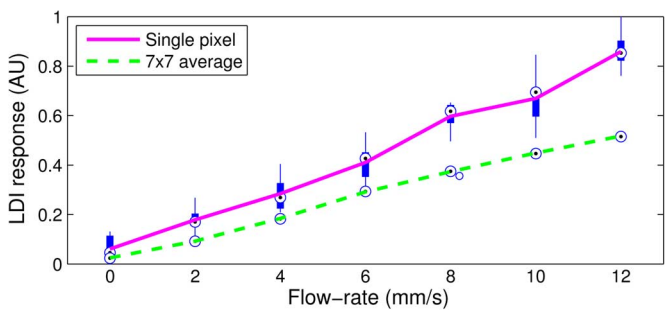


Fig. 16. Box plot and mean plot of 10 samples of a single pixel versus the group average of 49 (7 × 7) pixels under 16b ADC resolution without CDS for different flow-rates.

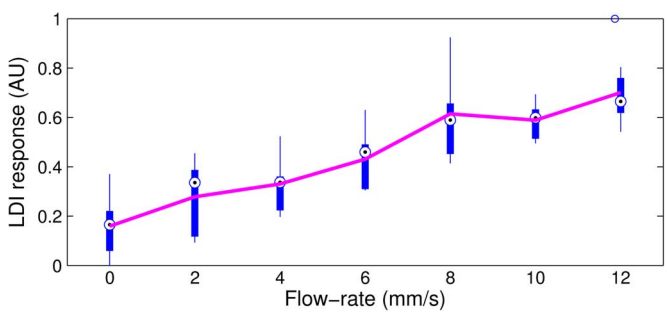


Fig. 17. Box plot and mean (line plot) of 10 samples of a single pixel under 16b ADC resolution with CDS for different flow-rates.

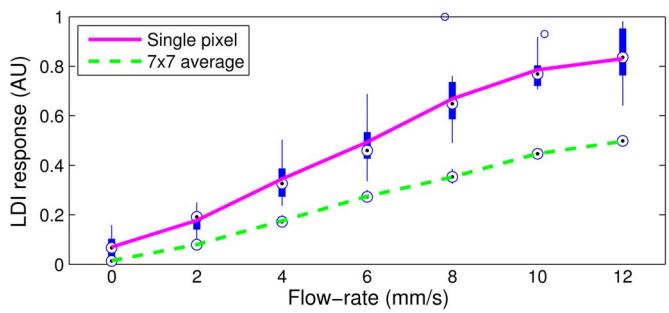


Fig. 18. Box plot and mean plot of 10 samples of a single pixel versus the group average of 49 (7 × 7) pixels under 10b ADC resolution without CDS for different flow-rates.

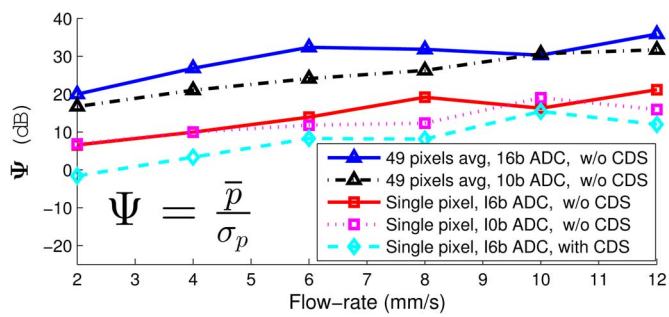


Fig. 19. SNR comparison across the various sensing configurations used in Figs. 16–18.

compared to single pixel values. This indicates that the perfusion noise has very little correlation between pixels. On average, 4.4 dB of improvement is observed when the ADC resolution is increased from 10b to 16b ($ER = 13.6$b). This falls in well with the 3.1 dB lower-bound estimated in Table II (10b case) from Section II-C because the pixel circuit makes up for the

dominant share of noise power. On average, CDS deteriorates Ψ by 6.9 dB. This is close to the 6 dB upper-bound estimated in Section II-D.

V. Conclusion

LDI sensing precision in relation to pixel size, ADC resolution, and CDS is analyzed. A prototype sensor with non-CDS PMOS reset pixel and low-noise SAR ADC is presented to improve this precision. The phantom serum measurement results match well with the expected theoretical values. The SAR ADC is able to achieve high effective resolution without sacrificing energy efficiency thanks to its low-noise time-domain comparator. It has the lowest FoM amongst published works making it suitable for future mobile LDI applications.

Appendix A
The Effect of Digital CDS on the First Moment of LDI

The digital CDS process is depicted in Fig. 2. Let $X(\omega)$ be the pixel output PSD (discrete-time Fourier transform version of $S(v)$) with a response up to $F_s/2$ (F_s is the sampling frequency) or π. The analog input to the ADC, $Y(\omega)$, is an up-sampled version of $X(\omega)$ modulated with $0.5, -0.5, 0.5\ldots$, or $0.5cos(\pi n)$. The quantized $Y(\omega)$ is passed though the CDS function

$$|H_{CDS}(\omega)| = |e^{-j\omega\tau} - 1| = 2sin(\omega\tau/2). \tag{A.1}$$

Both the $1/f$ noise component, $N_{1/f}/\omega$, and the white noise component, N_w, are superimposed in the noise PSD, $N(\omega)$, and ADC quantization noise is lumped into N_w.

$$N(\omega) = \frac{N_{1/f}}{\omega} + N_w \tag{A.2}$$

The $1/f$ noise component and the white noise component are analyzed separately. Applying the first moment, M_1, from (2) to the $1/f$ noise power and taking into account that both the signal and its modulated image (centered at 0 and 2π respectively) fold into the post-CDS Nyquist band yields

$$P_{1/f,CDS} = \frac{N_{1/f}}{2}\int_0^{\pi}\frac{2}{\omega}4sin^2\left(\frac{\omega}{4}\right)\omega \mathrm{d}\omega + \frac{N_{1/f}}{2}\int_0^{\pi}\frac{2}{2\pi-\omega}4cos^2\left(\frac{\omega}{4}\right)\omega \mathrm{d}\omega. \tag{A.3}$$

The non-CDS case is simply $P_{1/f,non-CDS} = 2\pi N_{1/f}$, and

$$\frac{P_{1/f,CDS}}{P_{1/f,non-CDS}} \approx 0.91. \tag{A.4}$$

CDS simply doubles the white noise power

$$\frac{P_{w,CDS}}{P_{w,non-CDS}} = 2. \tag{A.5}$$

Appendix B
DAC Calibration

This calibration scheme prioritizes the minimization of the ADC's Differential Non-Linearity (DNL) error. It is used in the absence of an accurate reference for estimating INL. For each ADC input, $V_{sig}(i)$, generated by the commercial DAC at step i, the SAR ADC quantizes it to a N bit binary word, $a_{ij}|_{j=1,2,\ldots,N}$, by a combination of its weights w_j

$$V_{sig}(i) = \sum_{j=1}^{N} a_{ij}w_j \tag{B.1}$$

where $w_1, w_2, \ldots, w_N$ represent the capacitor weights from LSB to MSB. Fig. 6 shows the case of $N = 19$ where w_1 and w_N corresponds to C_{01} and C_{28}. Let N' be the non-redundant resolution of the ADC ($N' = 16$ in this case). If a ramp of $S \approx 2^{N'}$ uniform steps is generated by the commercial DAC, the corresponding ADC output is described by

$$\mathbf{D} = \mathbf{AW} \tag{B.2}$$

where the matrices D, A, and W are defined as

$$\mathbf{D} = \begin{bmatrix} V_{sig}(2) \\ V_{sig}(3) \\ \vdots \\ V_{sig}(S) \end{bmatrix} - \begin{bmatrix} V_{sig}(1) \\ V_{sig}(2) \\ \vdots \\ V_{sig}(S-1) \end{bmatrix} \tag{B.3}$$

$$\mathbf{A} = \begin{bmatrix} a_{2(N)} & a_{2(N-1)} & \cdots & a_{21} \\ a_{3(N)} & a_{3(N-1)} & \cdots & a_{31} \\ \vdots & \vdots & \ddots & \vdots \\ a_{S(N)} & a_{S(N-1)} & \cdots & a_{S1} \end{bmatrix} - \begin{bmatrix} a_{1(N)} & a_{1(N-1)} & \cdots & a_{11} \\ a_{2(N)} & a_{2(N-1)} & \cdots & a_{21} \\ \vdots & \vdots & \ddots & \vdots \\ a_{(S-1)(N)} & a_{(S-1)(N-1)} & \cdots & a_{(S-1)1} \end{bmatrix} \tag{B.4}$$

$$\mathbf{W} = \begin{bmatrix} w_N & w_{N-1} & \ldots & w_1 \end{bmatrix}^T. \tag{B.5}$$

In practice, each row of A is averaged across a large number of consecutive ramps. Each sample, $V_{sig}(i)$, within a ramp represents one DAC step. When A is long enough to cover all ADC code changes in the ramp, it will have sufficient eigenvalues to regress all entries in W. If $S < 2^{N'}$, A may be too sparse to give reliable estimates of all the LSB weights in W. In that case, the LSB weights can be linearly extrapolated from the last reliable MSB weight [28]. While the DNL can be accurately estimated from this calibration data, INL measurements are still subject to fluctuations in the reference and supply.

From (B.2), the weight matrix, W, can be projected by

$$\mathbf{W} = (\mathbf{A^T A})^{-1}\mathbf{A^T D}. \tag{B.6}$$

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