A 0.096-mm² 1–20-GHz Triple-Path Noise-Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration

Haohong Yu®, Yong Chen®, Member, IEEE, Chirn Chye Boon®, Senior Member, IEEE, Pui-In Mak®, Fellow, IEEE, and Rui P. Martins®, Fellow, IEEE

Abstract—This article proposes a novel wideband common-gate (CG) common-source (CS) low-noise amplifier (LNA) with a dual complementary pMOS–nMOS configuration to provide a current-reuse output. Triple-path noise-cancellation is effectively revealed to eliminate the thermal noise of the two CG transistors. Simultaneously, partial cancellation of intrinsic third-order distortion of output-stage transistors improves the input third-order intercept point (IIP3). In addition, we embed a resistive feedback in one of the auxiliary CS amplifiers to balance the multiple tradeoffs between noise figure (NF), input matching (S11), and forward gain (S21). Fabricated in 65-nm CMOS, the proposed wideband LNA exhibits an IIP3 of 2.2–6.8 dBm and an NF of 3.3–5.3 dB across a 19-GHz BW while consuming 20.3 mW at 1.6 V. S11 is <−10 dB up to 23 GHz by designing a π-type input-matching network. The LNA exhibits a peak S21 of 12.8 dB and occupies a very compact die area of 0.096 mm².

Index Terms—CMOS, common gate (CG), common source (CS), input third-order intercept point (IIP3), noise figure (NF), partial distortion canceling, pMOS–nMOS configuration, resistive feedback, triple-path and dual-path noise canceling (NC), wideband input matching, wideband low-noise amplifier (LNA).

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1. INTRODUCTION

WIDEBAND circuits are promising for software-defined radios [1], [2] and broadband communication systems [3]. Specifically, the forefront wideband low-noise amplifier (LNA) determines the input sensitivity of the receiver and dominates its power dissipation. Many wideband LNAs have been reported, e.g., to cover the 3.1–10.6-GHz band for ultra-wideband (UWB) communication. Recently, prior works [4]–[9] have aimed to extend the LNA’s bandwidth (BW) beyond 20 GHz. In [9], a self-biased resistive-feedback together with a source-degeneration inductor is used to achieve good wideband input matching (S11). Yet, wideband S11 is challenging due to the parasitic capacitance of the CMOS devices, and the input impedance at high frequencies can be heavily affected by its imaginary part. In fact, S11 < −10 dB could not be achieved in a few prior works targeting 20 GHz [4]–[6]. The tradeoff between S11 and noise figure (NF) also imposes design challenges. Noise canceling (NC) is known for breaking the tradeoff between S11 and NF. Without the concern of the noise contribution from the input-matching transistor, S11 can be optimized with one additional degree of freedom. S11 can be easily designed below −10 dB with NC [10]–[21].

This article proposes a common gate (CG)-based NC LNA topology that uses a structure based on resistive-feedback common source (CS) as one of the auxiliary amplifiers in the NC path. Differing from a conventional CG-based NC LNA, the addition of the feedback resistor improves forward gain (S21), S11, and NF. The nMOS-based LNA topology is expanded to a stacked pMOS–nMOS configuration allowing current-reuse and third-order intercept point (IP3) improvement. By the aid of the pMOS–nMOS topology, the noise generated from the input CG transistors is canceled through three, instead of conventionally two, feed-forward paths. In contrast to [13], the explicit triple-path NC in our design is achieved at the output stage/node and the current-reuse configuration as an auxiliary amplifier is utilized as the output stage. The partial linearity improvement can be achieved through the auxiliary amplifier stage. Noises traveling through the three paths are analyzed and discussed in detail. A π-match network is used to facilitate an input matching up
TABLE I
CONFIGURATIONS AND PERFORMANCES OF THE STATE-OF-THE-ART NC LNAs

<table>
<thead>
<tr>
<th>Circuit Configuration</th>
<th>Fig. 1(a) in [10]</th>
<th>Fig. 1(b) in [11]</th>
<th>Fig. 1(c) in [13]</th>
<th>Fig. 1(d) in [15]</th>
<th>Fig. 2(a) Our work target</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stacked pMOS-nMOS</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Gain (dB) @ GHz</td>
<td>9.7 @ 4</td>
<td>16.8 @ 4</td>
<td>14.5 @ 0.3</td>
<td>17.5 @ 0.2</td>
<td>10 – 15</td>
</tr>
<tr>
<td>IIP3 (dBm) @ GHz</td>
<td>–6.2 @ 6</td>
<td>–4.5 @ 4</td>
<td>6 @ 0.9</td>
<td>14 @ 2</td>
<td>5 – 10</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>10.7</td>
<td>6.5</td>
<td>1.3</td>
<td>1.9</td>
<td>20</td>
</tr>
<tr>
<td>Headroom</td>
<td>(V_{gs} + V_{ds} + V_{RD})</td>
<td>(V_{gs} + V_{ds} + V_{RD})</td>
<td>(2V_{gs} + 2V_{RD})</td>
<td>(2V_{gs} + 2V_{RD})</td>
<td>(2V_{gs} + 2V_{RD})</td>
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<tr>
<td>Technology (nm)</td>
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<td>65</td>
<td>130</td>
<td>180</td>
<td>65</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>20</td>
<td>11.3</td>
<td>17.4</td>
<td>22</td>
<td>20</td>
</tr>
</tbody>
</table>

higher gain and lower NF than that in the CG configuration. Yet, prior works [11], [12] report an IIP3 of $\sim -4$ dBm and it is insufficient to suppress the intermodulation due to the increased coexistence of the adjacent blockers or transmitter on-chip leakage [13], [14]. IIP3 is vital to LNAs whose BW is as wide as 20 GHz, because many high-order harmonics can intermodulate with each other and generate a third-order interference within the 20-GHz range of interest.

To achieve high linearity performance in NC LNA designs, several modifications based on CG configuration are proposed as follows. As shown in Fig. 1(c), a stacked pMOS–nMOS configuration as the input-matching stage is combined with noise cancellation based on a CG configuration to obtain an excellent IIP3, which is above 10 dBm. By properly biasing the transistors, the distortion components generated by pMOS and nMOS will cancel each other and improve IIP3 [22]. Nevertheless, the high linearity performance [13], [14] is only achieved within a limited BW, i.e., less than 1.9 GHz. It is also interesting to observe that, in [13] and [14], noise from a single transistor travels in more than two paths, leading to an implicit multipath NC instead of the conventional two-path NC. However, this phenomenon is not mentioned or analyzed by the authors. The NC LNA in [15] combines a current mirror with CG configuration, as shown in Fig. 1(d), to avoid distortions caused by voltage-to-current conversion and to improve IIP3. Regrettably, due to the addition of a cascode transistor as a current mirror, the voltage headroom becomes constrained and a supply voltage as high as 2.2 V is necessary in [15]. Moreover, the study in [15] only has a BW of 1.9 GHz. Table I summarizes the pros and cons of the state-of-the-art NC LNAs. To obtain a good IIP3 over 20-GHz BW remains a challenge in the state of the art. The target of this work is to design an LNA with good linearity across a BW of 20 GHz. The target gain is set to a moderate 10–15 dB to avoid saturating the subsequent stage circuit, e.g., mixer. As no current mirror is used, our design has a lower headroom than that in [15].

II. OVERVIEW OF EXISTING NC LNA TOPOLOGIES

The NC LNA is categorized into two major types: CG and resistive-feedback based on the input-matching method. CG-based NC LNA is proposed by Liao and Liu [10] shown in Fig. 1(a); however, it has a low gain of 9.7 dB, a low IIP3 of $-6.2$ dBm, and a high NF of 4.5 dB. Generally, the resistive-feedback NC LNA [11], [12] [see Fig. 1(b)] provides to 20 GHz. With a die area of just 0.096 mm$^2$ and power of 20.3 mW, the LNA prototyped in 65-nm CMOS shows an attractive FOM [12] of 22.7 GHz.

The article is structured as follows. Section II reviews NC LNA designs in the literature. Section III introduces the proposed wideband LNA, followed by its implementation details in Section IV. Section V analyzes the effect of the resistive feedback, triple-path NC mechanism, and IIP3 improvement. Section VI summarizes the measurement results. Finally, Section VII draws the conclusions.

III. PROPOSED WIDEBAND LNA

Fig. 2(a) shows the proposed CG-based NC LNA with a resistive-feedback auxiliary amplifier and a current-reuse...
output. The feedback resistor \( R_f \) improves input matching and in-band gain ripple to be detailed in Section V. In our proposed topology, a single pMOS transistor \( M_6 \) is utilized to replace one nMOS transistor \( M_3 \) and one resistor \( R_{D2} \) in a conventional CG-based NC LNA [see Fig. 1(a)]. \( M_6 \) together with \( M_3 \) form a current-reuse configuration at the output stage. Compared with the current-mirror-based NC LNAs [see Fig. 1(d)], which use a diode-connected transistor \( M_3 \) and consume large voltage headroom (i.e., one \( V_{GS} \) across the gate and source terminals), our LNA is more headroom-efficient.

Fig. 2(b) presents the NC principle of the proposed wideband LNA. Herein, \( r_o \) is the equivalent resistance of the parallelly connected source–drain resistance of \( M_3 \) and \( M_6 \). The noise current of the input-matching transistor \( M_2 \) generates opposite-polarity noise voltages at the source and drain of \( M_2 \). The amplification by \( M_1 \) and \( M_6 \), respectively, inverts the polarity of both noise voltages. Thereafter, the noise voltages at the output generated through the two paths have opposite polarities and cancel each other. Signal voltage as input located at the source of \( M_2 \) travels to the output via two paths. The first path is through \( M_2 \) and then \( M_6 \). The second path is through the resistive-feedback CS amplifier formed by \( M_3 \). Both paths invert the signal voltages, adding them up at the output. Unlike the auxiliary amplifiers in the conventional CG-based NC LNA [see Fig. 1(a)], which uses two nMOS transistors \( M_2 \) and \( M_3 \), we employ the current-reuse configuration \( (M_6 \) and \( M_3 \)).

Fig. 3 shows how the introduction of pMOS facilitates the evolution from the basic architecture to the pMOS–nMOS complementary configuration. The CG-configured \( M_1 \) and \( M_2 \) form the input-matching stage, \( M_3 \), \( M_4 \), and \( R_F \) become an inverter forming the first auxiliary amplifier. \( M_5 \) and \( M_6 \) are CS-configured, creating the second and third auxiliary amplifiers, respectively. After the above evolution, current-reuse topology has been achieved at \( M_1 \) and \( M_4 \) stages as well as at \( M_5 \) and \( M_6 \) stages. Moreover, multiple prior works [13], [15], and [22] have indicated that a complementary pair will benefit the linearity performance of the amplifier. The impact of the evolved pMOS and nMOS complementary structure on IIP3 of the proposed LNA will be detailed in Section V.

IV. WIDEBAND LNA DESIGN DETAILS

Fig. 4 depicts the implementation of the proposed wideband LNA. We obtain the input \( \pi \)-match network with the matching capacitor and inductor, \( C_m \) and \( L_m \), respectively, as well as the parasitic capacitor \( C_x \) at node X. We add a testing buffer to drive the output capacitance and to provide output matching. To ensure good linearity, the testing buffer, which is the last stage, adopts resistive-degeneration configuration \( R_{(eq)} \). \( R_L \) is the 50-Ω load resistor and \( C_b \) is the pad capacitor. \( L_p \) is series connected to the drain of the buffer transistor to alleviate the impact of \( C_L \) on the BW of the LNA core. We insert \( L_o \) in the front of the testing buffer to broaden the BW at its gate. Furthermore, \( C_y \) and \( C_b \) are parasitic capacitance at node Y and the gate–source capacitance of \( M_b \), respectively.

A. WIDEBAND INPUT-IMPEDANCE MATCHING

The main limiting factor in the broadband input-impedance matching is the parasitic capacitor of the input transistor, which deteriorates matching at high frequency. Fig. 5(a) shows the common method to broaden the frequency of input matching which is the addition of a series inductor before the input transistor [10], [11]. \( C_x \) is the gate–source capacitance of the input transistor and \( R_m \) is the input resistance, approximated to \( 1/g_m \), generated by the CG amplifier. The resulting input impedance is

\[
Z_{in} = \frac{L_m C_x R_{in}s^2 + L_m s + R_{in}}{C_x R_{in}s + 1} - \frac{-L_m C_x R_{in}s^2 + j\omega L_m + R_{in}}{j\omega C_x R_{in} + 1}
\]

By referring to (1), at a moderately high frequency, the second term \( j\omega L_m \) in the numerator cancels the effect of \( j\omega C_x R_{in} \) in the denominator to a certain extent. Yet, as the frequency increases to an even higher value, the effect of the first term
network can be formed when $C_m$ is (a) dB format and (b) Smith chart format. rewritten as illustrated in Fig. 5(b). Then, the input impedance can be

Fig. 5. Wideband input matching based on (a) L-match network and (b) $\pi$-match network.

$L_m C_x R_{in} s^2$ in the numerator begins to merge and the condition of input matching degrades again. Thus, only introducing $L_m$ limits the improvement of the matching range. A $\pi$-match network can be formed when $C_m$ is considered before $L_m$ as illustrated in Fig. 5(b). Then, the input impedance can be rewritten as

$$Z_{in} = \frac{L_m C_x R_{in} s^2 + L_m s + R_{in}}{L_m C_m C_x R_{in} s^3 + L_m C_m s^2 + (C_m + C_x) R_{in} s + 1}.$$  (2)

Based on (2), apart from dc, there is another frequency where the perfect input matching can be obtained. By carefully optimizing the value of $L_m$, the other matching frequency can be above 20 GHz.

Assume that the CG stage itself provides a reasonable $S_{11}$ of $-15$ dB at dc. Fig. 6 plots the $S_{11}$ under $C_m = C_x = 120$ fF and $L_m = 500$ pF, by using simply the CG configuration, $S_{11}$ is less than $-10$ dB for only 12 GHz. By adding $L_m$, the input-matching frequency range approaches 19 GHz. By using the $\pi$-match network, the input matching range is further extended to 26 GHz, ensuring $S_{11} < -10$ dB beyond 20 GHz. In a packaging scenario, $L_m$ can be formed by both on-chip inductor and bonding wire, and $C_m$ can be implemented by the discrete capacitor on the printed circuit board (PCB).

In Fig. 4, the resistance $R_{in, LNA}$ looking into the sources of matching stage transistors ($M_1$ and $M_2$) can be derived as

$$R_{in, LNA} = \frac{R_F + r_o}{2 g_m (R_F + r_o + g_{m5} R_D r_o) + 2 g_{m3} r_o + 1}$$  (3)

where $r_0 = r_{o3} || r_{o4} || r_{o5} || r_{o6}$, $r_{o3}$, $r_{o4}$, $r_{o5}$, and $r_{o6}$ are the source–drain resistance of $M_3$, $M_4$, $M_5$, and $M_6$, respectively. $g_{m3}$ is the transconductance of $M_x$ ($x = 1$–6), and we can assume $g_{m1} \approx g_{m2}$, $g_{m3} \approx g_{m4}$, and $g_{m5} \approx g_{m6}$ to simplify the following analysis. $R_D$ is the load resistor in series connected to the drain of the CG stage. $R_F$ is a feedback resistor between the gate and the source of the inverter formed by $M_1$ and $M_4$. Its effect on input-impedance matching gain as well as NF will be discussed in detail in Section V. Here, considering $R_{in, LNA} = R_S$ and $C_m = C_x$, $S_{11}$ becomes

$$|S_{11}| = \frac{-L_m C_m R_S^2 s^3 + (L_m - 2 C_m R_S^2) s}{L_m C_m R_S^2 s^3 + 2 L_m C_m R_S s^2 + (L_m + 2 R_S C_m) s + 2 R_S}.$$  (4)

Furthermore, $C_x$ in Fig. 4 is the total parasitic capacitance, including the source–drain capacitance of $M_1$, $M_2$, $M_3$, and $M_4$ at node X. $S_{11}$ calculation results based on (4) will be plotted in Fig. 22(a) in Section VI.

B. Frequency Response of $S_{21}$

Referring to Fig. 4, the forward gain of the LNA can be divided into two parts: the first $A_0$ (from $V_i$ to $V_X$) provided by the input-matching network and the second $A_1$ (gain from $V_X$ to $V_B$) set by the core of the LNA. According to the small-signal equivalent circuit shown in Fig. 7, the voltage gain from node Y to the gate of the testing buffer transistor is given by

$$\frac{V_B}{V_Y} = \frac{C_b R_{deg} s + g_{mb} R_{deg} + 1}{L_o C_b s^2 + C_b R_{deg} s + g_{mb} R_{deg} + 1}$$  (5)

where $g_{mb}$ and $C_b$ are the transconductance and gate–source capacitor of $M_B$, respectively. $R_{deg}$ is the degeneration resistor. $L_o$, the inductor in series connected to the gate of $M_B$, prevents the LNA’s BW from being deteriorated by the parasitic capacitance at node Y. Equation (5) supposes that the source–drain resistor of $M_B$, $r_b$, is large, such that $Z_{out}$ has little impact on $V_B / V_Y$. Then, the voltage gain from nodes Y to X becomes

$$\frac{V_Y}{V_X} = \frac{-2 g_{m1} g_{m3} R_D R_F + 2 g_{m3} R_F - 1}{Z_y + R_F} Z_y$$  (6a)

where $Z_y$ is the total impedance at node Y, given by (6b) and $C_y$ is the total parasitic capacitance at node Y. Therefore,
the gain ($A_v$) of LNA’s core, which is the gain from node $X$ to the gate of the testing buffer, becomes

$$A_v = \frac{V_B}{V_X} \frac{V_Y}{V_X} = -\frac{C_R R_{\text{deg}} s + g_{mb} R_{\text{deg}} + 1}{L_o C_b s^2 + C_b R_{\text{deg}} s + g_{mb} R_{\text{deg}} + 1} \frac{2 g_{m1} g_{m5} R_D R_F + 2 g_{m3} R_F - 1}{Z_Y + R_F}. \quad (7)$$

On the other hand, the voltage gain ($A_0$) of the input-matching network is given by (8a), as shown at the bottom of this page

$$Y_s = Z_s^{-1} = 2 g_{m1} + \frac{2 g_{m1} g_{m5} R_D Z_Y + 2 g_{m3} Z_Y + 1}{R_F + Z_Y}. \quad (8b)$$

Herein, $Y_s$ is the inverse of the impedance $Z_s$. $S_{21}$ is twice the voltage gain in a 50-Ω system with impedance matching and given by

$$S_{21} = 2 A_0 A_v. \quad (9)$$

$S_{21}$ calculation results based on (9) will be plotted in Fig. 22(b) in Section VI.

### C. Frequency Response of NF

The major noise sources in the LNA are the channel thermal noise from $M_1$, $M_2$, $M_3$, $M_4$, $M_5$, and $M_6$, as well as the thermal noise from $R_D$ and $R_F$. Fig. 8 shows the small-signal equivalent circuit of Fig. 4 for NF calculation. Furthermore, the transfer functions of the noise current sources to node $Y$ are the same for $M_3$, $M_4$, $M_5$, and $M_6$. Thus, Fig. 8 only exhibits one of the four noise current sources. The same applies to $M_1$ and $M_2$. The noise factor of $M_1$ is given by (10a), as shown at the bottom of the next page. In (10a), $Z_s$ is written as

$$Z_s = \frac{L_m C_m R_s s^2 + L_m s + R_s}{L_m C_m C_s R_s s^3 + L_m C_s s^2 + (L_m s + C_m R_s) s + R_s Y_s + 1}. \quad (10b)$$

Fig. 8 also shows that $Z_s$ is the impedance looking toward the source from the parasitic capacitor $C_s$. $\gamma$ is the coefficient of the channel noise and $\alpha = g_{m1}/g_{d0}$, where $g_{d0}$ is the zero-bias drain conductance. Equation (10a) reveals that we can achieve a perfect NC if $g_{m5} R_D(1 + R_F/Z_s) + 1 = 2 g_{m3} R_F$, where the left side is a complex number and the right side is a real number. Then, a perfect NC cannot be achieved, however, a good approximation will be $\Re[g_{m5} R_D(1 + R_F/Z_s) + 1] = 2 g_{m3} R_F$. Note that the transfer functions from $I_{m,M1}$ and $I_{m,M2}$ to the node $Y$ are equal. A similar case is true for $I_{m,M3}$, $I_{m,M4}$, $I_{m,M5}$, and $I_{m,M6}$. Thus, the contribution of $M_2$, $M_3$, $M_4$, $M_5$, and $M_6$ for the noise factor is given by

$$F_{M2} = \frac{g_{m2}}{g_{m1}} F_{M1} \quad (11)$$

$$F_{M1} = \frac{g_{m1}}{g_{m3}} F_{M3} \quad (12)$$

$$Z_Y = \frac{r_o (L_o C_b s^2 + R_{\text{deg}} C_b s + g_{mb} R_{\text{deg}} + 1)}{L_o C_b C_s r_o s^3 + (C_b C_s R_{\text{deg}} r_o + L_o C_b) s^2 + [C_b (R_{\text{deg}} + r_o) + C_s r_o (1 + g_{mb} R_{\text{deg}})] s + g_{mb} R_{\text{deg}} + 1} \quad (6b)$$

$$A_0 = \frac{V_X}{V_s} = \frac{1}{L_m C_m C_s R_s s^3 + L_m (C_m R_s Y_s + C_s) s^2 + (L_m s + C_m R_s) s + R_s Y_s + 1}. \quad (8a)$$

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where $F_{M3}$ is derived in (13), as shown at the bottom of this page, and $i$ takes 4, 5, and 6. Apart from the transistor channel thermal noise, the thermal noise from resistors $R_D$ and $R_F$ is also taken into consideration. The two noise factors’ contributions $F_{RD}$ and $F_{RF}$ from $R_D$ and $R_F$ can be obtained in (14) and (15), as shown at the bottom of this page, respectively. Finally, by taking the parasitic resistor ($R_m$) of $L_m$ into account, the overall noise factor is derived as

$$F = 1 + \frac{R_m}{R_S} + \sum_{n=1}^{6} F_{Mn} + 2F_{RD} + F_{RF}. \quad (16)$$

We will plot the NF calculation results based on (16) in Fig. 22(c) in Section VI.

V. Design Considerations and Simulation Results

Fig. 9 shows the complete schematic of the proposed wideband LNA. We employ three capacitors $C_{i1}$, $C_{i2}$, and $C_{i3}$ for dc-decoupling in the forward path and voltages $V_o$, $V_p$, $V_{n2}$, $V_{p2}$, and $V_B$ to bias the transistors $M_2$, $M_1$, $M_5$, $M_6$, and $M_B$, respectively. We use an off-chip dc block at the input in order to keep the internal bias condition of the LNA’s core from any external circuitry interference. Here, $C_m$ is composed of 90-fF ESD capacitance and other parasitic capacitances of $\sim 30 \ fF$. Fig. 9 shows the source of our following analysis. We run extensive circuit simulations on Cadence Virtuoso for verifying our analysis.

A. Effects of $RF$

According to (3), the utilization of $RF$ increases the input admittance by introducing the term $(2g_{m3}r_0 + 2g_{m1}g_{m5} \times R_Dp + 1)/(R_F + r_0)$. Without $R_F$, i.e., $R_F$ is equal to infinity, a larger $g_{m1}$ is required in order to reach the same input matching condition. In Fig. 10(a), we plot $S_{11}$ under the situations where we only use CG and various values of $R_F$ in addition to CG. Considering a CG-only situation, we adjust the size of $M_1$ and $M_2$ to obtain the same dc matching condition when $R_F$ is 1 kΩ. Yet, larger sizes of $M_1$ and $M_2$ produce larger parasitic capacitance and further results in a degradation of $S_{11}$ at a higher frequency. By comparing $S_{11}$ in three different situations with $R_F$ equal to 500 Ω, 1 kΩ, and infinity, we can observe that a smaller $R_F$ will lead to a better $S_{11}$, but the effect of $R_F$ on $S_{21}$ and NF still needs to be studied to find an adequate value of $R_F$.

As plotted in Fig. 10(b), we compare $S_{21}$ under different circumstances where we only use CG and various values of $R_F$ in addition to CG. Under the CG-only situation, due to the increase in the size of the input transistors for matching purposes, the BW reduces significantly. Based on (7), the term $(2g_{m1}g_{m5}r_0 + 2g_{m3}R_F - 1)/(Z_y + R_F)$ indicates that the introduction of $R_F$ will lower the gain of the proposed LNA. Such a gain becomes lower as $R_F$ decreases in Fig. 10(b), but $R_F$ can be used to facilitate a flatter in-band gain variation by reducing the gain at lower frequency. This can be explained by the fact that $R_F$ is a real impedance and it has higher influence on the gain at a lower frequency range than at higher frequency. Therefore, by properly choosing the value of $R_F$, we can broaden LNA’s BW, reducing the in-band gain variation while maintaining a moderate gain of $\sim 13 \ dB$.

Considering a CG-only situation, due to the poor input matching at high frequency and the large gain difference between low and high frequencies, NF [see Fig. 10(c)] goes up rapidly with frequency. With the introduction of $R_F$, we obtain a better input matching and flatter gain, leading to a flatter NF across the frequency of interest. However, Fig. 10(b) and (c) shows a tradeoff between a low NF and a flat gain. Fig. 10(d) plots the simulated IIP3 versus $R_F$. It is found that $R_F = 1 \ k\Omega$ gives an optimized IIP3 of around 5 dBm. Note that IIP3 is optimized to 5 dBm by different methods in the work. The other method is discussed in detail in Section V-C. Therefore, we set $R_F$ of 1 kΩ to optimize IIP3 and also to provide a good balance between a low $S_{11}$, a flat gain, and a low NF.

$$F_{M1} = \frac{g_{m1}}{R_{m1}A_0A_1^2} \times \gamma \left| \frac{Z_y(2g_{m1}R_FZ_yZ_F + Z_S) - 2g_{m3}R_FZ_yZ_S}{Z_y(2g_{m1}R_FZ_yZ_F + Z_S) + Z_S} \right|^2$$

$$F_{M3} = \frac{g_{m3}}{R_{m3}A_0A_1^2} \times \gamma \left| \frac{Z_y(2g_{m1}R_FZ_yZ_S + Z_S + R_F)}{Z_y(2g_{m1}R_FZ_yZ_S + Z_S) + Z_S} \right|^2$$

$$F_{RD} = \frac{1}{R_D R_{S3} |A_0A_1|^2} \times \gamma \left| \frac{2g_{m1}g_{m5}R_DZ_yZ_S + 2Z_yZ_S(g_{m1} + g_{m3}) + 2g_{m1}R_FZ_yZ_S + R_F + Z_y + Z_S}{2g_{m1}g_{m5}R_DZ_yZ_S + 2Z_yZ_S(g_{m1} + g_{m3}) + 2g_{m1}R_FZ_yZ_S + R_F + Z_y + Z_S} \right|^2$$

$$F_{RF} = \frac{1}{R_F R_{S3} |A_0A_1|^2} \times \gamma \left| \frac{2g_{m1}g_{m5}R_DZ_yZ_S + 2Z_yZ_S(g_{m1} + g_{m3}) + 2g_{m1}R_FZ_yZ_S + R_F + Z_y + Z_S}{2g_{m1}g_{m5}R_DZ_yZ_S + 2Z_yZ_S(g_{m1} + g_{m3}) + 2g_{m1}R_FZ_yZ_S + R_F + Z_y + Z_S} \right|^2$$

Fig. 9. Complete schematic of the proposed wideband LNA.
B. Triple-Path NC

Fig. 11(a) depicts how to realize the conventional NC in CG-based NC LNA. The channel thermal noise of $M_2$ generates two off-phase noise voltages at the drain and source of $M_2$. The two noise voltages are both source-inverted and cancel each other due to their off-phase polarity. In the proposed LNA, we create an additional NC path with $M_1$ and $M_5$, as shown in Fig. 11(b). Part of $I_{n,M_2}$ flows through $M_1$ and $R_D$, and it produces a noise voltage at the drain of $M_1$, which has an opposite phase to the noise voltage at the drain of $M_2$. These two noise voltages are both source-inverted by pMOS and cancel each other at the output. Fig. 11(c) plots the overall NC scheme. The noise voltage generated by $I_{n,M_2}$ through $M_6$ (path A) is canceled by the noise through a conventional NC path, $M_3$ and $M_4$ (path B), as well as the noise through an extra NC path, $M_1$ and $M_5$ (path C) in the proposed design. On the other hand, signal voltages generated through all three paths (A, B, and C) have the same polarity.
and add up at the output. Fig. 12 shows the small-signal equivalent circuit used to study the NC mechanism in the proposed wideband LNA. We add an ac current source $I_{ac, M2}$ across the drain and source of $M2$ to emulate its channel thermal noise. We studied the effect of the additional NC path across 0–20 GHz by comparing the noise currents flowing through $M5$ and $M6$. Transfer functions $H_{n, A}$ and $H_{n, C}$ can be defined as

$$I_{n, M5} = H_{n, A} I_{ac, M2}$$
$$I_{n, M6} = H_{n, C} I_{ac, M2}$$

where $H_{n, A}$ and $H_{n, C}$ are given in (18a) and (18b), as shown at the bottom of this page, respectively. Herein, $I_{n, M5}$ and $I_{n, M6}$ are the noise currents flowing through $M5$ and $M6$, respectively. Furthermore, we define $H_{n, ac}$ as the sum of $H_{n, A}$ and $H_{n, C}$

$$H_{n, ac} = H_{n, A} + H_{n, C}.$$  

According to (18a) and (18b), $H_{n, A}$ and $H_{n, C}$ have opposite polarity, indicating that they can cancel each other. Fig. 13(a) displays the simulated and calculated $H_{n, A}$, $H_{n, C}$, and $H_{n, ac}$. We obtained the simulation results by setting $I_{ac, M2}$ to unity and plotting the drain current through $M5$ and $M6$. Noise current from the additional NC path (path C) cancels part of the noise current through $M6$ (path A). This is supported by the fact that $H_{n, ac}$ is lower than $H_{n, A}$ across the entire BW in both the calculation and the simulation. Similarly, noise from pMOS $M1$ is also canceled by the additional NC path (path A in this case), and the cancellation effect is also supported by both calculation and simulation [see Fig. 13(b)].

After noises through $M5$ and $M6$ cancel each other, the remaining noise is then canceled by the noise through $M1$, $M4$, and $RF$ (path B). Based on Fig. 12, the noise through path B can be expressed by

$$I_{n, M3} + I_{n, M4} + I_{n, RF} = H_{n, B} I_{ac, M2}$$

where $I_{n, M3}$, $I_{n, M4}$, and $I_{n, RF}$ are the noise currents flowing through $M3$, $M4$, and $RF$, respectively. Thereafter, the overall transfer function of $I_{n, M2}$ to the output becomes

$$H_{M2, overall} = H_{n, AC} + H_{n, B}$$

where $H_{n, B}$ is derived as (20b), shown at the bottom of this page. Furthermore, (21) is consistent with (10a). Fig. 14(a) and (b) shows the overall NC effect of noise caused by $M2$ and $M1$, respectively. Here, we can define the cancel ratio (CR) to evaluate the NC effect as

$$CR = 1 - \frac{|H_{n, AC} + H_{n, B}|}{|H_{n, AC}|}. \quad (22)$$

We obtain a good NC effect for both $M1$ and $M2$ at dc as CR is equal to 1. CR for $M1$ and $M2$ remains a minimum value of 0.5 and 0.43 over 20-GHz BW, respectively.

Fig. 15(a)–(c) plots a summary of the major noise contribution sources at 2, 10, and 20 GHz, respectively. $R_{DN}$ and $R_{TP}$ are the resistors connected to the drain of $M2$ and $M1$, respectively. Noise contributions from $M1$ and $M2$ are not dominating due to a high noise-canceling ratio at 2 and 10 GHz. By observing noise contributions from the source resistor, the simulated NF is 2.88 dB at 2 GHz, 3.58 dB at 10 GHz,
of the transconductance of the neutralization of the first and second derivative of the
C. Partially Distortion Canceling

We apply a partial distortion cancellation which focuses on the
neutralization of the first and second derivative of the transconductance of $M_5$ and $M_6$. A complementary pMOS and nMOS pair can have a low second-order and third-order distortion under specific bias conditions. Fig. 16 presents the small-signal equivalent circuit of Fig. 9 for IIP3 analysis. The study of the partial distortion cancellation focuses on the core of the LNA, which starts from $V_X$ to $V_Y$. $g_{m12}$ is the sum of $g_{m1}$ and $g_{m2}$, $g_{m34}$ is the sum of $g_{m3}$ and $g_{m4}$, and $g_{m56}$ is the sum of $g_{m5}$ and $g_{m6}$. We use an analysis approach similar to [13] and [15]. Distortions of the transistors are considered up to the third order. Applying Kirchhoff’s current law at node $V_1$ and node $V_Y$, we obtain

$$V_i = \frac{R_D}{2} \left( g_{m12} V_X + g_{m34} V_Y^2 + g_{m56} V_Y^3 \right)$$

$$V_X - V_Y = g_{m34} V_X + g_{m34} V_Y^2 + \frac{g_{m56} V_Y^3}{2} + \frac{V_Y}{Z_Y}$$

where $g'_{m1}$ and $g''_{m1}$ (i takes 12, 34, and 56) are the first and second derivatives of the transconductance of the complementary pairs $M_1$,$M_2$, $M_3$ and $M_4$, and $M_5$ and $M_6$, respectively. By solving (23), the relationship between $V_X$ and $V_Y$ becomes

$$V_Y = -\frac{Z_Y}{8(Z_Y+R_F)} \left( A_1 V_X + A_2 V_Y^2 + A_3 V_Y^3 \right)$$

where

$$A_1 = 4 R_D R_F g_{m12} g_{m56} + 8 R_F g_{m34} - 8$$

$$A_2 = R_D^2 R_F g_{m34} g_{m56}^2 + 2 R_D R_F g_{m12} g_{m34} + 4 R_F g_{m34}^2$$

$$A_3 = \frac{1}{6} R_D^3 R_F g_{m34}^2 g_{m56}^2 + R_D^3 R_F g_{m12} g_{m34}^2 + 4 R_D R_F g_{m34} g_{m56} + 4$$

Therefore, IIP3 of LNA’s core is written as

$$IIP3 = \sqrt{\frac{4}{3} \frac{A_1}{A_2}}$$

According to (24d) and (25), $g'_{m56}$ and $g''_{m56}$ are directly related to IIP3. Small values of $g_{m56}$ and $g_{m56}$ under the proper bias voltage can improve the linearity performance. Fig. 17(a)–(c) shows the simulated $g_{m56}$, $g'_{m56}$ and $g''_{m56}$ versus the gate bias voltage (i.e., $V_{B2} = V_{B3} = V_{B2}$). At around $V_{B2} = 0.86$ V, we obtain a good accumulation effect of $g_{m5}$

Fig. 14. Overall NC ratio of channel thermal noise of (a) nMOS $M_2$ and (b) pMOS $M_1$.

Fig. 15. Simulated relative noise contributions by individual components at (a) 2 GHz, (b) 10 GHz, and (c) 20 GHz.

Fig. 16. Small-signal equivalent circuit for IIP3 analysis.

and 4.11 dB at 20 GHz, respectively, showing an increase of 1.3 dB across the 20-GHz range.

Fig. 17. (a) Transconductance. (b) First-order derivatives of the transconductance of the complementary forward stage. (c) Second-order derivatives of the transconductance of the complementary forward stage. (d) IIP3 versus the gate bias voltage ($V_{B2}$).
Fig. 18. Simulation results versus frequency under different process corners and temperatures of (a) $S_{11}$, (b) $S_{21}$, and (c) NF. Simulation results versus $V_{B2}$ under different process corners and temperatures of (d) IIP3. Simulation results versus temperature under TT corner of (e) IIP3.

and $g_{m6}$, leading to a maximum total transconductance for $M_5$ and $M_6$ stages. Moreover, we achieve a good cancellation of $g_{m5}''$ and $g_{m6}''$, resulting in $g_{m56}''$ close to 0. Although $g_{m56}''$ is not exactly 0 at this bias voltage, a clear cancellation of $g_{m5}''$ and $g_{m6}''$ can be observed at $V_{B2} = 0.86$ V in Fig. 17(c). In Fig. 17(d), simulated IIP3 of the proposed wideband LNA reaches a maximum value of 5 dBm at $V_{B2} = 0.88$ V, which is consistent with the above analysis.

Detailed simulation results of our proposed wideband LNA will be plotted in Figs. 22–24. Note that the pre- and postsimulations denote the schematic and post-layout simulations with the parasitics, respectively. We observe a good consistency between the calculated and simulated results, indicating the validity of our analysis and design approach.

D. Corner and Monte-Carlo Simulation Results

To evaluate the robustness of our proposed wideband LNA, its performance under various process corners and temperatures is examined based on the post-layout simulation. Fig. 18(a) and (b) plots the simulated $S_{11}$ and $S_{21}$ under typical and worst-case scenarios, respectively. Under the worst-case SS corner and 125 °C, $S_{11} < -9.5$ dB is maintained, and the worst BW and dc gain are 18 GHz and 12 dB, respectively. Fig. 18(c) shows that NF deteriorates at high temperature and it is improved at low temperature, which is commonly expected. Fig. 18(d) presents the IIP3 against $V_{B2}$ under extreme corners and temperatures. It is worth to note that an optimal bias point exists under every condition. For the worst case, i.e., SS corner and -40 °C, the optimal IIP3 maintains at 2.5 dBm. A temperature-sweep simulation is also conducted to investigate the detailed impact of temperature on IIP3 and the result is plotted in Fig. 18(e). Across a range of -40–125 °C, IIP3 is maintained above 2.5 dBm and the highest IIP3 is 5.2 dBm at 40 °C.

Monte-Carlo (MC) simulation is conducted to further verify the effect of process variation and mismatch. Fig. 19(a) presents the low-frequency (i.e., around 1 GHz) gain distribution for MC simulation. The mean value is 13.36 dB and the standard deviation is 0.58 dB. MC results for IIP3 are plotted in Fig. 19(b), with a mean value and a standard deviation of 2.3 and 2.12 dB, respectively. It is observed that most of the points fall above 2 dBm. Yet, IIP3 varies in MC simulation results since this distortion cancellation mechanism is sensitive to bias condition. The deviations caused by temperature and process variations are within the acceptable range. MC results of NF at various frequencies are plotted in Fig. 19(c)–(e). The mean value of NF increases with frequency, which is consistent with results in Fig. 10(c). Standard deviation is maintained <0.2 dB from 2 to 20 GHz.

VI. MEASUREMENT RESULTS

Fig. 20 shows the die photo of the proposed wideband LNA implemented in 65-nm CMOS occupying a compact active area of $0.31 \times 0.31$ mm$^2$. Herein, the dimensions (coil only) of $L_m$, $L_o$, and $L_b$ are 76 $\mu$m $\times$ 76 $\mu$m, 120 $\mu$m $\times$ 20 $\mu$m, and 125 $\mu$m $\times$ 125 $\mu$m, respectively. Their quality factors are 8.6, 8, and 7, respectively. All of the three single-ended inductors consist of multiple turns and three metal layers. The top metal is aluminum, middle layer is copper, and bottom metal is aluminum as well. The prototype draws 12.6 mA
Fig. 19. Histogram of Monte-Carlo simulation results of (a) gain at 1 GHz, (b) IIP3 at 5 GHz, (c) NF at 2 GHz, (d) NF at 10 GHz, and (e) NF at 20 GHz.

Fig. 20. Die photograph of the fabricated wideband LNA.

from a supply voltage of 1.6 V, consuming a total power of 20.1 mW.

As shown in Fig. 21, we performed the normal S-parameter measurement using an Agilent PNA-X Vector Network Analyzer (N5245A). The NF measurement was conducted on probe-station using Agilent PNA-X N5245A. Note that the NF measurement option (option 029) needs to be installed in N5245A to measure NF. The cable setup is the same as the normal S-parameter measurement. The basic measurement steps are: 1) setup a noise channel, such as noise frequency, test frequency, and test power, on PNA; 2) execute a noise calibration using E-cal module and noise source (346 C); and 3) measure NF which is just the same way as the normal S-parameter measurement.

Fig. 22 compares the calculated, simulated, and measured results of $S_{11}$, $S_{21}$, and NF of the proposed wideband LNA. $S_{11}$ is below $-10 \text{ dB}$ up to 23 GHz [see Fig. 22(a)]. $S_{11}$ shows a dip at around 19 GHz, indicating the effect of the π network. In Fig. 22(b), the peak of $S_{21}$ is 12.8 dB with a 3-dB BW of 19 GHz, from 1 to 20 GHz. Across the above frequency range, the in-band gain variation is 2.8 dB; nevertheless, its variation is 1.9 dB in post-layout simulation. Measured $\text{NF}_{\text{min}}$
and \( \text{NF}_{\text{max}} \) are 3.3 dB at 3.5 GHz and 5.3 dB at 13.5 GHz, illustrated in Fig. 22(c), respectively. In-band variation of NF is only 2 dB from 1 to 20 GHz, which is competitive with the state of the art. The calculated results based on (4), (9), and (16) derived in Section III are consistent with the simulated and measured results. Fig. 23(a) shows that the measured IIP3 is 5.8 dBm, when two-tone signals with equal power levels at 10 and 10.1 GHz are applied to the prototype. Fig. 23(b) shows that the measured IIP3 at different center frequencies (2, 5, 10, 15, and 20 GHz) with space \( \Delta f = 100 \) MHz is always larger than 0 dBm. Measured \( P_{1\text{dB}} \) is also plotted with a range of \(-13\) to \(-8\) dBm across the BW. The difference between IIP3 and \( P_{1\text{dB}} \) is slightly larger than the conventional 10 dB in theory, due to the above-mentioned IIP3 improvement technique, which does not necessarily improve \( P_{1\text{dB}} \). The results also show a good linearity performance across a wide range of frequencies. The group delay based on the measured S-parameter is plotted in Fig. 24. It shows a low minimum group delay of 26 ps at 6.5 GHz and a maximum group delay of 75 ps at 18 GHz.

Table II benchmarks the performance of our proposed wideband LNA with the prior works. The prototyped wideband LNA has an NF flatness of 0.1 dB/GHz, which is competitive with other previous wideband LNAs in Table II. NF flatness is characterized as \( (\text{NF}_{\text{max}} - \text{NF}_{\text{min}})/\text{BW} \), which represents how fast NF increases over a certain range of frequency. Although Chang and Shawn [6] reported a super NF flatness, it needs a larger area and an off-chip bias-T as an RF choke at the output, which is usually infeasible in a full receiver integration. This work also has a moderately low NF, better IIP3, and more compact area compared to other LNAs whose
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<th>Freq. Range (GHz)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>NF Flat. (dB/\text{GHz})</th>
<th>IIP3 (dBm)</th>
<th>Power (mW)</th>
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Upper $f_{\text{sat}}$ larger than 10 GHz

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NC technique used

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<th>IIP3 (dBm)</th>
<th>Power (mW)</th>
<th>Area (mm$^2$)</th>
<th>FOM$_1$</th>
<th>FOM$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[29] MWCL’17</td>
<td>SiGe 130nm</td>
<td>0.3 – 15</td>
<td>37.3</td>
<td>1.8 – 2.2</td>
<td>0.03</td>
<td>-27.3$^a$</td>
<td>52</td>
<td>0.46</td>
<td>-22.5</td>
</tr>
<tr>
<td>[30] TMTT’11</td>
<td>GaAs 500nm</td>
<td>0.5 – 43.5</td>
<td>8.5</td>
<td>4.2 – 22</td>
<td>0.41</td>
<td>9.5$^a$</td>
<td>225</td>
<td>2</td>
<td>8.9</td>
</tr>
</tbody>
</table>

Non-CMOS

<table>
<thead>
<tr>
<th>Tech.</th>
<th>Freq. Range (GHz)</th>
<th>Gain (dB)</th>
<th>NF (dB)</th>
<th>NF Flat. (dB/\text{GHz})</th>
<th>IIP3 (dBm)</th>
<th>Power (mW)</th>
<th>Area (mm$^2$)</th>
<th>FOM$_1$</th>
<th>FOM$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[33] VLSI’15</td>
<td>90nm</td>
<td>0.1 – 7.0</td>
<td>12</td>
<td>5.5 – 6.5</td>
<td>0.14</td>
<td>-9</td>
<td>0.75</td>
<td>0.23</td>
<td>5.2</td>
</tr>
<tr>
<td>[34] TCASI’18</td>
<td>130nm</td>
<td>0.7 – 4.6</td>
<td>10.8</td>
<td>3.5 – 4.5</td>
<td>0.26</td>
<td>5</td>
<td>6.16</td>
<td>0.18</td>
<td>14.9</td>
</tr>
<tr>
<td>[38] TMTT’08</td>
<td>90nm</td>
<td>0.2 – 9.0</td>
<td>10</td>
<td>4.2 – 7.8</td>
<td>0.41</td>
<td>-8</td>
<td>20</td>
<td>0.066</td>
<td>-17.4</td>
</tr>
<tr>
<td>[39] TMTT’16</td>
<td>90nm</td>
<td>0.1 – 2.2</td>
<td>12.3</td>
<td>4.9 – 6.0</td>
<td>0.52</td>
<td>-9.5</td>
<td>0.4</td>
<td>0.005</td>
<td>1.3</td>
</tr>
</tbody>
</table>

$^a$ Calculated from OIP3, $^A$ Calculated from $P_{\text{dd}}$. 

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fiers, it seems that the NC technique introduces some extra of the art. The achieved FOM 1 of 22.7 GHz for the wideband LNA has either very high gain [29] or very wide BW [30]. However, their FOM is inferior to our work due to their poor linearity or high power consumption. In Table II, two types of FOMs are employed to evaluate the overall performance of the wideband LNA

\[
FOM_1 = 20 \log_{10} \left( \frac{\text{IIP}_3 \text{[mW]} \times \text{Gain[lin]} \times \text{BW[GHz]}}{P_{dc} \text{[mW]} \times (\text{NF}_{\text{min}} \text{[dB]} - 1)} \right)
\]  

\[
FOM_2 = 20 \log_{10} \left( \frac{\text{IIP}_3 \text{[mW]} \times \text{Gain[lin]} \times \text{BW[GHz]}}{P_{dc} \text{[mW]} \times \text{NF Flatness[dB/GHz]}} \right) \]

FOM$_1$ in [8] and [12] uses the lowest NF while FOM$_2$ takes NF flatness into account. Also, Guo et al. [15] and Im [31] employ linearity enhancement techniques and achieve better IIP3 than our work; however, the proposed wideband LNA achieves a very wide BW, which is more than 10× wider than the BW of [15] and [31]. To summarize Table II, our proposed wideband LNA is a very promising topology due to very wide BW, low-and-flat NF, high linearity, and better overall FOMs.

VII. CONCLUSION AND BRIEF DISCUSSION ON NC TECHNIQUE

This article reported a novel wideband LNA architecture that targets high linearity and broadband amplification. The effects of the dual-complementary topology, feedback resistor, and triple-path noise cancellation have been analyzed in detail. Realized in 65-nm CMOS, the prototype LNA measures a BW of 19 GHz, an NF of 3.3 dB at 3.5 GHz, and an IIP3 of 5.8 dBm at ~10 GHz while achieving a very compact die area of 0.096 mm$^2$. The measurement agrees well with the calculation and simulation. The achieved FOM$_1$ of 22.7 GHz and FOM$_2$ of 43.8 GHz are favorably comparable to the state of the art.

Due to the introduction of the additional auxiliary amplifiers, it seems that the NC technique introduces some extra noise. Regarding recent works [13]–[15] and our work, the additional circuitry is not only used to cancel noise from input matching transistors but also utilized to improve IIP3. The feed-forward NC technique is also employed in radio frequency receiver designs [35]–[37]. Murphy et al. [35] and Wu et al. [36] implemented switches to turn on/off the NC function and so as to obtain the improvement of NF, with the help of the NC technique. By recalling Fig. 18, we can observe that the temperature shows a greater impact on NF, while the process-corner variations are slightly affecting NF performance. As shown in Fig. 19, MC simulations show that the standard deviation of NF is <0.2 dB, ranging from 2 to 20 GHz. However, to further control noise cancellation, especially its dependence on the temperature, digital calibration could be implemented into the circuit.

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