An Inverse-Class-F CMOS Oscillator With Intrinsic-High-Q First Harmonic and Second Harmonic Resonances

Chee Cheow Lim, *Student Member, IEEE*, Harikrishnan Ramiah, *Senior Member, IEEE*, Jun Yin, *Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— This paper details the theory and implementation of an inverse-class-F (class-F^{-1}) CMOS oscillator. It features: 1) a single-ended PMOS-NMOS-complementary architecture to generate the differential outputs and 2) a transformer-based two-port resonator to boost the drain-to-gate voltage gain (A_V) while creating two intrinsic-high-Q impedance peaks at the fundamental (f_{LO}) and double ($2f_{LO}$) oscillation frequencies. The enlarged second harmonic voltage extends the flat span in which the impulse sensitivity function (ISF) is minimum, and the amplified gate voltage swing reduces the current commutation time, thereby lowering the $-g_m$ transistor's noise-to-phase noise (PN) conversion. Prototyped in 65-nm CMOS, the class-F^{-1} oscillator at 4 GHz exhibits a PN of –144.8 dBc/Hz at a 10-MHz offset, while offering a tuning range of 3.5–4.5 GHz. The corresponding figure of merit (FoM) is 196.1 dBc/Hz, and the die area is 0.14 mm^2.**

***Index Terms*— Figure of merit (FoM), flicker noise upconversion, inverse-class-F (class-F^{-1}) oscillator, phase noise (PN), second harmonic resonance, voltage-biased oscillator.**

I. Introduction

THE trend toward denser modulation schemes in imminent RF communication systems has continuously driven the development of high-purity *LC* oscillators with low power consumption [1]–[11]. To gain insight into their performance limits, their figure of merit (FoM) that normalizes the phase noise (PN) to power, offset and carrier frequencies, can be re-expressed in terms of the quality factor (Q) of the *LC* tank, power efficiency η, and total effective noise factor ΣF [12] as

$$\text{FoM} = 10\log_{10}\left(\frac{Q^2\eta}{\sum F}\cdot\frac{2}{10^3 kT}\right) \quad (1)$$

where ΣF is the total effective noise normalized to the tank stationary noise. Considering the oscillation amplitude V_P and tank impedance R_P, we can express $\eta = P_{RF}/P_{dc}$, with $P_{RF} = V_P^2/2R_P$. Accordingly, a high V_P is desired to improve the PN performance. For a typical current-biased class-B oscillator, its current source contributes a significant amount of noise (in both $1/f^2$ and $1/f^3$ PN regions) [5], [13] and limits V_P. For this reason, the voltage-biased oscillator without the tail current source is desired, but its $-g_m$ transistors can enter into the deep-triode region under a large V_P, raising their noise contribution substantially [14], [15]. The second harmonic filtering [1] can be applied to suppress such noise contribution. By adding a tail tank resonating at the doubled LO frequency ($2f_{LO}$), as shown in Fig. 1, the tank loading effect can be alleviated even when the $-g_m$ transistors enter into the deep-triode region, since there is a high tail impedance Z_{TAIL} in series. Q (Q_{TAIL}) of the tail tank should be high enough to maximize Z_{TAIL}, such that the noise contribution of the $-g_m$ transistors can be minimized, ideally leading to $\Sigma F = 1+\gamma$ [1], [16], where γ is the channel noise coefficient of the MOS transistor.

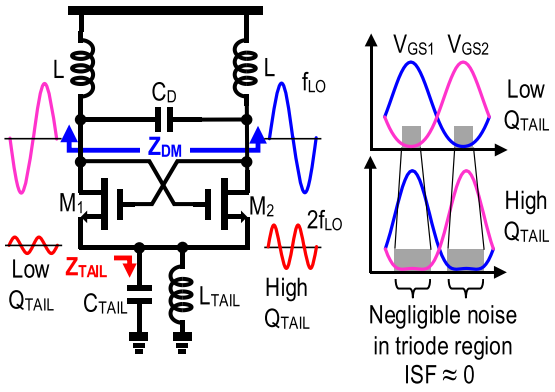

Fig. 1. CM-resonance-based *LC* oscillator with an extra tail tank $L_{TAIL}C_{TAIL}$.

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C. C. Lim is with the Department of Electrical Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia, and also with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China.

H. Ramiah is with the Department of Electrical Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia.

J. Yin is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: junyin@umac.mo).

P.-I. Mak is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, and also with the Faculty of Science and Technology, Department of Electrical and Computer Engineering, University of Macau, Macao, China.

R. P. Martins is with the State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, also with the Faculty of Science and Technology, Department of Electrical and Computer Engineering, University of Macau, Macao, China, and on leave from the Instituto Superior Técnico, University of Lisbon, Lisbon, Portugal.

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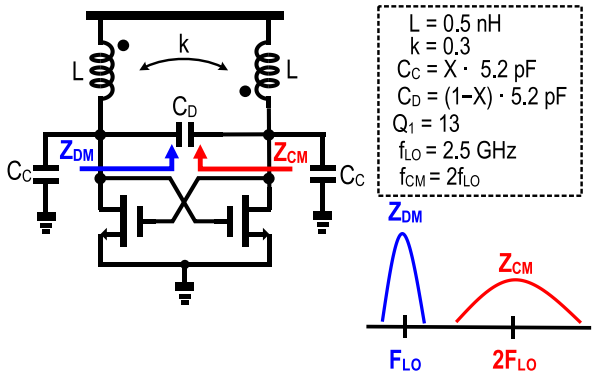

Fig. 2. *LC* oscillator with implicit CM resonance. (Q_1 represnts the tank Q-factor at f_{LO}.)

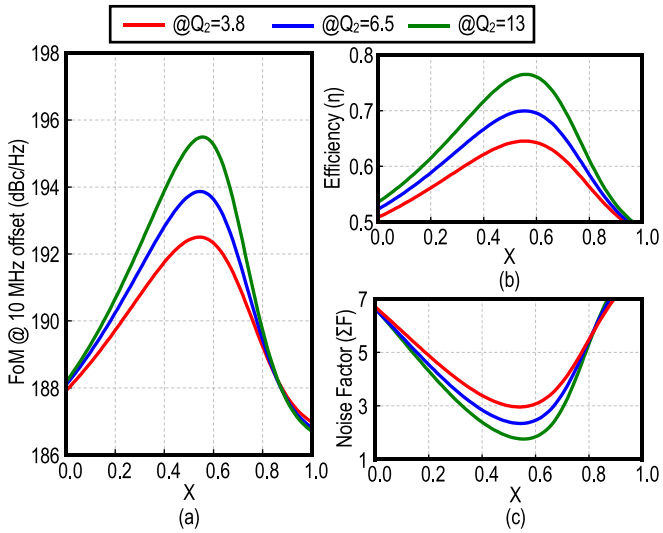

Fig. 3. Simulated (a) FoM at 10-MHz offset, (b) efficiency, and (c) noise factor against $X = C_C/(C_C + C_D)$ at different Q_2 for the *LC* oscillator with implicit CM resonance in Fig. 2.

From the viewpoint of the impulse sensitivity function (ISF) [17], when a second harmonic voltage is generated, the gate-to-source voltage of the $-g_m$ transistors is reshaped. Ideally, there is no noise upconversion in the shaded area, as the output phase is insensitive to the channel noise (modeled as current impulse). A high Q_{TAIL} extends such a shaded area by enlarging the second harmonic voltage, but at the cost of die area to accommodate the extra tail inductor.

Recently, Shahmohammadi *et al.* [10] and Murphy *et al.* [11] revealed that the implicit common-mode (CM) resonance of the *LC* tank itself can be placed at $2f_{LO}$ by properly choosing the mutual coupling coefficient k of the differential inductor and the ratio between the single-ended (C_C) and differential capacitances (C_D), as exhibited in Fig. 2. However, the best FoM reported in [18] stays ~2.5 dB away from the explicit design [1] (Fig. 1). To gain more insight, we sweep the capacitance factor $X = C_C/(C_C + C_D)$ from 0 to 1, i.e., the tank capacitance from fully differential to fully CM. It shows that a high tank Q-factor at $2f_{LO}$ (Q_2) is demanded to improve η and $\sum F$, as well as the FoM, like Fig. 3 presents. Unfortunately, for differential spiral inductors

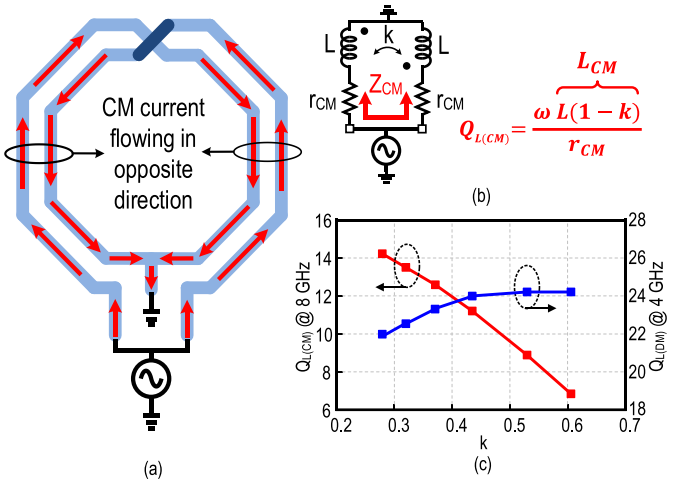

Fig. 4. (a) CM current excitation. (b) Simple model of CM current excitation. (c) $Q_{L(CM)}$ (left) and $Q_{L(DM)}$ (right) against k from EM simulation.

as illustrated in Fig. 4(a), $Q_{L(CM)}$ is relatively low due to unavoidable magnetic flux cancellation. The CM current in the adjacent windings flows in the opposite direction, raising the ac resistance and reducing the inductance at CM oscillation [Fig. 4(b)] [10]. Such electromagnetic (EM) simulations maintain the inner diameter and sweep the spacing between the two turns to change k and $Q_{L(CM)}$, while keeping a relatively constant L. As shown in Fig. 4(c), a lower k yields a higher $Q_{L(CM)}$ at the cost of chip area. Hence, the required large C_D-to-C_C ratio can hardly be realized at high frequency when all the capacitor banks are off [11]. Moreover, the Q-factor of the single-ended switched-capacitor arrays (SCAs) is inherently lower than the differential SCAs for achieving the same tuning range [19], which further degrades Q_2.

Seeking to circumvent the aforesaid issues, this paper proposes an inverse-class-F (class-F^{-1}) CMOS oscillator [20]. Without resorting from any explicit or implicit CM resonant techniques, we obtain concurrently intrinsic-high-Q first harmonic and second harmonic resonances via a transformer-based two-port resonator. Together with the drain-to-gate voltage gain provided by the transformer, the noise contribution of the $-g_m$ transistors can be significantly suppressed.

This paper is organized as follows. Section II presents the design insight of the transformer-based tank to arrive at the class-F^{-1} operation, followed by the analysis of the circuit's noise-to-PN conversion mechanisms using the ISF theory in Section III. The measurement results are summarized in Section IV, and finally, the conclusion is drawn in Section V.

II. Class-F^{-1} Oscillator Operation

A. Concept of Class-F^{-1} Operation

Fig. 5(a) shows a single-ended NMOS-only oscillator with a 1:n transformer ($n > 1$), where n is the transformer turn ratio defined by $n = k_m \times \sqrt{(L_S/L_P)}$. As the transformer-based tank can provide two resonant peaks, it is possible to map them to f_{LO} and $2f_{LO}$, respectively. Furthermore, as Fig. 5(b) illustrates, when the drain current I_D containing the first

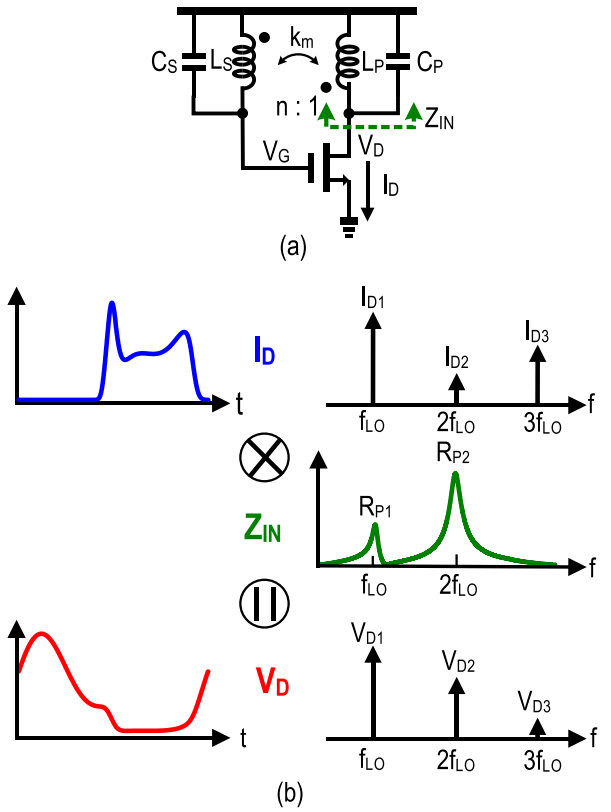

Fig. 5. (a) Preliminary class-F^{-1} oscillator with a single-ended output. (b) Its current and voltage waveforms under the class-F^{-1} operation.

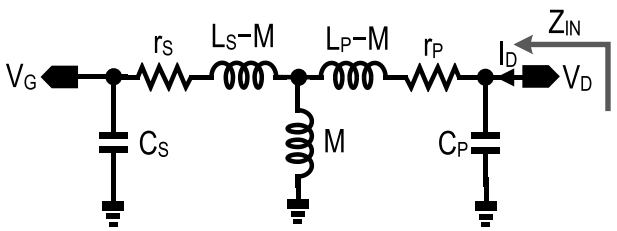

Fig. 6. Equivalent circuit of the transformer-based tank.

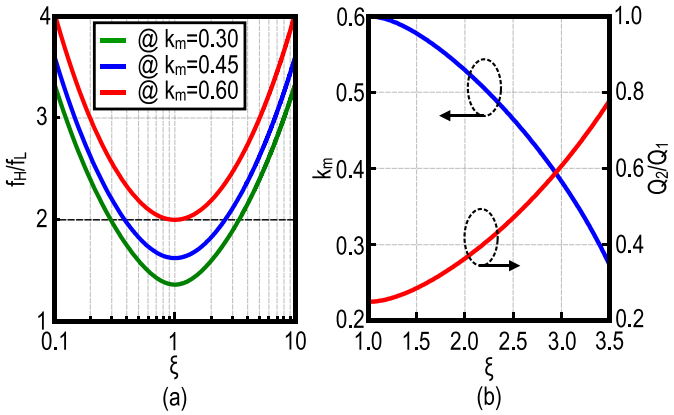

Fig. 7. (a) f_H/f_L and (b) k_m (left) and Q_2/Q_1 (right) as a function of ξ.

three harmonics is multiplied with the tank input impedance $Z_{IN} = V_D/I_D$, large first (V_{D1}) and second (V_{D2}) harmonic voltages are generated, justifying its class-F^{-1} operation [21] (i.e., squarelike I_D and half-sinusoidal V_D).

Note that the transformer tank has been widely used in the oscillator design for different purposes. In [22] and [23], the dual-resonance frequencies of the transformer tank are utilized to extend the frequency tuning range. When configured as a one-port resonator, the transformer tank does not provide extra advantages on the PN and FoM performance if the high resonant frequency is not properly tuned at the oscillator's harmonic frequencies [24]. If configured as a two-port resonator, the voltage gain from the drain node to the gate node of the $-g_m$ transistors helps to suppress the PN contribution from the transistor [4], [24]. In [6], the class-F oscillator uses the transformer-based tank to shape the drain waveform by mapping the high-band resonance frequency to $3f_{LO}$, which can reduce the noise contribution from the $-g_m$ transistors. In this paper, the single-ended oscillator architecture makes it possible to map the high-band resonance frequency to $2f_{LO}$, which would be more effective to suppress the transistor noise as will be detailed later in Section III.

B. Design Considerations of Transformer-Based Tank

Fig. 6 depicts a simplified model of the transformer-based tank in Fig. 5 [22], in which the following analysis assumes that the $-g_m$ transistors work as a transconductor that exhibits a large output impedance and does not affect the impedances of the transformer tank. The mutual inductance induced by the magnetic coupling is $M = -k_m\sqrt{L_P L_S}$. The low (f_L) and high (f_H) resonant frequencies are given by

$$f^2_{L(H)} = \frac{1+\xi \mp \sqrt{(1+\xi)^2 - 4\xi\left(1-k_m^2\right)}}{2L_S C_S\left(1-k_m^2\right)} \tag{2}$$

where ξ is a ratiometric given by $\xi = L_S C_S / L_P C_P$. Fig. 7(a) plots the ratio of f_H/f_L against ξ for different k_m. To map f_L to f_{LO} and f_H to $2f_{LO}$ (i.e., $f_H/f_L = 2$), we arrive at

$$16\xi^2 + \left(100k_m^2 - 68\right)\xi + 16 = 0 \tag{3}$$

where $k_m \leq 0.6$ is the necessary condition for satisfying the class-F^{-1} operation. Following the analysis in [6], we only consider $\xi > 1$ since it can maximize the high-band impedance R_{P2}. Fig. 7(b) shows, using (3), the variation of k_m against ξ, suggesting that a high ξ requires a low k_m in order to ensure $f_H/f_L = 2$. Next, the input impedance Z_{IN} at f_{LO} and $2f_{LO}$ can be expressed as

$$R_{P1} = \frac{8}{25}\cdot\frac{Q_P L_P}{\sqrt{L_S C_S}}\cdot\frac{\sqrt{5\xi(1+\xi)^3}\cdot(4-\xi)}{4\xi^2\left(\frac{Q_P}{Q_S}\right) - \xi\left(1+\frac{Q_P}{Q_S}\right)+4} \tag{4}$$

$$R_{P2} = \frac{1}{25}\cdot\frac{Q_P L_P}{\sqrt{L_S C_S}}\cdot\frac{\sqrt{5\xi(1+\xi)^3}\cdot(1-4\xi)}{\xi^2\left(\frac{Q_P}{Q_S}\right) - 4\xi\left(1+\frac{Q_P}{Q_S}\right)+1} \tag{5}$$

where Q_P and Q_S are the intrinsic Q of the primary and secondary coils, respectively. Both impedances are a strong function of $Q_{P(S)}$ and ξ. Fig. 8(a) plots R_{P1} and R_{P2} for different L_P, revealing that a higher ξ will reduce R_{P1} and raise R_{P2}, favoring the PN performance.

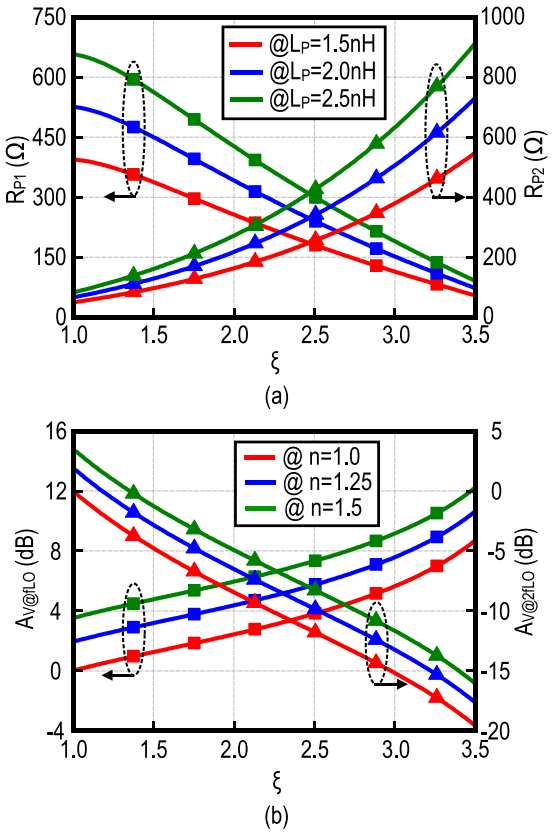

Fig. 8. (a) R_{P1} (left) and R_{P2} (right) and (b) transformer voltage gain at first harmonic (left) and second harmonic (right) as a function of ξ ($Q_P = Q_S = 13.5$ and $f_S = 1/(2\pi\sqrt{L_S C_S}) = 3.2$ GHz).

The Q-factor of the transformer-based tank at f_{LO} (Q_1) and $2f_{LO}$ (Q_2) is evaluated by

$$Q_{1(2)} = \frac{f}{2}\left|\frac{d}{df}\angle Z_{21}\right|_{f=f_{LO}(2f_{LO})} \tag{6}$$

where $Z_{21} = V_G/I_D$ is

$$Z_{21}(f) = \frac{2\pi f \xi Q_P L_1 k_m n}{-\left(\frac{f}{f_S}\right)^4 \cdot \left(1+\frac{Q_P}{Q_S}\right) + \left(\frac{f}{f_S}\right)^2 \cdot \left(1+\xi\frac{Q_P}{Q_S}\right)}. \tag{7}$$

According to (2), (3), (6), and (7), the ratio of Q_2/Q_1 can be obtained as

$$\frac{Q_2}{Q_1} = -\frac{1}{4}\cdot\frac{4\xi^2 - \xi\left(1+\frac{Q_S}{Q_P}\right) + 4\frac{Q_S}{Q_P}}{\xi^2 - 4\xi\left(1+\frac{Q_S}{Q_P}\right) + \frac{Q_S}{Q_P}}. \tag{8}$$

Fig. 7(b) plots (8), suggesting that maximizing Q_2 is necessary by increasing ξ, which is beneficial for noise suppression [9], [14].

Since the drain-to-gate voltage gain of the transformer is defined by $A_V = V_G/V_D$, by using (2) and (3), A_V of the first harmonic ($A_{V@f_{LO}}$) and the second harmonic ($A_{V@2f_{LO}}$) voltages is a function of ξ and n expressed, respectively, as

$$A_{V@f_{LO}}(\xi) = \frac{n\sqrt{-4\xi^2+17\xi-4}}{\sqrt{\xi}\cdot(4-\xi)} \tag{9}$$

$$A_{V@2f_{LO}}(\xi) = \frac{n\sqrt{-4\xi^2+17\xi-4}}{\sqrt{\xi}\cdot(4\xi-1)} \tag{10}$$

Fig. 8(b) plots (9) and (10) in decibel against ξ, suggesting that $A_{V@f_{LO}}$ goes up with ξ. $A_{V@2f_{LO}}$ is smaller than 1 for $\xi > 1.4$ and drops quickly as ξ increases. Since the first harmonic drain voltage V_{D1} is amplified at the gate while the second harmonic voltage V_{D2} is attenuated by the limited transformer's resonant bandwidth, the gate voltage would predominantly contain the first harmonic component only. Thus, only the first harmonic voltage needs to be considered for reliability. Yet, $-g_m$ transistors are vulnerable to breakdown if $A_{V@f_{LO}}$ is excessively large. Another design tradeoff is that, if f_{LO} is fixed with large ξ and n, it demands a tiny C_P that is hard to be realized in practice.

In summary, a small ξ favors low-power applications, but if a minimum PN is necessary, ξ should be maximized providing that the $-g_m$ transistors still operate within the reliability limit. In this paper, we choose $\xi = 3$, which corresponds to $k_m = 0.38$. EM simulation shows that the intrinsic Q s for the primary (L_P) and secondary (L_S) coils are 19 and 17, respectively. $Q_P = 19$ and $Q_S = 17$ at 4 GHz. The Q-factor of the switched capacitors mainly depends on the tuning range. By choosing the Q-factors of C_P and C_S as 47 and 65, respectively, and absorbing the loss of capacitors into the transformer coils for simplicity, we can reasonably assume $Q_P = Q_S = 13.5$, which results in tank Q-factors $Q_1 = 14$ at f_{LO} and $Q_2 = 9.3$ at $2f_{LO}$, respectively.[1]

Although $|Z_{in}|$ has two peaks, i.e., R_{P1} and R_{P2}, at both f_{LO} and $2f_{LO}$ and $R_{P2} > R_{P1}$, the class-F^{-1} oscillator can only oscillate at the frequency f_{LO} since the transformer is configured as a two-port resonator with an inverted magnetic coupling from drain-to-gate nodes, so that the loop gain fulfills the phase condition only at the low frequency f_{LO}, forming a positive feedback around the loop [23], [25].

C. Class-F^{-1} Oscillator With Differential Outputs

To generate the differential outputs, we stack the PMOS- and NMOS-based class-F^{-1} oscillators and merge their respective transformer-based tanks together as shown in Fig. 9(a). Such transistor stacking resembles the current reuse oscillator topology that was first proposed in [26]. However, it only achieves an FoM of 189.3 dBc/Hz since there is no second harmonic resonance to block the transistor noise located at around $2f_{LO}$. The center tap of the two coils is shorted to provide self-biasing at $V_{DD}/2$, given that M_P and M_N are sized such that $g_{m,p} = g_{m,n}$. This self-biased scheme eliminates the extra bias circuit and its noise contribution.

Fig. 9(b) plots the corresponding voltage waveforms. Although the drain voltages V_{DN} and V_{DP} have a significant amount of second harmonic component (i.e., $V_{D2}/V_{D1} = 0.4$), the gate voltage only predominantly contains the first harmonic component only as expected. The peak-to-peak gate voltages V_{GP} and V_{GN} are ~1.45 V. From simulations, V_{GD}, V_{GS}, and V_{DS} of the two transistors are within the breakdown limits across all the process corners. Even though the two transistors

[1] $Q1$ and $Q2$ are slightly different from [20] due to a calculation mistake in that work.

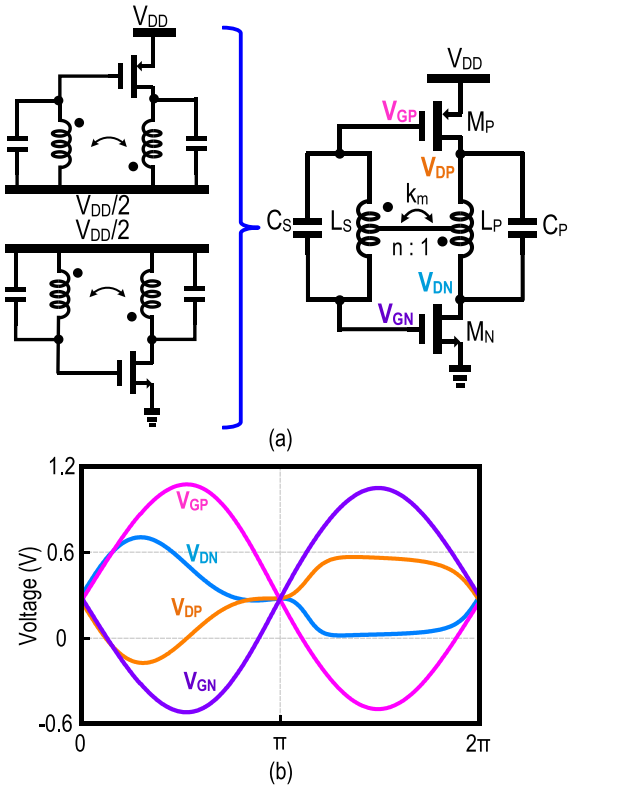

Fig. 9. (a) Class-F^{-1} oscillator with a PMOS-NMOS-complementary topology to generate the differential outputs. (b) Its corresponding voltage waveforms.

enter into the deep-triode region, their PN contributions are very low as elaborated next.

III. Phase Noise and Frequency Pushing Analysis

A. Thermal Noise Upconversion

According to Hajimiri's linear time-variant model [17], the PN of an RF oscillator at an offset frequency Δf is [2], [6]

$$L(\Delta f) = 10\log_{10}\left[\frac{\sum_{\rm i} N_{\rm L,i}}{2q_{\rm max}^2 \Delta f^2}\right] \tag{11}$$

where $q_{\rm max}$ is the maximum charge swing at output and $\sum_{\rm i} N_{\rm L,i}$ is the total effective noise produced by the ith devices, with

$$N_{\rm L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_{\rm i}^2(\theta)\overline{i_{n,i}^2(\theta)}d\theta \tag{12}$$

where $\overline{i_{n,i}^2(\theta)}$ is the white current noise power spectral density (PSD) of the ith device and $\Gamma_{\rm i}(\theta)$ is the corresponding ISF. To study the PN mechanism of the class-F^{-1} oscillator, it is convenient to normalize (12) to the tank stationary noise following the definition in the introduction earlier, which is

$$\sum F = \sum_i \frac{R_{\rm P}}{4KT}\cdot\frac{1}{2\pi}\int_0^{2\pi}\Gamma_{\rm i}^2(\theta)\cdot\overline{i_{n,i}^2(\theta)}d\theta. \tag{13}$$

With it, we can model, as in Fig. 10, the noise sources of the class-F^{-1} oscillator. $R_{\rm P}$ models the transformer tank loss, while $G_{\rm ds,n(p)}$ and $g_{\rm m,n(p)}$ represent the channel conductance and transconductance of the NMOS and PMOS transistors,

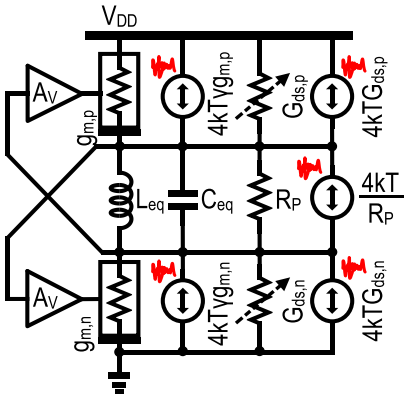

Fig. 10. Noise sources of the Class-F^{-1} oscillator.

respectively. Furthermore, even if the channel is the only physical noise source of the transistor, due to the large signal swing at the gate and drain nodes, the transistors will transit between the saturation and triode regions when turned on. For this reason, we artificially split the transistor current noise PSD into $\overline{i_{\rm n,GM}^2} = 4kT\gamma g_{\rm m}(\theta)$ and $\overline{i_{\rm n,GDS}^2} = 4kTG_{\rm ds}(\theta)$, representing the noise PSD due to $G_{\rm m}$ and $G_{\rm ds}$, respectively [15]. As such, we can evaluate ΣF, consisting of the effective noise factor of the tank ($F_{\rm TANK}$), $g_{\rm m}$ ($F_{\rm GM}$), and $G_{\rm ds}$ ($F_{\rm GDS}$), respectively, by substituting $\overline{i_{n,\rm TANK}^2} = 4kT/R_{\rm P}$, $\overline{i_{n,\rm MOS(G_M)}^2}$, and $\overline{i_{n,\rm MOS(G_{DS})}^2}$ into (13) [6]. Using (12) and (13), (11) becomes

$$L(\Delta f) = 10\log_{10}\left[\frac{KT}{2Q_1^2}\cdot\frac{R_{\rm P1}}{V_{\rm P}^2}\cdot\left(\frac{f_{\rm LO}}{\Delta f}\right)^2\sum F\right]. \tag{14}$$

Therefore, we can compare the PN upconversion mechanism between the class-F^{-1} and implicit CM resonance topologies (Fig. 2). We keep the same Q_1 (= 14), $R_{\rm P1}$ (= 250 Ω), and $V_{\rm DD}$ (= 0.6 V) for both the class-F^{-1} and the implicit CM resonance topologies. Under these constraints, ΣF and η are the only parameters determining the FoM. For class F^{-1}, we choose $k_{\rm m} = 0.38$ and $\xi = 3$, which gives $Q_2 = 9.3$. For an implicit CM resonance, $k = 0.33$ is chosen for design practicality, resulting in $Q_2 = 6.3$. Fig. 11(a)–(d) shows the drain, gate voltage and current waveforms of these two topologies.

Fig. 11(e) presents the simulated tank ISF ($\Gamma_{\rm T}$). $\Gamma_{\rm T}$ is minimum at the flat span of the drain voltage. However, Class-F^{-1} has a much wider span for a minimum ISF. This is due to a larger $V_{\rm D2}$ (generated by a higher $R_{\rm P2}$ and Q_2), which shapes the drain voltage to a wider flat region, when compared with the implicit CM resonance where the transistor is off between π to 2π. For the PN contribution from the tank, the $F_{\rm TANK}$ of the Class-F^{-1} topology is only slightly less [Fig. 11(f)] since the tank noise source, i.e., 4 $kTR_{\rm P}$, is white noise, and the larger span for minimum $\Gamma_{\rm T}$ does not aid significant noise reduction.

For the noise contribution from $G_{\rm ds}$, the flat span of the low transistor ISF $\Gamma_{\rm MOS}$ [Fig. 11(g)] and $\Gamma_{\rm MOS}^2$ [Fig. 11(h)] is wide enough to cover the region where $G_{\rm DS}$ starts to increase abruptly, although $G_{\rm DS}$ of class-F^{-1} is larger than that of the implicit CM resonance topology due to the amplified

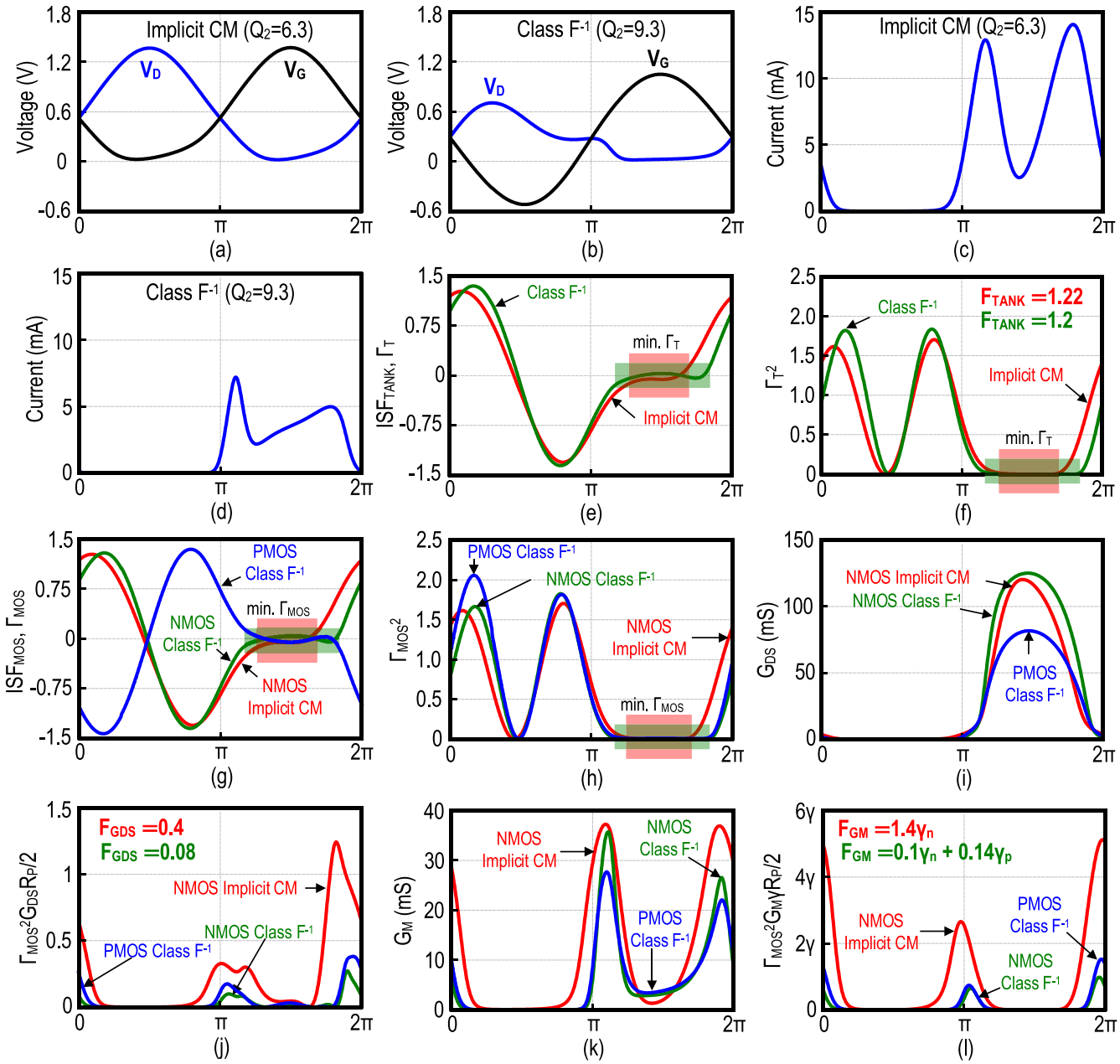

Fig. 11. Comparison of circuit-to-PN conversion mechanisms between the implicit CM resonance and class-F^{-1} oscillators in Fig. 2. (a) Gate and drain voltages of the implicit CM resonance oscillator. (b) Gate and drain voltages of the class-F^{-1} oscillator. (c) Drain current of implicit CM resonance oscillator. (d) Drain current of class-F^{-1} oscillator. (e) Simulated tank ISF ($\Gamma_{\rm T}$). (f) PN contribution from the tank. (g) Simulated transistor ISF ($\Gamma_{\rm MOS}$). (h) Simulated $\Gamma^2_{\rm MOS}$. (i) Channel conductance $G_{\rm DS}$ of the transistors. (j) PN contribution from the $G_{\rm DS}$. (k) Transconductance $G_{\rm M}$ of the transistors. (l) PN contribution from $G_{\rm M}$.

gate voltage as shown in Fig. 11(i). Therefore, $F_{\rm GDS}$ will be suppressed to its minimum when compared with the implicit CM resonance topology with a narrow span of the minimum $\Gamma_{\rm MOS}$ [Fig. 11(j)].

For the noise contribution from $g_{\rm m}$, owing to the voltage gain from drain-to-gate nodes, a larger gate voltage of the Class-F^{-1} topology also helps in reducing the time that the transistors stay in the saturation region, resulting in a shorter transition time of $g_{\rm m}$ [Fig. 11(k)]. Together with the wide span of the minimum $\Gamma_{\rm MOS}$, $F_{\rm GM}$ is also significantly reduced when compared with that of the implicit CM resonance topology as shown in Fig. 11(l).

Interestingly, the analysis is consistent with [6], in which $F_{\rm GM}$ and $F_{\rm GDS}$ can be approximated by $2\Gamma^2_{\rm MOS,rms}R_{\rm P}\gamma\, G_{\rm M,EFF}$ and $2\Gamma^2_{\rm MOS,rms}R_{\rm P}G_{\rm DS,EFF}$, respectively, where $G_{\rm D,SEFF}$ is the tank loading effect of the $-g_{\rm m}$ transistor. Since class-F^{-1} has a large $R_{\rm P2}$, the loading effect is heavily minimized even if the transistors are driven into the deep-triode region [9], [11], [14]; hence, its $G_{\rm DS,EFF}$ is very small. Also, energy conservation enforces that the effective transconductance is entailed to overcome both the tank loss and $G_{\rm DS,EFF}$ [15], such that

$$G_{\rm M,EFF} = \frac{1}{A_{\rm V}}\left(\frac{1}{R_{\rm P}} + G_{\rm DS,EFF}\right) \tag{15}$$

TABLE I
PERFORMANCE COMPARISONS OF DIFFERENT OSCILLATOR TOPOLOGIES

	F_{TANK}	F_{GM}	F_{GDS}	ΣF	η	FoM† (Cal.)	FoM (Sim.)
Class-B [16]&*	1	γ_n	0	2.29	0.64	194.2	N/A
Dynamic-Biased Class-C [5]*	1	γ_n	0	2.29	0.77	195	N/A
Class-F [6]*	0.7	$0.7\gamma_n$	0.27	1.87	0.5	194	N/A
Implicit CM [11]# (Q_2 = 6.3)	1.22	$1.4\gamma_n$	0.4	3.42	0.74	193.1	192.8
Implicit CM [11]# (Q_2 = 9.3)	1.17	γ_n	0.22	2.68	0.82	194.6	194.3
Class F^{-1}# (Q_2 = 9.3)	**1.2**	**$0.1\gamma_n$ +$0.14\gamma_p$**	**0.08**	**1.6**	**0.88**	**197.2**	**196.7**

&Assume the current source is ideal and does not contribute noise
*Data extracted from its corresponding work
Data obtained from simulation, f_{LO} = 4 GHz
†Assume Q_l = 14, γ_n = 1.29, γ_p = 1.35 and use equation (1)

which shows that $G_{M,EFF}$ for class-F^{-1} is also lower than $G_{M,EFF}$ of the implicit CM resonance, leading to a lower F_{GM}.

By using F_{TANK}, F_{GM}, and F_{GDS} obtained from Fig. 11 and substitute them into (1), the FoM of class-F^{-1} and implicit CM resonance with Q_2 of 6.3 can be calculated as 197.2 and 193.1 dBc/Hz. Compared with the simulated results directly obtained from the harmonic balance simulator in spectreRF, as shown in the last column of Table I, the calculated FoM of both topologies is slightly higher than the simulated one. To be precise, Γ_T and Γ_{MOS} are not entirely zero across the wide flat span when the $-g_m$ transistors enter the deep-triode region if the tank losses are modeled by a voltage noise source with a low series resistance [7], because noise current flowing from M_P to M_N through L_P still can produce a random phase shift to the output voltage. Consequently, F_{TANK}, F_{GM}, and F_{GDS} are slightly underestimated using the parallel equivalent R_P model in Fig. 10. Table I also gives the noise factors of the implicit CM topology with a higher Q_2 of 9.3. As expected, a higher Q_2 helps to reduce F_{GM} and F_{GDS} and increase the power efficiency. However, its F_{GM} and F_{GDS} are still much larger than those of the class-F^{-1} topology due to the lack of voltage gain from the drain-to-gate nodes of the $-g_m$ transistors.

Table I compares the FoM of different oscillator topologies. The values of γ_n and γ_P are extracted from the noise simulation in the 65-nm CMOS technology. For the sake of completeness, the FoM of the implicit CM resonance with a high Q_2 is also evaluated with an unpractical value of $k = 0.18$. Class F^{-1} has a higher F_{TANK} compared to class-B, class-C, and class-F due to the large impedance at $2f_{LO}$, which shapes the drain voltage and the ISF waveform into a non-sinusoidal one. Note that this extra loss was not considered by the simplified tank model in [24]. Nonetheless, device noise in class-F^{-1} is suppressed to a minimum. Specifically, class-F and implicit CM resonance improve F_{GDS} by reshaping the drain voltage by creating a tank impedance at $3f_{LO}$ for the former, and $2f_{LO}$ for the latter. By further improving Q_2 and impedance at $2f_{LO}$, F_{GDS} of the proposed class-F^{-1} is close to the class-B oscillator using an ideal current source and the class-C in which the $-g_m$ transistors are prevented from entering the deep-triode region due to a small oscillation amplitude. Thanks to the small $G_{DS,EFF}$ and a large voltage gain from the transformer, the class-F^{-1} also achieves a much lower F_{GM} than all the other four topologies. It is worth noting that the voltage gain can also be implemented in the class-C topologies through a transformer coupling from source-to-gate terminals [2]. Assuming a voltage gain of 2.5 is implemented in the dynamic-biased class-C topology in Table I, its F_{GM} can be reduced to $\gamma_n/2.5$, which further improves the FoM to 196.7. However, such a voltage gain would reduce the maximum drain voltage swing that keeps the transistors in the saturation region.

From another prospect, the large gate swing makes M_N and M_P operate more like switches, which reduces their noise contributions in the triode region (F_{GDS}) similar to the class-D oscillator [7]. Moreover, a recent work in [27] also showed that the noise contribution of the transistors can be close to negligible in the series-*LC* resonance topology. Overall, the proposed class-F^{-1} eases the inherent tradeoff between the large output swing and ΣF, exhibiting the best FoM performance with the highest η and lowest ΣF.

B. Flicker Noise Upconversion

For the proposed class-F^{-1} oscillator, since the phase of tank impedance at $2f_{LO}$ is zero, the second harmonic current will flow through a purely resistive path, which minimizes the flicker noise upconversion caused by the Groszkowski effect [10].

The $1/f$ noise current of the $-g_m$ transistor can be modeled as [10]

$$\overline{i_{1/f}^2(t)} = \frac{K}{WLC_{ox}} \cdot \frac{1}{f} \cdot g_m^2(\omega_0 t) \tag{16}$$

where K is a process-dependent constant, W and L are the channel width and length, and C_{ox} is the unit area oxide capacitance. Thus, the flicker noise source is a cyclostationary process with a noise modulating function $\alpha(\omega_0 t) = g_m(\omega_0 t)/g_{m,max}$. According to [17], the flicker noise to PN upconversion is prevented if the effective ISF defined as $\Gamma_{MOS,EFF}(\omega_0 t) = \Gamma_{MOS}(\omega_0 t) \cdot \alpha(\omega_0 t)$ has a zero dc value. Based on Fig. 11(g) and (h), the absolute value of Γ_{MOS} in the vicinity of π is lower compared to that at 2π (vice versa applies for G_M [Fig. 11(k)]). The effect of asymmetry of these two waveforms compensate each other, such that the symmetry of $\Gamma_{MOS,EFF}(\omega_0 t)$ is well maintained, yielding a dc value as low as 0.0011 (Fig. 12).[2]

According to [17], the $1/f^3$ noise corner can be approximated by

$$\omega_{1/f^3} \approx \frac{1}{2} \cdot \omega_{1/f} \cdot \left(\frac{\Gamma_{EFF,dc}}{\Gamma_{EFF,H1}}\right)^2 \tag{17}$$

where $\omega_{1/f}$ is the $1/f$ noise corner frequency of the device, $\Gamma_{EFF,H1}$ is the first harmonic of Γ_{EFF}, which is 0.035 extracted from simulation. Therefore, ω_{1/f^3} can be very low, as the value of $(\Gamma_{EFF,dc}/\Gamma_{EFF,H1})^2 = 9.88 \times 10^{-4}$ even if $\omega_{1/f}$ is as high as several MHz.

[2]It should be noted that the AM-to-PM conversion of the non-linear parasitic capacitances in the SCAs and varactors are not taken into account for the analysis.

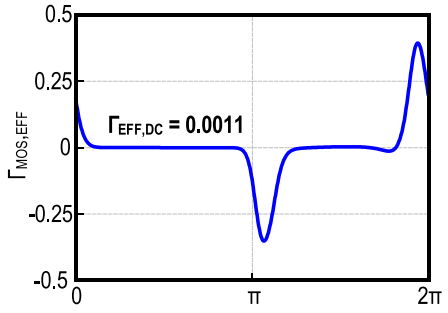

Fig. 12. Effective ISF of the class-F^{-1} oscillator.

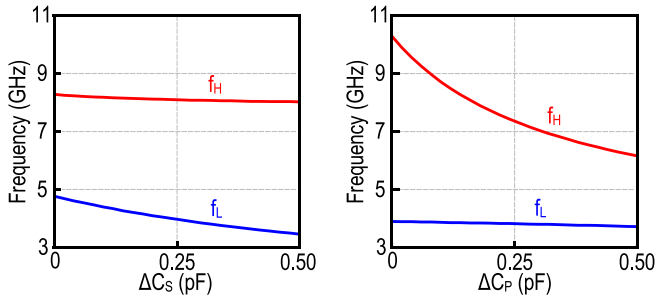

Fig. 13. Low and high band freqeucies of the transformer tank versus ΔCs (left) and ΔC_P (right).

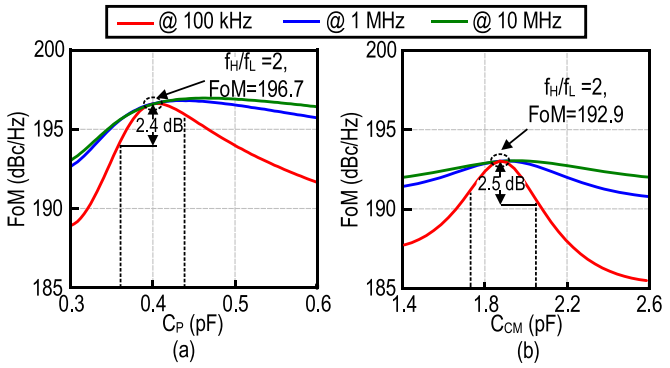

Fig. 14. Simulated FoM of (a) class-F^{-1} oscillator versus C_P and (b) implicit CM resonance oscillator ($Q_2 = 6.3$) versus C_{CM}. (Total tank capacitance $C_{CM} + C_{DM}$ is kept constant.)

C. FoM and Robustness of the Class-F^{-1} Oscillator

The two frequency bands of the transformer tank, i.e., f_L and f_H in the class-F^{-1} oscillator, can be controlled almost independently by tuning C_S and C_P, respectively, as confirmed by Fig. 13. Thus, the oscillation frequency $f_L = f_{LO}$ can be changed by tuning C_S while C_P can be adjusted to guarantee $f_H = 2f_{LO}$.

Fig. 14(a) shows the FoM variation of the class-F^{-1} oscillator. When C_P is tuned to 0.4 pF, we achieve an optimum point where f_H of the transformer based tank is mapped to $2f_{LO}$, minimizing the $1/f^3$ noise corner as the FoM at 100 kHz, 1 MHz, and 10 MHz converges to 196.7 dBc/Hz.

The FoM at 1-M/10-MHz offset where the PN is dominated by the thermal noise is relatively constant, which only degrades by $\sim$1 dB when C_P varies by $\pm$10%. The sensitivity

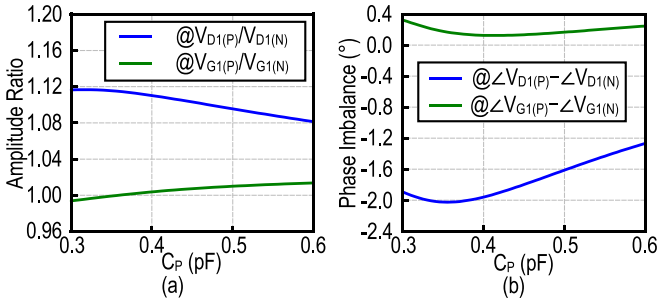

Fig. 15. (a) Amplitude ratio and (b) phase imbalance between the differential output at the drain and gate nodes.

of the FoM at 100-kHz offset is determined by both Q_2 and the oscillator loop gain [11]. Since the large loop gain of the class-F^{-1} oscillator compensates the effect of a higher Q_2 ($= 9.3$), its FoM degradation [Fig. 14(a)] caused by the misalignment between f_{LO} and $2f_{LO}$ is similar to that of the implicit CM-resonance oscillator with a smaller $Q_2 (= 6.3)$ [Fig. 14(b)].

Operating at 4 GHz, the imbalance between the differential outputs of the class-F^{-1} oscillator induced by asymmetrical parasitic capacitances of NMOS and PMOS transistors can be kept small. The simulation shown in Fig. 15 indicates that the amplitude ratio and phase error of the drain voltages are 1.11 and $-1.95°$, respectively. They are further suppressed to 1.006 and 0.12° for the gate voltages owing to the voltage gain provided by the transformer.

D. Frequency Pushing

The Groszkowski effect can also induce the frequency pushing when the supply voltage varies. Considering the relationship between the frequency shift and harmonic current given by [28]

$$\left|\frac{\Delta\omega}{\omega_0}\right| = \frac{1}{Q^2}\sum_{n=2}^{\infty}\frac{n^2}{n^2-1}\cdot\left|\frac{I_{Hn}}{I_{H1}}\right|^2 \tag{18}$$

where I_{Hn} and I_{H1} are the nth harmonic and the fundamental components of the tank current, respectively. Usually, the second harmonic current is dominant over the other high-order harmonic currents. In the conventional *LC*-oscillator without the second harmonic resonance, the second harmonic current flows through the tank capacitor. The supply voltage variation will induce the change of the I_{H2}/I_{H1} ratio so that the oscillation frequency will be shifted to restore the balance between the reactive and inductive energies of the tank.

In the proposed class-F^{-1} topology, the frequency pushing due to the Groszkowski effect is significantly suppressed since I_{H2} flows through a purely resistive path when f_{LO} and $2f_{LO}$ are perfectly aligned, i.e., $f_H = 2f_{LO}$ in Fig. 16(a). The residue small frequency pushing is induced by the Groszkowski effect due to the high-order harmonics and change of parasitic capacitance (C_{GS} and C_{GD}) of the $-g_m$ transistors. It is interesting to observe that the frequency pushing can be either positive or negative depending on the relationship between f_H and $2f_{LO}$ [Fig. 16(a)]. When

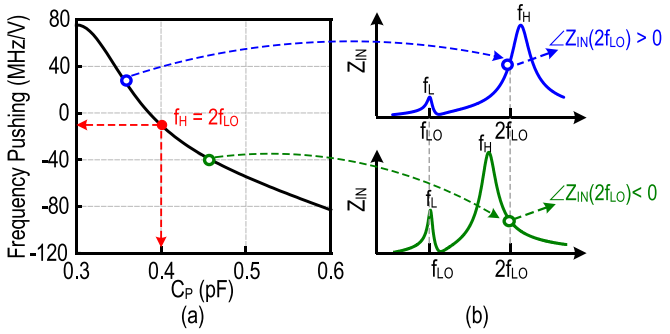

Fig. 16. (a) Simulated frequency pushing defined as $(f_{LO}@V_{DDH} - f_{LO}@V_{VDDL})/(V_{DDH} - V_{DDL})$ against C_P by varying V_{DD} from 0.55 V (V_{DDL}) to 0.65 V (V_{DDH}) and (b) tank impedance Z_{IN} when $f_H > 2f_{LO}$ (upper) and $f_H < 2f_{LO}$ (lower).

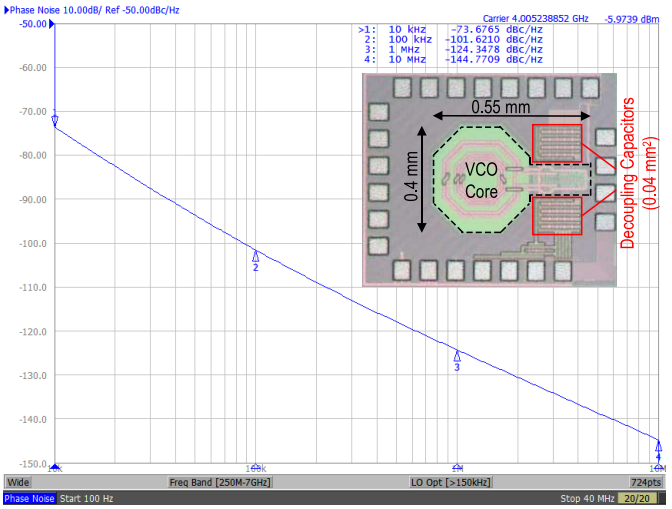

Fig. 17. Screenshot PN profile at 4 GHz and chip micrograph of the fabricated class-F^{-1} oscillator in 65-nm CMOS.

$f_H < 2f_{LO}$, the phase of tank impedance Z_{in} is negative at $2f_{LO}$ [Fig. 16(b)] and I_{H2} flows through a capacitive path. A higher V_{DD} raises I_{H2}/I_{H1}, requiring a lower oscillation frequency to re-balance the capacitive and inductive energy of the tank. On the other hand, the phase of tank impedance Z_{in} becomes postive [Fig. 16(b)] at $2f_{LO}$ when $f_H > 2f_{LO}$ and I_{H2} flows through an inductive path instead. Thus, the frequency shift caused by I_{H2} becomes positive as V_{DD} raises. When f_H is slightly higher than $2f_{LO}$, it is possible to achieve a zero frequency pushing by letting the positive frequency shift (caused by I_{H2}) and the negative frequency shift (caused by the high-order harmonic currents and parasitic capacitance) cancel each other, as illustrated in Fig. 16(a).

IV. Measurement Results

Fig. 17 shows the class-F^{-1} oscillator prototyped in 65-nm CMOS that occupies a core area of 0.14 mm^2 and the PN profile at 4 GHz measured by Keysight E5052B signal source analyzer. Thin-oxide devices with the oxide thickness of 2.3 nm are used for the $-g_m$ transistors. Their sizes are 37.5 μm/60 nm (NMOS) and 75 μm/60 nm (PMOS), respectively. As shown in Fig. 9(b), the maximum V_{GS} of the

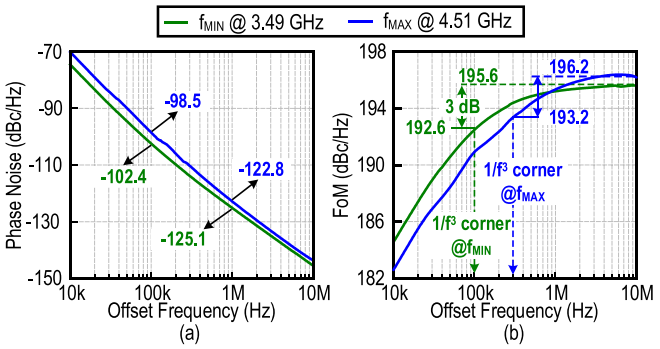

Fig. 18. (a) Measured PN and (b) FoM against offset frequency at $V_{DD} = 0.6$ V.

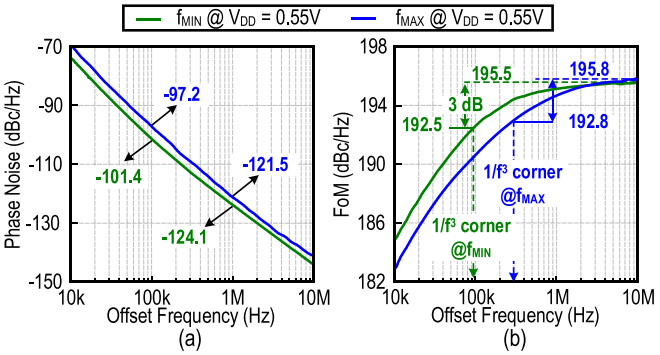

Fig. 19. (a) Measured PN and (b) FoM against offset frequency at $V_{DD} = 0.55$ V.

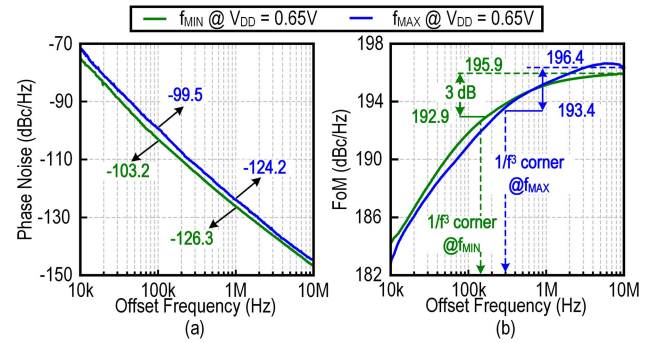

Fig. 20. (a) Measured PN and (b) FoM against offset frequency at $V_{DD} = 0.65$ V.

$-g_m$ transistors is 1.1 V at $V_{DD} = 0.6$ V, which is slightly larger than the standard supply voltage of 1 V. We can use the oxide breakdown scaled-model and the measured data given in [8] and [29] to evaluate the long-term reliability of the $-g_m$ transistors due to the time-dependent dielectric breakdown, which is the main failure mechanism for the voltage-controlled oscillator (VCO). The calculated lifetime for a 0.01% failure rate at 140 °C is $\sim 5 \times 10^{14}$ s (well exceeding 10 years). If a standard V_{DD} of 1 V is required, there would be an extra voltage drop on the regulator which increases the VCO power consumption and degrades its FoM. However, it could also be advantageous for the class-F^{-1} VCO to achieve large output swing and low PN at a low V_{DD} since the supply voltage of wireless transceivers is constantly dropping, both

TABLE II

PERFORMANCE BENCHMARK WITH THE STATE-OF-THE-ART *LC* OSCILLATORS

	Topology	CMOS Tech.	Tuning Range (%)	V_{DD} (V)	Freq. (GHz)	Power (mW)	PN (dBc/Hz)		FoM [1] (dBc/Hz)		Freq. Pushing (MHz/V)	$1/f^3$ Corner (kHz)	Die Area (mm^2)	Passives
							100 kHz	10 MHz	100 kHz	10 MHz				
[1]	NMOS+2f_{LO} tail inductor filtering	0.35μm	1-1.2 (18%)	2.5	1.2	9.1	-117 *	-162.5 #	189	195	N/A	N/A	N/A	2 inductors
[2]	Class-C	130nm	4.9-5.65 (14%)	1	4.9	1.4	-99 *	-143.3 †	191.3	195.6	N/A	200 *	N/A	1 inductor
[6]	Class-F	65nm	2.95-3.8 & (25%)	1.25	3.7	15	-103.6	-152.8	183.2	192.4	18-50	700	0.12	1 xfmr
[7]	Class-D	65nm	3-4.8 (46%)	0.4	3	6.8	-101	-149.5	182.2	190.7	140-480	800	0.12	1 inductor
[8]	Class-F_2	65nm	3.6-4.4 & (20%)	1.3	4.35	41	-109	-155	185.6	191.6	22-42	350	0.26	2 xfmrs
[9]	CMOS+2f_{LO} xfmr tail filtering	55nm	3.7-4.2 & (13%)	1.5	4.0	6.3	-100 *	-151.4 *	184	195.4	1.5-30	400	0.19	1 inductor, 1 xfmr
[10]	Class-$F_{2,3}$	40nm	5.4-7.0 (25%)	1	5.4	12	-105.3	-146.7	189.1	190.5	12-23	60	0.13	1 xfmr
[11]	NMOS Implicit CM resonance	28nm	2.85-3.75 (27.2%)	0.9	2.89	6.6	-108.1	-152	188	192.5	6-30	200	0.15	1 inductor
[30]	CMOS Implicit CM resonance	28nm	4.7-5.4 (13.8%)	0.7	5.3	0.5	-92 *	-138 *	189.5	195.5	N/A	200	0.18	1 xfmr
[31]	Transformer Feedback	180nm	3.65-3.97 (8.4%)	0.5	3.8	0.57	N/A	-139 #	N/A	193	273	N/A	0.23	1 xfmr
[32]	Tail ISF Manipulation	130nm	1.7%	1.4	2.4	4.2	-109 *	-148.4 #	190.3	189.8	N/A	N/A	0.09	1 inductor
[33]	Transformer-based inverted CMOS	130nm	1.68-2.07 (20.8%)	1.5	1.86	1.71	-109.1	-150.2 #	192.2	193.3	9.3-35.1	13	0.34	1 xfmr
[34]	Pulse-tail feedback	180nm	4.54-4.8 (5.57%)	1.2	4.55	1.35	-103.6	-143.4	195.5	195.3	N/A	0.7	0.98 @	1 inductor
This Work	CMOS Inverse-Class-F	65nm	3.49-4.51 (25.5%)	0.6	3.49	1.2	-102.4	-145.6	192.5	195.6	4.5	100	0.14	1 xfmr
					4.51	1.14	-98.5	-143.7	191	196.2	15	300		

* Estimated from PN plot # Normalized from 1 MHz offset † Normalized from 3 MHz offset & After on-chip divide-by-2 @ Include test pad

[1] $\text{FoM} = -\text{PN} + 20\log_{10}(f_{\text{LO}}/\Delta f) - 10\log_{10}(P_{\text{DC}}/1\text{ mW})$

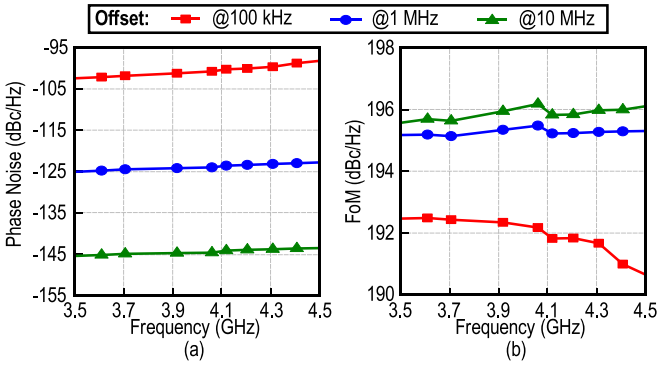

Fig. 21. Measured (a) PN and (b) FoM against tuning frequency.

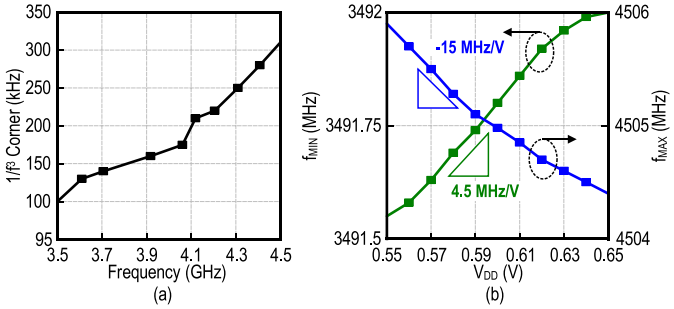

Fig. 22. Measured (a) $1/f^3$ PN corner against frequency and (b) frequency pushing at $f_{\min}$ and $f_{\max}$.

as required by the safe operation of the advanced CMOS technology, and as a mean to save power simultaneously [7]. We designed a 2-to-4-turn tapped transformer ($k_m = 0.38$) with $L_P = 2.28$ nH ($L_S = 4.28$ nH) and $Q_P = 19$ ($Q_S = 17$). C_P (C_S) employs 6-bit (5-bit) MOM switchable capacitors with an LSB of 11 fF (20 fF), and an additional varactor for fine-tuning purpose. Thick-oxide devices are employed in C_S switching to withstand the large differential voltage swing of V_{GN} and V_{GP}.

The class-F^{-1} oscillator is tunable from 3.49 to 4.51 GHz. Fig. 18(a) shows the PN profile of $f_{\min}$ to $f_{\max}$ when the power consumption ranges between 1.14 and 1.2 mW at $V_{DD} = 0.6$ V. Plotting the corresponding FoM in Fig. 18(b), the maximum FoM ranges between 195.6 and 196.2 dBc/Hz in the $1/f^2$ region.

To verify the robustness of the class-F^{-1} oscillator under different V_{DD}, we measured the PN and its corresponding FoM at $V_{DD,MIN} = 0.55$ V and $V_{DD,MAX} = 0.65$ V as shown in Figs. 19 and 20, respectively. The FoM variation is only ~0.6 dB at $f_{\max}$ and ~0.4 dB at $f_{\min}$.

Fig. 21(a) and (b) illustrates the measured PN and the FoM, respectively, across the tuning frequency at 100-kHz, 1-MHz, and 10-MHz offsets. The FoM at 10-MHz offset is consistently maintained, which agrees well with the simulation results described earlier, whereas at 100-kHz offset, the FoM varies between 190.9 and 192.5 dBc/Hz, translating to a flicker noise corner ranging from 100 to 300 kHz as exhibited in Fig. 22(a). The frequency pushing shows a +4.5 and −15 MHz/V

at $f_{\min}$ and $f_{\max}$, respectively, as presented in Fig. 22(b). Furthermore, they have an opposite trend due to the different control voltage for the varactor at $f_{\min}$ and $f_{\max}$.

Table II summarizes the performance and benchmarks of this paper with the state-of-the-art low PN oscillator.[3] By using only a transformer tank and achieving a competitive tuning range of 25.5%, our class-F^{-1} oscillator reveals the highest FoM at the 10-MHz offset. References [2], [9], [30], and [34] have a comparable FoM performance of ∼195.5 dB/Hz at a smaller frequency tuning range.

V. Conclusion

A class-F^{-1} oscillator with a single-ended PMOS-NMOS-complementary topology has been reported. By exploiting the transformer-based two-port resonator to generate a high-Q and high-impedance peak at $2f_{\mathrm{LO}}$, drain voltage can be reshaped, thus increasing the flat span in which the ISF is minimum. The transformer also provides a drain-to-gate voltage gain to reduce the current commutation time. These two features significantly surpress the circuit noise to PN conversion while improving the power efficiency. Prototyped in 65-nm CMOS, the class-F^{-1} oscillator shows a state-of-the-art FoM over a wide tuning range, low $1/f^3$ corner, and low frequency pushing.

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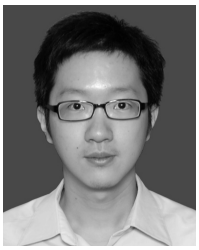

Chee Cheow Lim (S'14) was born in Kuala Lumpur, Malaysia. He received the B.E. degree (Hons.) in electrical and electronic engineering from the Asia Pacific University of Technology and Innovation, Kuala Lumpur, in 2014. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering, University of Malaya, Kuala Lumpur.

From 2014 to 2017, he was a Research and Teaching Assistant with the Analog, Digital, and RF Research Group, University of Malaya. From 2017 to 2018, he was a Research Assistant with the State-Key Laboratory of Analog and Mixed Signal VLSI, University of Macau, Macau, China. His research interests include CMOS analog and radio frequency integrated circuits and systems for wireless applications.

Mr. Lim was a recipient of the Best Final Year Project Award in 2014 and the IEEE ISSCC Student Travel Grant Award in 2018.

Harikrishnan Ramiah (M'10–SM'15) received the B.Eng. (Hons), M.Sc., and Ph.D. degrees in electrical and electronic engineering, in the field of analog and digital IC design, from Universiti Sains Malaysia, Penang, Malaysia, in 2000, 2003, and 2008, respectively.

In 2002, he was with Intel Technology, Sdn. Bhd, Penang, performing high-frequency signal integrity analysis. In 2003, he was with SiresLabs Sdn. Bhd, CyberJaya, Malaysia, working on 10-Gb/s SONET/SDH transceiver solution. He is currently an Associate Professor with the Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia, working in the area of RF integrated circuit (RFIC) and RF energy harvesting circuit design. He has authored or co-authored several papers in technical publications. His main research interests include analog-integrated circuit design, RFIC design, VLSI system design, and radio frequency energy harvesting power management module design.

Dr. Ramiah is a member of the Institute of Electronics, Information, and Communication Engineers. He is a Chartered Engineer of Institute of Electrical Technology and a Professional Engineer registered under the Board of Engineers Malaysia. He was a recipient of the Intel Fellowship Grant Award from 2000 to 2008. He had received a continuous international research funding in recognition of his work from 2014 to 2018, such as the Motorola Foundation Grant.

Jun Yin (M'14) received the B.Sc. and M.Sc. degrees in microelectronics from Peking University, Beijing, China, in 2004 and 2007, respectively, and the Ph.D. degree in electronic and computer engineering from The Hong Kong University of Science and Technology, Hong Kong, in 2013.

He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China. His research interests are on the CMOS radio frequency-integrated circuits for wireless communication and radar systems.

Pui-In Mak (S'00–M'08–SM'11) received the Ph.D. degree from the University of Macau (UM), Macau, China, in 2006.

He is currently a Full Professor with the Faculty of Science and Technology—ECE, UM, where he is an Associate Director (Research) with the State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests are on analog and radio frequency circuits and systems for wireless and multidisciplinary innovations.

Dr. Mak was a member of Board-of-Governors of the IEEE Circuits and Systems Society from 2009 to 2011. He was the TPC Vice Co-Chair of ASP-DAC in 2016. He was a TPC Member of A-SSCC from 2013 to 2016 and ESSCIRC in 2016 and 2017, and has been a TPC Member of ISSCC since 2016. He was a Distinguished Lecturer of the IEEE Circuits and Systems Society in 2014 and 2015 and the IEEE Solid-State Circuits Society in 2017 and 2018. Since 2018, he has been the Chair of the Distinguished Lecturer Program of the IEEE Circuits and Systems Society. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I from 2010 to 2011 and from 2014 to 2015 and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II from 2010 to 2013. He was a Senior Editor of the IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS from 2014 to 2015, and an Editorial Board Member of the IEEE Press from 2014 to 2016. He has been an Associate Editor of the IEEE SOLID-STATE CIRCUITS LETTERS since 2017 and the IEEE JOURNAL OF SOLID-STATE CIRCUITS since 2018. In 2005, he was decorated with the Honorary Title of Value for scientific merits by the Macau Government. He was inducted as an Overseas Expert of the Chinese Academy of Sciences since 2018. He was a recipient or co-recipient of the DAC/ISSCC Student Paper Award in 2005, the CASS Outstanding Young Author Award in 2010, the National Scientific and Technological Progress Award in 2011, the Best Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II in 2012 and 2013, the A-SSCC Distinguished Design Award in 2015, and the ISSCC Silkroad Award in 2016.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, and Ph.D. degrees, as well as the Habilitation for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Technical University (TU) of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, TU of Lisbon (from 2013 University of Lisbon), since 1980. Since 1992, he has been on leave from IST, University of Lisbon. He was the Dean of the faculty with Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, from 1994 to 1997 and has been the Vice-Rector of UM since 1997. He was a Co-Founder of Chipidea Microelectronics, Macao branch (now is Synopsys, Macao branch) in 2001/2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory, UM, and elevated in 2011 to the State Key Laboratory of China (the first in Engineering in Macao), being its Founding Director. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed in 2013, as a Vice-Rector (Research) until 2018. Since 2013, he has been a Chair-Professor with UM, where he is currently with the Department of Electrical and Computer Engineering, FST. He has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 24 Ph.D. and 21 master's students. He has authored or co-authored seven books and 11 book chapters, and 144 papers in scientific journals and 301 papers in conference proceedings as well as other 64 academic works, in a total of 554 publications. He holds 28 U.S. patents and 2 Taiwanese patents.

Dr. Martins was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS in 2008, and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. He was the Vice President of (World) Regional Activities and Membership of the IEEE CASS in 2012 and 2013. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013 and 2014. He was a CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference in 2016. He was a Nominations Committee Member of the IEEE CASS in 2016 and 2017 and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). He is a member of the IEEE CASS Fellow Evaluation Committee in 2019. He was an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013. In the representation of UM, he was one of the Vice-Presidents from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities. He was nominated the Best Associate Editor of the IEEE TRANSACTIONS ONCAS II for 2012 to 2013. He was a recipient of the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001, and the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016. He was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia in 2010.