A Passive RFID Tag Embedded Temperature Sensor With Improved Process Spreads Immunity for a $-30°C$ to $60°C$ Sensing Range

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***Abstract*—We present an ultra-low power temperature sensor embedded in the passive RFID tag using the TSMC 1P6M 0.18 μm standard CMOS process. Substrate parasitic NPN bipolar pair is exploited to generate the temperature dependent current signals for thermal sensing. A time-domain readout scheme which has high immunity to the on-chip resistor, capacitor and clock frequency process-voltage-temperature (PVT) spreads is further proposed. Measurement results of the embedded sensor within the tag system shows a sensing accuracy of $\pm 1.5°C$ (3σ) from $-30°C$ to $60°C$ after one-point calibration at $20°C$, with a sensing resolution of $0.3°C$ and a sampling rate of 68 samples per second. The embedded sensor draws 0.35 μA from a 1 V supply at room temperature and occupies a chip area of 0.14 mm^2.**

***Index Terms*—CMOS temperature sensors, passive RFID tags, process compensation, time-domain conversion (TDC).**

I. Introduction

THE rapid evolution of integrated circuit techniques has made the ultra-high frequency (UHF) radio-frequency identification (RFID) tags reliable and cheap enough to be brought into commercial use. The passive RFID tags offer several advantages such as battery-less operation, wireless communication, high flexibility, low cost and fast deployment [1]. Together with various embedded sensing capabilities, they can be readily applied in smart heath-care applications [2], hazardous environment monitoring and many more [3]. Particularly, as temperature is a common physical parameter that is imperative to both the industry and daily life, thermal monitoring embedded in passive RFID tags is promising to be widely adopted [4].

Embedding the temperature sensing function into passive RFID tag brings new challenges in terms of system design. Firstly, the embedded sensor should be ultra-low power (in the order of sub-μW) to prevent loss in the RFID tag's sensitivity [5], [6]; Secondly, the occupied sensor area and its calibration effort should be minimized to maintain low cost. Thirdly, for passive tags, as the sensor is supplied by the on-chip power management unit (PMU) and a good supply rejection is necessary to achieve accurate sensing.

Recently, various fully passive RFID tags with embedded temperature sensors have been reported. In [2], the temperature dependency of the MOSFET's threshold voltage V_{th} is utilized for temperature sensing. The output frequency of a free running oscillator is designed to be temperature dependent. This sensor has high resolution ($0.035°\mathrm{C/LSB}$) and consumes only 110 nW power for $\pm 0.1°\mathrm{C}$ sensing accuracy from $35°\mathrm{C}$ to $45°\mathrm{C}$. However, two-point individual calibration significantly increases the tag cost. In [3], a BJT-based sensor with a 8-bit successive-approximation ADC readout is adopted. This sensor achieves $\pm 2°\mathrm{C}$ sensing error from $-10°\mathrm{C}$ to $120°\mathrm{C}$ while draining 20% power of the whole tag. Apart from its large sensing inaccuracy, the high sensing power overhead greatly degrades the tag sensitivity. In [5], temperature sensing can be achieved with only 100 nW additional power by system co-design and its sensing accuracy has been improved to $\pm 0.8°\mathrm{C}$ from $-20°\mathrm{C}$ to $30°\mathrm{C}$ with only one-point calibration by a gain compensation technique. However, this temperature sensor is prone to supply noise and capacitor spreads, making it less robust.

This work targets at a $-30°\mathrm{C}$ to $60°\mathrm{C}$ sensing range, which covers the temperature range of the cold chain food monitoring, medicines and health commodities storage range, as well as the general environment monitoring range [6], [7]. The embedded sensor power consumption is optimized in the system level. Meanwhile, a resistor, capacitor and on-chip clock frequency PVT variations compensation technique is embodied in a time-domain readout to improve the process spreads immunity. The fabricated tag prototype in the TSMC 0.18 μm 1P6M standard CMOS process occupies a die area of 1.24 mm^2, with a sensor area of 0.14 mm^2. The embedded sensor draws 0.35 μA current from the 1 V internal supply. System level measurement results from 12 samples after one-point calibration at $20°\mathrm{C}$ show a sensing inaccuracy of $\pm 1.5°\mathrm{C}$ (3σ) from $-30°\mathrm{C}$ to $60°\mathrm{C}$, with a sensing resolution of $0.3°\mathrm{C}$ and a sampling rate of 68 samples per second. This paper is organized as follows. Section II illustrates the design and the operation principle of this embedded temperature sensor. The potential error sources

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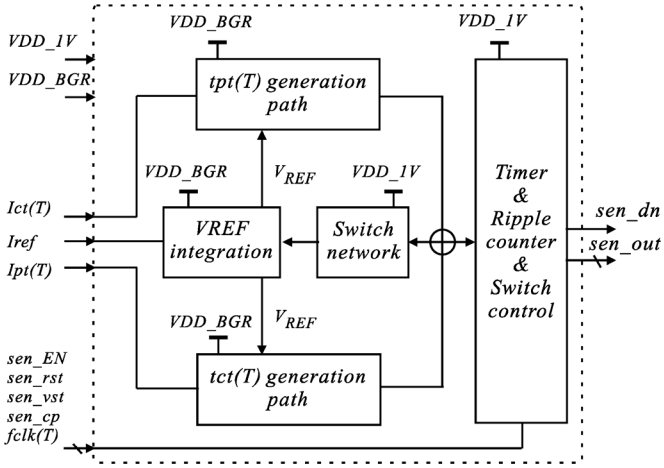

Fig. 1. Block diagram of the embedded temperature sensor with its associated system interfaces.

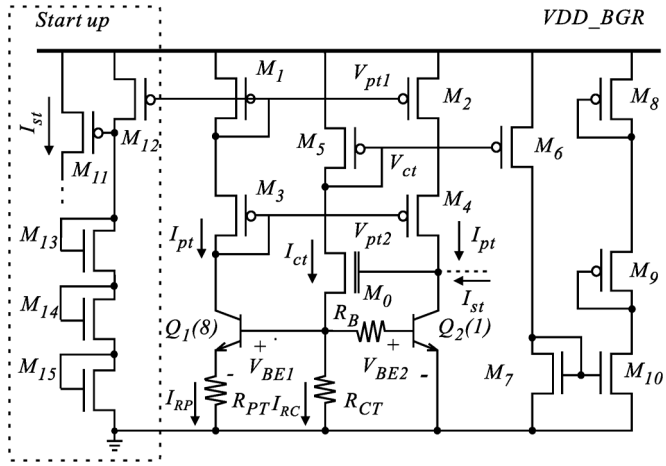

Fig. 2. The simplified temperature sensor frontend ($R_{PT} = 689\ \mathrm{k\Omega}$, $R_{CT} = 5.692R_{PT}$, $R_B = 1.18R_{PT}$, $I_{REF} = 102.5\ \mathrm{nA}$, $I_{PT} = 71.7\ \mathrm{nA}$, $I_{CT} = 32.6\ \mathrm{nA@20°C}$).

are identified and analyzed in Section III. Experimental results are presented in Section IV and Section V concludes this paper.

II. Proposed Temperature Sensor Design

Fig. 1 shows the block diagram of the embedded sensor and its interfaces with other system sub-blocks. The embedded sensor is powered by a low-dropout regulator (LDO) output VDD_1V. A bandgap reference supplied by VDD_BGR serves as the temperature sensor front-end and the system clock f_{clk} is used by the sensor for quantization purpose, with the critical control signals coming from the tag baseband, including sen_EN, sen_rst, sen_vst and sen_cp. In the tag system, the VDD_1V supply is shared by the clock generator and the system modulator/demodulator; the bandgap reference is shared by all the LDOs and the clock generator, while the system clock is shared by the tag baseband for command executions.

A. Temperature Sensor Frontend

For reduced power consumption, this sensor utilizes the system bandgap reference to generate the sensing signals instead of constructing a dedicated sensing frontend, with the penalty of reduced SNR and degraded signal linearity. Two matched vertical NPN transistors with 8:1 emitter area ratio serve as the sensing devices, which are operating in their forward-active regions [6]. In Fig. 2, with the same collector biasing current, two CTAT voltages V_{BE1} and V_{BE2} are developed across the base-emitter of Q1 and Q2; while their difference, ΔV_{BE}, is PTAT, as expressed below [8]

$$V_{BE}(T) = \frac{kT}{q} ln \frac{I_{bias}}{I_s} \tag{1}$$

$$\Delta V_{BE}(T) = \frac{kT}{q} ln(8) \tag{2}$$

where k is the Boltzmann constant, T is the bipolar junction temperature in Kelvin, q is the electron charge, I_{bias} is the bipolar collector biasing current and I_s is the bipolar saturation current.

For the designed frontend, the $I_{pt}(T)$ current amplitude can be derived as

$$I_{pt}(T) = \frac{kT}{q} ln(8) \left[R_{PT} + \frac{R_{PT}}{\beta_{F1}(T)} - \frac{R_B}{\beta_{F2}(T)} \right]^{-1} \tag{3}$$

where R_B is the bipolar current-gain compensation resistor and $\beta_{F1,2}(T)$ are the current gains of $Q_{1,2}$ and can be estimated as

$$\beta_F(T) \approx \beta_{F0} \left(\frac{T}{T_r} \right)^{X_{TB}} \tag{4}$$

where T_r is the reference temperature, β_{F0} is the bipolar nominal current-gain at T_r and the exponent X_{TB} is an empirical parameter. Note that (4) is only an approximation. In practice, as $\beta_F(T)$ is slightly dependent on the collector biasing current density [9], $\beta_{F1}(T)$ and $\beta_{F2}(T)$ are therefore different. Such effect is verified by device simulation; and the simulated current-gain ratio $\beta_{F1}(T)/\beta_{F2}(T)$ is 0.85 ± 2% at different temperature, collector biasing condition and device process corners. In (3), if R_B is designed to be $(\beta_{F2}/\beta_{F1})R_{PT} = 1.18R_{PT}$, nonlinear content induced by $Q_{1,2}$ current gain difference can be minimized and (3) can be rewritten as

$$I_{pt}(T) = \frac{kT}{q} ln(8) \frac{1}{R_{PT}} \left[1 + \frac{\delta_{mis}}{\beta_{F1}(T)} \right]^{-1} \tag{5}$$

which can be purely PTAT and is independent of $\beta_{F1}(T)$ if there is no mismatch between R_{PT} and R_B (i.e. $\delta_{mis} = 0$). However, as a result of the strong temperature-dependency of $\beta_{F1}(T)$, mismatch in the resistors will introduce a non-PTAT content into $I_{pt}(T)$, which can not be completely trimmed out [8]. For the used TSMC 0.18 μm process, the nominal current-gain β_{F0} is 14 at $T_r = 20°\mathrm{C}$ and the exponent X_{TB} is 2.25. The resultant curvature error in $I_{pt}(T)$ is ±0.1°C for a ±10% mismatch between R_{PT} and R_B. However, if without including a compensation resistor R_B, the temperature dependence of $\beta_{F1}(T)$ directly deteriorates $I_{pt}(T)$ signal linearity, and the resultant curvature error could be as large as ±0.45°C within the target sensing range.

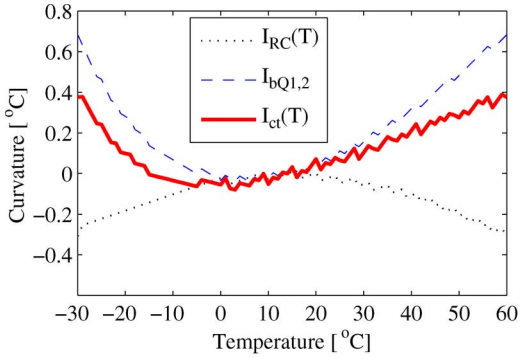

Fig. 3. Additional curvature introduced to $I_{ct}(T)$ by $Q_{1,2}$ base current; the curvature in $I_{RC}(T)$ and the overall curvature in $I_{ct}(T)$.

For the $I_{ct}(T)$ signal, its amplitude can be derived as

$$I_{ct}(T) = I_{bQ1,2}(T) + I_{RC}(T) \tag{6}$$

$$I_{bQ1,2}(T) = \frac{2.18 I_{pt}(T)}{\beta_{F1}(T)} \tag{7}$$

$$I_{RC}(T) = \frac{I_{pt}(T)}{\beta_{F2}(T)} \frac{R_B}{R_{CT}} + \frac{kT}{q} ln \frac{I_{pt}(T)}{I_s(T)} \frac{1}{R_{CT}} \tag{8}$$

Therefore

$$I_{ct}(T) \approx \frac{2.25 I_{pt}(T)}{\beta_{F1}(T)} + \frac{kT}{q} ln \frac{I_{pt}(T)}{I_s(T)} \frac{1}{R_{CT}} \tag{9}$$

where $I_{bQ1,2}(T)$ is the overall base current of Q_1 and Q_2, while $I_{RC}(T)$ is the current flows in R_{CT}. It can be observed that, as a result of the strong positive temperature dependency of $\beta_F(T)$, the concave shape base current could somehow compensate the intrinsic curvature of $I_{RC}(T)$. The simulated overall curvatures introduced to $I_{ct}(T)$ by $I_{bQ1,2}(T)$, $I_{RC}(T)$ and also the on-chip resistor's temperature coefficient are shown in Fig. 3. It can be seen that the overall linearity of the resultant $I_{ct}(T)$ signal of this sensor frontend is not deteriorated much due to the bipolar base current.

In the tag system, the sensor frontend is directly supplied by the rectifier output VDD_BGR, whose DC value is sensitive to the tag received RF power, especially when the input power is very small. Such VDD_BGR variation could directly propagate through the diode-connected PMOS to the bipolar collector and changes its base-collector voltage V_{BC}, which modulates the bipolar basewidth (early effect) and affects $V_{BE1,2}$ signal accuracy [9]. For the used NPN bipolar in TSMC 0.18 μm process, its forward early voltage VAF is as large as 50 V. Simulated PSRR of $I_{pt}(T)$ and $I_{ct}(T)$ are 38 dB and 66 dB at DC, respectively; indicating that a reasonable supply rejection can be still maintained under different input RF power conditions.

In the sensor frontend, cascoded current mirrors $M_1 - M_4$ with large transistor length are used to obtain an accurate $I_{pt}(T)$ replica. Meanwhile, a native transistor M_0 together with M_5 are used to buffer and mirror the $I_{ct}(T)$ signal. $M_6 - M_{10}$ are added to form a cascoded configuration for better $I_{ct}(T)$ mirroring accuracy. Since during current integration, the drain voltage of the bottom PMOS gradually increases and is subject to strong channel-length modulation, with a cascoded PMOS, the mirrored $I_{ct}(T)$ can be kept constant during the whole integration period. $M_{11} - M_{15}$ serve as the start-up for the bandgap reference core. After power-on, a startup current I_{st} from M_{11} is injected into the Q_2 bipolar branch and pulls the circuit out of the ALL-ZERO state. Once the internal nodes reach the target operation point, a scaled $I_{pt}(T)$ current mirrored by M_{12} develops a voltage through $M_{13} - M_{15}$ which is sufficient to cutoff M_{11}. A reference current I_{ref} can be obtained by adding a scaled $I_{pt}(T)$ to $I_{ct}(T)$. The derived I_{ref}, $I_{pt}(T)$ and $I_{ct}(T)$ are injected into the sensor readout for further signal conversion. This frontend core draws 0.6 μA current from a 1.35 V nominal output of the rectifier. Other sensing errors due to process spreads will be analyzed in detail in Section III.

B. On-Chip System Clock

In this design, a low power ring oscillator clock generator is employed instead of using a power-hungry one based on injection-locking method. As a result, increased jitter content and frequency spread in the system clock is expected [10]. The simulated system clock frequency varies from 2.3 MHz to 4.15 MHz at all possible device corners using the TSMC 0.18 μm 1P6M CMOS process, drawing 1.5 μA current from the 1 V supply. As the sensor reuses this system clock for quantization purpose, extra care should be taken to ensure the sensor performance. Fortunately, the clock jitter is a random noise that can be minimized by using clock averaging. However, the clock frequency spread could change the sensor gain if it is directly utilized for quantization as in traditional time-to-digital (TDC) readouts. Such gain error cannot be corrected except by using a costly two-point calibration [11]. Section III illustrates the clock spread compensation principle and the quantitative analysis to minimize the influence of the clock jitter on this embedded sensor so as to achieve accurate temperature sensing within the target sensing range using only one-point calibration.

C. Temperature Sensor Readout

Fig. 4 shows the simplified circuit implementation of the embedded temperature sensor readout and its corresponding timing diagram. It consists of three capacitor, C_{ref}, C_{pt} and C_{ct}, two comparator branches A_1 and A_2, and other digital blocks. Once the sensor is enabled by sen_EN, $M_2 - M_4$ are turned on to steer the current signals from the sensor frontend. Meanwhile, all the capacitors and digital blocks will be reset by sen_rst. Afterwards, sen_vst is exerted and C_{ref} starts to integrate I_{ref} for N_0 clock cycles. At the end of the integration, M_1 is triggered to bypass I_{ref}, with C_{ref} holding the derived voltage V_{REF}, which can be expressed as

$$V_{REF} = \frac{N_0 I_{ref}}{f_{clk} C_{ref}} \tag{10}$$

After that, $I_{pt}(T)$ and $I_{ct}(T)$ start to charge up C_{pt} and C_{ct}, simultaneously. By real-time comparing the top plate voltages V_{cpt} and V_{cct} of C_{pt} and C_{ct} with V_{REF}, two asynchronous rising edges will be triggered at the comparator outputs. These two signals are XORed and a temperature modulated pulse-width $t_{PW}(T)$ can be obtained. The relationship between the derived $t_{PW}(T)$ and the temperature is

$$t_{PW}(T) = t_{ct}(T) - t_{pt}(T) = \frac{C_{ct} V_{REF}}{I_{ct}(T)} - \frac{C_{pt} V_{REF}}{I_{pt}(T)} \tag{11}$$

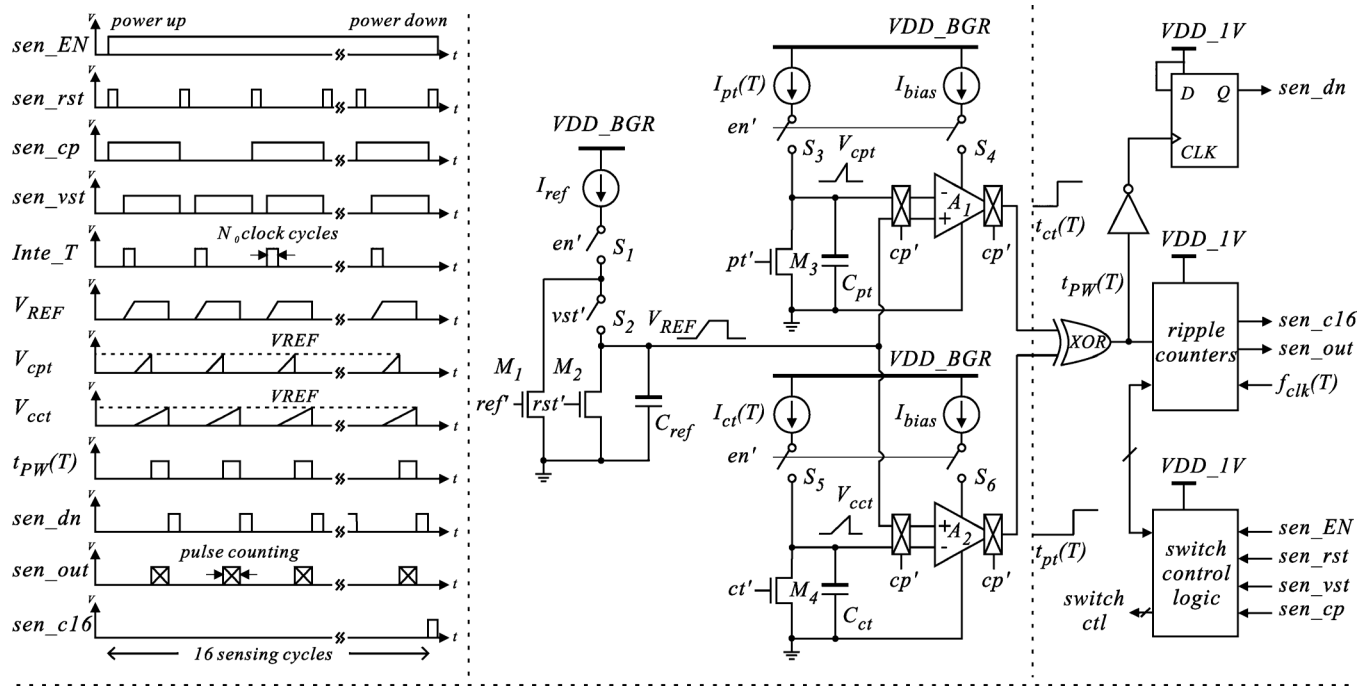

Fig. 4. Implementation of the proposed temperature sensor core (right) and its corresponding timing diagram (left).

using (10)

$$t_{PW}(T) = \frac{N_0 I_{ref}}{f_{clk} C_{ref}} \left[\frac{C_{ct}}{I_{ct}(T)} - \frac{C_{pt}}{I_{pt}(T)} \right] \tag{12}$$

Assume that the first-and second-order temperature coefficients (TC) of $I_{pt}(T)$ and $I_{ct}(T)$ are k_{p1}, k_{p2} and k_{c1}, k_{c2}, respectively. Since their higher order coefficients are small and negligible, at the reference temperature T_r, $I_{pt}(T)$ and $I_{ct}(T)$ can be written as

$$I_{pt}(T) \approx I_{pt}(T_r) \left[1 + k_{p1}(T - T_r) + k_{p2}(T - T_r)^2 \right] \tag{13}$$

$$I_{ct}(T) \approx I_{ct}(T_r) \left[1 + k_{c1}(T - T_r) + k_{c2}(T - T_r)^2 \right] \tag{14}$$

rewrite (12) by replacing $I_{pt}(T), I_{ct}(T)$ with (13), (14) and performing taylor expansion [6]

$$\begin{aligned} t_{PW}(T) \approx \frac{N_0 I_{ref}}{f_{clk} C_{ref}} \Bigg\{ & \left[\frac{C_{ct}}{I_{ct}(T_r)} - \frac{C_{pt}}{I_{pt}(T_r)} \right] \\ & - \left[\frac{C_{ct} k_{c1}}{I_{ct}(T_r)} - \frac{C_{pt} k_{p1}}{I_{pt}(T_r)} \right] (T - T_r) \\ & + \left[\frac{C_{ct} \left(k_{c1}^2 - k_{c2} \right)}{I_{ct}(T_r)} - \frac{C_{pt} \left(k_{p1}^2 - k_{p2} \right)}{I_{pt}(T_r)} \right] \\ & \times (T - T_r)^2 \Bigg\} \end{aligned} \tag{15}$$

from (15), the derived $t_{PW}(T)$ contains a positive first-order TC and a second-order non-linear term. With $T_r = 20°\mathrm{C}$, the simulated current amplitudes of I_{pt} and I_{ct} are 71.7 nA and 32.6 nA, respectively. Meanwhile, the simulated TC for k_{p1}, k_{c1} are 4.64 $\mathrm{m}/°\mathrm{C}$, -3.23 $\mathrm{m}/°\mathrm{C}$ and -81.8 $\mathrm{p}/°\mathrm{C}$, -0.45 $\mathrm{n}/°\mathrm{C}$ for k_{p2}, k_{c2}, respectively. Because $k_{p2} \ll k_{p1}^2$ and $k_{c2} \ll k_{c1}^2$, the second-order non-linear term dominated by $k_{p1,c1}$ can be minimized at the reference temperature if (16) is satisfied

$$\frac{C_{pt} k_{p1}^2}{I_{pt}(T_r)} \approx \frac{C_{ct} k_{c1}^2}{I_{ct}(T_r)} \tag{16}$$

thus (15) is simplified to

$$\begin{aligned} t_{PW}(T) \approx \frac{N_0 I_{ref}}{f_{clk} C_{ref}} \Bigg\{ & \left[\frac{C_{ct}}{I_{ct}(T_r)} - \frac{C_{pt}}{I_{pt}(T_r)} \right] \\ & - \left[\frac{C_{ct} k_{c1}}{I_{ct}(T_r)} - \frac{C_{pt} k_{p1}}{I_{pt}(T_r)} \right] (T - T_r) \Bigg\} \end{aligned} \tag{17}$$

This temperature-dependent pulse-width $t_{PW}(T)$ is then digitized with a ripple counter, with its falling edge triggers sen_dn, indicating the end of one sensing cycle. Afterwards, the baseband issues sen_rst and sen_vst again to restart such sensing procedures for averaging purpose. Another ripple counter is utilized to record the total number of averaged $t_{PW}(T)$. One temperature sampling is finished after 16 sensing cycles, and sen_cnt16 is exerted. The number of averaged samples is a tradeoff between the circuit random noise suppression and the sensor sampling rate, which is analyzed in Section III-D.

In the sensor readout, a continuous-time comparator is implemented using a traditional current-mirror based amplifier with cross-coupled loading for improved comparator gain. A source follower is implemented as the output stage to prevent kick-back noise during pulse transition. In order to reduce the comparators' power consumption, their output branches are cut off immediately after $t_{pt}(T)$ and $t_{ct}(T)$ are exerted. In this manner, even though the averaged power consumption of the sensor core is greatly reduced, there will be instantaneous short-duration high peaking currents, as indicated in Fig. 5. As a small area for

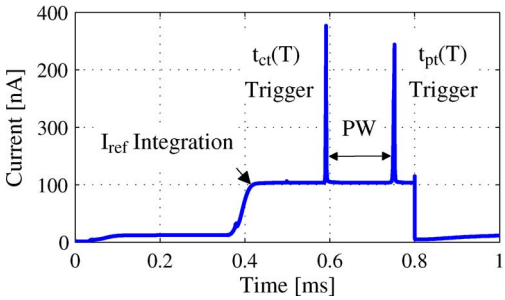

Fig. 5. Overall transient current of the continuous-time comparators.

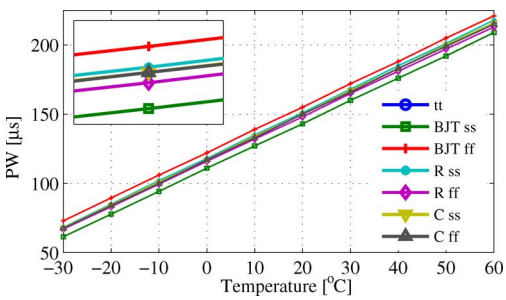

Fig. 6. Simulated temperature modulated pulse width under different device corners (tt: typical corner for all devices; BJT ss: slow corner for the bipolar; R ss: slow corner for the resistor; C ss: slow corner for the capacitor).

reduced tag cost is normally required, limited filtering capacitors together with large peaking currents can result in substantial drop in the supply voltage, causing the tag to malfunction. For this comparator, these instantaneous currents are limited by the current-mirror ratio, which is designed to be below 400 nA to achieve negligible (<1 mV) drop in the supply VDD_1V.

III. Sensing Error Analysis

As other circuit non-idealities can also degrade the sensor performance, including the effects of device PVT spreads, comparator delay and offset, switch charge injection, capacitor charge leakage, as well as device noise. These issues have to be analyzed during design phase and corresponding techniques are needed to deal with these issues in order to achieve the required sensing accuracy.

A. Process Spreads

As stated in Section II-B, the ring oscillator clock is highly process dependent and requires clock compensation if one-point calibration is targeted. As shown in (17), the temperature modulated pulse-width $t_{PW}(T)$ is designed to be dependent on f_{clk}. After digitization with the same system clock f'_{clk}, the derived digital output is

$$D(T) = t_{PW}(T) \cdot f'_{clk} \tag{18}$$

if we ignore the clock jitter effect (separately discussed in section III-E), f'_{clk} is equal to f_{clk}. By combining (17) and (18)

$$D(T) = N_0 \left\{ \frac{C_{ct}}{C_{ref}} \cdot \frac{I_{ref}}{I_{ct}(T_r)} \cdot [1 - k_{c1}(T - T_r)] - \frac{C_{pt}}{C_{ref}} \cdot \frac{I_{ref}}{I_{pt}(T_r)} \cdot [1 - k_{p1}(T - T_r)] \right\} \tag{19}$$

the digital output $D(T)$ is therefore independent of the on-chip system clock PVT variations. The error induced by the PVT variations of on-chip metal-insulator-metal (MIM) capacitors are also minimized as $D(T)$ only dependents on the physical matchings of these capacitors. In this work, C_{ref} is designed to be twice the size of C_{pt} and C_{ct}, as a tradeoff between the chip area, the kT/C noise level and the sampling speed. All the on-chip capacitors are common-centroid laid out with dummy units surrounded for better matching.

The resistor process spreads affect the sensor in a different manner. In order to trace the resistor process variation effects, (19) is rewritten in the voltage domain

$$I_{ref} = \frac{\alpha \Delta V_{BE}(T)}{R_{PT}} + \frac{V_{BE}(T)}{R_{CT}} \tag{20}$$

$$D(T) = N_0 \cdot \frac{C_{pt}}{C_{ref}} \cdot I_{ref} \cdot \left[\frac{R_{CT}}{V_{BE}(T)} - \frac{R_{PT}}{\Delta V_{BE}(T)} \right] \tag{21}$$

where α is a constant to derive a reference current I_{ref}; by replacing (20) and the on-chip resistors' ratio into (21)

$$D(T) = N_0 \cdot \frac{C_{pt}}{C_{ref}} \cdot \left[\alpha \Delta V_{BE}(T) + \frac{V_{BE}(T)}{5.692} \right] \times \left[\frac{5.692}{V_{BE}(T)} - \frac{1}{\Delta V_{BE}(T)} \right] \tag{22}$$

from (22), only $V_{BE}(T)$ can be affected by the on-chip resistor spreads, which alters the bipolar collector biasing currents and thus $V_{BEQ1,2}$ deviate from their nominal values. Provided that the resistor process spread δ_R is constant over the target sensing range, it therefore has the same effect as the spread of the bipolar saturation current $I_s(T)$, δ_{I_s} [8]. The overall digital error Δe_1 induced by δ_R and δ_{I_s} is

$$\Delta e_1 \approx \frac{N_0(\delta_{I_s} + \delta_R)}{2} \left[\frac{1}{I_{ct}(T_r)R_{CT}} + \frac{1}{I_{pt}(T_r)R_{PT}} \right] \frac{kT}{q} \tag{23}$$

hence Δe_1 is PTAT that can be mostly trimmed out, providing the possibility to achieve good sensing accuracy for this ultra-low power embedded senor with a time-domain readout. Fig. 6 shows the simulation results of $t_{PW}(T)$ from -30°C to 60°C at some different device corners. It can be observed that the capacitor spread introduces only negligible error, while the resistor spread and the bipolar spread introduce PTAT errors which can be trimmed out after fabrication.

B. Comparator Delay and Offset

In Section II-C, the comparators are assumed to have zero delay and offset and the target pulses are triggered once the top plate voltages of C_{pt} and C_{ct} reach V_{REF}. However, the continuous-time comparators in Fig. 4 conduct small currents and have limited voltage gain, a non-negligible delay $\Delta t_d(T)$ is needed to charge up the comparator output loading. As the sensor readout exploits a pseudo-differential architecture, $\Delta t_d(T)$ as a common mode content in both $t_{ct}(T)$ and $t_{pt}(T)$ can be canceled after conversion.

To deal with the comparator offset, a time-domain offset cancelation scheme similar to the correlated double sampling (CDS) technique is employed. Assume the offsets of the comparator A_1 and A_2 are v_{A1} and v_{A2}, respectively. During the

odd sensing cycles, V_{REF} is connected to the positive input nodes of A_1, A_2. The output pulse-width $t_{PW1}(T)$ is

$$t_{PW1}(T) = \frac{C_{ct}[V_{REF} + v_{A2}]}{I_{ct}(T)} - \frac{C_{pt}[V_{REF} + v_{A1}]}{I_{pt}(T)} \quad (24)$$

during the even sensing cycles, V_{REF} is reconfigured to connect to the negative input node of the comparator A_1, A_2. The output pulse-width $t_{PW2}(T)$ is

$$t_{PW2}(T) = \frac{C_{ct}[V_{REF} - v_{A2}]}{I_{ct}(T)} - \frac{C_{pt}[V_{REF} - v_{A1}]}{I_{pt}(T)} \quad (25)$$

after averaging (24) and (25), the error introduced by the comparator offsets become negligible. Moreover, the comparator offsets' long-term shifting are also minimized.

C. Charge Injection and Charge Leakage

For this sensor, the switch charge injection will be directly translated to DC offsets on the capacitors. There are three scenarios where switch charge injection occurs: 1) at the start of each sensing cycle where all the capacitors are reset by NMOS switches; 2) each time when the current from the sensor frontend is switched in for integration; 3) when I_{ref} is switched away from C_{ref} by S_2 after V_{REF} is obtained. As C_{ref} is twice the size of C_{pt} and C_{ct}, M_2 is also twice sized as that of $M_{3,4}$ so that all the capacitors start integration at the same common mode voltage level. The resultant common mode errors can then be effectively reduced by the pseudo-differential readout.

In (10) and (11), V_{REF}, V_{cpt} and V_{cct} are all assumed to only depend on the integration currents, the corresponding capacitor sizes and the integration time. However, though the reset transistors $M_2 - M_4$ and the bypass switch S_2 are in their OFF state during integration, their leakage currents through weak inversion conduction could affect the accuracy of these voltage signals. The weak inversion current of a MOSFET can be expressed as [12]

$$I_{sub}(T) = \mu_0 C_{ox} \frac{W}{L}(m-1)V_T^2 e^{\frac{V_{GS}-V_{th}}{mV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \quad (26)$$

where V_{th} is the MOSFET threshold voltage, V_T is the thermal voltage, C_{ox} is the gate oxide capacitance, μ_0 is the zero bias mobility and $m > 1$ is the body effect coefficient. For reduced leakage currents, the reset and bypass switches $M_1 - M_4, S_2$ are all stacked transistors with small W/L ratio, which slightly sacrifices their driving abilities. Notice that with zero gate voltage, the leakage current can be approximated to be independent of V_{DS} if $V_{DS} > 100$ mV [12]. In this design, the integration time required to make $V_{REF}, V_{cpt}, V_{cct} > 100$ mV is relatively short (i.e. 1/6 t_{pt}). A constant leakage $I_{sub0}(T)$ is thus utilized to estimate the switch leakage induced maximum sensing error.

During the sensing operation, $I_{sub0}(T)$ continuously discharges C_{pt} and C_{ct}, and there are two leakage paths that discharges C_{ref}, which gives

$$t_{pt}(T)'\,[I_{pt}(T) - I_{sub0}(T)] = C_{pt}[V_{REF} - \Delta V_{REF}] \quad (27)$$

$$\Delta V_{REF} = \frac{2I_{sub0}(T)}{C_{ref}} \times \left[t_{pt}(T)' + \frac{N_0}{f_{clk}(T)}\right] \quad (28)$$

where ΔV_{REF} denotes the capacitor voltage drop on C_{ref}. Solving for $t_{pt}(T)'$ gives

$$t_{pt}(T)' = t_{pt}(T) - \frac{I_{sub0}(T)}{I_{pt}(T)} \frac{N_0}{f_{clk}(T)} \quad (29)$$

similarly,

$$t_{ct}(T)' = t_{ct}(T) - \frac{I_{sub0}(T)}{I_{ct}(T)} \frac{N_0}{f_{clk}(T)} \quad (30)$$

(29) and (30) give the final leakage induced digital error Δe_2

$$\Delta e_2 = N_0 \cdot I_{sub0}(T) \left[\frac{1}{I_{pt}(T)} - \frac{1}{I_{ct}(T)}\right] \quad (31)$$

which is a temperature-dependent error and cannot be trimmed out. Simulated $I_{sub0}(T)$ for the used $0.5\ \mu\text{m}/(0.5\ \mu\text{m} \times 4)$ stacked transistor is less than 3 pA at 60°C. A maximum error of 0.03 LSB (corresponding to 0.01°C for 0.3°C/LSB) will be introduced according to (31), where I_{pt}, I_{ct} and N_0 are 84.5 nA, 26.8 nA and 384, respectively. It can be concluded that such switch leakage current won't deteriorate the sensor performance much.

D. Thermal Noise Sources

For a time domain readout, thermal noise either in voltage domain or current domain will be converted into temporal jitter content [13]. Since low frequency noise sources, such as flicker noise, affect the sensor in a similar way as that of the comparator delay and offset, they are mostly canceled after conversion. Extra care should be taken for other remaining noise sources to ensure the conversion accuracy, including the clock jitter, the comparator noise and the white noise due to current integration.

1) Clock Jitter: Thermal noise in the clock generator are mainly translated into clock jitter. For the embedded sensor, as stated in Section III-A, as long as the equivalent clock frequency f_{clk} during V_{REF} integration and f'_{clk} during $t_{PW}(T)$ digitization are the same, the clock compensation is perfect. However, time-varying jitter could deteriorate this compensation.

$$f'_{clk} = (1 + \delta_j) f_{clk} \quad (32)$$

where δ_j is the difference between the equivalent clock frequency of f_{clk} and f'_{clk} and this δ_j directly introduces a time-varying gain error to the sensor output. To satisfy the EPC-C1G2 communication requirements [14], the designed nominal system clock is 2.3 MHz and the simulated clock standard deviation (STD) is 5.2% at 60°C. The clock jitter level can be reduced by increasing the ring oscillator power and degrading the tag sensitivity, which is a net tag performance loss. During the design phase, the maximum influence of δ_j is predicted by theoretically modeling the clock jitter with an unbounded gaussian distribution [10], to verify whether further optimization of this system clock is needed for the target sensing accuracy.

For this sensor, one sensing cycle needs about 900 μs, which is 2000 clock cycles, with the sensor digital output to be 180 at

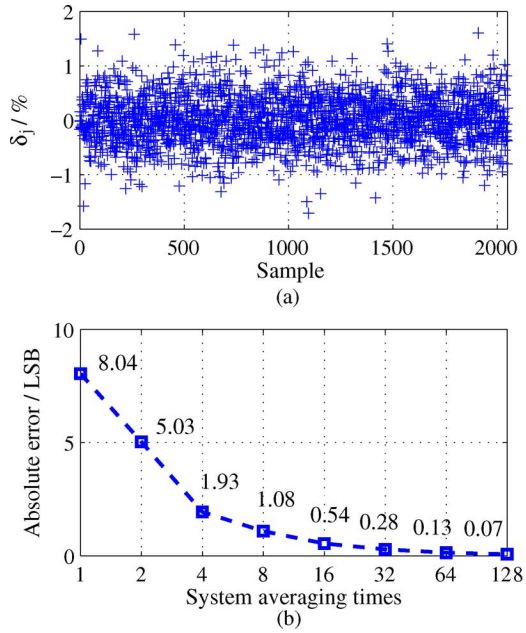

Fig. 7. (a) Modeled δ_j after clock averaging within one sensing cycle; (b) maximum error in LSB introduced after different times of system level averaging.

$-30°$C and about 500 at 60°C. The influences of δ_j can be predicted by the following steps: 1) construct a clock pool which contains 2000 Gaussian distributed clock data, with 2.3 MHz as the data expectation and 5.2% as the STD; 2) randomly select $N_0 = 384$ data from the clock pool for V_{REF} integration and perform data averaging, with j_{ref} denotes the difference between 2.3 MHz and the obtained averaged data; 3) similarly, randomly select 180 data points from the pool and perform averaging for $t_{PW}(T)$ digitization, with j_{pw} denotes the difference between 2.3 MHz and the averaged value, thus one data point $\delta_j = j_{ref} - j_{pw}$ is obtained. Note that 180 is the minimum number of clock cycles that can be averaged during $t_{PW}(T)$ digitization, which is the worst case for j_{pw} prediction. Step (1)–(3) is repeated for 2048 times, and the modeled δ_j is shown in Fig. 7(a). It can be seen that the maximum value is as large as $\pm 1.6\%$. Since at 60°C, the sensor digital output is about 500, the translated maximum random error is ± 8 LSB (i.e. $\pm 2.4°$C for $0.3°\text{C/LSB}$), which is unacceptably high.

In order to further minimize this clock jitter influence, system level averaging is adopted to tradeoff the conversion time with a reduced clock power consumption while achieving the required sensing accuracy. Fig. 7(b) shows the absolute LSB error against different numbers of system averaging samples, and the required number of averaging samples required to achieve a maximum of ± 0.5 LSB jitter induced error is 16. More averaging times can be chosen if an increase in accuracy is necessary, with the tradeoff of increased conversion time.

2) White Noise Integration and Comparator Noise: For the sensor, both the white noise integrated by the capacitor and the comparator input-referred noise accumulated on the capacitor will be translated to temporal errors in $t_{pt}(T)$ and $t_{ct}(T)$. For long channel devices, the white noise in the current integration path can be expressed as [13]

$$\overline{I_n^2} \approx \frac{8}{3} kTg_{m1} \cdot \Delta f \tag{33}$$

where g_{m1} is the PMOS current mirror transconductance and Δf is the integration bandwidth. Since integrating a current for a fixed amount of time is analogous to filtering the signal with a sinc filter in the frequency domain, Δf can be approximated by $1/T_{inte}$ where T_{inte} is the current integration time [13]. Therefore, the integrated white noise on a capacitor C_{inte} is

$$\overline{V_{n1}^2} \approx \frac{8}{3} kTg_{m1} \cdot \frac{T_{inte}}{C_{inte}^2} \tag{34}$$

meanwhile, the input-referred voltage noise on C_{ref}, C_{pt} and C_{ct} from the comparator can be expressed by

$$\overline{V_{n2}^2} \approx \frac{8}{3} kT \left(\frac{2}{g_{m2}} + \frac{3.5g_{m3}}{g_{m2}^2} \right) \cdot \frac{T_{inte}}{C_{inte}^2} \tag{35}$$

where g_{m2} is the comparator input NMOS transistor transconductance. g_{m3} is the cross-coupled PMOS transconductance. The timing error $\overline{T_n^2}$ can be obtained by dividing the overall noise voltage by the square of the capacitor integration speed $(I_{inte}/C)^2$. For the $t_{pt}(T)$ signal, timing error due to the circuit thermal noise is

$$\overline{T_n^2} = \left[\frac{8}{3} kTg_{m1} + \frac{8}{3} kT \left(\frac{2}{g_{m2}} + \frac{3.5g_{m3}}{g_{m2}^2} \right) \right] \frac{t_{pt}}{I_{pt}(T)^2} \tag{36}$$

from (36), the calculated maximum temporal error in $t_{pt}(T)$ is less than 1 ns. As the $t_{PW}(T)$ signal is in the order of hundreds of μs, sufficient SNR can still be maintained even taking the thermal noise induced timing error in $t_{ct}(T)$ into consideration.

IV. Measurement Results

Fig. 8(a) is the microphotograph of the fabricated RFID tag with the embedded temperature sensor, the 4 pads shown are for the tag antenna, extra pads exists for chip testing. The functionality of the sensor tag is wirelessly demonstrated and its performance is characterized with wired testing, with the measurement setup shown in Fig. 8(b). The complete die is placed inside a temperature chamber, together with a calibrated PT-100 thermometer L250 from Labfacility as a reference. The logic analyzer generates the custom commands and feeds into the signal generator for modulating, with a 900 MHz carrier. The sensor tag is wire-connected to the signal generator output to receive the RF power and sensing commands. A Tempmaster-PRO from Labfacility, which is 4-wire configured to cancel the wiring parasitic resistance, is adopted for the reference thermometer readout. Finally, the sensor digital output is compared against the reference thermometer reading to analyze its sensing linearity as well as the inter-die sensing spreads.

In terms of clock frequency spread, Fig. 9(a) shows the measured clock frequency, where a 7.5% inter-die clock frequency variation is observed. Moreover, for the same die, a frequency variation of as high as 6% exists at the two temperature extremes. To validate the clock frequency compensation scheme of the embedded sensor, an external clock from 1.5 MHz to 3 MHz is applied to the tag by disabling the tag internal clock. Fig. 9(b) shows the measured relative sensing errors for different external clock frequencies. It can be observed that the sensor output keeps constant with a clock frequency ranging from 2 MHz to 3 MHz, exhibiting a high clock frequency spread

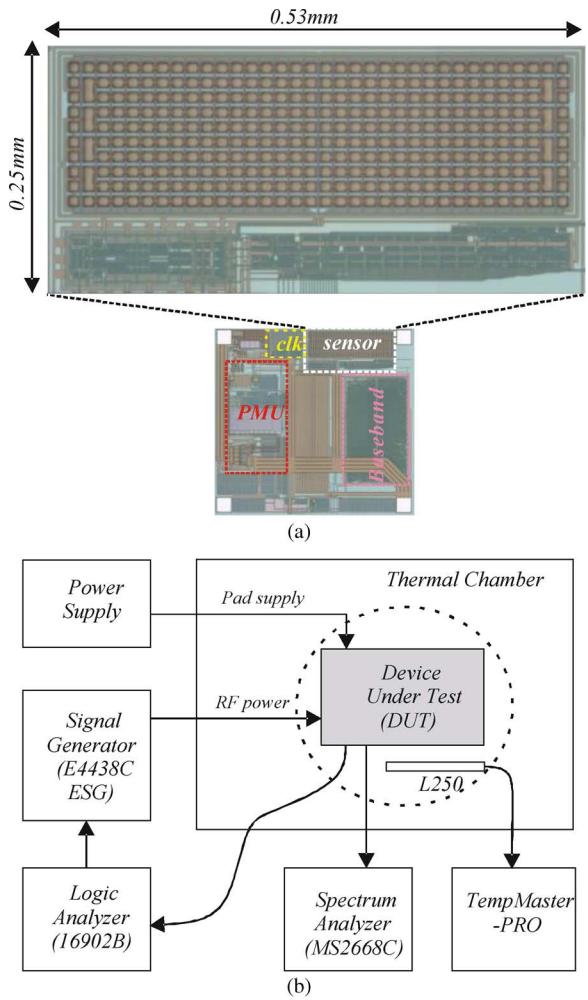

Fig. 8. (a) Microphotograph of the fabricated RFID tag with the designed embedded temperature sensor; (b) block diagram of the measurement setup for the embedded temperature sensor.

immunity. When the clock frequency is low, the current integration time becomes too long, leading to signal distortions especially when the sensor supply is only 1 V. This non-linear integration on the top plates voltages of C_{pt} and C_{ct} deteriorates the sensor performance. Notice that the designed system clock frequency would not fall into the low frequency range even in the worst process corner.

Because the sensor tag needs RF power to activate the internal building blocks, input power variation might affect the working states of the internal blocks (i.e. the rectifier's output) and the substrate noise environment. The sensor tag is tested under different input power levels to examine its sensing robustness. Fig. 10(a) shows the measured relative errors of the sensor tag under different input RF power levels (without matching the tag impedance and the 50 Ω output impedance of the signal generator). When the input power P_{in} is small, the received power P_{eff} by the tag is not adequate to activate all the tag loadings, leading to signal deterioration and a larger sensing error is observed. By increasing P_{in}, the sensor output becomes stable and exhibits no sensing shift within a wide range from 6 dBm to 10 dBm. However, if the input power is too high, the on-chip power-limiter will convert the excess power into heat which

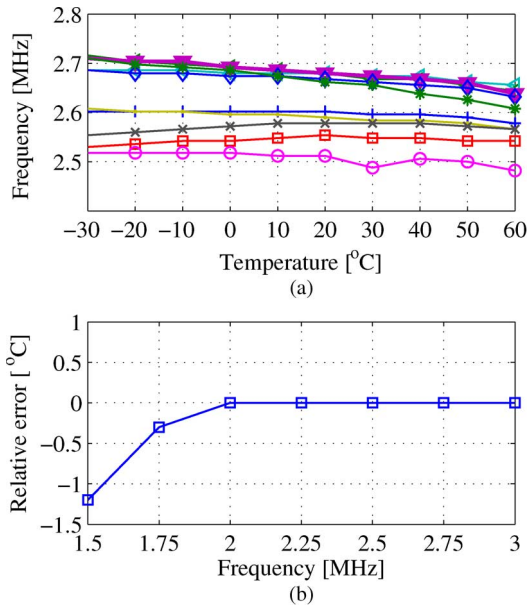

Fig. 9. (a) Measured system clock frequency at different temperatures; (b) relative sensing errors under different external clock frequencies.

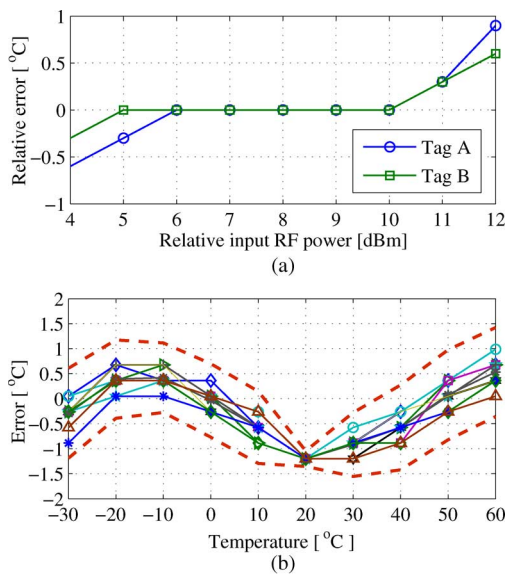

Fig. 10. (a) Measured relative sensing errors for different input RF power; (b) measured sensing error of 12 sensor tags after one-point calibration at 20°C.

then heats up the bipolar junctions. For bear die testing, this substrate heat is not effectively released and translates to a sensing error. This should not be a problem after deployment, as the sensor tag is normally attached to a larger thermal mass in typical applications, and the junction temperature change would be small even under high input power situation.

To check the sensor tag performance, 12 tag samples which lie in the nominal tag operation range are tested, with a 3.5 mW∼10 mW (6 dBm∼10 dBm) effective radiated power output from the RFID tester. A master curve is obtained by linearly fitting the averaged output data from 4 samples tags. Afterwards, individual PTAT calibration against the master curve is performed at 20°C. And the 3σ spread is evaluated with the measured 12 dies with an additional 0.5 LSB error added [5]. The remaining error profiles after calibration are shown in Fig. 10(b). A sensing error of ± 1.5°C (3σ) is achieved from -30°C to

TABLE I
COMPARISON OF REPORTED PASSIVE RFID TAG EMBEDDED CMOS TEMPERATURE SENSORS

	Technology	Sensing Power	Temp. range (°C)	Resolution	Inaccuracy	Calibration	Sampling Rate	FOM1† (nJ · °C²)	FOM2† (nJ · %²)
JSSC [8][a]	65 nm	10 μW	-75 to 125	0.03°C	±0.2°C	1-point	2.2 sa/s	0.75	2310
JSSC [16][a]	160 nm	5.1 μW	-55 to 125	0.02°C	±0.3°C	1-point	188 sa/s	0.011	0.75
JSSC [5][b]	180 nm	0.12 μW[c]	-10 to 30	0.20°C	-0.8/1.0°C	2-point	33 sa/s	0.14	72.9
JSSC [6][b]	180 nm	0.104 μW[c]	-20 to 30	0.35°C	±0.8°C	1-point	25 sa/s	0.51	42.6
CICC [15][b]	180 nm	0.22 μW	0 to 100	0.1°C	-1.6/3.0°C	2-point	100 sa/s	0.22	466
This work[b]	**180 nm**	**0.35 μW**[c]	**-30 to 60**	**0.3°C**	**±1.5°C**	**1-point**	**68 sa/s**	**0.46**	**57.2**

† $\mathrm{FOM1} = \mathrm{Energy/Conversion} \times \mathrm{Resolution}^2$; $\mathrm{FOM2} = \mathrm{Energy/Conversion} \times \mathrm{Relative\ inaccuracy}^2$; $\mathrm{Relative\ inaccuracy}(\%) = 100 \times \mathrm{Max\ Error/Specified\ Temperature\ Range}$;
[a] stand-alone temperature sensor targets at high resolution and high precision;
[b] passive RFID embedded temperature sensor targets at ultra-low power;
[c] sensor power without including the power to generate the supply and clock;

60°C. It can be observed from Fig. 10(b) that the sensing accuracy is linearity-limited instead of process spread limited. This sensor has a sensing resolution of 0.3°C and the conversion time is 14.5 ms, which is 68 samples/second.

Table I compares the performance of the proposed embedded temperature sensor with other state-of-the-art temperature sensor works, which have different performances and have different target applications. [8], [16] are stand-alone temperature sensors, targeting at high accuracy and high resolution. [2], [5], [6], [15] are passive RFID tag embedded sensors targeting at ultra-low power and moderate sensing accuracy. According to the smart temperature sensor performance survey [16], [17] has the best energy efficiency (FOM1, FOM2), while our work achieves a good tradeoff among robustness, sensing power and sensing accuracy in the passive RFID platform. Moreover, this work requires only one-point calibration for its process immunity, which ensures the sensing tag to be low cost.

V. CONCLUSION

An embedded temperature sensor in a passive RFID tag is designed, measured and demonstrated in this paper. Comprehensive analysis on the possible noise sources including the effects of device PVT spreads, comparator delay and offset, switch charge injection, capacitor charge leakage, as well as device noise are discussed. Circuit techniques such as offset cancelation, clock frequency compensation and multiple sample averaging are presented and verified. The fabricated sensor occupies an area of 0.14 mm^2 in the 1.24 mm^2 tag using TSMC 0.18 μm 1P6M standard process. Measurement results indicate that this embedded sensor achieves a sensing accuracy $\pm 1.5°\mathrm{C}$ (3σ) of from $-30°\mathrm{C}$ to 60°C after only one-point calibration.

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