Two-Step Channel Selection—A Novel Technique for Reconfigurable Multistandard Transceiver Front-Ends

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***Abstract*—This paper starts with a review of the prevailing channel-selection techniques utilized so far in the design of wireless transceiver analog front-ends before describing a novel *two-step channel-selection* technique, which handles the traditionally unwanted *image*, in radio frequency-to-intermediate frequency (RF-to-IF) or IF-to-RF frequency conversion, as a useful adjacent channel of the desired one, and selects deliberately either of them from IF to baseband (or baseband to IF). Thus, one more channel-selection possibility is created for both low-IF receivers and two-step-up transmitters. The consequential benefits of introducing channel selection at IF consist of two. First, many design specifications (such as phase noise and settling time) of the RF frequency synthesizer and local oscillator can be substantially relaxed. Second, a low-IF/zero-IF reconfigurable receiver and a direct-up/two-step-up reconfigurable transmitter can be synthesized to match better with narrowband-wideband-mixed multistandard systems. The operating principles of such architectures are presented in easy-to-understand complex-signal spectral-flow illustrations, and their practicability is demonstrated in the design of a Bluetooth/IEEE 802.11FH/HomeRF multistandard receiver. SPECTRE simulation results validate the reconfigurable functionalities mainly implemented by a triple-mode channel-select filter and a multifunctional sampling-mixer scheme.**

***Index Terms*—Analog front-end (AFE), Bluetooth, channel selection, Home RF, intermediate frequency (IF), IEEE 802.11 WLANs, low-IF, multistandard, narrowband, receiver, radio frequency (RF), transmitter, transceiver, wideband, zero-IF.**

I. Introduction

In addition to the aggressive requests of high integration and low-power dissipation, multistandard compatible is another essential feature of emerging wireless transceiver integrated circuits (ICs) to allow seamless interswitching one terminal through diverse cellular and wireless-network communication standards [1]. Prospective receiver analog front-ends (AFEs) for attaining those requirements are presently restricted in zero-intermediate frequency (zero-IF) and low-IF architectures, whose operating principles can be pictorially described by the complex-signal spectral-flow (CSSF) illustrations in Fig. 1(a) and (b), respectively. The basic components are the mixer, the frequency synthesizer (FS), the local oscillator (LO) with in-phase (I) and quadrature (Q) outputs (I/Q-LO), the channel-select filter (CSF), and the analog-to-digital (A/D) converter. Off-chip and power-hungry image-reject filters, hardly required in superheterodyne architectures, are no longer needed in zero-IF or low-IF architecture, since the image rejection is realized by signal cancellation in two parallel-operating channels (I and Q). However, when multistandard compatibility needs to be addressed, especially for narrowband-wideband-mixed applications, either zero-IF or low-IF implementation will encounter certain obstacles.

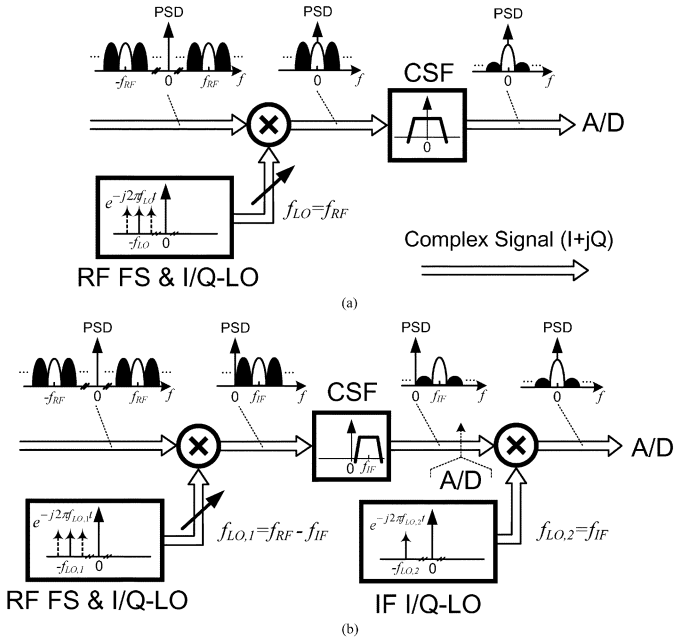

Fig. 1. CSSF illustrations of (a) zero-IF and (b) low-IF, where the A/D converter can be placed before or after the secondary mixing.

The zero-IF receiver is highly appropriate for both wide-band or spread-spectrum access standards such as WCDMA [2] and IEEE 802.11a/b/g [3], on the ground that the most problematic flicker noise and dc offset are only superimposed on a very small fraction of the desired channel. Thus, without excessive degradation in signal quality, those interferences can be suppressed, for instance, through capacitive coupling. Moreover, the image crosstalk due to unavoidable channel mismatch (namely, I/Q mismatch [4]) will be at a minimum level, as the image is only the upper (or lower) sideband of the one desired.

In contrast, for narrow-band standards the removal of flicker noise and dc offset also significantly damages the channel

Manuscript received April 29, 2004; revised October 26, 2004. This work was supported by the University of Macau Grant RG069/02-03S/MR/FST. This paper was recommended by Associate Editor W. Namgoong.

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Digital Object Identifier 10.1109/TCSI.2005.851722

spectra since spectrally efficient modulations generally peak at dc. To alleviate those pitfalls, the low-IF architecture [5] was therefore invented and demonstrated for the global system for mobile communication (GSM) application by downconverting the desired channel, in frequency, only to the vicinity of dc. Such a solution exhibits comparable integratability as zero-IF receiver and it is therefore extensively used in many narrow-band applications today, like in Bluetooth [6], global positioning system (GPS) [7], DCS-1800 [8], and IEEE 802.15.4 [9]. They are efficient mainly because the image-rejection requirement at relatively low IF is still a practical value. However, it is very unfeasible in applications like WCDMA. The adjacent channel selectivity (ACS) test case of WCDMA indicates that, in zero-IF operation, the required image rejection is 25 dB, whereas in low-IF operation the minimum value is 75 dB.

These architectural boundaries are the main rationales for restricting zero-IF architecture in wide-band applications, whereas narrow-band applications are generally designed in low-IF one. However, today urged wireless systems are typically narrow-band and wide-band mixed such as: WCDMA with GSM [10] and Bluetooth with IEEE 802.11b [11]. To address the demand, a low-IF/zero-IF reconfigurable receiver appears as a new alternative, since their radio-frequency (RF) AFEs are theoretically identical [see Fig. 1(a) and (b)]. For some standards that share the same spectrum, e.g., 2.4 GHz industrial-scientific-medical (ISM) band, the radio can be shared. The remaining inconsistency predominantly relies on the IF-to-baseband part, such that two dedicated IF-to-baseband chains for zero-IF and low-IF operations were still essential in the past designs [11], [12]. Their solutions, however, inefficiently enlarge the area required and may not be possible if more and more standards needed to be complied, imposing then the exploration of new techniques that can maximize the reusability of functional blocks.

This paper proposes both architectural and circuit techniques to synthesize a low-IF/zero-IF reconfigurable receiver and its complementary direct-up/two-step-up reconfigurable transmitter in one chain. Such architectures are originated from a two-step channel-selection (2-SCS) technique, which aims at relaxing both phase-noise and locking-time requirements of the RF phase-locked loop (PLL) FS through both analog [13] and digital [14] techniques. At the circuit level, novel structures consisting of a triple-mode CSF and a multifunctional sampling-mixer scheme satisfying both low-IF and zero-IF modes, are also proposed [15], [16].

The IC implementation of the proposed channel-selection technique comprising a frequency-downconversion I/Q-multiplexer [17], which can also be embedded in a pipelined A/D converter for digitization of both I and Q channels in one chain [18], will not be addressed here for brevity.

In Section II, the principles of the conventional and proposed channel-selection techniques are presented. Their advantages and disadvantages are also discussed. Based on the principles developed, a receiver design for multistandard applications is described in Section III. Effective circuit solutions for implementing the functional blocks and their simulated performances

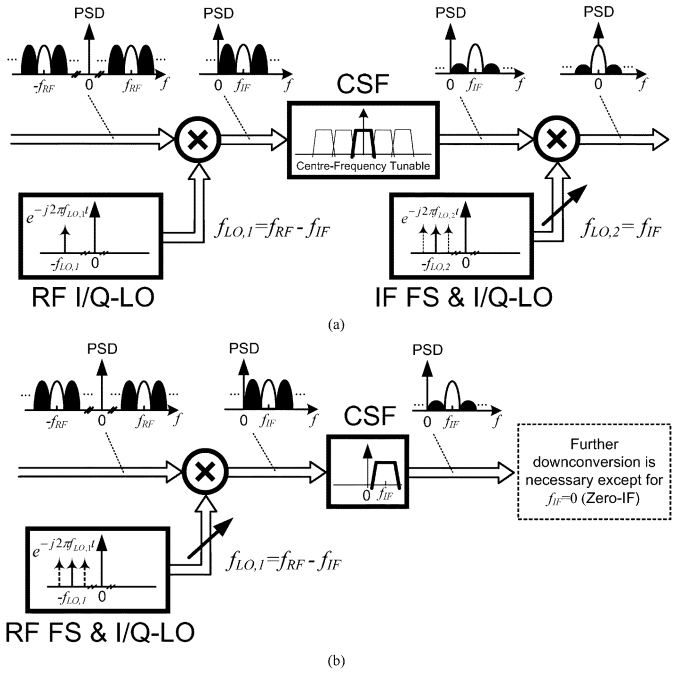

Fig. 2. CSSF illustrations of conventional channel-selection methods. (a) Case A. (b) Case B.

are addressed together in Section IV. Finally, a transmitter embedding similar techniques is briefly summarized in Section V, and the conclusions are drawn in Section VI.

II. Conventional and Proposed Channel-Selection Schemes

Almost all voice- and data-centric standards utilize (or partially utilize) frequency-division multiple-access (FDMA) to divide the entire frequency bands into channels for multiple users. The mission of the AFE is to retrieve the sought channel from the air, amplifying it and downconverting it from RF to baseband for demodulation. This process is well known in superheterodyne receivers, namely, the sought channel is gradually downconverted and filtered from RF to different IFs, and finally to the baseband. On the other hand, image-reject receivers use a series of steps for channel selection, which usually comprise the combination (with possible permutations) of the three main blocks, the FS, the LO and the CSF. Depending on the operating frequency (i.e., RF or IF) and movability of the blocks, it will typically lead to the subsequent two alternative architectures $-\boldsymbol{A}$ and $\boldsymbol{B}$.

A. Conventional: Fixed $\mathrm{LO_{RF}}$+ Varying IF

The first type of architecture [19] is depicted in Fig. 2(a), where a fixed-frequency RF LO $(\mathrm{LO_{RF}})$ is exploited to perform a large step of RF-to-IF downconversion. After that, the desired channel is extracted at a relatively low-IF value by using a center-frequency-controllable CSF. Ultimately, the sought channel can be downconverted to the baseband by utilizing another FS and LO. This structure, first, highly relaxes the phase-noise requirement of the RF LO because it is free from locking. Second, since the channel-select filtering is performed prior to the IF-to-baseband downconversion, the operating

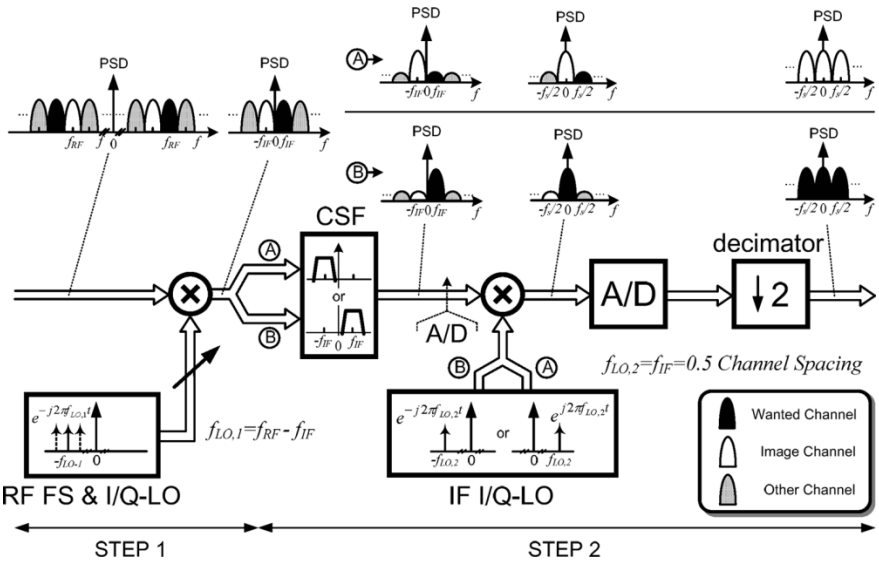

Fig. 3. CSSF illustration of low-IF receiver with 2-SCS technique, where the A/D converter can be placed before or after the secondary mixing.

frequency and the phase-noise requirement of the IF FS and LO can be highly reduced. However, the main bottleneck of this permutation is the required broadband-tunable filter, which requires accurate control of the center frequency. For instance, in Bluetooth, if the entire band (totally 79 channels) is downconverted to baseband in the first mixing, a 1-MHz bandpass filter with 79 different center frequencies in a range of 80 MHz (-40 to 40 MHz) is needed. Moreover, the agility of the filter should be high to perform also frequency hopping. With such rigid constraints, it would be very difficult to apply this method in modern applications. However, a special case of this architecture was reported for DECT application, namely wide-band IF double-conversion receiver [20], which employs a fixed-frequency LO cooperating with a wide-band lowpass filter in the first downconversion, whereas the channel selection is shifted to the second IF. In this way, the operating frequency of the succeeding stages can be reduced, but this benefit comes at the expense of an increase in the linearity requirements of the wide-band lowpass filter to prevent channel-to-channel intermodulation.

B. Conventional: Varying $\mathrm{LO_{RF}}$+ Fixed IF

A second alternative architecture [21] is shown in Fig. 2(b) that uses a RF FS and a $\mathrm{LO_{RF}}$ to cover all the possible channel positions in the RF frequency band of interest, then the desired channel is downconverted to the baseband, at which only a fixed CSF is needed. This structure is well appropriate for the state-of-the-art IC designs since the current developments of FSs (based on PLL architectures) have presented results of operating frequencies in the gigahertz range with adequate performance. On the other hand, a fast-settling and broadband-tunable oscillator is much easier to implement than its filter counterpart, and a baseband filter is much simpler and more power-efficient than a bandpass one. The exhibition of these compromised features confirms the suitability of this type of architecture for almost all kinds of image-reject receivers (e.g., Hartley, low-IF, Weaver and zero-IF) [21].

Concisely, the two traditional architectures just presented include movable circuit blocks either at the IF (***Case A***) or RF (***Case B***). A novel method efficiently combining both alternatives will be described next.

C. Proposed Two-Step Channel Selection: Coarse-Varying $\mathrm{LO_{RF}}$+Fine-Varying IF

The technique, as its name implies, uses the partition of the channel selection process between the RF and IF AFEs, such that only a *coarse* selection is necessary at the RF and a fine selection will be completed at the IF. The key to turn this technique efficient is a new concept of image.

It is well known that image is an unwanted interference in frequency conversion (either up or down). In image-reject receivers, after quadrature downconversion and based on complex-signal analysis, the desired channel and its image (twice the IF offset in frequency from the desired one) will be located at the same IF but with a complex conjugate representation. Now, suppose the IF AFE can flexibly select either of them, a channel selection is accomplished without any prerequisite needed in the radio part. To implement such a technique, some specific IF values, i.e., $n + 0.5$ channel spacing (CS) for $\mathrm{n} = 0, 1, 2, 3\ldots$, should be used to select one of the adjacent channels as the image of the desired one. For instance, Fig. 3 can describe the entire operation if half (i.e., 0.5) CS is selected. Such operation has two different IF-to-baseband operation modes, labeled as $\mathbf{A}$ and $\mathbf{B}$, where the CSF has a tunable center frequency at either $+\mathrm{IF}$ or $-\mathrm{IF}$, while the IF LO needs to provide not only the conventional 0° and 90°, but also 180° and 270°, to make a selection between the upper and lower sidebands. The A/D converter can be placed prior or after the secondary mixing to trade the A/D conversion rate with the mixer implementation (i.e., analog or digital). The final shared operations are decimation and image elimination through a simple digital filter.

As introduced next, the required IF values will not pose any limitation, rather, it has other advantageous features. For the reconfigurable functionalities, only simple analog circuitry with digital control is needed.

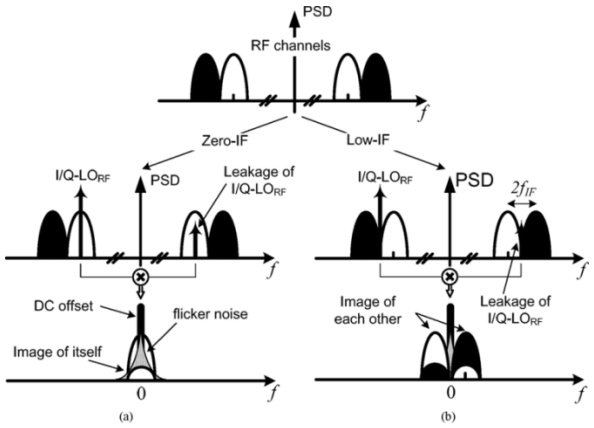

Fig. 4. CSSF illustration of interference locations (with also I/Q-mismatch). (a) $\mathrm{IF} = 0$. (b) $\mathrm{IF} = 0.5$ CS.

- *IF Selection*—When $\mathrm{IF} = 0$ (i.e., zero IF), the image channel is the sideband of the desired signal itself as shown in Fig. 4(a), although the image-rejection requirement is much relaxed, the low-frequency disturbance becomes very serious. Conversely, when the IF value gets higher, the required image rejection needs to be increased by the power difference between the image and the desired channel. To establish a good compromise between the low-frequency disturbance and the image interference, half channel-spacing (CS) can be chosen [5], as shown in Fig. 4(b). This situation is especially true since in most wireless communication standards, the power of the adjacent channels increases with their frequency offset from the desired one. For example, in GSM (Bluetooth), the power of the first adjacent channel is only 18 dB (5 dB) higher than the desired one, the required image rejection is therefore only $\sim$32 dB ($\sim$20 dB). Furthermore, the LO will be locked in between every channel, any unwanted LO leakage (e.g., through the substrate) will not degrade the signal quality. For the succeeding filter and A/D converter, however, their operating frequency has to be increased with the IF, implying higher power consumption. In general, only up to four CS will be used as the IF in image-reject receivers to satisfy many design tradeoffs [6]–[9]. This indicates that the proposed "$n + 0.5$ CS IF" with $\mathrm{n} = 0$ to 3 are feasible, and will not complicate the whole design.
- *Functional blocks for second step*—As mentioned in Sub-Section II.B, a RF FS can effectively be used for the first step. For the second step, we propose to implement the CSF by slightly modifying the structure of a conventional complex (or polyphase) filter, while the four-phased IF I/Q LO can be replaced by a sampling-mixer scheme embedding a programmable analog double-quadrature sampling (A-DQS) technique [13]. In this way, the circuit overheads can be minimized.

To give a better description about the practicability of those functional blocks, the design and implementation will be presented in Section IV, based on a practical receiver design that will be addressed in Section III. In the meantime, the advantages of such a technique are highlighted first.

- *Simplified channel up/down-conversion at RF*—The resulting simplification brought by the two-step channel selection is explained by using Fig. 5, which is based on a series of Bluetooth GFSK modulated channels that are being selected in the ISM band. To demonstrate the benefits of the proposed channel selection technique, three cases are considered and compared. Conventionally, in low-IF architecture, when the IF equals to 0.5 channel-spacing (*case 1*), each channel requires a LO for downconversion. Differently, with the novel proposed architecture (*case 2*), the step-size of the FS is doubled, which implies that the division ratio (also named as modulus) in the PLL will be halved since selection between C_5 and C_6, or C_7 and C_8 will be done at the IF. For an integer-N frequency synthesizer, a large step size implies a higher reference frequency can be utilized. Thus, the loop bandwidth (BW) of the PLL is also enlarged by the same factor tor shorten the PLL settling time and reduce the phase noise from the local oscillator without the stability and overshoot penalties. Moreover, a higher reference frequency reduces the division ratio in the modulus, as well as the the phase noise contributed by the reference frequency. Furthermore, fewer locking positions also simplify the modulus anatomy, thereby enhancing the channel speed. The detailed relationships among all of these issues are clearly analyzed and discussed in [22].

  The principles above referred can be further extended to other or multiple IF values. For instance, if both 0.5 and 1.5 channel-BW spacings are considered (i.e., double IF's), the FS locking positions could then be changed to *case 3*, as shown in Fig. 5 also. The channels C_9, C_{10}, C_{11} and C_{12} would be downconverted together by the RF LO, $f_{\mathrm{LO},9-12}$. The selection between the four channels can be performed by a filter with four center-frequency positions, and a two-frequency-four-phased IF I/Q LO. The step-size of the FS can be extended to four channels spacing to further enhance the abovementioned relaxations. These features are decisively important for frequency-hopping spread-spectrum (FHSS) systems such as Bluetooth, where the PLL settling time and phase noise always contribute a design trade-off. RF-to-IF channel partitioning is therefore a key way to make compromise between these two relevant PLL characteristics.

  Similarly, the abovementioned considerations are also valid for two-step-up transmitter; allowing only one specification-relaxed FS and LO to fulfill both transmit and receive operations in a transceiver.
- *Facilitated reconfigurations in receiver and transmitter*—Another corollary of two-step channel selection is the fact that when two (or four) narrow-band channels are considered as a wide-band one [in Fig. 5, *cases 2 and 3*], the LO can now be located at the carrier of the wide-band channel to perform direct frequency down (up) conversion, i.e., a zero-IF (direct-up) operation! Of course, the BW of two (or four) narrow-band channels is usually not exactly equal to a wide-band channel, but in order to fix it the cost would be a BW-tunable lowpass

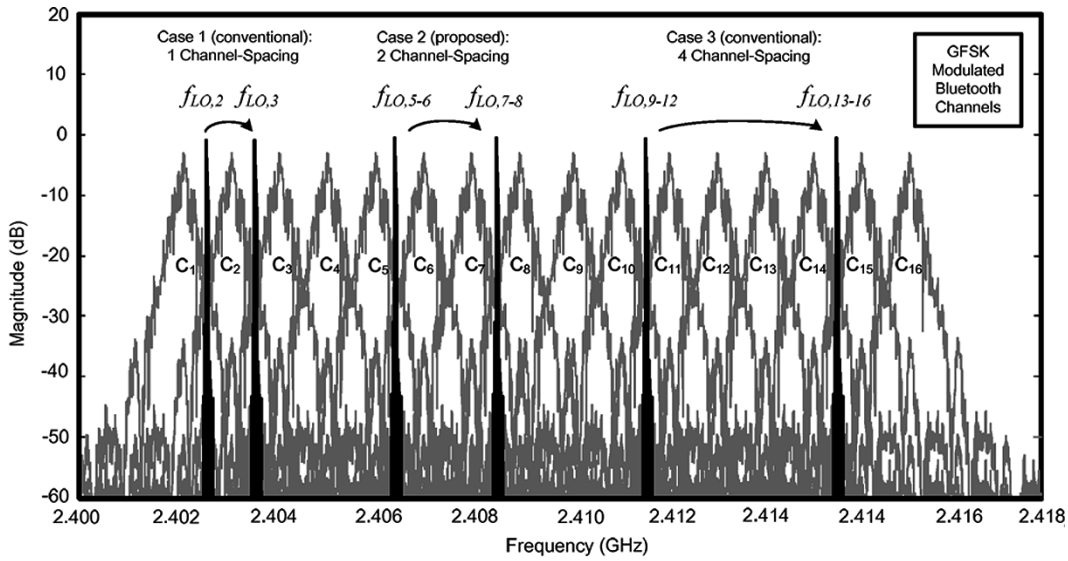

Fig. 5. LO locking positions with conventional structures (case 1) and with the novel proposed 2-SCS technique (cases 2 and 3).

TABLE I
SUMMARY OF KEY PHY SPECIFICATIONS OF 2.4-GHz ISM BAND FHSS STANDARDS

Standard	Channel Spacing	Data Rate	Distance	Hop Rate
Bluetooth	1 MHz	1 Mbps	10 M	1600 Hop/s
HomeRF	5 MHz	5,10 Mbps	100 M	75 Hop/s
IEEE802.11FH	1 MHz	1,2 Mbps	150 M	2.5 Hop/s

filter, which is commonly needed in multistandard compatible designs [23]. The IF-to-baseband downconversion in low-IF receiver can be bypassed, resulting in a clear advantage to the receiver that can operate in low-IF mode for narrowband, or zero-IF mode for wideband. Similarly, reuse the principle in transmitter design allows also two modes of operation, i.e., two-step-up and direct-up.

To show how these two advantages smooth the progress of multistandard receiver design, an example reinforcing these techniques will be presented next. For simplicity, two narrow-band channels in low-IF mode would be considered as one wide-band channel in zero-IF one.

III. LOW-IF/ZERO-IF RECONFIGURABLE RECEIVER DESIGN

A. System-Design Overview

The three selected standards for our demonstration are Bluetooth, IEEE 802.11FH, and HomeRF [24]. Their key physical layer (PHY) specifications are summarized in Table I. As the table shows, their PHY are very similar and they operate in the same frequency band, only one antenna and transceiver RF AFE will be sufficient to satisfy both transmit and receive operation requirements, thus allowing the implementation of compact and high-performance multistandard transceivers. Moreover, in the baseband AFE, automatic-gain control (AGC) blocks cooperating with both filters and A/D converters will allow efficient equalization (likely required in 802.11FH and HomeRF), as well as coherent Gaussian frequency shift-keying (GFSK) demodulation in the digital signal processor (DSP). The remaining design challenges are associated with their different CS and channel BWs, leading to several design tradeoffs or extra requirements on the functional blocks that can be highlighted as follows:

1) Interference by Low-Frequency Disturbance or Image: As mentioned before, the image problem can be considerably relaxed if the receiver is implemented in zero-IF being also highly appropriate for the wide-band HomeRF. However, flicker noise and dc offset problems require AC-coupling or other dc-offset cancellation circuits, which will damage the narrow-band Bluetooth and IEEE 802.11FH signals and lengthen the receiver settling time. Alternatively, by employing low-IF architecture to avoid the low-frequency disturbance, it would be at the circuit overhead of an IF downconverter and an IF I/Q LO, a RC-CR network or a clock-frequency divider for I/Q-phase generation, as well as of an increase in the required image rejection.

2) FS and LO: Although the covered standards operate in the same spectrum, this does not eliminate the need for different locking positions and step-sizes for different CS. Moreover, due to the FHSS feature of covered standards, agile FS and high spectral-purity oscillator are still mandatory.

3) CSF: Independent to the architecture (low-IF or zero-IF), a filter with tunable BW is required to comply with both narrow-band and wide-band channels.

B. Proposed Receiver Architecture

A low-IF/zero-IF reconfigurable receiver, as depicted in Fig. 6, is proposed to address the aforesaid trade-offs and requirements. The receiver, which would be in low-IF mode for Bluetooth and IEEE 802.11FH, and in zero-IF mode for HomeRF, will be composed by the following functional blocks:

1) IF Selection for Different Applications: The standard approval selectivity requirement is the main concern for IF selection. For Bluetooth, the power of the 1st adjacent channel is comparable to the desired channel as shown in Fig. 7. To stay far from the low-frequency disturbance and to compromise with the image rejection, half-channel-spacing IF is a good choice. In case the low-frequency disturbance is still serious, higher IF

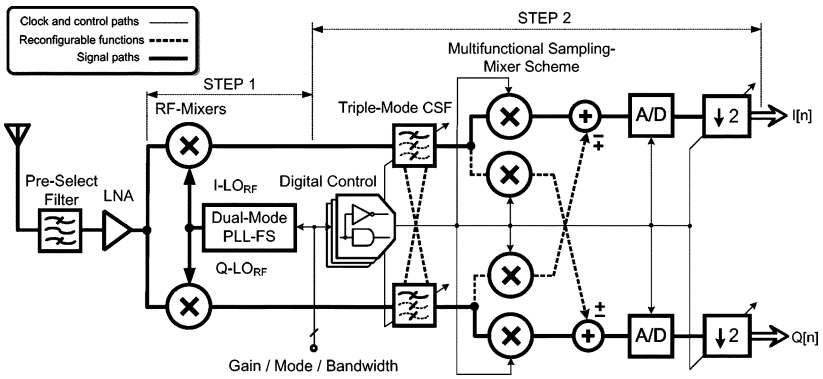

Fig. 6. Proposed low-IF/zero-IF reconfigurable receiver.

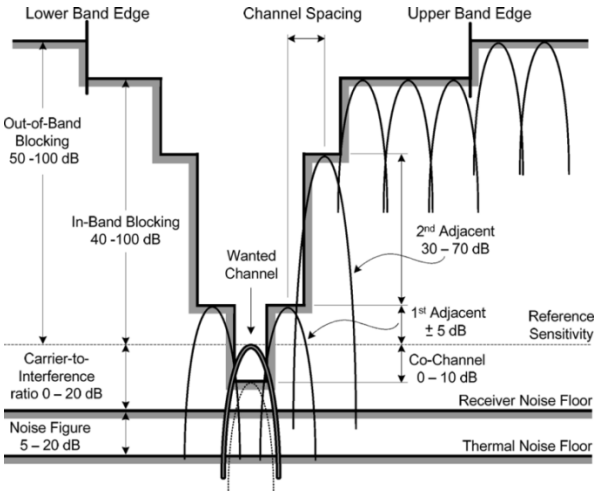

Fig. 7. Selectivity requirements of Bluetooth.

values can be chosen, of course, the overhead is the highly increased image-rejection requirement. In these particular applications, half-channel-spacing is selected to match the proposed channel-selection technique on one hand, minimize the low-frequency disturbance and the required image rejection ($\sim$20 dB) on the other. The situation is similar for IEEE 802.11FH, but for HomeRF, its BW is much wider and the frequency-hopping speed is slow, so zero IF with offset cancellation is chosen.

2) Dual-Mode FS: Since the RF FS only provides *coarse* channel selection, both phase-noise and settling-time requirements are relaxed. This implies the use of a simple integer-N PLL, rather than its fractional-N counterpart that suffers from spurs. Moreover, in integer-N architecture, only two additional frequency dividers would be sufficient to provide two different step-sizes based on one reference clock, the reference frequency therefore can be kept high enough to maintain low phase noise. A possible topology for the proposed application is illustrated in Fig. 8.

3) Triple-Mode CSF: To achieve high dynamic range and also provide image rejection, active-RC based polyphase filters are usually the most adequate architecture, which also simultaneously allow programmability in gain, BW and center frequency. Additionally, by using some digital control, it can be configured as a wide-band lowpass filter (LPF) for zero-IF,

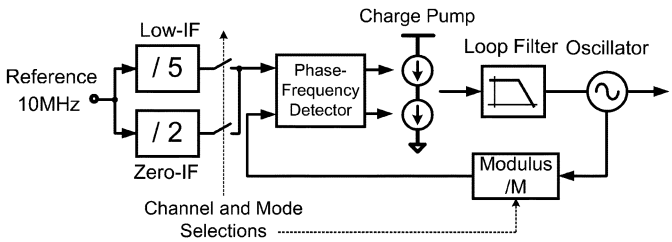

Fig. 8. Single-band dual-mode integer-N PLL-FS.

or a narrow-band positive-/negative-complex bandpass filter (+C-BPF/−C-BPF) for low-IF. (The details will be presented in Section IV).

4) Multifunctional Sampling-Mixer Scheme: In low-IF mode, the scheme will perform DQS for downconversion (i.e., I/Q phases are inherently generated digitally), channel selection and secondary image rejection. Alternatively in zero-IF mode, the scheme performs simple baseband sampling for digitization [16]. The mode selection can be implemented again by simple digital control, and is embedded in the clock-phase generator. The details will also be addressed later; meanwhile, the overall working principles are presented first.

C. Step-1: RF AFE in Low-IF Mode

The reconfigurable receiver architecture (Fig. 6) is characterized by performing the channel selection in two steps. Similar to the conventional approach in the RF AFE, the first step comprises a RF selection that will include a pre-selection filter and a low-noise amplifier (LNA) for acquiring and amplifying the required RF channels. After that, a FS performs the frequency downconversion at the first stage of mixers. The corresponding CSSF illustrations are shown in Fig. 9(a), with the selected IF value set to 0.5 channel-spacing and the assumption that the sought radio channels, at the first step of 2-SCS, are channels C_N and C_{N+1}, leading to the pre-selected RF input signal $x_{\rm RF}(t)$

$$x_{\rm RF}(t) = C_N \cos[2\pi f_N t + \Phi_N(t)] + C_{N+1} \cos[2\pi f_{N+1} t + \Phi_{N+1}(t)] + C_{N+2} \cdots \quad (1)$$

where C_N, f, and Φ are the envelope, frequency, and phase of the radio channels, respectively. In the second step, depending

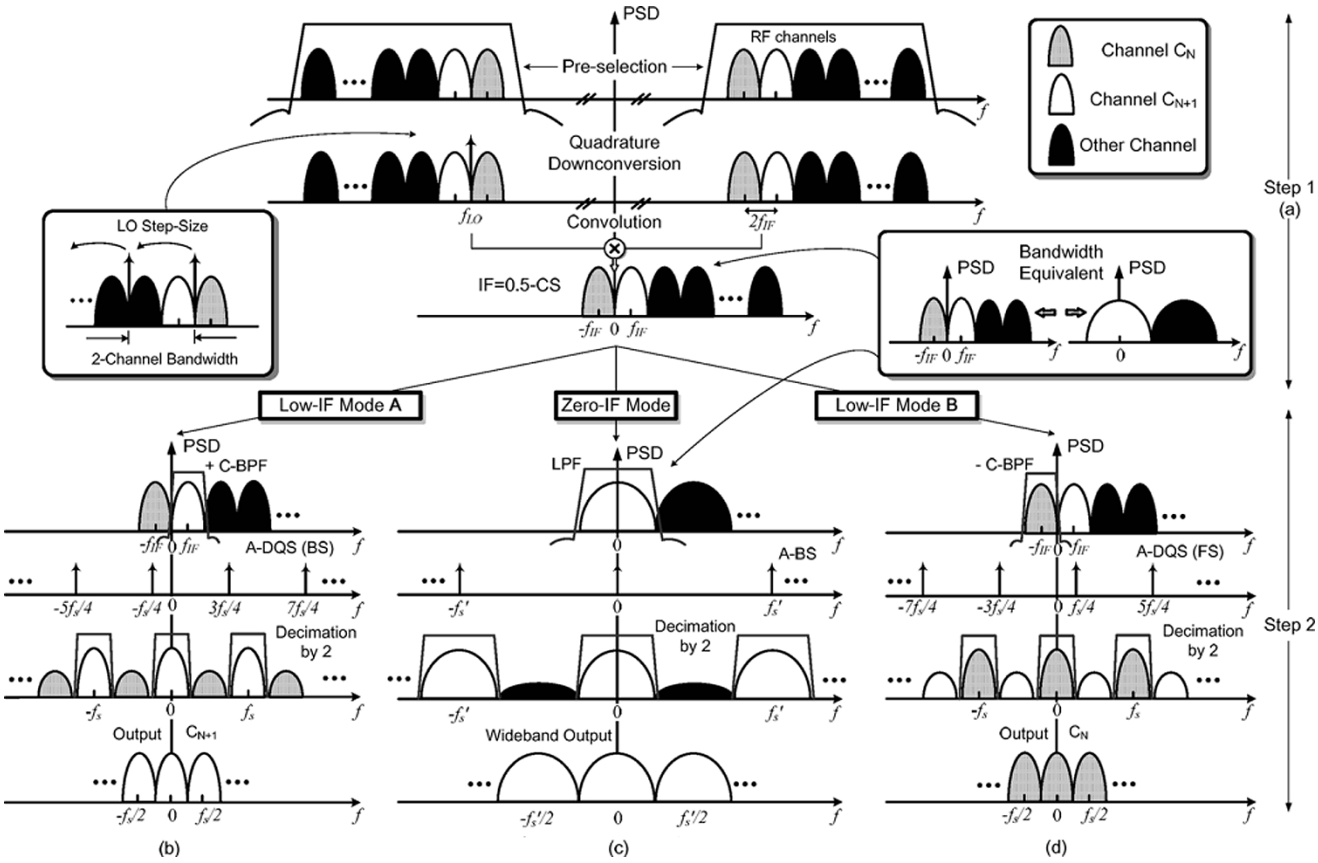

Fig. 9. CSSF illustrations of receiver showed in Fig. 6. (a) Step-1: RF AFE. (b) Step-2: low-IF mode-A. (c) Step-2: zero-IF. (d) Step-2: low-IF mode-B.

on the desired channel, which will be either C_N or C_{N+1}, two alternatives should be considered.

D. Step-2: IF AFE in Low-IF Modes A and B

Illustrated in Fig. 9(b) and (d) are the proposed second steps in low-IF modes A and B, respectively. The CSF would be implemented by a reconfigurable complex bandpass filter with two possible passbands ("dual-mode") that can be centered at either $-f_{\rm IF}$ or $f_{\rm IF}$ for selecting between channels C_N and C_{N+1}, respectively. The programmable A-DQS, performed by a multifunctional sampling-mixer, will result in either a backward or forward frequency shifting in low-IF modes A or B, respectively. Once the sampling frequency is four times of the IF (i.e., 2 MHz in this case), [13], [14] this kind of DQS technique can inherently provide frequency downconversion and sampling functions, with an additional flexibility for controlling the acquisition of either the upper or lower sideband. In forward frequency shifting, channel C_N will be obtained at $\pm nf_s$ for $n = 0, 1, 2\ldots$ whereas channel C_{N+1} (image of C_N) is shifted to $\pm nf_s/2$ for $n = 1, 3, 5\ldots$ Similar results can also be obtained in backward frequency shifting, where the roles of channels C_N and C_{N+1} will be reversed. Both cases do not suffer from the problematic dc offset and flicker noise as the frequency values are now shifted to $\pm nf_s/4$, for $n = 1, 3, 5\ldots$ Afterwards, the $y(nT)$ can be digitized by two Nyquist A/D converters, and the final I and Q data at a rate of $f_s/2$ can be obtained after passing through a high-order digital decimation filter for sharp-transition filtration and decimation.

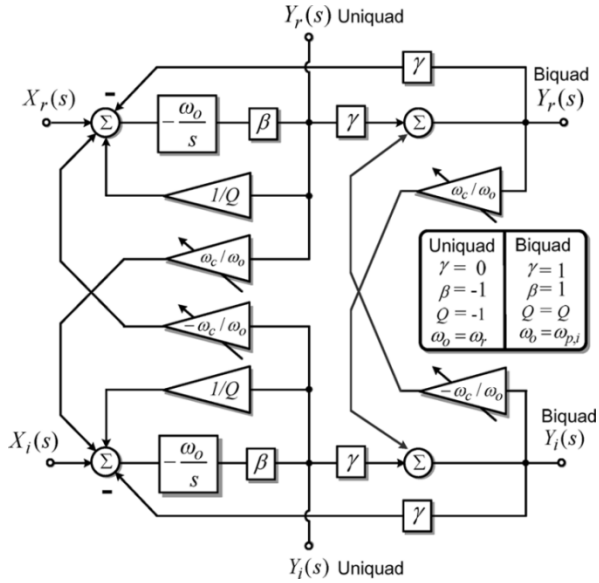

Fig. 10. Block schematics of center-frequency-tunable uniquad/biquad stages.

E. Step-2: IF AFE in Zero-IF Mode

With the same RF AFE, the main difference in the zero-IF mode, when compared with low-IF, relies on the baseband part. Once two narrow-band channels are considered as a single wideband one, as shown in the upper part of Fig. 9(c), the LO is at the same frequency as the channels' carrier in order to directly downconvert it to dc. The CSF should be now in the low-

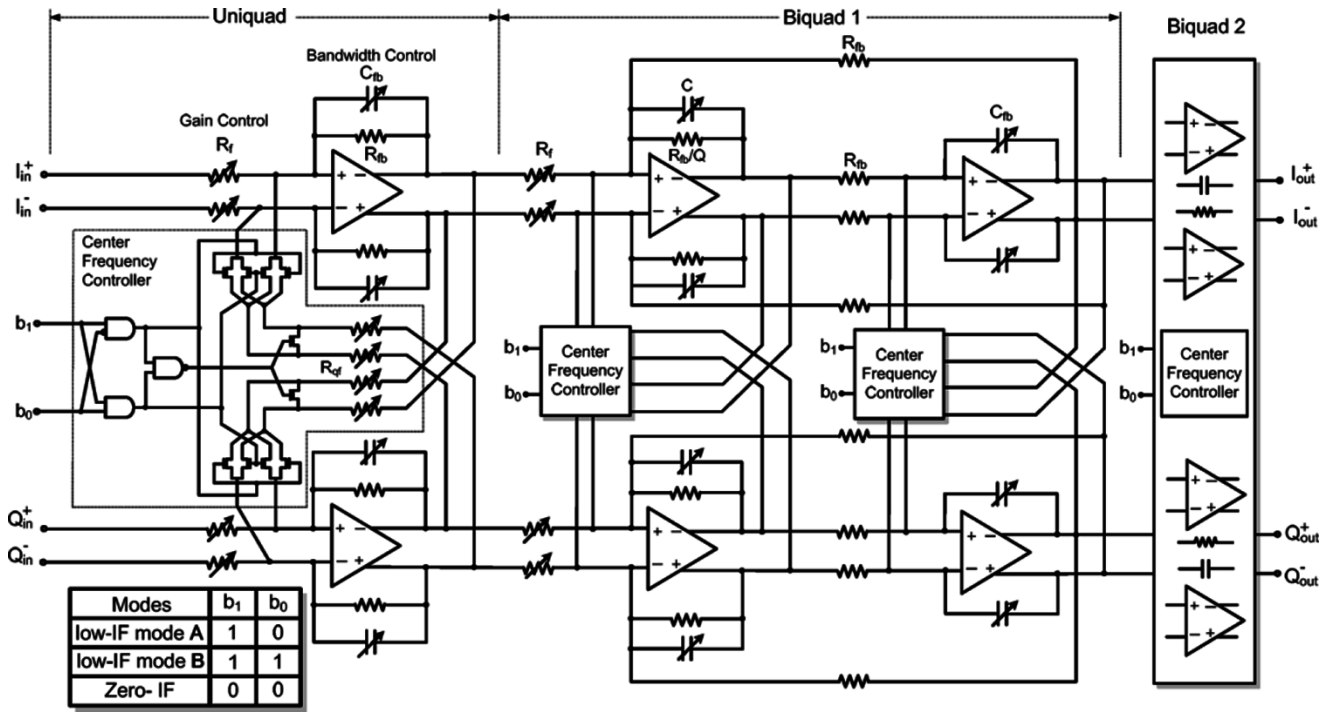

Fig. 11. Triple-mode CSF with active-RC realization.

pass mode. Regarding the double quadrature sampling, it will be replaced by its sub-set operation—analog-baseband sampling (A-BS). The sampling frequency f_s is increased to 10 MHz in order to match the HomeRF standard with an oversampling ratio (OSR) of two to reduce aliasing. Clearly and independent to the modes of operation, the final demodulation will be performed at dc, allowing the use of high-effective analog zero-IF GFSK demodulator [25] or digital coherent demodulator.

The subsequent digital operations in zero-IF mode will be analogous to those in low-IF mode, and they can be implemented in the DSP.

IV. Reconfigurable IF AFE Design

To implement a receiver adequate for the previously referred applications (except for the simple modification needed in the FS presented in Fig. 8), only the IF-to-baseband functional blocks need to be reconfigured as introduced next.

A. Triple-Mode CSF

1) Basic Principles: To fulfill the filtering modes described in Fig. 9, only a small number of center-frequency locations are needed. By doing lowpass-to-complex-bandpass linear transformation defined by $j\omega \rightarrow j\omega - j\omega_c$ (where ω_c is the tunable center frequency), the characteristics of the filter such as phase linearity and passband ripple are all preserved after transformation. If the filter is an even nth-order all-pole filter, the transfer function can be written as

$$H(s+j\omega_c) = \prod_{i=1}^{n/2} \frac{K_i \cdot \omega_{p,i}^2}{(s+j\omega_c)^2 + (\omega_{p,i}/Q_{p,i})(s+j\omega_c) + \omega_{p,i}^2} \tag{2}$$

whereas an odd nth-order one has the form

$$H(s+j\omega_c) = \frac{K_r \cdot \omega_r}{(s+j\omega_c) + \omega_r} \cdot \prod_{i=1}^{(n-1)/2} \frac{K_i \cdot \omega_{p,i}^2}{(s+j\omega_c)^2 + (\omega_{p,i}/Q_{p,i})(s+j\omega_c) + \omega_{p,i}^2} \tag{3}$$

where $s = j\omega, K_i$, and K_r are constants, ω_r is the real pole and $Q_{p,i}$ is the quality factor of the conjugate pole pairs with pole frequency $\omega_{p,i}$. Based on (2) and (3), the generalized block schematics of uniquad and biquad implementation can be depicted in Fig. 10. It showed that by changing the quadrature-feedback factors between the I and Q channels, the center frequency can be controlled to form the intended filtering modes, i.e., lowpass ($\omega_c = 0$), negative ($\omega_c = -\omega_c$) or positive ($\omega_c = +\omega_c$) complex bandpass.

2) Implementations: Wireless transceivers require a high-linear filter for channel selection, an active-RC realization constitutes an adequate choice. Fig. 11 shows the simplified 5th-order implementation, where the complex uniquad has been obtained by modifying the circuit presented in [26] (which has been traditionally used to construct high-order polyphase filters through cascading) with the introduction of a center-frequency controller. However, to realize an higher order Butterworth characteristic with complex poles, a novel complex biquad structure will be proposed here, which is based on the Tow-Thomas architecture. By using a simple capacitor (resistor) bank [27] in the *feedback* capacitor C_{fb}'s (forward resistor R_f's), the BW (gain) can be digitally scaled. The filter center frequency will be set-up by a 2-bit digital controller, which organizes the MOS array of switches in such a way that it will either connect the I/Q cross-feedback resistors R_{qf}'s to the common-mode voltage for centering the filter at DC, or switches the differential terminals to centre the filter at either $+\omega_c$ or $-\omega_c$. This type

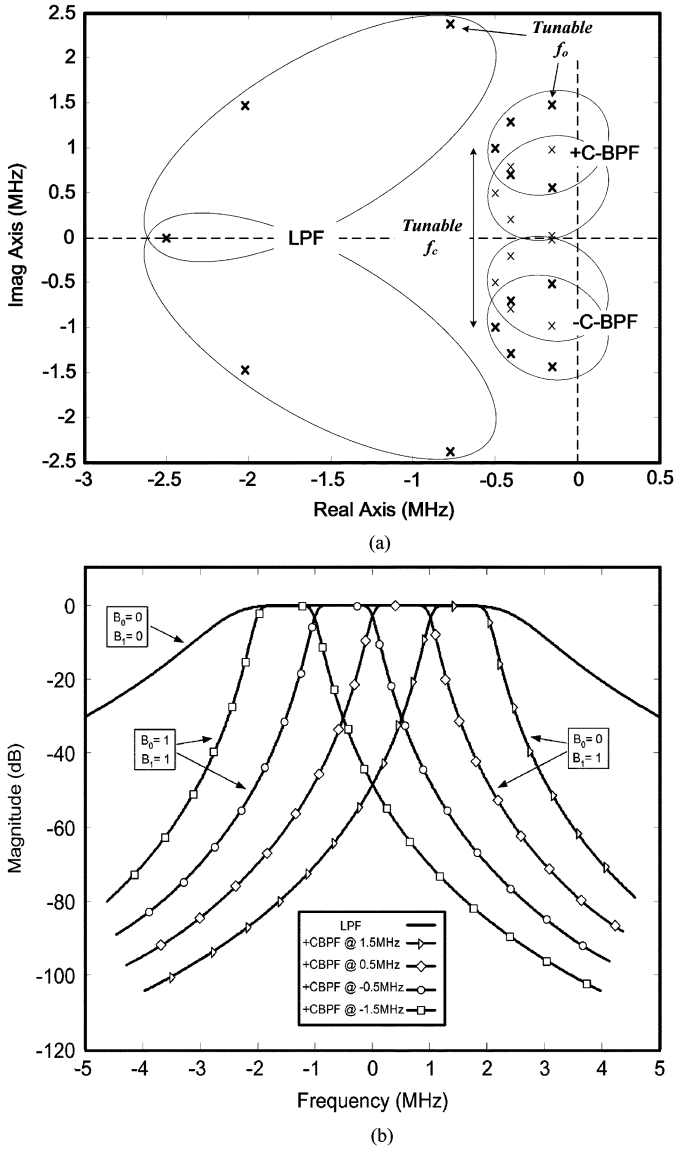

Fig. 12. Triple-mode filter. (a) Pole-zero plot. (b) Magnitude responses.

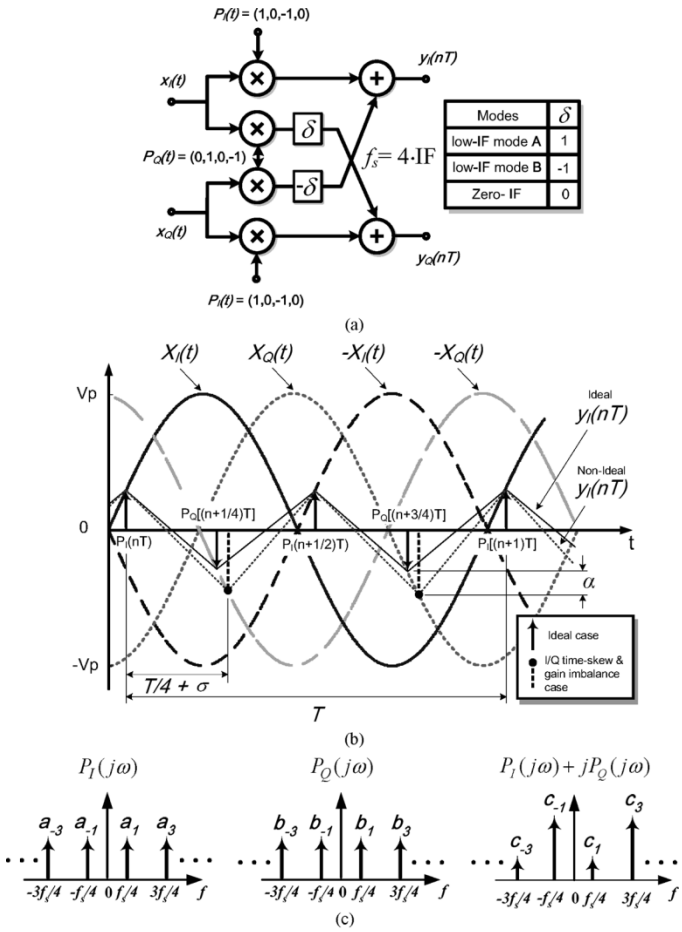

Fig. 13. (a) Block schematic of A-DQS/A-BS. (b) Time-domain illustration of ideal and nonideal A-DQS in low-IF mode A. (c) Non-ideal output spectrum of A-DQS in low-IF mode A.

of arrangement allows the elimination of the loading effects in mode-switching (mode-A or mode-B), and reduces the distortion caused by the MOS switches since the R_{qf}'s are always connected to either the common-mode or the virtual ground of the op-amp. In addition, the different R_{qf}'s are also implemented by resistor banks allowing further enlargement of the center-frequency range of adjustability.

Another important consideration is the fact that ac-coupling does not raise any problem in both low-IF and zero-IF modes because HomeRF is wide-band and the corresponding settling time requirements are very low (i.e., slow-frequency hopping, as presented in Table I). For the Bluetooth and IEEE 802.11FH, since 99% of their power is concentrated in the frequency range between 70–430 kHz, this implies that either AC-coupling or a slight increase in the dynamic range of the A/D converter can effectively alleviate the dc offset and the flicker noise problem.

3) Simulation Results: The tunable pole locations and the triple-mode simulated frequency responses of the baseband filter, obtained with the parameters of a 0.35-μm CMOS in SPECTRE, are shown in Fig. 12(a) and (b), respectively. In zero-IF mode with 5-MHz BW, the first adjacent channel suppression is approximately 30 dB. In low-IF mode, the BW is changed to 1 MHz, and the center frequency is controlled to be at either 0.5 or 1.5 MHz to show possibility of double-IF channel selection, being the first adjacent channel rejection also approximately 30 dB.

B. Multifunctional Sampling-Mixer Scheme

1) Basic Principles: By employing the A-DQS technique [13] to achieve the downconversion and channel selection, no real FS, LO and I/Q phase generator are needed. The block schematic of the multifunctional sampling-mixer scheme is shown in Fig. 13(a). Firstly, in low-IF mode-A or mode-B, the sampling frequency $f_s(1/T_s)$ is set to four times the intermediate frequency, $f_{\rm IF}$, to transform the mixing operation to a sequence of integer-weighted analog sampling of values $\cos(n\pi/2) = [1, 0, -1, 0]$ and $\sin(n\pi/2) = [0, 1, 0, -1]$. These values imply that the implementation can be differential in the analog domain [13] or sign-bit flipping between -1 and 1 in the digital domain [14] to obtain the 4-phases LO signal, $e^{\pm j2\pi f_{LO}t} = e^{\pm j(\pi/2)n} = \cos((\pi/2)n) \pm j\sin((\pi/2)n)$ for $\mathrm{n} = 1, 2, 3\ldots$ The ideal complexiod are shown in Fig. 9(b) and (d) for low-IF mode-A and mode-B, respectively. However, due

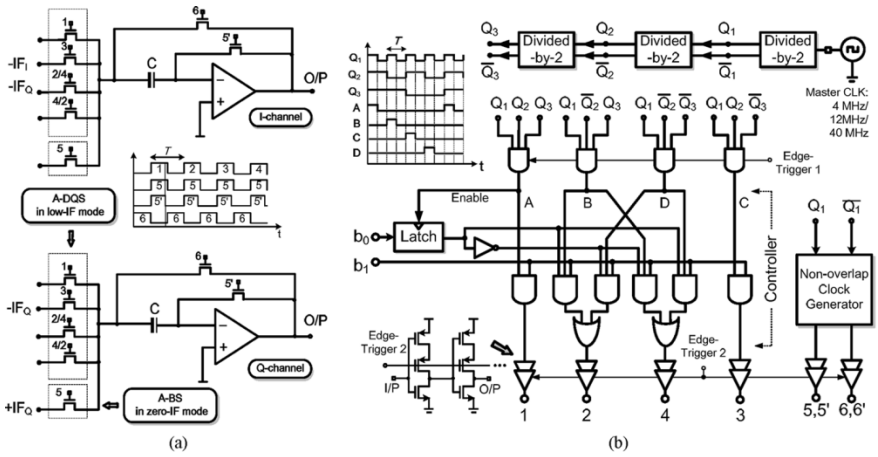

Fig. 14. (a) A multifunctional sampling mixer scheme and (b) channel/mode selections embedded clock-phase generator (the digital control code b_0 and b_1 are given in Fig. 11).

to unavoidable gain and I/Q-time-skew mismatches between the I and Q channels, the frequency-shifting and image-rejection features of A-DQS will not be exact. Such a nonideality can be described mathematically by a series of impulse samples represented by (consider (4)–(8) with lower signs for low-IF mode-A and upper signs for mode-B)

$$\begin{aligned} P(t) &= P_I(t) + jP_Q(t) \\ &= \sum_{n=-\infty}^{\infty} [\delta(t - nT_s) - \delta(t - nT_s - T_s/2)] \\ &\quad + j(1+\alpha) \sum_{n=-\infty}^{\infty} [\pm\delta(t - nT_s - T/4 - \sigma) \\ &\quad \mp \delta(t - nT_s + T/4 - \sigma)] \end{aligned} \tag{4}$$

where α and σ (assume $\sigma \ll T/4$) are the normalized gain and time-skew error between $P_I(t)$ and $P_Q(t)$, respectively. The time-domain illustration is shown in Fig. 13(b) for low-IF mode-A, where $x_I(t) = V_p \cos(\omega_{\mathrm{IF}} t)$ and $x_Q(t) = V_p \sin(\omega_{\mathrm{IF}} t)$ are assumed as the differential inputs, and only $y_I(nT)$ is presented for simplicity. The Fourier transform of $P(t)$ yields

$$\begin{aligned} P(j\omega) &= \sum_{k=-\infty}^{\infty} 2\pi a_k \delta(\omega - \omega_{\mathrm{IF}}) \\ &\quad + j \sum_{k=-\infty}^{\infty} 2\pi b_k \delta(\omega - \omega_{\mathrm{IF}}) \\ &= \sum_{k=-\infty}^{\infty} 2\pi c_k \delta(\omega - \omega_{\mathrm{IF}}) \end{aligned} \tag{5}$$

where $\omega_s = 2\pi f_s, a_k, b_k$, and c_k are the Fourier coefficients of the real part, imaginary part, and their complex-sum, respectively, given by

$$a_k = \begin{cases} \dfrac{2}{T}, & \text{for } k = 2n+1 \\ 0, & \text{otherwise} \end{cases} \tag{6}$$

$$b_k = \begin{cases} \dfrac{2}{T}(1+\alpha) e^{-jk\pi\left(\frac{2\sigma}{T} \pm \frac{1}{2}\right)}, & \text{for } k = 2n+1 \\ 0, & \text{otherwise} \end{cases} \tag{7}$$

$$\begin{aligned} c_k &= a_k + jb_k \\ &= \begin{cases} \dfrac{2}{T}\left[1 + (1+\alpha) e^{-jk\pi\left(\frac{2\sigma}{T} \pm \frac{1}{2}\right)}\right], & \text{for } k = 2n+1 \\ 0, & \text{otherwise} \end{cases} \end{aligned} \tag{8}$$

for $n = \pm 1, \pm 2, \pm 3 \ldots$ The nonideal complexiod output spectrums, $P_I(j\omega), P_Q(j\omega)$, and $P_I(j\omega) + jP_Q(j\omega)$ in low-IF mode-A are shown in Fig. 12(c), and the image-rejection ratio (IRR) can be quantified by

$$\mathrm{IRR} = \frac{|c_1|^2}{|c_{-1}|^2} = \frac{1 + (1+\alpha)^2 + 2(1+\alpha)\cos(\varepsilon)}{1 + (1+\alpha)^2 - 2(1+\alpha)\cos(\varepsilon)} \tag{9}$$

where ε is the time-skew-induced phase mismatch such that $\varepsilon = 2\pi\sigma/T$. From (6), the IRRs are 32 dB (34 dB) for a 0.025 (0.02) relative gain mismatch when combined with 2.5° (2°) phase mismatch. These values of IRRs are practically achievable and they can be added together with the image rejection of the triple-mode CSF providing in total ∼60-dB image rejection in the IF AFE, which represents a significant improvement when compared with conventional structures that achieve usually 30 dB without tuning or trimming [28].

It is also noteworthy that the proposed sampling-mixer scheme is different from the traditional sub-sampling mixer because the sampling frequency is Nyquist and there is pre-filtering prior to the sampling. The signal-band noise floor therefore will not be increased by any sub-sampling factor due to wideband-noise aliasing [29].

In zero-IF mode, the sampling mixer is reduced to a sub-set of the previous structure, and it will be designated as analog baseband sampling (A-BS) also shown in Fig. 13(a). It can be obtained by deactivating the quadrature-phase sampler $P_Q(t)$, and changing $P_I(t)$ and $P_I(j\omega)$ to $P_I'(t)$ and $P_I'(j\omega)$, respectively, which can be expressed by

$$P_I'(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_s') \tag{10}$$

$$P_I'(j\omega) = \sum_{k=-\infty}^{\infty} 2\pi a_k' \delta(\omega - k\omega_k') \tag{11}$$

where

$$a'_k = \begin{cases} \dfrac{1}{T} & \text{for } k = 0, \pm 1, \pm 2, \ldots \end{cases} \tag{12}$$

2) Implementations: The circuit solution implementing those sampling schemes is depicted in Fig. 14(a), which is based on a simple half-delay offset-compensated sample-and-hold (S/H) pair, which can serve as the front-end of an A/D converter [18], (i.e., no extra cost). In low-IF mode, the sequential clock sampling 1–4 performs the double quadrature sampling and by alternating the clock phases 2 and 4 the selection between the upper and lower sideband is achieved. Instead, in zero-IF mode, the S/H pair performs simple equal-period sampling. On the other hand, a 2-bit input digital controller will perform the selection of the different modes of operation, with the circuit structure presented in Fig. 14(b). Such a controller is composed by pure digital circuitry, and it can be efficiently embedded in the clock-phase generator to alter phase 2 and 4. The sequential clock phases 1–4 are generated via three division-by-2 circuits implemented with D-flip-flops. This approach is simple in structure and also eliminates the different propagation delays experienced in the dividers as they are synchronized in the logical operation—AND with "*Edge-Trigger 1*". The outputted phases A to D are subsequently passed to another simple logic circuit, which can either switch-ON/OFF through a 2-bit control code and/or rearrange the sampling sequence between 1-2-3-4 or 1-4-3-2 for channel selection. This selection will be triggered by phase A assuring that the sampling sequences are in the desired order, and also certifying that the time needed for each channel switching is four sampling periods. In the proposed applications with ± 0.5-channel-BW IF (or both ± 0.5 and ± 1.5), 2 μs (~ 0.667 μs) is required for 2-MHz (6-MHz) sampling frequency, which is only 0.32% ($\sim 0.0267\%$) of the channel hopping time specified in the Bluetooth standard (625 μs/hop). Such a value is already the fastest requirement, as referred in Table I. The final gate-driving buffers are synchronized again by "*Edge-Trigger 2*" to further compress the sampling errors. Since the proposed channel-selection technique only acts transparently in the control paths in discrete-time domain, no settling transients are observed when switching, which is usually not possible in the conventional continuous-time mixing approach. The phases 5, and its early switched-off version 5', are the general nonoverlapping clock phases exploited in switched-capacitor circuits to eliminate the charge injection and clock feedthrough, and more importantly here they are those that will eliminate the mismatch in the analog switches and simplify the image problem to a self-image only, and turning double quadrature sampling inherently insensitive to I/Q mismatch [30], [31].

3) Simulation Results: Considering that the baseband sampling is a well-known technique its simulation results will be omitted here and then only the results of double quadrature sampling in forward shifting will be addressed next.

By applying a pair of complex input signal, $C_1 e^{-j2\pi f_{\text{in}} t} + C_2 e^{j2\pi f_{\text{in}} t}$, with f_{in}=1 MHz and setting the sampling frequency, f_s, to 10 MHz, the obtained power spectrum density (PSD) of the I channel is shown in Fig. 15(a) (the Q channel's result would be identical in magnitude but different in phase).

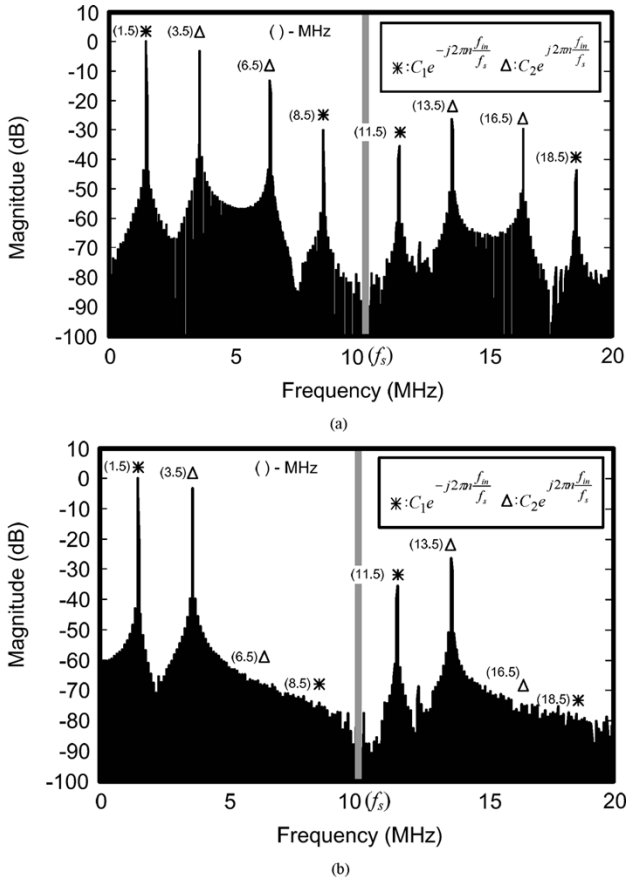

Fig. 15. Simulated PSD's (a) I channel. (b) $|I + jQ|$.

Taking the complex sum PSD$|I + jQ|$ will lead to the simulated results plotted in Fig. 15(b). As observed, the input is not only sampled-and-held but also forwardly shifted by 2.5 MHz $(f_s/4)$ such that the sampled components, $C_1 e^{-j2\pi n(f_{\text{in}}/f_s)}$ and $C_2 e^{-j2\pi n(f_{\text{in}}/f_s)}$, will be located at $nf_s + (f_s/4) + f_{\text{in}}$ and $nf_s + (f_s/4) - f_{\text{in}}$ for $n = 1, 2, 3 \ldots$, respectively. The attenuation of their magnitudes is due to the sample-and-hold effect. Through optimum system-to-transistor-level design, the image-rejection simulations based on certain artificial mismatch assignments, on the I and Q channels, achieved IRR $= 41$ dB/50 dB/76 dB for 2% gain, 0.5° phase and 2% capacitance mismatches, respectively [15].

V. Direct-Up/Two-Step-Up Reconfigurable Transmitter

The proposed technique implemented in the receiver can be analogously adopted in the transmitter to allow one PLL FS per transceiver and it shares the same phase noise and settling time relaxations. As depicted in Fig. 16, a mixed architecture of the direct-up and two-step-up transmitter is presented. In direct-up mode, single upconversion has a simple and efficient architecture, but it suffers from LO-pulling as the frequency of the LO is the same as the desired frequency location. In two-step-up mode, the first IF is set to half CS to reduce the effect of LO-LO self-modulation at RF since the LO frequency can be offset from the RF signal frequency. Regarding the IF value, again, it can be selected as either a positive or nega-

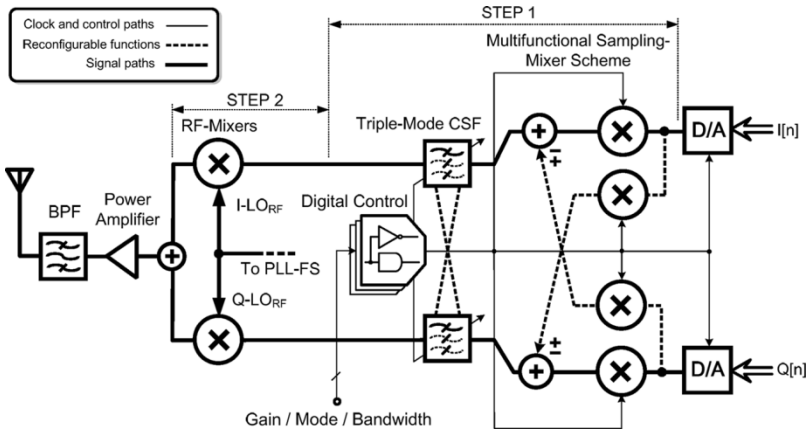

Fig. 16. Proposed direct-up/two-step-up reconfigurable transmitter.

TABLE II
COMPARISONS OF DIFFERENT RECEIVER AND TRANSMITTER ARCHITECTURES. (FoM = (Flexibility/Complexity))

RECEIVERS							
Architecture	**Image Susceptibility**	**1/*f*-Noise and DC-Offset Susceptibility**	**No. of Mixer**	**No. of Frequency Synthesizer**	**No. of Local Oscillator**	**No. of Filter and Types**	**FoM**
Zero-IF [2]	Low	High	2 at RF	1 at RF	1 at RF	2 LPFs	High
Low-IF [5]	Medium	Low	2 at RF, 4 at Low IF	1 at RF	1 at RF, 1 at IF	1 C-BPF	Low
Wide-band IF [20]	Medium	Low	1 at high IF, 2 at Low IF	1 at IF	1 at RF, 1 at IF	2 LPFs	Medium
Low-IF /Zero-IF Reconfigurable (Proposed)	Low [1]	Low/High Flexible	2 at RF [2]	1 at RF [2]	1 at RF [2]	1 C-BP/LP Tunable Filter	Very High
TRANSMITTERS							
Architecture	**Interference Susceptibility [3]**	**LO-Pulling Susceptibility**	**No. of Mixer**	**No. of Frequency Synthesizer**	**No. of Local Oscillator**	**No. of Filter and Types**	**FoM**
Direct-up [1]	Medium	High	2 at RF	1 at RF	1 at RF	2 LPFs	Medium
Two-step-up [32]	Medium	Low	2 at RF, 4 at Low IF	1 at RF	1 at RF, 1 at IF	2 LPFs	Low
Direct-up /Two-step-up Reconfigurable (Proposed)	Medium/Low [4] Flexible	High/Low Flexible	2 at RF [2]	1 at RF [2]	1 at RF [2]	1 C-BP/LP Tunable Filter	High

[1] In low-IF mode, the proposed IF AFE rejects the image twice, one by the sampling-mixer scheme, and the other by the triple mode CSF.

[2] The IF channel selection and downconversion are embedded into an S/H pair (Section-IV-B). No real mixer, oscillator and synthesizer are needed at IF.

[3] The image induced by *I/Q* mismatch in the D/A, LPF and mixer, and the low-frequency disturbance, i.e. *1/f* noise and DC offset.

[4] Embedding frequency upconversion in the D/A and replaces the LPF with the triple-mode C-BPF give a good compromise in interference susceptibility (Section-V).

tive IF, like in the receiver path, through the developed multifunctional sampling-mixer scheme. Different from the conventional two-step-up transmitter [32], the A-DQS upconversion can be embedded into the S/H units of typical switched-capacitor digital-to-analog converters (D/As), or implemented in current mode for current-steering D/As [33]. The lowpass filter used in conventional case [32] can be replaced by the proposed triple-mode filter which rejects, simultaneously, the residue images due to sample-and-hold effects and I/Q mismatch. Moreover, with capacitive coupling embedded in the cascaded stages, flicker noise and dc offset generated from the filters can be suppressed without degrading the signal quality, because the signal has been now frequency shifted to the IF prior filtering. The final upconversion is carried in the second step as usual.

VI. CONCLUSION

As the multistandard compatibility of wireless terminals becomes much more imperative than before, the standalone operation of either low-IF or zero-IF receiver will no longer be adequate enough to support narrowband-wideband-mixed multistandard applications. This paper introduced a two-step channel-selection technique to combine the beneficial features of low-IF and zero-IF implementations together in one reconfigurable receiver. As a result, with only small alteration needed in the RF AFE (two frequency dividers added to the FS), both narrow-band and wide-band signals can be processed flexibly in their respectively preferred low-IF and zero-IF operating modes. Additionally, the technique also relaxes the FS and LO design difficulties through channel-selection partitioning between the RF and IF AFEs, and balance the design trade-offs between image rejection and low-frequency disturbance eliminations. Those techniques and functional blocks are also transformable to the transmitter design to form an equally flexible direct-up/two-step-up reconfigurable transmitter. Certain comparisons were made in Table II to illustrate the versatility of the developed receiver and transmitter against the conventional ones. All the new techniques developed here form the corner-

stone for our future developments of a complete multistandard transceiver.

ACKNOWLEDGMENT

The authors would like to thank W.-I. Mok and K.-H. Ao Ieong, *University of Macau*, Macao, R. Reis, N. Ramalho, *Chipidea Microelectronics. S.A.*, Portugal, and J. Janssens, *AnSem NV*, Belgium, for their valuable discussions; and the reviewers for their imperative comments and suggestions.

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