Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection

Ka-Fai Un, *Member, IEEE*, Feifei Zhang, *Student Member, IEEE*, Pui-In Mak, *Fellow, IEEE*, Rui P. Martins, *Fellow, IEEE*, Anding Zhu, *Senior Member, IEEE*, and Robert Bogdan Staszewski, *Fellow, IEEE*

***Abstract*—The digital transmitter (DTX) offers both high power efficiency and frequency flexibility by merging signal amplification and modulation in the switching power amplifier. Yet, the back-end high-speed digital baseband interface is challenging and bulky for obtaining low out-of-band noise. This brief provides an analytical study of the DTX linear interpolation technique, which can be easily utilized for optimizing the replica rejection and noise-filtering capabilities of the DTX.**

***Index Terms*—Digital transmitter (DTX), digital baseband, linear interpolation, modulation, noise filtering, out-of-band noise, quantization noise, replicas.**

I. Introduction

FOR THE digital transmitter (DTX) design, switching power amplifiers have been widely utilized for their high power efficiency [1], [2]. Yet, it is not trivial to add filters in the signal path to reject the output replicas and quantization noise [3]. The charge-based filtering technique was proposed to suppress the noise floor [4], but the charge-sharing operation limits its output power capability. Thus, without filtering for both noise and sampling replicas, it is hard for a SAW-less DTX to fulfill the stringent out-of-band noise specification (e.g., −160 dBc/Hz in [5]). An in-phase-and-quadrature (I/Q) DTX can outperform the polar topology in terms of noise floor, e.g., −130 dBc/Hz in [6] and −112 dBc/Hz in [7], at a 100-MHz offset, as the latter can suffer from time misalignment between the amplitude and phase modulation paths [7]–[9].

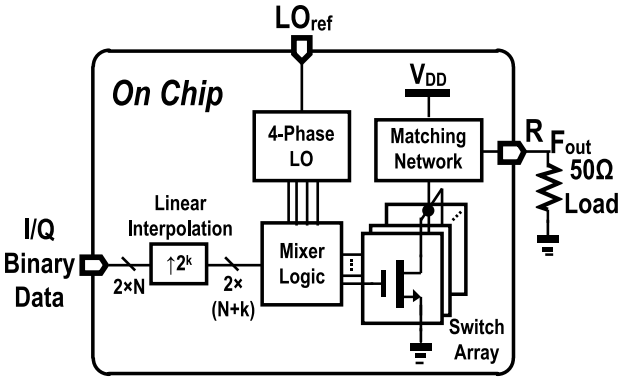

Fig. 1. Typical interpolative DTX. The switching power amplifier is driven by high-speed digital data to suppress the quantization noise and replicas.

The quantization noise of the DAC array [10], dominates the noise floor of an I/Q-mixing digital-to-analog converter (DAC), which is strongly related with its baseband sampling frequency and resolution (as outlined in Fig. 1). For example, a signal, e.g., a sampling rate of 320 MS/s leads to roughly a 6-dB lower noise floor than that at 80 MS/s [11]. The noise floor can be suppressed by increasing either of them, but the high-speed digital input/output (I/O) interface is challenging and bulky [12]. Also, the resolution is limited by the device matching precision [10]. For example, the effective number of bits (ENOB) is only 6.9 bits out of its 9-bit resolution in [6]. Rather than these, exploiting on-chip interpolation for the baseband signals can relax the speed of the digital interface.

In this brief, we analyze the tradeoff between the resolution, sampling frequency and linear interpolation, and quantify their effects to the noise and replicas rejection.

After the Introduction, Section II presents the analysis of the DAC noise with respect to its resolution and sampling rate. Section III discusses the linear interpolative I/Q DTX for suppressing the sampling replicas and noise floor. Section IV

Manuscript received December 31, 2018; accepted March 4, 2019. Date of publication March 7, 2019; date of current version December 26, 2019. This work was supported in part by the Microelectronic Circuits Centre Ireland and in part by the Macau FDCT—SKL Fund and the University of Macau—under Grant MYRG2018-00244-AMSV. This brief was recommended by Associate Editor I. W. H. Ho. *(Corresponding author: Pui-In Mak.)*

K.-F. Un is with the UCD School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland, on leave from the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China.

F. Zhang, A. Zhu, and R. B. Staszewski are with the UCD School of Electrical and Electronic Engineering, University College Dublin, Dublin 4, Ireland.

P.-I. Mak is with the State Key Laboratory of Analog and Mixed-Signal VLSI, ECE Department, Faculty of Science and Technology, University of Macau, Macau, China (e-mail: pimak@umac.mo).

R. P. Martins is with the State Key Laboratory of Analog and Mixed-Signal VLSI, ECE Department, Faculty of Science and Technology, University of Macau, Macau, China, on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1649-004 Lisbon, Portugal.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2019.2903561

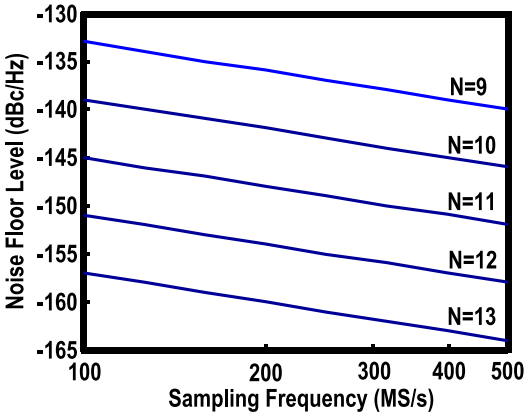

Fig. 2. Noise floor level versus sampling frequency over different ENOBs.

discusses the simulation results, and finally we draw the conclusions in Section V.

II. DAC Noise

The signal-to-noise ratio (SNR) of a DAC with respect to quantization noise can be formulated as,

$$SNR = \frac{P_S}{\int_0^{\frac{f_s}{2}} P_{NF}(f)df}, \tag{1}$$

where P_s is the signal power in mW, $P_{NF}(f)$ is the noise power density in mW/Hz and f_s is the sampling frequency of the DAC. When the signal frequency is not a sub-harmonic of f_s, the quantization noise can be regarded as random and is flat in the frequency domain. Thus, (1) can be calculated as,

$$SNR(dB) = \frac{P_S}{P_{NF}}(dB) - 10\,log\,f_s + 3.01. \tag{2}$$

As the SNR of the DAC is related to the ENOB $SNR(dB) = 6.02N + 1.76$, the relative noise floor level P_{NF}/P_s in dBc/Hz can be derived as,

$$P_{NF}/P_S(dB) = -(6.02N + 10\,log\,f_s - 1.25), \tag{3}$$

where N is the ENOB of the DAC. The level of the noise floor can be suppressed by raising either the ENOB of the DAC or the sampling frequency. Every 6-dB lower noise floor can be realized by adding 1-bit resolution, or quadrupling the sampling frequency, as shown in Fig. 2. Considering the I/O pin count, raising the resolution of the DAC is more favorable as we only have $(N+1)$ bits for each channel to obtain a 6-dB lower noise floor. However, we have to increase f_s by $4\times$, or equivalently having $4N$ bits for each channel with the same f_s, for the same data throughput.

Comparing with a single DAC, the SNR and noise floor level of an I/Q $2 \times N$-bit DAC remain unchanged since the I- and Q-channel signals are orthogonal. The total power of signal and noise are the power sums of the individual channels. Besides, the quantization noise is also filtered by the zero-order hold (ZOH), but its response is frequency dependent and will be discussed in Section IV.

III. Interpolative I/Q DTX

A. Sampling Replicas Suppression

As the complex baseband signal $s(t)$ has a finite sampling frequency. The sampled signal $s_s(t)$ can be expressed as,

$$s_s(t) = s(t) \sum_{n=-\infty}^{\infty} \delta(t - nT_s), \tag{4}$$

which is the multiple of the signal and an infinite impulse train, where T_s is the sampling period. Since the Fourier transform of the impulse train is also an impulse train with a spacing of f_s, replicas of the fundamental signal occur at the multiples of f_s. As adding reconstruction filters is not trivial in DTX design, the replicas can only be filtered by a ZOH response, where the ZOH signal can be defined as $s_{ZOH}(t) = s_s(t) * h_1(t)$ with $*$ being the convolution operation and $h_1(t)$ given by,

$$h_1(t) = \begin{cases} 1/T_s & |t| \le T_s/2 \\ 0 & otherwise. \end{cases} \tag{5}$$

The frequency response of $h_1(t)$ can be calculated as,

$$H_1(jf) = F\{h_1(t)\} = \int_{-\infty}^{\infty} h_1(t)e^{-j2\pi ft}dt = \frac{1}{\pi T_s f}\sin(\pi T_s f), \tag{6}$$

where $F\{.\}$ is the Fourier transform operation. Thus, the ZOH can provide a *sinc* response for the replicas. Considering that the maximum frequency of the baseband signal is at $f_{BB,max}$, the replica with the least suppression is at $f_s - f_{BB,max}$. In order to obtain $\ge$ 40-dB rejection for the replicas, the over-sampling rate (OSR) defined as $OSR = f_s/BW$ should be ≥ 50 that is unacceptably high for GHz operation, where BW is the signal bandwidth which is $2\times$ of $f_{BB,max}$ for a double-sideband signal.

To suppress the replicas, a continuous linear interpolated signal $s_{LI}(t) = s_s(t) * h_{LI}(t)$ is a possible solution, with $h_{LI}(t) = h_1(t) * h_1(t)$. Thus, the continuous linear interpolation operation can achieve a $sinc^2$ rejection. Yet, a continuous linear interpolation requires infinite resolution and sampling frequency in the digital domain or bulky ramp generation circuits in the analog domain.

Here the linear interpolation function can be approximated as a staircase response. The staircase signal can be simply generated by full adders from the original binary data if the interpolation ratio is a power of 2. Then, the resolution and the sampling frequency of the interpolated signal increase accordingly. A linearly interpolated-by-2 response can be written as,

$$h_2(t) = \begin{cases} 1/T_s & |t| \le T_s/4 \\ 1/(2T_s) & T_s/4 < |t| \le 3T_s/4 \\ 0 & otherwise. \end{cases} \tag{7}$$

The frequency response of $h_2(t)$ can be calculated as,

$$H_2(jf) = F\{h_2(t)\} = \frac{1}{\pi T_s f}\sin(\pi T_s f)\cos(\frac{\pi T_s f}{2}). \tag{8}$$

Comparing with the ZOH response, the linearly interpolated-by-2 response has additional zeros at the odd multiples of f_s. The required OSR is relaxed to 6.47 for achieving a 40-dB replica rejection near f_s. However, the

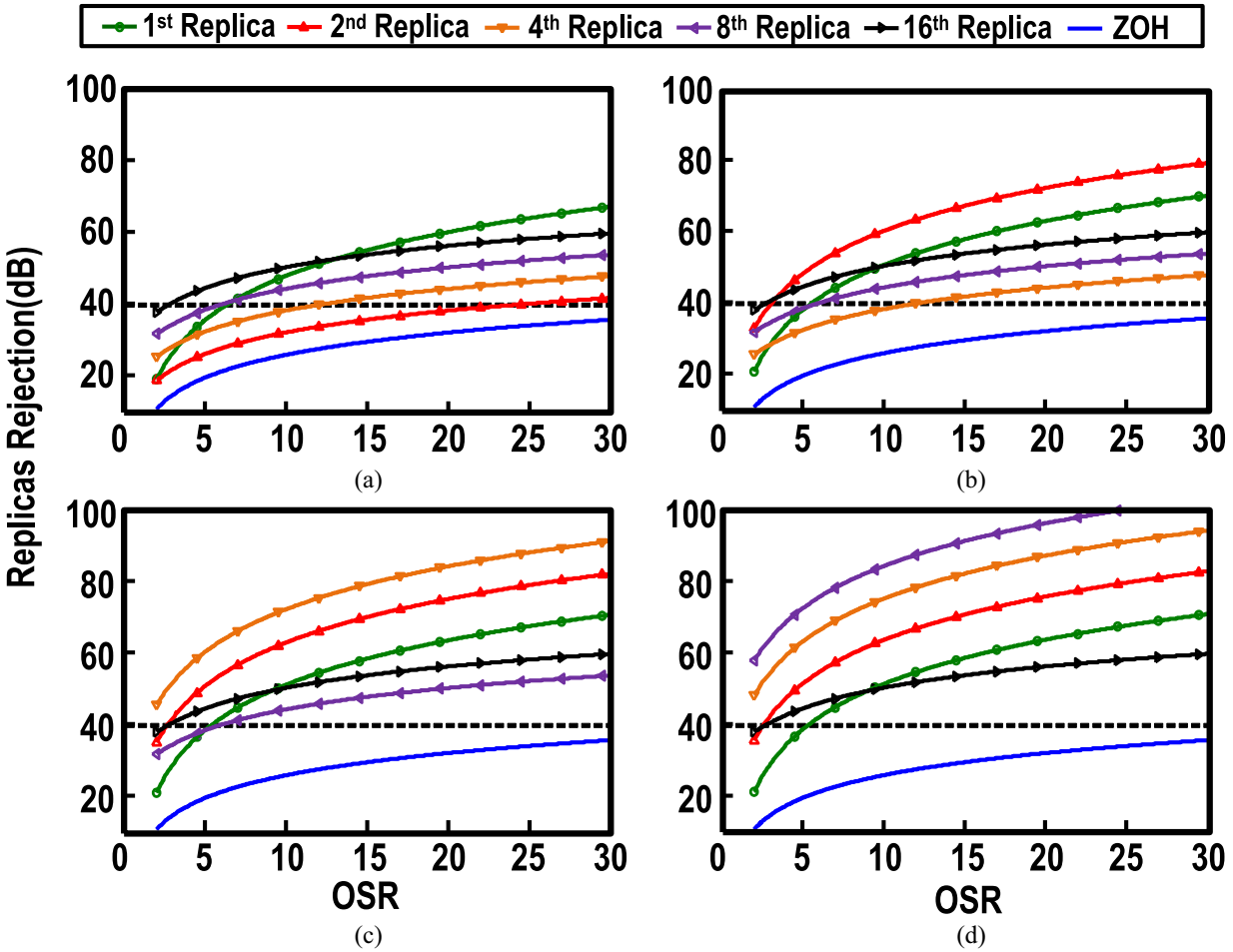

Fig. 3. Replicas rejection versus different OSR for, linearly interpolated (a) by-2, (b) by-4, (c) by-8, and (d) by-16, comparing it with a zero-order hold.

replica near $2f_s$ is not rejected by the addition zeros due to the interpolated-by-2 operation. The required *OSR* is 25 for achieving 40-dB replica rejection in the vicinity of $2f_s$.

Generalizing it to be a 2^k-step response, the frequency response will become,

$$H_{2^k}(jf) = \frac{1}{\pi T_s f}\sin(\pi T_s f)\prod_{n=1}^{k}\cos(\frac{\pi T_s f}{2^n}). \tag{9}$$

Replicas up to $(2^k - 1)$-th harmonics can be rejected. Fig. 3(a) to (d) compare the replicas rejection with different interpolation rates. To obtain 40-dB rejection for all sampling replicas, Table I summarizes the required *OSR* for different linear interpolation rates. It shows that the *OSR* is limited by the non-suppressed replicas when the interpolation rate is up to 8. The *OSR* is halved for every 2× interpolation due to the $\frac{1}{f}$ rejection. Yet, the first replica is dominant for 16× interpolation because extra interpolation steps do not contribute to the first replica rejection. The optimal interpolation rate is 8/16 where the required *OSR* for achieving 40-dB replica rejection is 6.25/5.4. A 16× can further reduce the required *OSR* by 13.6% from the 8× one but the operating frequency for the 16× interpolation circuit will be almost 1.72× higher. For instance, the effective bandwidth of a 20-MHz IEEE 802.11g signal is 16.25 MHz. The minimum required f_s to achieve 40-dB replica rejection for 8×/16× interpolation is 101.6/87.75 MHz. Thus, choosing f_s to be 120/100 MHz for them can leave margin for the rejection due to mismatches. The operating frequency of the interpolation circuit will be 0.96/1.6 GHz, thus implementing 16× interpolation can be much more power hungry. Also, a band-limited output matching network can possibly contribute to the eighth replica rejection, meaning the required OSR for the 8× interpolation can further decrease.

TABLE I
REQUIRED OSR FOR ACHIEVING 40-DB REPLICA REJECTION AT DIFFERENT INTERPOLATION RATES

Linear Interpolation Rate	1×	2×	4×	8×	16×
Required OSR	50	25	12.5	6.25	5.4
Dominant Replica	1st	2nd	4th	8th	1st

B. Sampling Replicas Suppression

The quantization noise can be filtered by the interpolation responses while they are frequency dependent. The filtered power spectral density (PSD) of the quantization noise can be written as,

$$N_Q(f) = \left|H_{2^k}(jf)\right|^2 P_{NF}(f). \tag{10}$$

TABLE II
THE NOISE REJECTION ABILITY OF THE INTERPOLATION FUNCTIONS AT DIFFERENT BANDS

f_a	$11f_s/16$	$13f_s/16$	$15f_s/16$	$17f_s/16$	$19f_s/16$	$21f_s/16$	$23f_s/16$	$25f_s/16$
f_b	$13f_s/16$	$15f_s/16$	$17f_s/16$	$19f_s/16$	$21f_s/16$	$23f_s/16$	$25f_s/16$	$27f_s/16$
$R(1, f_a, f_b)$	–10.3 dB	–16.7 dB	–28.9 dB	–19.2 dB	–14.9 dB	–13.5 dB	–13.5 dB	–14.9 dB
$R(2, f_a, f_b)$	–18.3 dB	–29.4 dB	–51.2 dB	–32.1 dB	–23.0 dB	–18.5 dB	–16.5 dB	–16.5 dB
$R(4, f_a, f_b)$	–19.8 dB	–31.4 dB	–54.2 dB	–36.3 dB	–28.3 dB	–25.1 dB	–24.9 dB	–27.2 dB
$R(8, f_a, f_b)$	–20.1 dB	–31.9 dB	–54.9 dB	–37.2 dB	–29.4 dB	–26.5 dB	–26.5 dB	–29.1 dB
$R(16, f_a, f_b)$	–20.2 dB	–32.0 dB	–55.1 dB	–37.5 dB	–29.7 dB	–26.8 dB	–26.9 dB	–29.5 dB

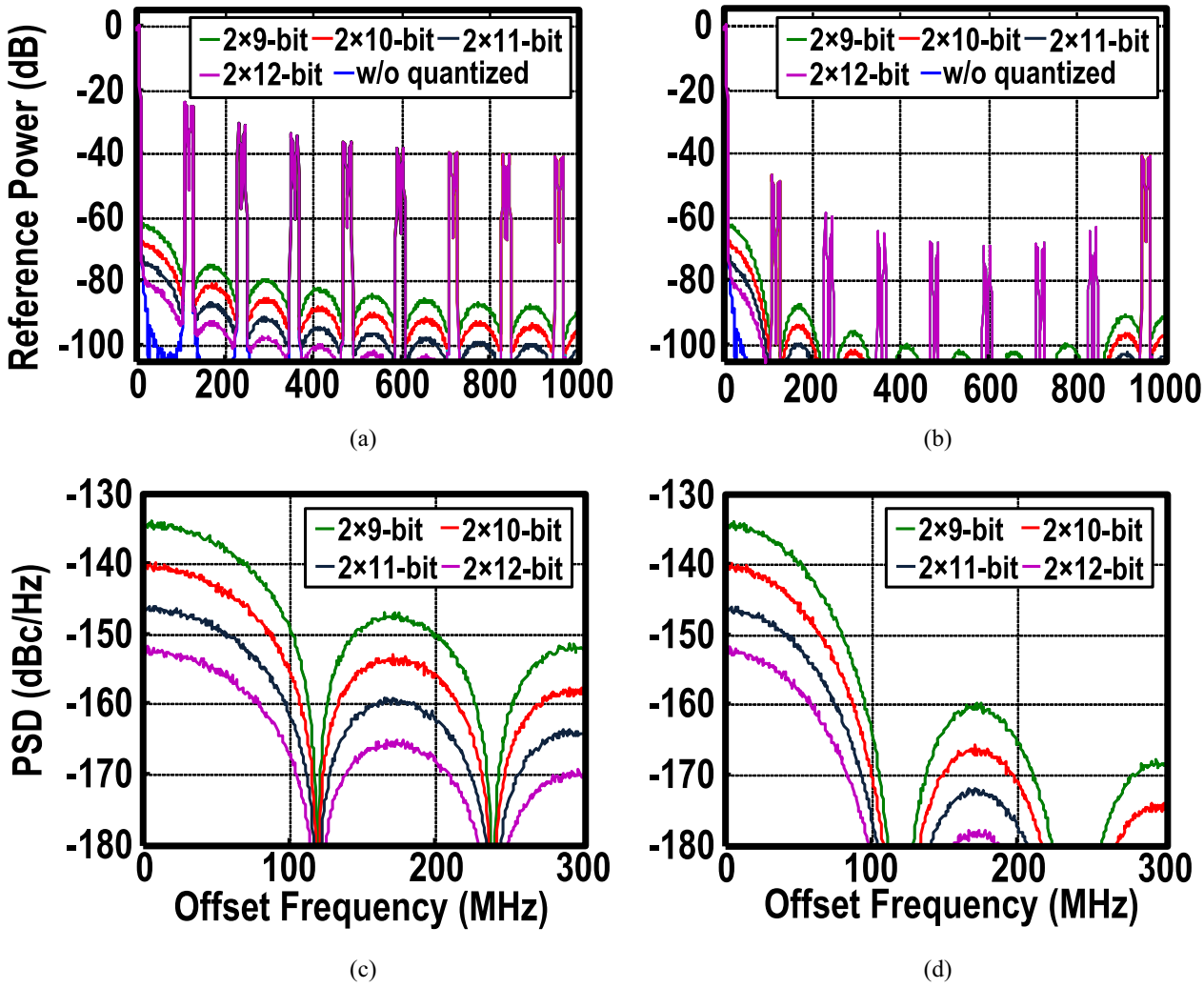

Fig. 4. The OFDM spectrum for, (a) without linear interpolation, (b) with 8× linear interpolation, and the PSD of the quantization noise for, (c) without linear interpolation, and (d) with 8× linear interpolation.

The noise floor level is usually reported at a specific frequency offset from the carrier frequency in a transmitter design. Rather than that, the average power gain within a certain bandwidth can be defined as,

$$R\left(2^k, f_a, f_b\right) = 10\,log\left(\frac{1}{f_b - f_a}\int_{f_a}^{f_b} \left|H_{2^k}(jf)\right|^2 df\right), \quad (11)$$

which is proportional to the total noise power. Table II summarizes certain values of $R(2^k, f_a, f_b)$ at different bands with different interpolation ratios. Without interpolation, the quantization noise is suppressed by 13.5 dB with the ZOH effect while it is suppressed by 26.5 dB with 8× interpolation. When the offset frequency is $<13f_s/16$, the rejection is even lower but the noise is gradually dominated by the spectrum regrowth due to the nonlinearity of the circuit as the offset frequency decreases.

The 8× interpolation can provide 2.2 bits more than the ZOH effect. By combining the noise suppression from the filtering and the noise floor derived in Section II, the overall

achievable noise floor can be calculated. Supposing that the sampling frequency is chosen to be 120 MHz, without interpolation, a noise floor of $-150/-160$ dBc/Hz is achievable with 9.5/11.1-bit ENOB. However, a noise of -160 dBc/Hz is achievable with 9.0-bit ENOB with $8\times$ interpolation.

IV. Simulation Results and Discussion

An IEEE 802.11g orthogonal frequency division multiplexing (OFDM) signal has been generated to verify the derived results, with the sampling frequency chosen to be 120 MHz as explained. Fig. 4(a) and (b) present the simulated OFDM spectrums. The first replica is suppressed to $-24.4/-47.2$ dBc without/with interpolation, respectively. Fig. 4(c) and (d) plot the PSDs of the quantization noise. The noise level at DC matches the theoretical values derived in Section II. The noise floor of $2 \times 9/2 \times 10/2 \times 11/2 \times 12$-bit ENOB is $-147/-153/-159/-165$ dBc/Hz all at 95 MHz offset without interpolation. The noise floor of 9-bit ENOB is -160 dBc/Hz at 96 MHz offset with $8\times$ interpolation. In practice, extra caution should be taken for generating the test signal as the noise floor can be easily overwhelmed by the spectrum leakage due to limited memory length.

Even with the suppressed replicas 20 to 40 dB higher than the noise floor, to further increase such suppression higher order interpolation [13] or RF filtering is necessary. The former requires power hungry FIR filters operating up to 1 GHz [14] to increase the sampling rate and resolution. However, the truncation effect will cause additional noise and DC error [15], [16]. For the latter, it will require a high-Q bandpass filter that is typically the off-chip SAW filter, or more recently on-chip frequency-tunable N-path filters [17], [18] suitable for multi- band multi-standard applications. Otherwise, a higher sampling frequency has to be selected.

V. Conclusion

The linear interpolation technique not only can suppress the replicas of the sampling in an RF DTX, but also can lower the quantization noise floor level. In this brief, we have analyzed in detail the tradeoff between the sampling frequency and resolution with the linear interpolation ratio. The results are backed by quantitative examples concerning the practical hardware limits at RF. It is revealed that linear interpolation can aid effectively sampling-frequency reduction without sacrificing the replica rejection. It can also relax the resolution of the baseband signal for smaller I/O pin count.

References

[1] H. Wang *et al.*, "A highly-efficient multi-band multi-mode all-digital quadrature transmitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1321–1330, May 2014.

[2] M. S. Alavi, R. B. Staszewski, L. C. N. de Vreede, and J. R. Long, "A wideband 2×13-bit all-digital I/Q RF-DAC," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 732–752, Apr. 2014.

[3] A. Kosari, H.-S. Kim, and D. D. Wentzloff, "A MURS band digital quadrature transmitter with class-B I/Q cell sharing for long range IoT applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 729–733, Jun. 2018.

[4] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "An incremental-charge-based digital transmitter with built-in filtering," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3065–3076, Dec. 2015.

[5] M. Ingels, D. Dermit, Y. Liu, H. Cappelle, and J. Craninckx, "A 2×14bit digital transmitter with memoryless current unit cells and integrated AM/PM calibration," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2017, pp. 324–327.

[6] R. Bhat and H. Krishnaswamy, "Design tradeoffs and predistortion of digital cartesian RF-power-DAC transmitters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 11, pp. 1039–1043, Nov. 2016.

[7] S.-M. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.

[8] J. S. Walling and D. J. Allstot, "Linearizing CMOS switching power amplifiers using supply regulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 7, pp. 497–501, Jul. 2010.

[9] W.-H. Yu, X. Peng, P.-I. Mak, and R. P. Martins, "A high-voltage-enabled class-D polar PA using interactive AM–AM modulation, dynamic matching, and power-gating for average PAE enhancement," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 11, pp. 2844–2857, Nov. 2017.

[10] Z. Bai, A. Azam, D. Johnson, W. Yuan, and J. S. Walling, "Split-array, C-2C switched-capacitor power amplifiers," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1666–1677, Jun. 2018.

[11] S.-M. Yoo *et al.*, "A class-G switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 5, pp. 1212–1224, May 2013.

[12] S. Spiridon *et al.*, "A 375 mW multimode DAC-based transmitter with 2.2 GHz signal bandwidth and in-band IM3<-58 dBc in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1595–1604, Jul. 2013.

[13] T. Buckel *et al.*, "A novel digital-intensive hybrid polar-I/Q RF transmitter architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 12, pp. 4390–4403, Dec. 2018.

[14] V. K. Parikh, P. T. Balsara, and O. E. Eliezer, "All digital-quadrature-modulator based wideband wireless transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2487–2497, Nov. 2009.

[15] P. W. Wong, "Quantization and roundoff noises in fixed-point FIR digital filters," *IEEE Trans. Signal Process.*, vol. 39, no. 7, pp. 1552–1563, Jul. 1991.

[16] L. Koskinen, M. Kosunen, S. Lindfors, and K. Halonen, "Truncation DC-error elimination in FIR filters," in *Proc. IEEE Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2000, pp. 1292–1295.

[17] G. Qi, P.-I. Mak, and R. P. Martins, "A 0.038mm^2 SAW-less multi-band transceiver using an N-path SC gain loop," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2055–2070, Aug. 2017.

[18] P. Song and H. Hashemi, "A 13$^{\text{th}}$-order CMOS reconfigurable RF BPF with adjustable transmission zeros for SAW-less SDR receivers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 416–418.