A 550-μW 20-kHz BW 100.8-dB SNDR Linear-Exponential Multi-Bit Incremental $\Sigma\Delta$ ADC With 256 Clock Cycles in 65-nm CMOS

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***Abstract*— This paper presents an incremental analog-to-digital converter (IADC) with a two-phase linear-exponential accumulation loop. In the linear phase, the loop works as a first-order structure. The noise-coupling (NC) path is then enabled in the exponential phase thus boosting the signal-to-quantization-noise ratio (SQNR) exponentially with a few number of clock cycles. The two-phase scheme combines the advantages of the thermal noise suppression in the first-order IADC and SQNR boosting in the exponential mode. The uniform-exponential weight function allows the data weighted averaging (DWA) technique to work well, leading to the rotation of the multi-bit DAC mismatch error. Meanwhile, this scheme does not destroy the notches, which can be utilized to suppress the line noise. Implemented in 65-nm CMOS under 1.2-V supply, the analog-to-digital converter (ADC) achieves an signal-to-noise + distortion ratio (SNDR)/dynamic range (DR) of 100.8 dB/101.8 dB with 20-kHz bandwidth (BW), 550 μW, and 0.134 mm^2, resulting in Walden/Schreier FoM$_W$/FoM$_S$ of 153 fJ/176.4 dB, respectively. The differential and integral nonlinearities are +0.27 LSB/−0.27 LSB and +0.84 LSB/−0.81 LSB, respectively.**

***Index Terms*— Analog-to-digital converter (ADC), data weighting average, dynamic element matching (DEM), high linearity, incremental ADC (IADC), linear-exponential accumulation, mismatch error, multi-bit, notch, sigma delta, two phase.**

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I. Introduction

OVERSAMPLING has been used to implement high-resolution analog-to-digital converters (ADCs). For the conventional $\Sigma\Delta$ modulator or the noise-shaping SAR, the following decimation filter requires order-dependent differentiators, resulting in long latency. On the contrary, incremental ADCs (IADCs) provide a Nyquist-like conversion [1]–[3], with a periodic memory clearing both in the analog modulator and the digital decimator. Thus, IADCs have attracted attention for applications in sensors, wearable devices, and instrumentation, for its low latency, easy multiplexing, and simple digital filtering properties. Meanwhile, the IADC is a Nyquist-type ADC and suffers no idle tone, which allows it to become a good candidate for the high-performance audio system.

In the first-order IADC, the required number of clock cycles is 2^N for an N-bit resolution. First-order structures are slow due to the required large number of clock cycles but the first-order sample weightings are uniform, making the thermal noise reduction and the data weighting average very effective. On the other hand, a high-order structure can significantly reduce the number of clock cycles, increasing the bandwidth (BW) or reducing the op-amp power for the same BW [4]. However, a high-order structure causes non-uniform sample weightings, reducing the effectiveness of data weighted averaging (DWA) and thermal noise suppression by oversampling.

A second-order incremental zoom-ADC [5] utilized the DWA technique to diminish the impact of DAC mismatch errors. The linearly decreasing weighting of the second-order structure reduces the effectiveness of the DWA technique. With an oversampling ratio (OSR) of 2k, the achieved linearity is 6 ppm. In addition, this architecture suffers from an input-clipping problem, and it is more suitable for a dc signal. A smart-dynamic element matching (DEM) algorithm from [6], determinedly selecting the capacitor elements in a Tetris' way, was proposed to compensate for the DAC element mismatch. However, the algorithm complexity increases exponentially with the order, quantizer bit, and OSR. Meanwhile, both works have a thermal noise penalty factor of 1.3 (details presented in Section II). In the work from [7], a dynamic integrator slicing technique was presented to reduce the first integrator's power by utilizing the input weighting function. However, there is a tradeoff between the first integrator power and the input-signal power,

such that the effectiveness of the integrator slicing technique depends on the weighting function. For the first order, this technique is not effective because of the originally uniform weighting, while high-order architectures inherently suffer from a thermal noise penalty (a factor of 1.8 in the third-order structure). Meanwhile, it used a single-bit quantizer to keep the linearity, because of the squarely decreasing DAC weighting. As a consequence, the loop demands power-hungry op-amps for a large output swing.

Hybrid combinations of incremental $\Sigma\Delta$ and Nyquist ADCs have been proposed to improve the converter efficiency [8]–[12]. A multi-step IADC with a single op-amp [11] uses multi-slope extended counting to achieve 16-bit resolution with 320 clock cycles. With the non-amplified residue voltage processed in the back-end stages, the limitation of the back-end resolution was the comparator noise, especially at low supply. Then, a long-conversion time was required to resolve more bits in the first stage when the overall resolution increased. In addition, the first stage employs a single-bit quantizer. Thus, the loop needs a power-hungry op-amp. In the work from [12], a two-step scheme uses a high-resolution flash ADC and a multi-bit DAC to reduce the op-amp swing and to relax the errors in the second stage. However, the 31-level quantizer increases the areas of the flash and the DWA logic. The cyclic ADC needs an extra capacitor to store the residue voltage, which reduces the feedback factor. The two-step architecture is more sensitive to the inter-stage gain error.

This paper presents a single-loop two-phase exponential-incremental converter that accumulates the residue in a fast and stable approach, reported in [13]. In the first phase, it works as a first-order IADC and accumulates the signal linearly for 246 cycles. In the second phase, it enables a noise-coupling (NC) path to boost exponentially the signal-to-quantization-noise ratio (SQNR) by 66 dB with 10 clock cycles. Furthermore, the uniform-exponential weighting allows the DWA to work well to average the element mismatch error of the feedback DAC. Thus, we employ a 17-level quantizer to reduce the op-amps' swings. The proposed single-loop two-phase exponential accumulation sequence combines the benefits of the thermal noise and the DAC mismatches suppression from the first-order linear phase and the SQNR boosting capability in the subsequent exponential accumulation phase.

We organized this paper as follows. Section II describes the exponential IADC concept. Then, we present the two-phase structure to explain the system-level tradeoffs in Section III. Section IV illustrates the circuit implementation and the non-ideality analysis. Section V exhibits the measurement results demonstrating the effectiveness of the proposed circuit structure, and Section VI concludes the paper.

II. Exponential Incremental ADC

A. Basic Conceptual Architecture and Timing

In the traditional single-loop IADCs, the loop consists of one integrator or cascading integrators. Thus, the signal is accumulated linearly to bi-quadratically with increasing clock cycles per conversion (or OSR), from first- to fourth-order IADCs, respectively [14]. However, an exponential integrator

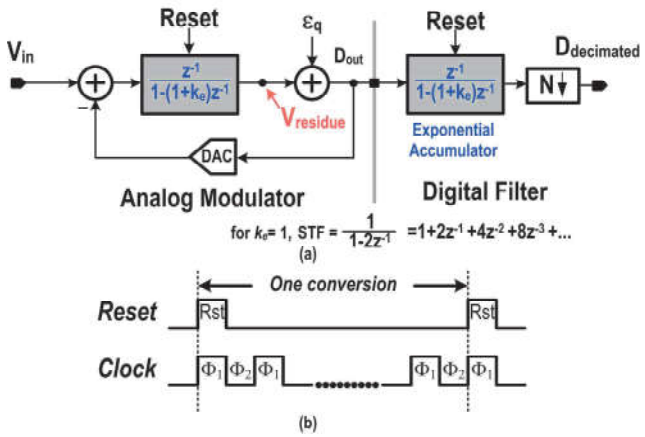

Fig. 1. Conceptual diagram of an exponential IADC and its timing diagram.

offers a faster accumulation, achieving the resolution in a fewer number of clock cycles.

Fig. 1 shows the basic concept of an exponential IADC. The integrator transfer function has changed to an exponential type, where k_e is a coefficient related with the speed of accumulation. We can analyze the working principle of the exponential IADC in the time domain as presented next. After the reset operation, both the analog modulator and the digital filter accumulate from zero until the activation of the next reset signal. In the analog domain, the loop accumulates the difference between the input signal and the tracking DAC. In the digital domain, the filter accumulates the bit stream. Ideally, the feedback DAC represents the bit-stream information. Then, at the end of one conversion with N clock cycles, the exponential integrator output can be expressed as follows:

$$V_r(N) = \sum_{i=1}^{N} [(V_{\text{in}}[i] - D_{\text{out}}[i] V_{\text{ref}m}) \times W(i)] \tag{1}$$

and

$$V_{\text{ref}m} = V_{\text{FS}}/(L-1) \tag{2}$$

$$D_{\text{out}}[i] \in [0, L-1] \tag{3}$$

$$W(i) = (1+k_e)^{N-i} \tag{4}$$

where L is the number of levels in the quantizer and V_{FS} is the full-scale reference. The factor $W(i) = (1+k_e)^{N-i}$ in (4) represents the weights of the signal during the accumulation process. This weight is sample variant in the expoential IADC, similar to high-order incremental structures. Thus, the estimation of the average input signal V_{in} can be described as

$$V_{\text{in}} = \frac{\sum_{i=1}^{N} D_{\text{out}}[i] V_{\text{ref}m} W(i)}{M} + \frac{V_r(N)}{M} \tag{5}$$

and

$$M = \sum_{i=1}^{N} W(i) \tag{6}$$

where M is the input gain of the signal, i.e., the sum of the signal weights during the accumulation process. The feedback DAC tracks the input signal, thus $V_{\text{ref}m}$ bounds the integrator. Therefore, the $V_r(N)$ represents the residue voltage and the

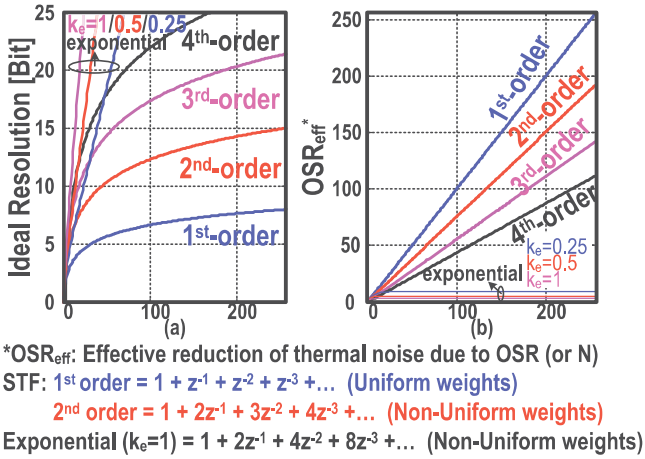

Fig. 2. (a) Theoretical resolution of an exponential IADC and traditional order-based IADCs versus OSR (or N). (b) Effective reduction of thermal noise due to OSR (OSR_{eff}) of the exponential IADC and the traditional IADCs versus OSR.

decimation filter output can be regarded as the digitization of the input signal. The theoretical resolution is

$$R = \log_2[M(L-1)] \approx \log_2 \begin{pmatrix} (1+k_e)^N \\ k_e \end{pmatrix} + \log_2(L-1). \tag{7}$$

As such, we can conclude that the resolution of the exponential IADC depends on the OSR, the coefficient k_e and the quantizer level. The larger the coefficient k_e, the larger the accumulation slope is. A multi-bit quantizer enhances the resolution by reducing the residue voltage boundary.

Assuming the quantizer is a two level, Fig. 2(a) intuitively demonstrates the relationship between resolution versus the coefficient k_e and the OSR N. When compared with the traditional IADCs, the proposed scheme digitizes the signal in a faster way. Considering an SQNR of 120 dB, the theoretical required clock cycles are 1449/186/73 from second to fourth order. However, the required clock cycles for the exponential scheme are 55/32/20 periods (with $k_e = 0.25/0.5/1$). Then, the proposed scheme can achieve high resolution with a fewer clock cycles, especially when we choose a large coefficient k.

B. Thermal Noise and DWA Considerations

Apart from the SQNR, thermal noise is another fundamental limiting factor that must be carefully considered in high-resolution ADCs. The same type of concern holds for the utilization of the DWA technique in case of using a multi-bit DAC.

With the oversampling operation, the input-referred thermal noise can be ideally suppressed by OSR (i.e., the number of clock cycles N) by the following equation:

$$V^2_{n,\text{input\_uniform}} = \frac{2kT}{C_s}\frac{1}{N}. \tag{8}$$

However, high-order IADCs have a thermal noise penalty due to the non-uniform weights in the signal accumulation, i.e., the OSR_{eff} (the effective OSR for thermal noise reduction) will be reduced as Fig. 2(b) shows. The monotonic decreasing weighting in traditional high-order IADCs results in a thermal noise penalty [14]. The input-referred noise of such converter could be calculated with the sum of the squared weightings divided by the square of the weighting's sum

$$V^2_{n,\text{input\_non\_uniform}} = \frac{V^2_{n.\text{total}}}{M^2} = \frac{2kT}{C_s}\frac{\sum_{i=1}^{N} W(i)^2}{\left[\sum_{i=1}^{N} W(i)\right]^2} \tag{9}$$

where $V^2_{n.\text{total}}$ is the total output noise, M is the total gain of the input-signal accumulation, as shown in (6), and $W(i)$ is the weights from (4). For higher loop orders, the thermal noise penalty will also be higher, because of the faster accumulation slope. The penalty factor can be expressed by dividing (9) by (8)

$$\text{Penalty Factor} = N\frac{\sum_{i=1}^{N} W(i)^2}{\left[\sum_{i=1}^{N} W(i)\right]^2}. \tag{10}$$

Table I presents the penalty factors that are 1.3/1.8/2.3 from second to fourth order (when N is sufficiently large). The situation is worsen in the exponential cases. For example, at an OSR = 256, the OSR_{eff} is also 256 for a first-order IADC, thus retaining the full benefit of oversampling. But the second, fourth order and exponential ($k_e = 1$) would have the OSR_{eff} decreased by 23%, 57%, and 99%, respectively [Fig. 2(b)].

The sample-variant weighting property affects the input referred thermal noise for a given sampling capacitor C_s in the exponential scheme (detailed analysis in the Appendix). From (11), the input-referred kT/C noise is no longer related to the OSR anymore, but only to the coefficient k_e

$$V^2_{n,\text{input}} = \frac{2kT}{C_s}\frac{1}{1+\frac{2}{k_e}}. \tag{11}$$

As Fig. 2(b) intuitively highlights, (11) indicates that with the increasing of clock cycles per conversion, the benefit of thermal noise reduction is not growing with the OSR. From Table I as well, the advantage of oversampling did not appear in (11). The principal reason is that the weightings, like the traditional high-order IADCs, are non-uniform. Regrettably, the situation in the exponential scheme is worsen because the weighting decreases exponentially rather than gradually like in conventional high-order IADCs.

Finally, high-resolution IADCs that use multi-bit quantizers require advanced DEM techniques to guarantee the targeted linearity. Nevertheless, Table I also shows that the non-uniform weights in high-order and exponential IADCs lead to the same treatment of the DEM weighting like in the discussion of the thermal noise suppression before, namely, the penalty trends still apply similar to the DEM effectiveness. For example, [6] used a smart DEM for a second-order IADC, but its implementation is relatively complicated.

III. Proposed Linear-Exponential IADC

A. Overall Architecture

The penalty of oversampling on the thermal noise is that the weightings of both the high order and exponential struc-

TABLE I
ARCHITECTURE COMPARISON OF IADCS

	1st-order	2nd-order	3rd-order	4th-order	Exp (k_e=1/0.5/0.25)	Proposed Linear-Exp (k_e=1)
Resolution (log_2)	$\binom{N_1}{1}$	$\binom{N_2}{2}$	$\binom{N_3}{3}$	$\binom{N_4}{4}$	$\sum_{i=1}^{N}(1+k_e)^{N-i}$	$(N_L+1)*2^{(N_E+1)}$
N (or OSR) for 20b Resolution	$N_1 = 1048576$	$N_2 = 1449$	$N_3 = 186$	$N_4 = 73$	$N_E = 20/32/55$	N = 256 (246 1st order + 10 Exp)
Input referred kT/C noise	$\frac{1}{N_1}\left(\frac{2kT}{C_s}\right)$	$\frac{1.3}{N_2}\left(\frac{2kT}{C_s}\right)$	$\frac{1.8}{N_3}\left(\frac{2kT}{C_s}\right)$	$\frac{2.3}{N_4}\left(\frac{2kT}{C_s}\right)$	$\frac{1}{3/5/9}\left(\frac{2kT}{C_s}\right)$	$\frac{1.03}{N}\left(\frac{2kT}{C_s}\right)$
Multi-bit DAC + DWA	√	x	xx	xxx	xxxx	√
STF's Notches	Yes	No	No	No	No	Yes

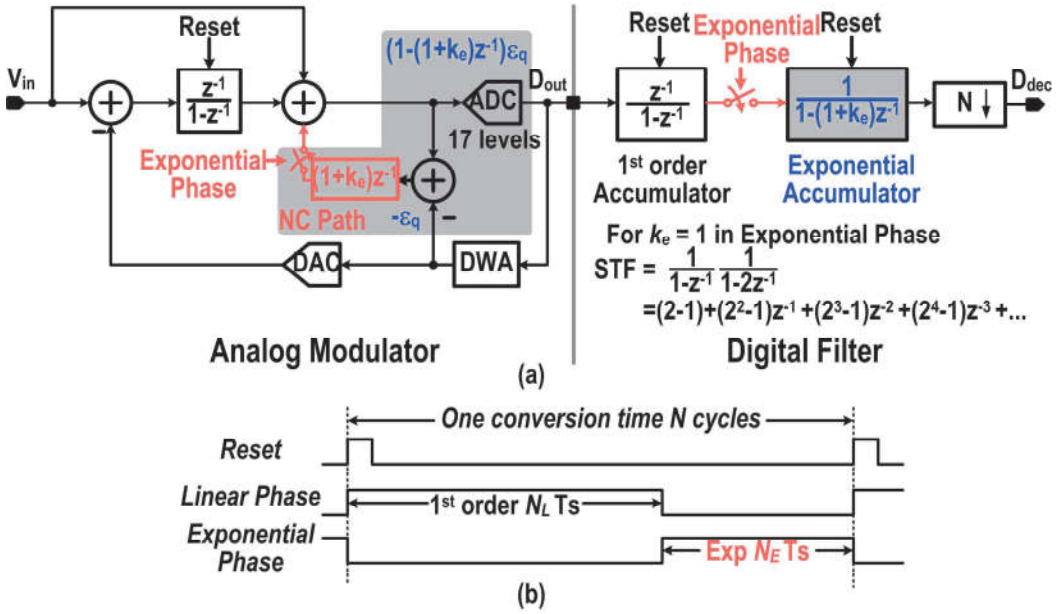

Fig. 3. (a) Block diagram of a two-phase linear-exponential incremental converter. (b) Timing diagram of a two-phase IADC.

tures are non-uniform.[1] The first-order architecture provides a uniform weighting function but suffers from long-conversion time. The exponential scheme offers faster accumulation but suffers from the disastrous penalty of input-referred thermal noise. Thus, the basic idea in this paper is to combine the advantages and avoid the disadvantages.

The proposed two-phase linear-exponential scheme resolves such thermal noise limitation in exponential IADCs, by periodically deactivating the exponential accumulation at the beginning of the conversion. As Fig. 3 illustrates, only a first-order integrator is utilized at the beginning of the linear phase, with the loop working as a first-order structure for equal weights of 246 cycles, and the oversampling will fully contribute to the reduction of the thermal noise. In the exponential phase, we activate an extra NC path [15] which creates an exponentially accumulating loop in the remaining 10 cycles.

[1]Assuming the weightings are $w_1, w_2, ...w_N$, based on AM-GM inequality, $\sqrt{(w_1^2+w_2^2+\cdots+w_N^2)/N} \geq (w_1+w_2+\cdots+w_N)/N$, we can conclude that the input-referred kT/C_s noise is no less than $2kT/C_s/N$and the minimum condition is that all the weightings are uniform (i.e., first-order IADC weighting).

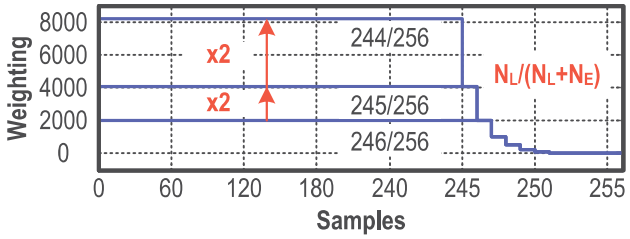

Fig. 4. Weighting function of a linear-exponential IADC with the $k_e = 1$ (normalized from the last sample).

When compared with Fig. 1(a), the overall signal transfer function (STF) changes to $(z^{-1}/1-z^{-1})(1/1-(1+k_e)z^{-1})$ (with reset of memory). The first-order term can increase the final SQNR. However, this does not affect too much the exponential accumulation since the first-order term is too weak when compared with the exponential term. Thus, the scheme with linear-exponential accumulation, works complementarily, combining the best features of thermal noise suppression and SQNR boosting.

The proposed scheme also allows the DWA technique to work well in averaging the mismatch error. Fig. 4 plots

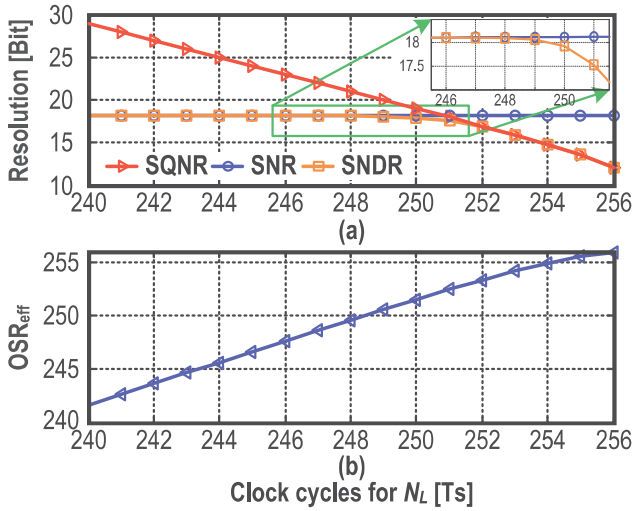

Fig. 5. (a) Resolution and (b) equivalent OSR for thermal noise versus clock cycles for the linear phase in the linear-exponential IADC.

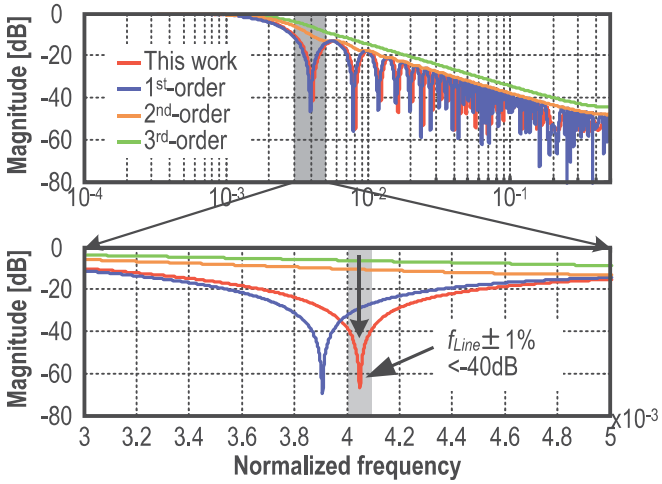

Fig. 6. Magnitude frequency response of the IADCs' decimation filter.

the weighting function of a linear-exponential IADC where the linear phase offers a uniform weighting function. The weightings at the exponential phase are not identical but they are much less significant as they are decreasing exponentially and are much lower than the weights in the linear phase.

B. Parameters' Selection

Considering the speed of loop accumulation, analog matching, and the complexity of the decimation filter, we chose the coefficient $k_e = 1$. The coefficient k_e has an impact on the maximum stable amplitude (MSA), because of the fed back quantization noise. Fortunately, the stable input range would be benefited from the increase of the quantizer bit, which will be analyzed next.

In practice, a small OSR would lead to a large sampling capacitor in a high-resolution ADC. Here, we chose an OSR of 256 to achieve low cost in terms of area, with an input-sampling capacitance of 8 pF. As Fig. 4 also shows, for 256 clock cycles, the more we allocate clock periods in the exponential phase, the larger the weighting will be in the linear phase. However, the thermal noise benefits will diminish. Generally, the following equations describe the weighting function:

$$W(i) = \begin{cases} 2^{N_e+1} - 1, & i \in [1, N_L] \\ 2^{N-i+1} - 1, & i \in [N_L + 1, N] \end{cases} \tag{12}$$

$$N = N_L + N_e \tag{13}$$

where N_L and N_e represent the number of clock cycles for linear and exponential phases, respectively, and N is the total number of clock cycles per conversion. Similar to the thermal noise discussion in the Appendix, the input-referred noise of the proposed scheme can be written as follows:

$$V_{n,\text{input}}^2 = \frac{V_{n.\text{total}}^2}{M_{\text{input,linear-exp}}^2} = \frac{2kT}{C_s} \frac{\sum_{i=1}^{N} W(i)^2}{\left[\sum_{i=1}^{N} W(i)\right]^2}. \tag{14}$$

For IADCs, the summation of the weighting during one conversion represents the theoretical resolution. Thus, the proposed scheme can obtain higher SQNR by tuning the number of clock cycles for linear phase and exponential phase. However, more periods for the second phase means that the OSR_{eff} for thermal noise is smaller. Fig. 5 exhibits the relationship between resolution and the overall OSR_{eff} for the proposed two-phase scheme versus N_L (the number of clock cycles in the linear phase) with a 17-level quantizer. To allow a sufficient margin in the kT/C noise of 110 dB and other circuit non-idealities, we select a clock cycle of $N_L = 246$ for the linear phase, with the exponential phase occupying the remaining $N_e = 10$ periods. Then, the thermal noise penalty factor is around 1.03, which is very close to the first-order IADCs from Table I. Such clock cycles distribution implies a good tradeoff between the SQNR and the kT/C noise.

C. Considerations About Maximum Stable Amplitude

In the proposed architecture, the NC path fed the quantizer noise back to the quantizer's input node. It increases the swing at the quantizer input, reducing the MSA of the IADC. However, we can maintain the stable input swing and the stability of the scheme by employing a multi-bit quantizer. Actually, we prefer to use a multi-bit quantizer to relax the op-amps specifications and to reduce the power consumption. For a M-step quantizer, the sufficient (but not necessary) input range for MSA can be estimated as follows [16]:

$$|u|_{\max} = M + 2 - \underbrace{\sum_{k=0}^{\infty} |h(k)|}_{\triangleq \|h\|_1} \tag{15}$$

$$\text{NTF} = \begin{cases} (1 - z^{-1}), & \text{linear phase} \\ (1 - z^{-1})(1 - 2z^{-1}), & \text{exp.phase} \end{cases} \tag{16}$$

where $h(k)$ is the impulse response of the noise transfer function and $\|h\|_1$ represents the 1-norm of $h(n)$ (note that the noise transfer function (NTF) here only serve the purpose of discussion on MSA, it does not mean the converter has noise-shaping property). As (15) and (16) present, the exponential-phase limits the MSA with the corresponding coefficient k_e.

Additional levels in the quantizer are beneficial for enlarging the MSA and reducing the integrator swing. Meanwhile, it allows the choice of a large coefficient k_e. But it leads to higher quantizer's power consumption, area, and DWA complexity. Considering these tradeoffs, we chose a 17-level quantizer.

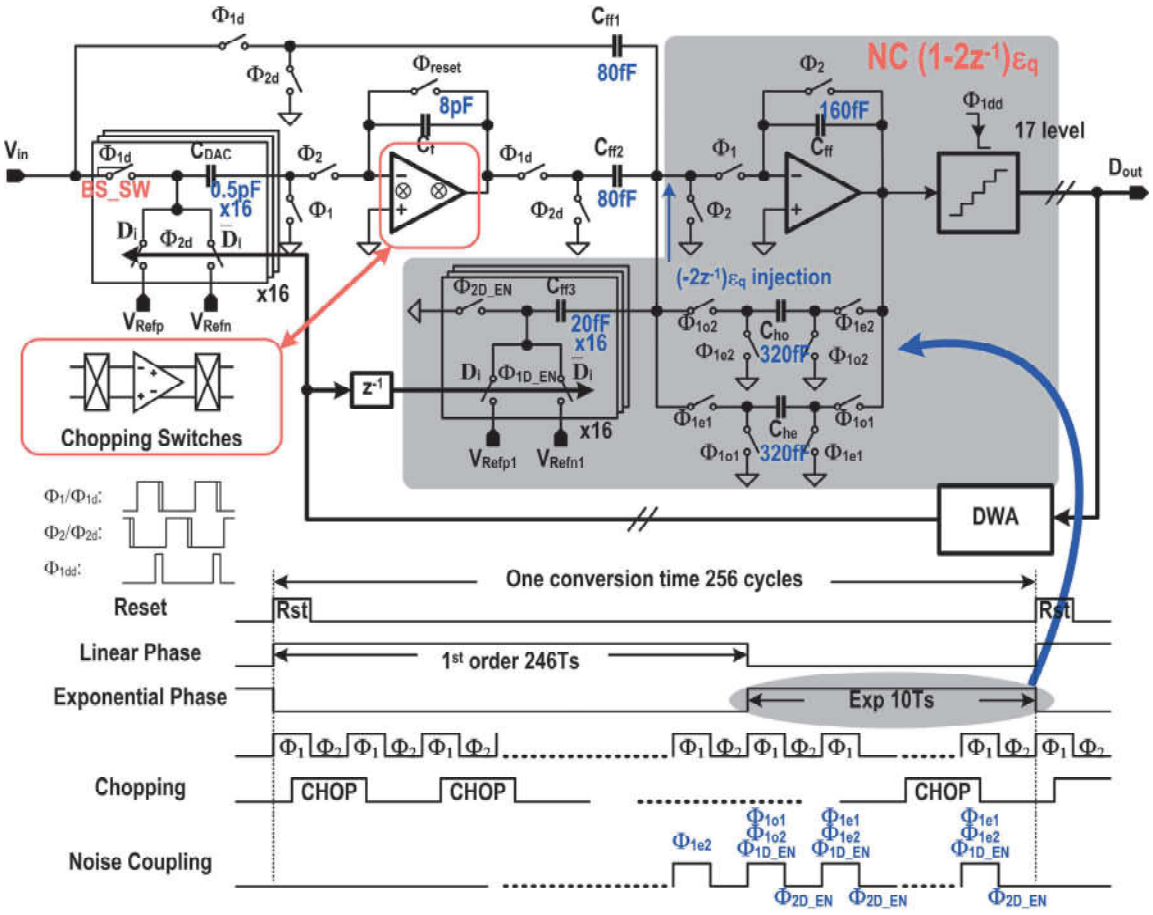

Fig. 7. Circuit diagram of the linear-exponential IADC and its timing diagram.

D. Decimation Filter Considerations for Incremental ADCs

The decimation filters of traditional IADCs exhibit simple structures (counter or cascaded counters). For the first-order architecture, the counter inherently provides notches (Fig. 6), which can be used to suppress the interferers' noise (such as the line frequency noise). However, the decimation filter of a high-order structure destroys the advantages, due to the non-symmetrical weighting function.

For the proposed scheme, we design the decimation filter directly from the weights in (12), with the magnitude-frequency response illustrated in Fig. 6 which shows that the notches still exist. The justification for it is the fact that most of the weighing sequence is uniform and the weights at the exponential phase are much smaller and decay exponentially. In this scheme, the first notch provides a suppression larger than 40 dB with a $\pm 1\%$ line frequency (f_l) variants. Consequently, by carefully selecting the ratio among the line noise frequency, sampling frequency, and the OSR, the notches can be set to suppress the fundamental line noise and its harmonics.

IV. Circuit Implementation

A. Overall Switched-Capacitor Circuitry

Fig. 7 shows the simplified circuit implementation of the proposed two-phase linear-exponential IADC. We exhibit only a single-ended implementation for simplicity, but the real circuit is fully differential. In the linear phase, the circuit works as a first-order IADC with a low-distortion feedforward structure. From the feedforward architecture, the quantization noise limits the voltage swing of the first integrator. It relaxes the op-amp specifications in terms of slew rate at the initial cycle, when compared with the traditional first-order feedback structure. The integrator is reset at Φ_1 in the first cycle, as illustrated in the timing diagram of Fig. 7. Φ_{1d}/Φ_{2d} is the slightly delayed version of Φ_1/Φ_2. Meanwhile, Φ_{1dd} is the comparator strobe signal. Also, the odd-part feedbacks the input information at Φ_{1o}, while the even-part feedbacks the input information at Φ_{1e}.

When the exponential phase is enabled, the NC network, composed by ping-pong capacitor arrays (C_{ho}, C_{he}) and the feedback DAC array (C_{ff3}), starts to work. From Fig. 7, one can see that the even part will work a cycle earlier than the odd part, right at the last cycle of the linear phase, to prepare the input information for the first cycle of the exponential phase.

For the SC circuitry, we employ a bootstrapped switch referred as BS_SW (Fig. 7) to ensure the critical input switches' linearity [17], [18]. We use the bottom-plate sampling to reduce the signal-dependent charge injection. Considering the flicker noise and offset, we apply a chopping technique in the first integrator. The non-overlap chopping clock reverses at the middle of Φ_1 with the virtual ground chopping switches enabled slightly earlier than the output chopping.

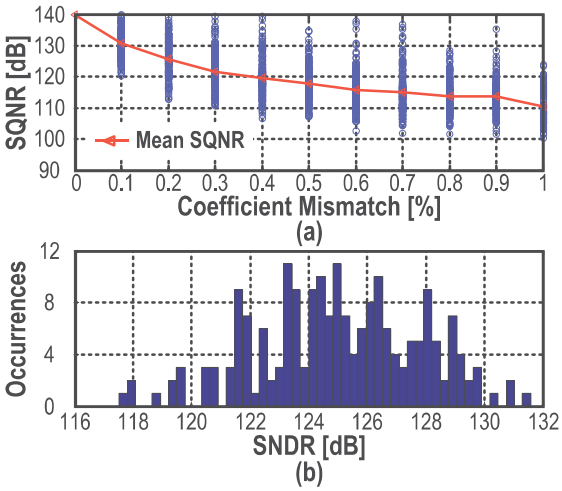

Fig. 8. Simulated SQNR of the IADC due to (a) mismatch error in NC networks and (b) sampling capacitor element mismatch error.

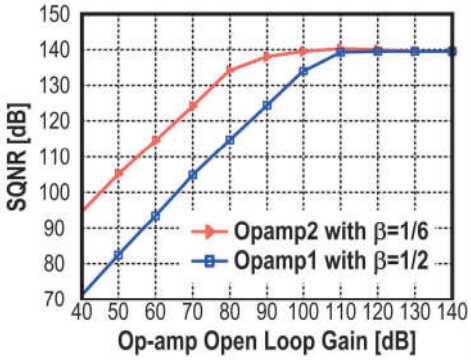

Fig. 9. Peak SQNR of the IADC with the finite gain of the op-amps (β is the feedback factor).

B. Influence of Capacitor Mismatch

When observing the coefficients, we should realize that the capacitor mismatches influence the transfer function matching between the analog modulator and the digital filter, as well as the DAC linearity. We built a behavioral model to study those effects.

Regarding the transfer function mismatch, two main concerns are the ratios between C_{DAC} (also used as the sampling capacitor) and C_F, as well as the NC capacitors. For the first term, the thermal noise determines the sampling capacitor size. In order to achieve an SNR due to kT/C noise of 110 dB, we select a total sampling capacitor of 8 pF with 256 clock cycles. Such size of capacitors can guarantee a sufficient integrator coefficient matching, to eliminate such type of error. As for the NC network, coefficients mismatch will generate a transfer function mismatch on the quantization noise of $(1-2z^{-1})\varepsilon_q$. As illustrated in Fig. 7, the capacitor ratios represent the coefficients. For each variation of the coefficients, including coefficient k_e, we launched Monte Carlo behavioral simulations with 200 samples per case. Fig. 8 (a) shows that the IADC can achieve an SQNR higher than 110 dB with a standard deviation of 0.2%, which is the matching level that can be guaranteed in 65-nm CMOS.

Regarding the DAC nonlinearity caused by element mismatch, there are two sources, the feedback DAC array and the NC capacitors array. To average the mismatch error in the feedback DAC, the scheme uses a simple DWA technique. Behavioral simulation shows that the utilization of DWA allows a 117-dB signal-to-noise + distortion ratio (SNDR) at least with a unit element $\sigma = 0.05\%$ for a sampling DAC unit cell [Fig. 8(b)]. Moreover, we adopted the 16-quadrant random walk and the common-centroid layout techniques to guarantee high-matching accuracy. When observing the NC capacitors array, the gain of the linear phase relaxes the matching requirement. The behavioral model shows that the SNDR is above 120 dB under the error of $\sigma = 0.2\%$ for a DAC unit element in the NC array without any DEM.

To summarize, capacitor mismatch is one of the main concerns for transfer function errors and it often limits the DAC linearity. The previous analysis shows that the matching requirements are not too critical and can be guaranteed with good reliability in the used CMOS process.

C. Op-Amps

Op-amps' finite-gain errors will change the integrator's transfer function, degrades the SQNR by imposing an integrator gain error and shifting the integrator's pole. We built a behavioral model to study the gain error tolerance.

Fig. 9 plots the simulation results of the SQNR versus the op-amps' open-loop finite gain. For such high-resolution converter, the op-amp gain requirement of the first integrator is as high as 86 dB for maintaining the SQNR >120 dB. On the other hand, the op-amp requirements of the adder are quite relaxed. In fact, the NC transfer function determines the second-op-amp specifications (>66 dB), and the input-referred error would be suppressed by the accumulation gain of the linear phase.

With the advanced low-voltage nanometer CMOS process, it is difficult to design a high-gain op-amp due to the small intrinsic gain of the transistors. However, the first op-amp benefits from the reduced output swing, allowed by the feedforward structure and the multi-bit quantizer. Thus, an energy-efficient single-stage, complementary-input, and gain-boosted telescopic op-amp can be utilized under a 1.2-V supply. Fig. 10(a) shows this topology that can almost double g_m and the open-loop gain [19], with less noise-contributing transistors.

To guarantee a stable operating point over the process corners, especially in such a low-voltage telescopic topology, we biased the op-amp with the process tracked design. Note that the nominal value of the op-amp virtual ground is around V_{CM}. Consequently, we can directly bias the transistors MGP and MGN with V_{CM}. This guarantees an identical V_{DS} of current source transistors MN1/2/3/4, and MP1/2/3, leading to a good current mirroring in such low-voltage environment over process variations. Simulation results show that the GBW is about 42 MHz with a deviation of 2% over the MOS process corner variation. Meanwhile, the open-loop gain at the typical corner is 97 dB with a 500-mV V_{pp} output swing, with the op-amp gain and GBW meeting the requirements over all corners.

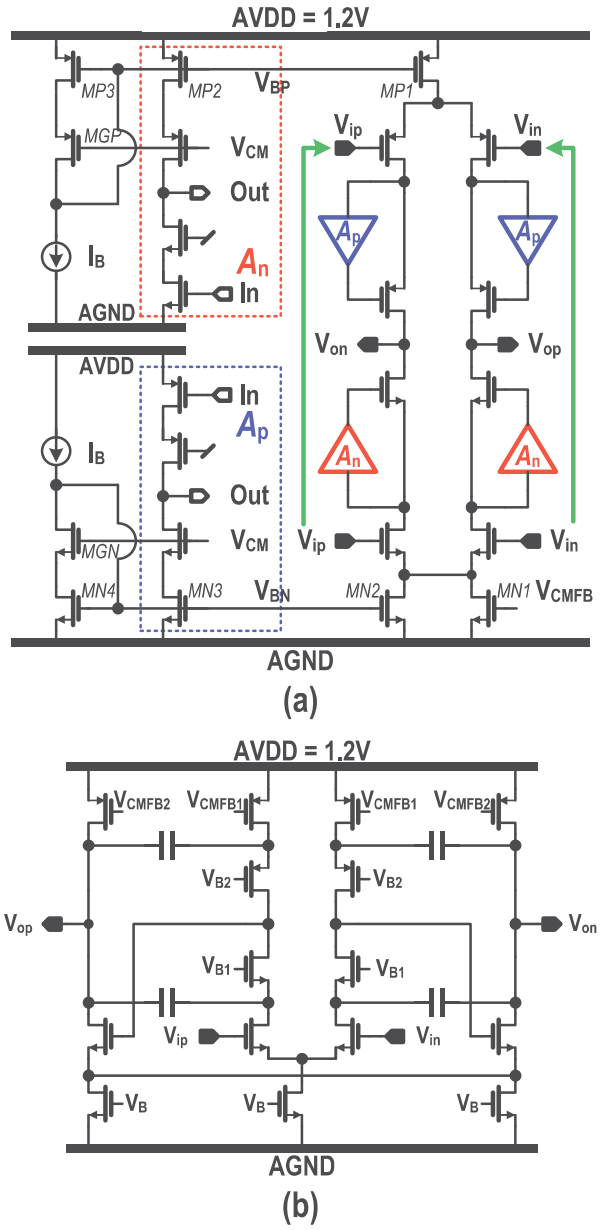

Fig. 10. Topologies of (a) first op-amp and (b) second op-amp.

The gain-scaling technique was often used in modulators to reduce the power consumption [20], [21], because the back-end quantizer has a lower resolution. Here, we have scaled down the quantizer reference by half, which can relax the design of the second op-amp because of the small output swing. Fig. 10(b) shows the topology of the second op-amp that uses a two-stage topology. We use a telescopic cascode in the first-stage to guarantee the gain requirement. Simulations show that the open-loop gain is above 70 dB in the maximum swing to ensure the performance.

D. Multi-Bit Quantizer

The reference scaling down technique will reduce the quantizer input signal. With reference half-scaled, the requirements on the flash quantizer were almost doubled, but it is not critical in the proposed design. To guarantee the performance of the flash, the comparator consists of a pre-amplifier and a strongARM latch, followed by an SR latch. With the auto-zero technique the input-referred offset meets the 17-level quantizer requirement.

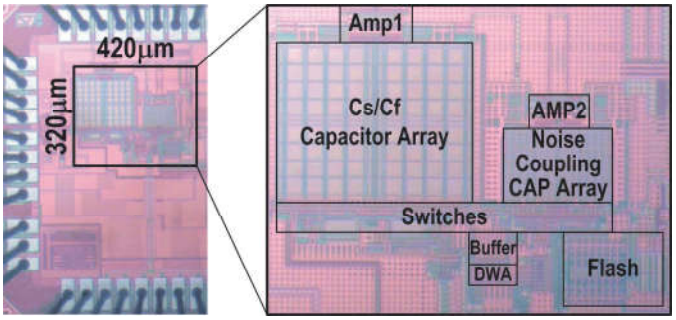

Fig. 11. Chip micrograph.

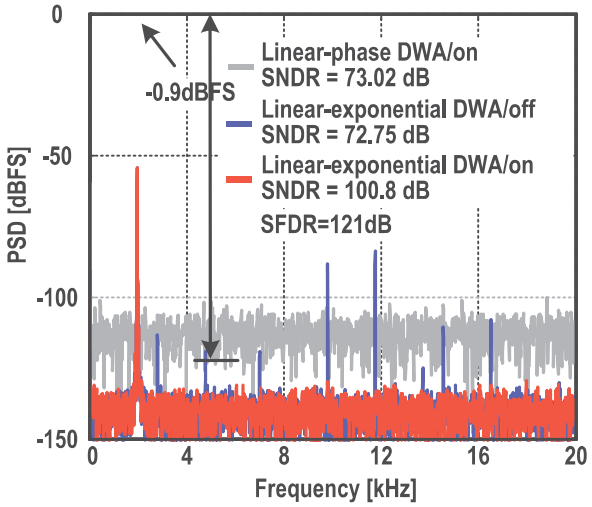

Fig. 12. Measured output spectra for linear phase with DWA on and linear-exponential phase with DWA off/on.

V. Experimental Results

Fig. 11 exhibits the chip micrograph of the prototype IADC that has been implemented in a 1P7M 65-nm CMOS process, occupying an active area of 0.134 mm^2 (320 μm $\times$ 420μm). Under a 1.2-V supply and 10.24-MHz sampling clock, 20-kHz BW, the analog modulator consumes 550 μW (48%—integrator, 33%—adder, 9%—digital, 4%—flash quantizer, and 5% others).

Fig. 12 displays the measured output spectrums of the IADCs with only linear-phase active with DWA and linear-exponential phase with/without DWA, respectively. It shows a measured SNDR of 73.02 dB with only the linear phase (DWA on). The SQNR limits the performance to a 12-bit level with a 246 cycle of linear phase. The SNDR improves to 100.8 dB with the exponential phase enabled. Fig. 12 also indicates the effectiveness of the DWA, increasing the SNDR by 28.0 dB. On the other hand, Fig. 13 shows that the utilization of the chopping technique improves the performance on flicker noise. The chopper modulator improves the SNDR by 5 dB and reduces the offset from 1.27 mV to 72.51 μV. Fig. 14 reveals the measured IADC's SNR/SNDR versus the input amplitude and the ADC achieves a dynamic range (DR) of 101.8 dB.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

Parameter	**This Work**	[7] ISSCC'18	[12] VLSI'18	[11] VLSI' 16	[22] JSSC'15	[23] TCASI'15	[24] ISSCC'18	[25] ISSCC'18	[26] VLSI'17
Architecture	**Linear-exponential IADC**	3rd-order IADC	Two-step IADC	Multi-slope IADC	Two-step IADC	CT IADC	Zoom ADC	SAR	Pipelined-SAR
Process(nm)	**65**	180	180	180	65	180	160	180	180
Supply (V)	**1.2**	3	3	1.5	1.2	1.2/1.8	1.8	5	1.8/5
Frequency (MHz)	**10.24**	30	55	0.642	0.192	0.32	2	1	2
Bandwidth (kHz)	**20**	100	625	1	0.250	4	1	500	1000
Power (μW)	**550**	1098	27700	34.6	10.7	34.8	280	19.7	11350
Peak SNDR (dB)	**100.8**	86.6	96.6	96.8	90.8	75.9	118.1	101.5	99.2
DR (dB)	**101.8**	91.5	100.1	99.7	99.8	85.5	120.3	102.7	100.5
FoMw(pJ/conv.)	**0.15**	0.31	0.40	0.32	0.76	0.85	0.21	1.97	0.07
FoMs(dB)	**176.4**	166.2	170.13	171.4	164.5	166.1	183.6	175.5	178.7
Area [mm^2]	**0.13**	0.36	0.72	0.5	0.2	0.34	0.25	4	3.87

$FoM_w = Power/(2^{ENOB} * 2BW)$; $FoM_s = SNDR + 10log(BW/Power)$;

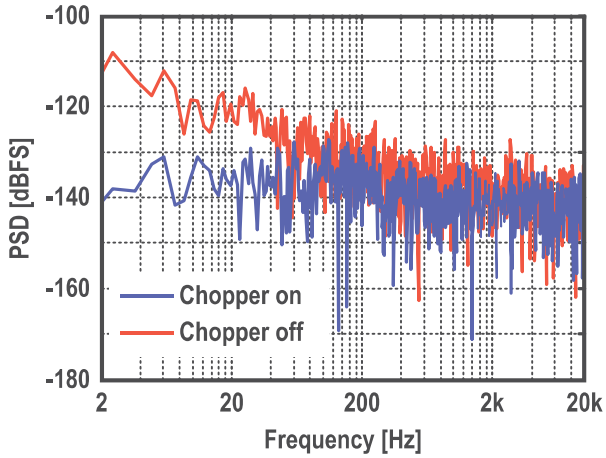

Fig. 13. Measured spectra for chopping turn on/off with shorted input.

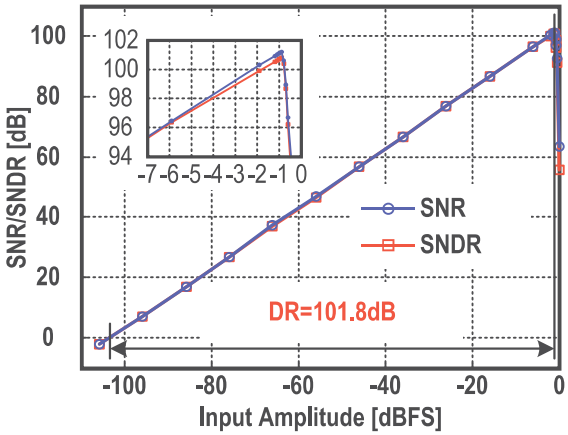

Fig. 14. Measured SNR/SNDR versus the input amplitude (DWA on).

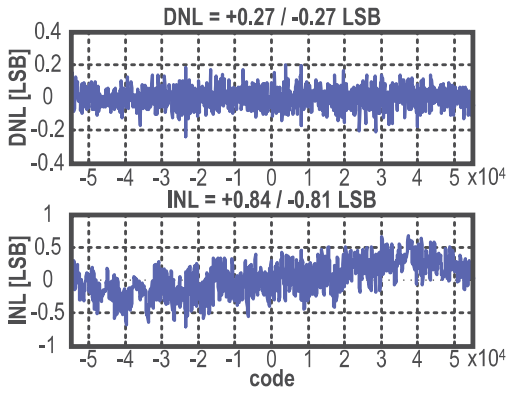

Fig. 15. Measured DNL/INL.

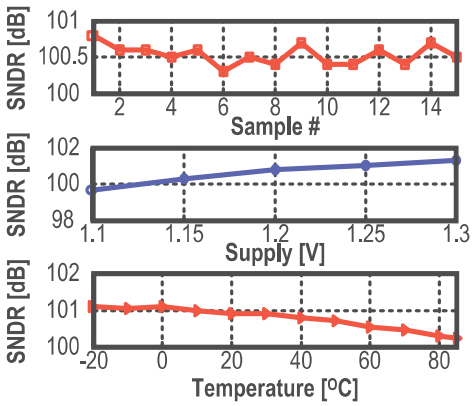

Fig. 16. Measured SNDR versus samples, V_{DD}, and temperature.

Fig. 15 presents the measured differential nonlinearity (DNL)/integral nonlinearity (INL) plots with DWA on. With the DWA technique rotating the DAC unit elements, the DNL/INL is 0.27 LSB/0.84 LSB, respectively. It confirms that the DWA technique works well in the proposed scheme and the non-uniform weighting at the exponential phase has less impact on the overall performance. Fig. 16 shows the measured SNDR spread among 15 samples, as well as from -20 °C to 85 °C and from $V_{DD} = 1.1$–1.3 V, all within 1.2-dB variations.

Table II presents the performance of this IADC and the comparison with previous works. The proposed circuit reaches competitive values, with a FoM$_S$ of 176.4 dB and a FoM$_W$ of 0.15 pJ/conv.-step, when compared with the state of the art. Fig. 17 shows the comparison with the previous ISSCC and VLSI works (data sourced from [27]). This paper achieves 100.8-dB SNDR with a competitive figure of merit (FoM) and

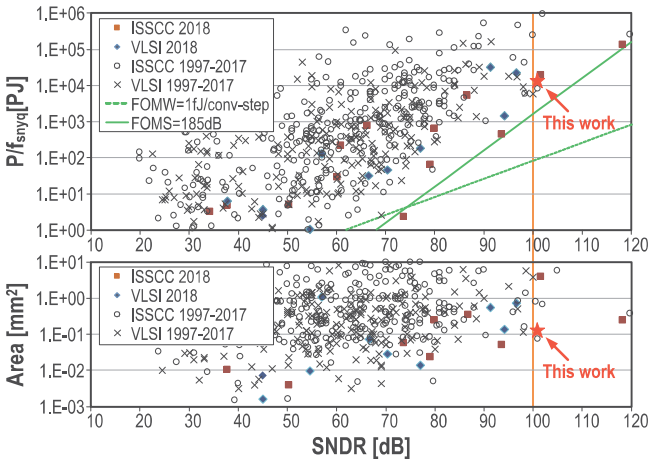

Fig. 17. Comparison with the previous works in ISSCC and VLSI.

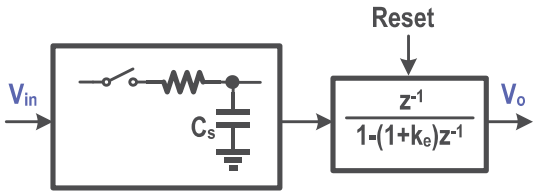

Fig. 18. Equivalent thermal noise model of the exponential IADC.

area under 1.2-V supply in a 65-nm CMOS process, which is quite good for integration with system-on-chip (SoC) chips.

VI. Conclusion

This paper proposed a single-loop linear-exponential IADC scheme, with well-balanced system-level considerations on the accumulation efficiency, the thermal noise penalty and the effectiveness of the DWA technique for DAC mismatch error. In the initial 246 cycles of the linear phase, the IADC works as a first-order architecture and fully utilizes the oversampling operation on thermal noise suppression. After that, the circuit reconfigured as an exponential phase, boosts the SQNR exponentially in 10 clock cycles. It achieved the exponential accumulation with the NC ping-pong SC circuit. The uniform-exponential weighting allows the DWA technique to work well in improving the linearity by rotating the multi-bit DAC elements. With a 17-level quantizer, the integrator can employ an energy-efficient complementary telescopic op-amp. Implemented in 65-nm CMOS with 1.2-V supply, the ADC reaches an SNDR/DR of 100.8 dB/101.8 dB with 20-kHz BW, while consuming 550 μW, resulting in FoM$_W$ and FoM$_S$ of 153 fJ-conv.-step/176.4 dB, respectively. The DWA technique produces high linearity with DNL/INL of 0.27 LSB/0.84 LSB.

Appendix

A. Input-Referred Thermal Noise for Exponential Incremental ADC

Fig. 18 shows the thermal noise in the sampling network added before the integrator. Furthermore, the thermal noise is injected into the exponential integrator and the noise power is kT/C_s. Thus, at the end of one conversion with N clock cycles, the noise power at V_o due to the kT/C_s noise injected only at the first cycle is

$$V_n^2(1) = \frac{2kT}{C_s}(1+k_e)^{2N-2} \tag{17}$$

where the factor of 2 accounts for the differential circuit in the real implementation. Generally, the noise power at V_o due to the kT/C_s noise injected at the ith clock cycles can be expressed as

$$V_n^2(i) = \frac{2kT}{C_s}(1+k_e)^{2N-2i}. \tag{18}$$

Thus, after one complete conversion, the total power at V_o due to kT/C_s noise injected by all the cycles is

$$V_{n,\text{total}}^2 = \frac{2kT}{C_s}\sum_{i=1}^{N}(1+k_e)^{2N-2i} \tag{19}$$

Furthermore, (19) is a geometric series with exponentially decaying kT/C_s noise power. With the exponential accumulation, the gain of the input at V_o is

$$G_{\text{in,exp}} = \sum_{i=1}^{N}(1+k_e)^{N-i}. \tag{20}$$

Thus, the input-referred thermal noise can be derived as

$$V_{n,\text{input}}^2 = \frac{V_{n,\text{total}}^2}{G_{\text{in,exp}}^2} = \frac{2kT}{C_s}\,\frac{(1+k_e)^{2N}-1}{k_e+2}\,\frac{k_e}{[(1+k_e)^N-1]^2}. \tag{21}$$

With a moderately larger coefficient k_e and an OSR N, we can assume that $(1+k_e)^N \gg 1$. The assumption, in fact, always stands up for a high-resolution IADC. Thus, (21) can be simplified as follows:

$$V_{n,\text{input}}^2 = \frac{2kT}{C_s}\,\frac{1}{1+\frac{2}{k_e}}. \tag{22}$$

That is, by taking the limit, the oversampling does not effectively contribute to the suppression of the kT/C noise in exponential IADCs.

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Outstanding Chapter Award, the Science & Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, the National State S&T Progress Award in 2011, and the 2012, 2014, and 2016 Macau S&T Invention Award and Progress Award. In recognition of his contribution in academic research and industrial development, he was a recipient of the Macau SAR Government Honorary Title of Value in 2010. He was also elected as the "Scientific Chinese of the Year 2012." He is the Honorary Founding Chairman of the SSCS Macau Chapter. He is appointed as a member of the S&T Commission of the China Ministry of Education and S&T Committee of Macau SAR. He is currently the TPC of ISSCC, the Sub-Committee Chair (Data Converters) of A-SSCC, the Analog Sub-Committee Chair of VLSI-DAT, and the Editorial Board Member of the Journal AICSP. He was the IEEE SSCS Distinguished Lecturer from 2014 to 2015 and the A-SSCC 2013 and ISSCC 2018 Tutorial Speaker. He was the Technical Review Committee of various IEEE journals and the Program Committee/Chair of the IEEJ AVLSIWS, the IEEE APCCAS, ICICS, PRIMEAsia, and ASP-DAC.

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Prof. Maloberti was a recipient of the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, the IEEE Millenium Medal, the 1996 IEE Fleming Premium, the ESSCIRC 2007 Best Paper Award, the IEEJ Workshop 2007 and 2010 Best Paper Award, and the IEEE CAS Society 2013 Mac Van Valkenburg Award. He is the Past President of the IEEE CAS Society. He was the VP Region 8 of the IEEE CAS from 1995 to 1997, an Associate Editor of the IEEE-TCAS-II, the President of the IEEE Sensor Council from 2002 to 2003, the IEEE CAS BoG Member from 2003 to 2005, and the VP Publications IEEE CAS from 2007 to 2008. He was the DL IEEE SSC Society from 2009 to 2010, and the DL IEEE CAS Society from 2006 to 2007 and 2012 to 2013.

Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D., and Habilitation degrees for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), Universidade de Lisboa, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since 1980, he has been with the Department of Electrical and Computer Engineering (DECE), IST. Since 1992, he has been on leave from IST. He is currently with the Faculty of Science and Technology (FST), Department of Electrical and Computer Engineering, University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. From 1994 to 1997, he was the Dean of the Faculty of the FST. Since 1997, he has been a Vice-Rector with the University of Macau. From 2008 to 2018, he was a Vice-Rector (Research) and a Vice-Rector Global Affairs since 2018. He was a Co-Founder of Synopsys, Macau, from 2001 to 2002, and created in 2003, the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to State Key Laboratory of China (the first in Engineering in Macau), where he became a Founding Director. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and at UM, has supervised (or co-supervised) 45 theses, Ph.D. (24) and master's (21). He has co-authored seven books and 11 book chapters, 466 papers, in scientific journals (162) and in conference proceedings (304), and 64 academic works, for a total of 580 publications. He holds 30 U.S. patents and two Taiwan patents.

Dr. Martins was a Nominations Committee Member of the IEEE CASS in 2016 and a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019. He was a Founding Chairman of both the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on CAS/COM from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society]. He was the General Chair of the 2008 IEEE Asia–Pacific Conference on CAS—APCCAS'2008 and was a Vice President of Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. He was a Vice-President (World) of the Regional Activities and Membership of the IEEE CASS from 2012 to 2013. He was the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. He was the Chair of the IEEE CASS Fellow Evaluation Committee in 2018.. In 2010 was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences in Lisbon, is the only Portuguese Academician living in Asia. He was a recipient of two government decorations: the Medal of Professional Merit from Macau Government (Portuguese Administration) in 1999, the Honorary Title of Value from Macau SAR Government (Chinese Administration) in 2001, the IEEE Council on Electronic Design Automation Outstanding Service Award 2016, and nominated Best Associate Editor of TRANSACTIONS ON CAS II from 2012 to 2013. He served as an Associate Editor for the IEEE TCAS II: EXPRESS BRIEFS from 2010 to 2013.