0.0012 mm^2, 8 mW, single-to-differential converter with < 1.1% data cross error and < 3.4 ps RMS jitter up to 14 Gbit/s data rate

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An extremely compact, doubly balancing single-to-differential converter (S2D) for high-speed wireline systems is reported. It incorporates a two-stage topology with 'coarse balancing' in the first stage and 'fine balancing' in the second stage by adopting a compact 'positive-feedback active inductor' that simultaneously boosts the signal bandwidth. Fabricated in 65 nm CMOS, the S2D measures < 1.1% data cross error and < 3.4 ps RMS jitter up to a 14 Gbit/s data rate. The die occupies 0.0012 mm^2 and consumes 8 mW.

Introduction: Wideband-balanced single-to-differential converters (S2D) find extensive applications in data [1] and clock [2] paths of broadband wireline transceivers. Especially for the former, as shown in Fig. 1, the S2D has to interface the single-ended transimpedance amplifier (TIA) with the multi-stage limiting amplifier that should operate differentially for optimised performance. This Letter describes a novel two-stage S2D using a current-reuse active inductor (AI), which is very power and area efficient, while ensuring superior differential balancing quality over a wide range of bandwidth (data rate).

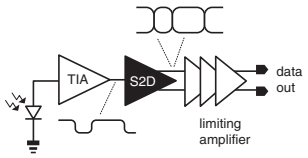

Fig. 1 *A wideband highly balanced S2D interfaces the TIA with the limiting amplifier*

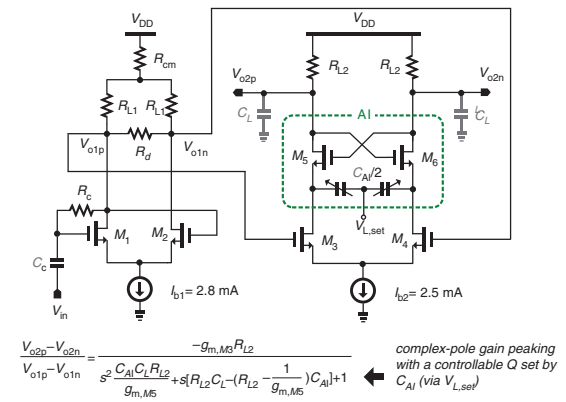

Fig. 2 *Proposed two-stage S2D with an AI-embedded second stage*

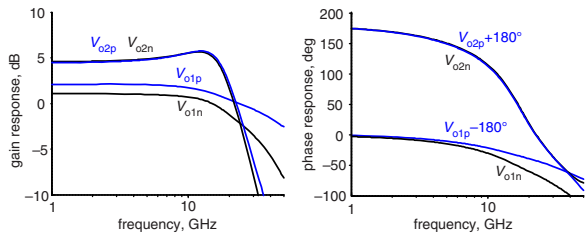

Fig. 3 *Simulated gain and phase responses at $V_{o1p,n}$ and $V_{o2p,n}$*

Proposed two-stage S2D with an AI: The schematic is depicted in Fig. 2. For area savings, the first stage employs an inductorless version of the S2D in [2]. The bandwidth limitation will be overcome in the second stage, to be described later. The first stage converts the single-ended input (V_{in}) into a coarsely balanced differential output (V_{o1p}, V_{o1n}). M_1 and R_c create a self-biased input common-mode level. They, along with M_2, also form a local feedback boosting the voltage gain and lowering the waveform distortion. R_{cm} optimises the output common-mode level. The layout-simulated AC responses of V_{o1p} and V_{o1n} are shown in Fig. 3. The gain (e.g. 1.1 dB at 15 GHz) and phase (e.g. 15.2° at 15 GHz) mismatches are still apparent, as plotted in Fig. 4. In terms of large-signal operation, a transient simulation with 160 mV_{pp} random data (PRBS 2^7–1) shows that the swing mismatch of V_{o1p} and V_{o1n} is ~16% up to 14 Gb/s (Fig. 5).

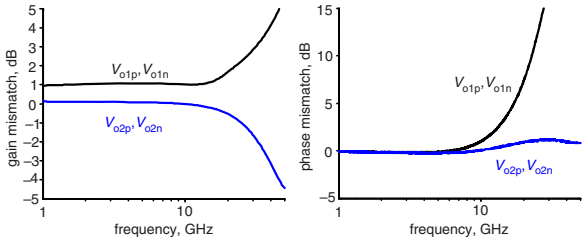

Fig. 4 *Simulated gain and phase mismatches at $V_{o1p,n}$ and $V_{o2p,n}$*

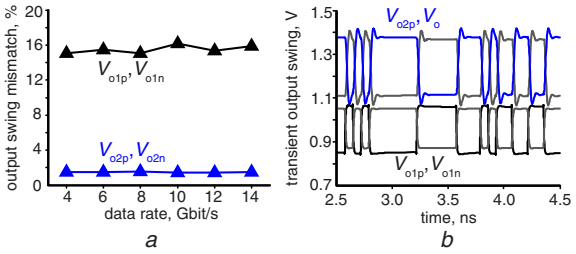

Fig. 5 *Simulation results*
a Output swing mismatch against data rate
b Transient waveforms at 14 Gbit/s under an input swing of 160 mV_{pp}

The second stage is to address the bandwidth and balancing issues. It is a differential amplifier with an embedded current-reuse AI. This AI was employed as a sub-circuit of a low-frequency lowpass filter reported in [3]. This work advances its use in a wideband S2D with large-signal operation, also revealing its differential balancing property. The AI ($M_{5,6}$ and C_{AI}) is directly stacked atop the differential pair ($M_{3,4}$). Owing to the improved parasitics of nanoscale CMOS and the simplicity of this highly transistorised AI, $M_{5,6}$ effectively operates as a wideband positive-feedback impedance converter, transferring the capacitive behavior of C_{AI} into inductive at $V_{o2p,n}$. For instance, with a 2.5 mA bias current (I_{b2}), a gain peak beyond 10 GHz is achievable. Other merits of this AI are: (1) no bias circuit, (2) easy and wide inductance tunability if C_{AI} is a MOS varactor that has a high Q factor, (3) high self-resonant frequency because of no inner parasitic poles and (4) power efficiency, as it can be merged with another circuit for current reuse.

Interestingly, the AI also serves as a 'differential' current buffer. It absorbs the currents from M_3 and M_4 with a differential input impedance ($2/g_{m5}$, where g_m is the transconductance of the corresponding MOSFET), forcing the two currents to undergo another balancing process before driving to R_{L2}. Differing from [4] as its differential balancer entails AC coupling for cross-connection between the gate and source terminals, here the balancing is wideband in nature because of direct DC coupling between the drain and gate terminals. The simulated AC responses at $V_{o2p,n}$ are plotted also in Fig. 3. Both bandwidth enhancement and gain-phase balancing are achieved. Up to 15 GHz, the gain (0.21 dB) and phase (2.2°) mismatches are effectively suppressed when comparing with $V_{o1p,n}$ (Fig. 4). In large-signal transient simulations, the swing mismatch at V_{o2p} and V_{o2n} is reduced to 1.5% up to 14 Gbit/s (Fig. 5).

Small-signal analysis gives the transfer function of the second stage (bottom of Fig. 2). Without affecting the power and feature of the differential balancing, the complex-pole peaking at 10 GHz can be set by putting a variable capacitor for C_{AI}, which can be optimised or calibrated via $V_{L,\,set}$ (e.g. 1.6–0.6 V lead to peaking between 1.59 and 4.7 dB) to accommodate different sizes of C_L for an optimised response. Here, C_L is associated with the size of the test buffer, which is not oversized for measurements beyond 14 Gbit/s, even though the S2D can operate up to 20 Gbit/s in layout simulations.

Experimental results: The S2D was fabricated in 65 nm CMOS. The die size was only 0.0012 mm^2 (Fig. 6). Both the input and output pads (120 fF capacitance) were tailored for double-wire bonding (600 pH inductance) to facilitate high-speed testing. The single-ended

data input with a PRBS of 2^7–1 was generated by a J-BERT N4903B. The output eye diagrams were captured via the DCA-X 86100D oscilloscope at 6 and 14 Gbit/s, as shown in Fig. 7. The measured key performances (RMS jitter, Pk-to-Pk jitter, data cross percentage and eye opening rate) under 4–16 Gbit/s data rates are plotted in Fig. 8. The low data cross error (< 1.1%) and low RMS jitter (< 3.4 ps) substantiate the feasibility of the proposed S2D. The eye opening rate drops to 40% at 16 Gbit/s as expected, which should be limited by the test buffer and PCB parasitic effects. Table 1 summarises the chip results with data input. The S2D also demonstrates promising performances for clock input, but because of the space limit these results are omitted.

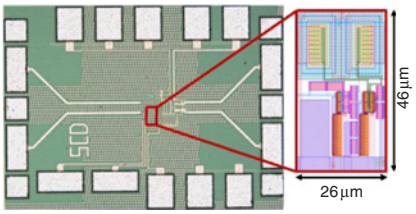

Fig. 6 *Chip photo of the S2D with a zoomed view of the active part*

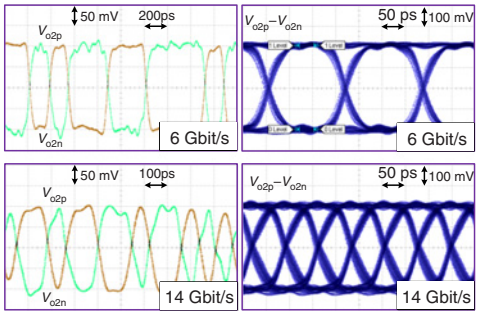

Fig. 7 *Measured single-ended outputs and differential eye diagrams measured at 6 Gbit/s (upper) and 14 Gbit/s (lower)*

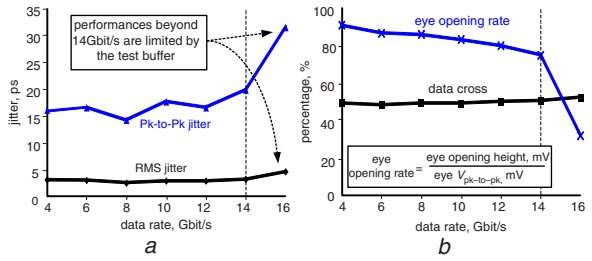

Fig. 8 *Measurement results*

a Pk-to-Pk jitter and RMS jitter against data rate
b Eye opening rate and data cross against data rate

Table 1: Performance summary

Technology	65 nm CMOS
Data rate	up to 14 Gbit/s
Data cross percentage	< 1.1%
RMS jitter	3.4 ps @ 14 Gbit/s
Pk-to-Pk jitter	20 ps @ 14 Gbit/s
Eye opening rate	75% @ 14 Gbit/s
Supply voltage	1.5 V
Power	8 mW
Die area	0.0012 mm^2

Conclusions: Thanks to the two-stage topology with a compact AI for bandwidth enhancement and differential balancing, the proposed S2D achieves very low data cross error, while inducing small jitter and eye opening rate degradation over a wide range of data rate. These beneficial features render this work a superior S2D candidate for cost and power reduction of wireline systems in nanoscale CMOS.

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One or more of the Figures in this Letter are available in colour online.

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