A 0.05- to 10-GHz, 19- to 22-GHz, and 38- to 44-GHz Frequency Synthesizer for Software-Defined Radios in 0.13-μm CMOS Process

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***Abstract*—This brief presents a fully integrated frequency synthesizer for software-defined radios covering not only all the existing wireless standards from 47 MHz to 10 GHz [including 14-band multiband orthogonal frequency-division modulation (MB-OFDM) ultrawideband (UWB)] but also the gigabits per second wireless communication around 60 GHz. A dual-band quadrature output voltage-controlled oscillatior reconfigurable as either a one-port oscillator for low power consumption or a two-port oscillator for low phase noise is employed as the core to generate all the frequencies from 47 MHz to 6 GHz. A multimode x3/x5/x7 injection-locked frequency multiplier and a single-sideband mixer with a tunable transformer-based narrow-band load are proposed to generate the carrier frequencies for the 14 MB-OFDM and impulse UWB bands with fast settling time, low power, and small chip area. An automatic amplitude calibration (APC) technique is proposed to greatly increase the locking range of the subharmonic injection-locked oscillators with achieving a given output amplitude. Implemented in a 0.13-μm CMOS process, the synthesizer prototype occupies an active area of 3 μm^2, consumes 33–83 mW in total, and measures phase noise of -139.6 dBc/Hz at 3-MHz offset from a 1.7-GHz carrier.**

***Index Terms*—Dual band, fast hopping, frequency synthesizer, injection-locked frequency multiplier (ILFM), injection-locked oscillator, millimeter-wave (mm-wave), software-defined radio (SDR), subharmonic injection, ultrawideband (UWB), voltage-controlled oscillator (VCO).**

I. Introduction

MODERN wireless radios are required to support many different standards with different carrier frequencies, bandwidth, and modulation schemes, in order to support different wireless service providers in different countries and regions and to fulfill end user's requirement for diverse applications such as voice, video, television broadcasting, games, and positioning. Such challenging demand has motivated the development of software-defined radios (SDRs), whose hardware cannot only be shared but also be readily reconfigured and defined by software to accommodate existing and incoming wireless standards and applications without involving additional expensive research and development period.

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As the key building block of such SDRs, SDR frequency synthesizers need to be reconfigurable to generate local oscillator (LO) signals with ultrawideband (UWB) frequency tuning range over many decades while still meeting the phase noise specifications with minimum power consumption. In [1]–[5], multiple voltage-controlled oscillators (VCOs), together with divide-by-2 dividers, are employed to cover the wide frequency band at the cost of large chip area occupied by multiple inductive coils. In [6], the required tuning range of VCO was reduced by employing mixers to perform frequency summing and subtraction. However, LC filters with extra inductive components are still required to alleviate the image and spurious emission problem. In addition, divider circuits with integer division ratios larger than 2 [7], [8] and fractional division ratios [9], [10] can also help reduce the tuning range requirement of the VCO. However, these dividers suffer from degradation in in-phase and quadrature-phase (IQ) accuracy. Moreover, fractional dividers would generate rich nonharmonic spurs, which would require complex calibration algorithm to reduce spur level [9], [10]. Recently, multiband and wideband VCOs are implemented for multistandard applications [11], [12]. By properly dealing with inductors or transformers (TFs), these VCOs can achieve multimode operations without increasing number of inductive coils while still keeping low phase noise performance.

In this brief, an UWB IQ LO generation system for SDRs is proposed to support not only all the existing wireless standards from 47 MHz to 10 GHz, including the 14-band multiband orthogonal frequency-division modulation (MB-OFDM) UWB standard, but also the 802.15.3c standard at the millimeter-wave (mm-wave) frequency from 57 to 66 GHz [13]. In addition, the proposed UWB frequency synthesis scheme based on a reconfigurable injection-locked frequency multiplier (ILFM) and a single-coil tunable narrow-band TF tank for the single-sideband (SSB) mixers helps minimize spur, power consumption, and chip area. Finally, subharmonic injection-locked oscillators (SH-ILOs) as frequency doubler and tripler with the automatic amplitude calibration (APC) technique are used to generate 20-GHz IQ and 40-GHz differential signals for dual-conversion transceivers operating from 57 to 66 GHz.

II. Proposed System Architecture

Fig. 1 shows the system architecture of the proposed SDR frequency synthesizer. A dual-band quadrature-output voltage-controlled oscillatior (QVCO) generates 3- to 4.2-GHz and 8.4- to 12-GHz IQ signals [12]. Together with divider A and Mux A, the 3- to 6-GHz IQ LOs can be generated. The 47-MHz-to-6-GHz IQ LOs are further derived with only divide-by-2 operation. The carriers for 14-band MB-OFDM UWB are generated by SSB mixing the fundamental frequency

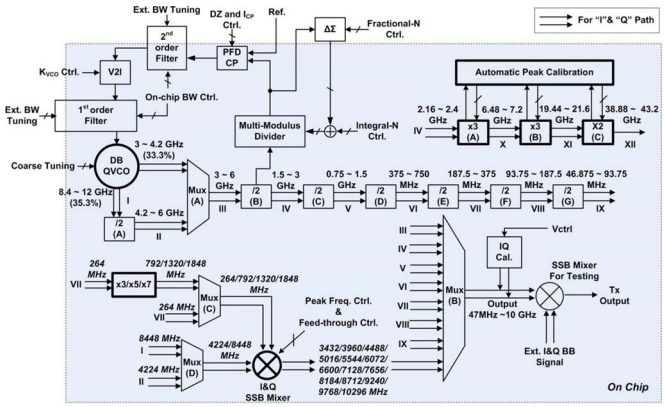
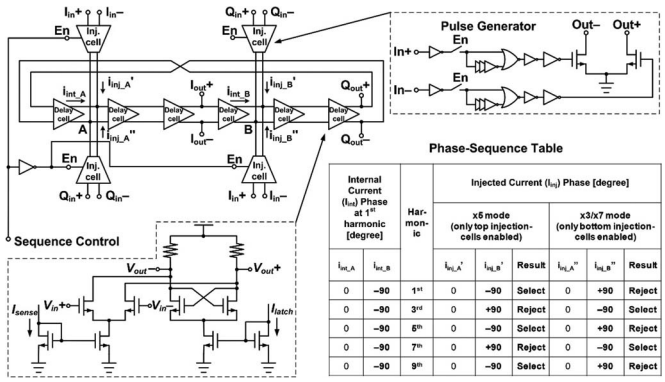


Fig. 1. System architecture of the proposed SDR frequency synthesizer.



Phase-Sequence Table

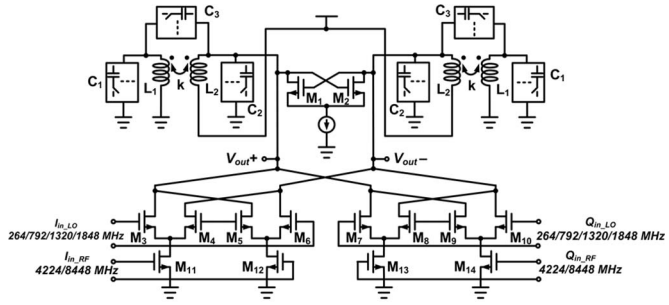
Internal Current (I_{int}) Phase at 1st harmonic [degree]		Har-monic	Injected Current (I_{inj}) Phase [degree]					
			x5 mode (only top injection-cells enabled)			x3/x7 mode (only bottom injection-cells enabled)		
i_{int_A}	i_{int_B}		i_{inj_A}'	i_{inj_B}'	Result	i_{inj_A}''	i_{inj_B}''	Result
0	−90	1st	0	−90	Select	0	+90	Reject
0	−90	3rd	0	+90	Reject	0	−90	Select
0	−90	5th	0	−90	Select	0	+90	Reject
0	−90	7th	0	+90	Reject	0	−90	Select
0	−90	9th	0	−90	Select	0	+90	Reject

Fig. 2. Schematic and phase sequence table of x3/x5/x7 ILFM.

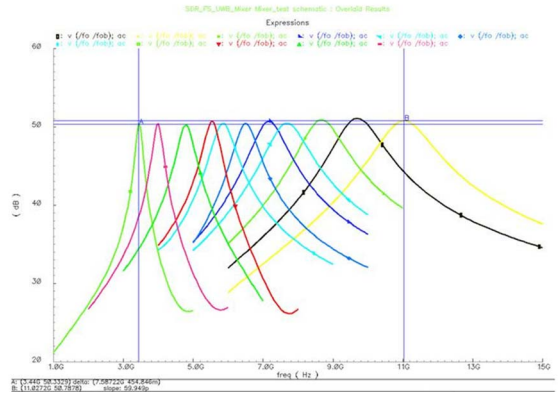
of 8448/4224 MHz, which is directly obtained from the outputs of the QVCO or of divider A, with the frequency of 264/792/1320/1848 MHz generated by feeding the output of divider E into a trimode x3/x5/x7 ILFM. For the mm-wave frequency generation, a frequency multiplier chain based on x3 and x2 SH-ILOs is employed to generate the 19- to 22-GHz IQ and 38- to 44-GHz differential signals by multiplying the output frequency of divider B by 9 and 18, respectively. These two LOs can be used for dual-conversion transceivers operating from 57 to 66 GHz to support the 802.15.3c standard. Here, an APC technique is proposed to maximize the output power of each SH-ILO. The QVCO's output frequency is controlled and stabilized by a phase-locked loop (PLL), with all the loop parameters highly reconfigurable, including adjustable dead-zone period, charge pump (CP) current, loop filter bandwidth, V2I converter's transconductance, and, thus, K_{VCO}.

III. Fast-Hopping UWB Tone Generation

Fig. 2 shows the block diagram of the proposed reconfigurable x3/x5/x7 ILFM for UWB tone generation together with the schematics of individual delay and injection cells. The core is a ring oscillator (RO) with an internal IQ sequence. Injection cells with opposite IQ sequences are employed to convert sinusoidal injection signals into narrow pulses with rich harmonics injected into RO. All even harmonics of input pulses are effectively rejected by using differential circuitry. RO exhibits an interesting property that it only accepts input harmonics of consistent IQ sequence with its own internal IQ sequence for better energy efficiency. As shown in the table in Fig. 2, in x5 mode, when only the top pair of injection cells are turned on,



(a)



(b)

Fig. 3. (a) Schematic of the SSB mixer with a TF-based tunable narrow-band load. (b) Simulated frequency tuning response of the TF-based LC tank (only dominant peak is plotted for clarity).

because the IQ sequence of the first, fifth, ninth,... harmonics of the injected current (I_{inj}) is consistent with the one of RO's fundamental harmonic current, they are selected by the RO. On the other hand, because the IQ sequence of the third, seventh,... harmonics of I_{inj} is reversed, they are rejected by the RO. In addition, by controlling the bias current I_{sense} and I_{latch} of the delay cells in Fig. 2 to adjust the RO's self-oscillation frequency close to 5× of input frequency, the first and ninth harmonics can be significantly filtered out because they are far away enough. In ×3/×7 mode, the third and seventh harmonics of I_{inj} are selected by enabling only the bottom pair of injection cells, which have the reversed input IQ sequence.

Fig. 3(a) shows the schematic of the SSB mixer with a TF-based tunable narrow-band load, which is able to achieve much better sideband rejection at the mixer's output than simply using a shunt-peaking wideband load. To make the peak frequency tunable in a wide frequency range from 3.432 to 10.296 GHz to cover all the 14-band carriers, a TF-based high-order LC tank is proposed. In Fig. 3, the TF is designed to be tightly coupled. As the analysis in [12] and [14], denoting $\omega_1 = (L_1C_1)^{-1/2}$ and $\omega_2 = (L_2C_2)^{-1/2}$ and assuming $\omega_2 > \omega_1$, the mixer load impedance Z_{22} seen from the secondary coil of the TF has two peak frequencies (one lower than ω_1, one higher than ω_2). The higher frequency peak would dominate and can be utilized when the notch-peak cancellation condition is fulfilled with a large frequency ratio ω_2/ω_1 by maximizing C_1 and limiting C_2. On the other hand, by keeping a small or a moderate C_1/C_2 ratio, the lower frequency peak becomes dominant and can be utilized. To further extend the frequency tuning range, a third switched-capacitor array C_3 is added across the primary and secondary coils, which provides another path to make L_1 in parallel with L_2. If C_3 increases, the effective L_1 is also increased.

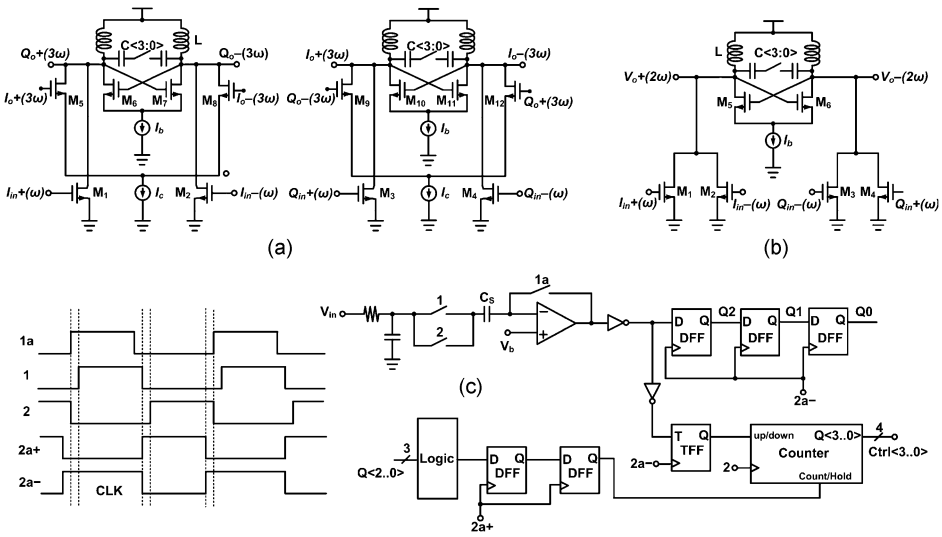


Fig. 4. Schematics of the (a) IQ x3 SH-ILO and the (b) differential x2 SH-ILO. (c) Schematic of APC and timing diagram for the controlling clocks.

As a result, the higher peak frequency is decreased. In Fig. 3(b), the postlayout simulations with TF electromagnetic (EM) model show that the desired dominant peak can be tuned from 3.4 to 11 GHz. Notice that image tone due to the IQ mismatch is $2f_{\rm LO}$ away from the desired output frequency, which is typically close but outside of the frequency range of the nondominant peak. However, the spurs due to harmonic mixing can be $4f_{\rm LO}$ away from the desired output frequency, which can fall into the frequency range of the nondominant peak. As a result, the frequency of the nondominant peak is carefully designed to be far away from the spurious tones.

IV. Millimeter-Wave Frequency Generation

In the mm-wave frequency generation part, the x3 and x2 subharmonic ILOs are cascaded to generate the LO at 19–22 and 38–44 GHz from div-2 (B) output, as shown in Fig. 1. Fig. 4(a) shows the schematic of the x3 SH-ILO with IQ outputs. Transistors M_{1-4} are hard switched by the IQ input signals at the input frequency ω to generate a strong third harmonic tone that locks a QVCO self-oscillating around 3ω. Fig. 4(b) shows the schematic of the x2 SH-ILO. The IQ input signals at the input frequency ω are applied to two push–push pairs to generate differential injection signals at the frequency 2ω. By doing so, the differential oscillator self-oscillating around 2ω can be naturally locked by the differentially injected currents. Although the phase information is lost from the input to the output, this x2 SH-ILO output is free of subharmonic tones because the odd-harmonic components of the input current are all cancelled by the push–push pair.

For the LC-based injection locked circuit, the mismatch between the input frequency and the LC tank's peak frequency would degrade the performance of the ILO in terms of the output swing, phase noise, and suppression of spurious tones and may even prevent the circuit from functioning. To enforce the alignment, existing calibration techniques employ an extra phase-locked loop to calibrate the peak frequency, which requires large chip area [15], [16]. In particular, a wideband and reliable frequency divider at mm-wave frequency is not easy to achieve with the used 0.13-μm process. Instead, a different technique APC is proposed here to calibrate the peak frequency in digital domain with negligible power and area. Making use of the property that the output swing is maximized when the LC tank's peak frequency is aligned with input frequency, the frequency calibration can be done by detecting and maximizing the output swing while adjusting the capacitor bank's control bits. It is worthwhile to note that, since the relationship between the loading capacitance and the output amplitude is not monotonous, a simple negative feedback loop would not work.

Fig. 4(c) shows the schematic and timing diagram of the proposed APC circuit, in which a squaring circuit is used to detect the output amplitude of the SH-ILO. Notice that clocks 1 and 2 are nonoverlapping clocks. They are the delayed versions of clocks 1a and 2a+ in several nanoseconds. During peak calibration, the biasing current $\rm I_b$ of the SH-ILO is much reduced to greatly enlarge the injection ratio and thus the locking range of the SH-ILO. At the rising edge of clock 1, the amplitude of the SH-ILO, i.e., $\rm V_{in}$, from the squaring circuit is sampled and stored in a sampling capacitor $\rm C_S$. At the rising edge of clock 2, the counter counts up or down by 1 and change the LC tank's peak frequency by tuning the capacitor bank $\rm C\langle 3:0\rangle$ in the LC tank of the SH-ILO, and the second sample of the amplitude $\rm V_{in}$ is obtained. By the falling edge of clock 2, the comparator compares the two samples and delivers the result to the shift register (SR). If the result is positive, the counter keeps counting toward the same right direction. Otherwise, the toggling register changes the counting direction. The states stored in the SR control the logic to hold the counter when the maximum amplitude $\rm V_{in,max}$ is found. Once the calibration is done, $\rm I_b$ of the SH-ILO is increased to its default value for larger output power.

V. Measurement Results

The proposed SDR frequency synthesizer is fabricated in a 0.13-μm CMOS process. Fig. 5 shows the chip photograph, which occupies an area of 2.5×1.5 mm^2, excluding pads.

To verify the effectiveness of the filtering provided by the proposed TF-based tunable narrow-band load of the SSB mixer, the same SSB mixer with a shunt-peaking wideband load is also implemented in another test chip. Fig. 6(a) summarizes the measured spur rejection in the MB-OFDM UWB mode. The frequency synthesizer achieves spur rejection from 31.3 to 41.5 dB for all the 14-band carriers with the proposed narrow-band filtering, whereas spur rejection from 15 to 26 dB is

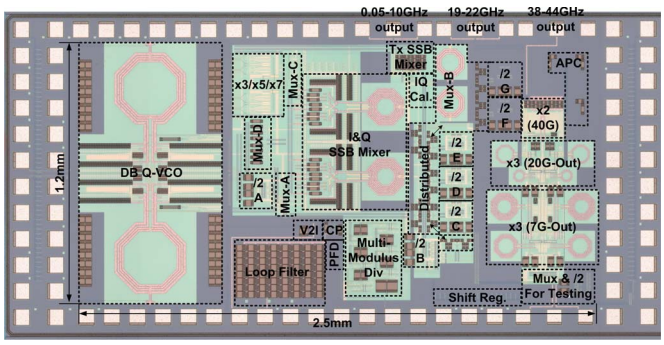


Fig. 5. Chip micrograph of the proposed SDR frequency synthesizer.

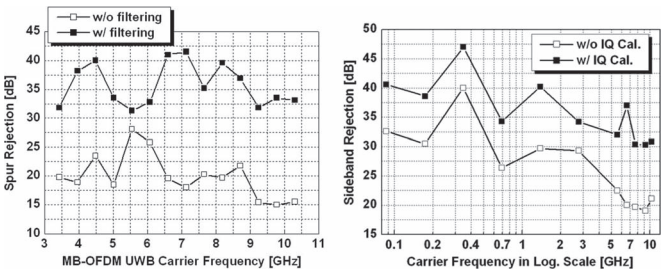


Fig. 6. (a) Measured spur rejections at MB-OFDM UWB mode. (b) Measured sideband rejection with and without IQ calibration.

obtained with a shunt-peaking wideband load. Fig. 6(b) shows the measured sideband rejection ratios (SBRs) with different carrier frequencies from 100 MHz to 10 GHz. Without IQ calibration, the SBR varies from 19 to 40 dB, corresponding to IQ phase error of from 1.1° to 12.6° assuming no amplitude mismatch. After the IQ calibration, the SBR is improved to from 30.3 to 47 dB, corresponding to IQ phase error of from 0.5° to 3.4°. Since the residue phase error is less than 5°, it can be further calibrated out by digital baseband.

Fig. 7(a) shows the measured swing with and without APC at the 20-GHz output. In both cases, the SH-ILO chain measures a continuous locking range from 18 to 22.5 GHz. Without APC, the single-ended output swing is above 400 mV within the required frequency range, whereas the minimum output swing is improved to 600 mV with APC enabled. Fig. 7(b) shows the single-ended swing at the 40-GHz output. The SH-ILO chain measures a continuous locking range from 36.9 to 44.1 GHz. Without APC, the output swing varies from 50 to 590 mV within the required frequency range. With the APC enabled, the output swing is improved to from 250 to 810 mV, respectively. In terms of effective locking range for a given minimum required output swing of 300 mV, the proposed APC technique improves the effective locking range of the whole SH-ILO chain from 5.5% (40.5 to 42.8 GHz) to 11.3% (39.2 to 43.9 GHz).

Fig. 8 shows the measured closed-loop phase noise at different offset frequencies, rms phase errors, IQ phase errors, and the associated power consumption across the entire output frequency range. At global system for mobile (GSM) mode, phase noise values of −141.7 and −139.6 dBc/Hz are measured at 3-MHz offset from 900-MHz and 1.7-GHz carriers, respectively. The rms phase error is below or around 1° for frequencies below 2.5 GHz and gradually increases to around 20° at 40 GHz. With IQ calibration, the measured IQ phase error is <3.4° from 47 MHz to 10 GHz. The measured reference spur is below −57 dBc. In MB-OFDM UWB mode, the spurs are below

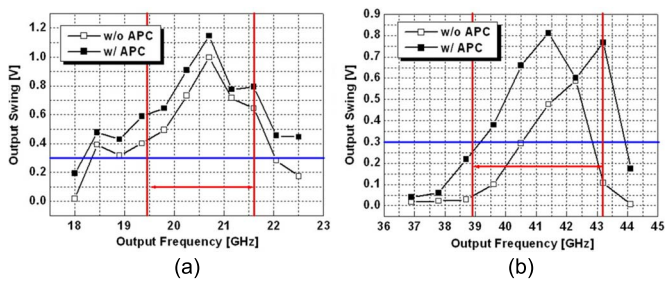


Fig. 7. Measured swings at SDR frequency synthesizer's (a) 20-GHz and (b) 40-GHz outputs.

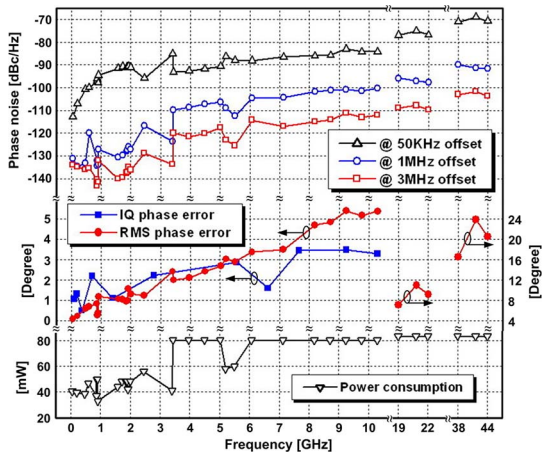


Fig. 8. Measured phase noise, IQ phase error, rms phase error, and power consumption as functions of carrier frequency.

−31 dBc, and the channel-hopping time is within 3.7 ns. Under a 1.2-V supply, the frequency synthesizer consumes around 33 mW for ZigBee standard (even with reducing VCO current at the expense of worse phase noise), 50 mW for GSM standard, 60 mW for wireless local area network standard, and 80 mW for UWB and 802.15.3c standard.

The detailed performance of the SDR frequency synthesizer is summarized and compared with the specifications in Table I. The frequency synthesizer meets the phase noise specifications for all the wireless standards, except DCS/PCS band GSM, in which the measured close-loop phase noise is degraded by 3 dB as compared with the open-loop measurement. Simulations show that the 3-dB degradation is contributed by small-size switches used for the QVCO's band selection, which can be easily fixed by increasing switch size with negligible extra parasitic capacitance as compared with loop filter. Table II compares the proposed SDR frequency synthesizer with other recently published wideband frequency synthesizers. It achieves the widest frequency range from 0.047 to 10 GHz, from 19 to 22 GHz, and from 38 to 44 GHz with better far-out phase noise performance. To our knowledge, this is the first wideband SDR frequency synthesizer that not only supports both the MB-OFDM and 802.15.3c UWB standards but also meets the phase noise specifications of the GSM standard.

VI. Conclusion

Combining several novel design techniques at both the system and circuit levels, a wideband IQ LO generation system for SDRs has been demonstrated to cover the frequency range from 0.047 to 10 GHz, from 19 to 22 GHz, and from 38 to

TABLE I
COMPARISON OF SPECIFICATIONS AND MEASUREMENT RESULTS

Standards		Out-Band Phase Noise[dBc/Hz]			In-Band Phase Noise [dBc/Hz]	RMS Phase Error
		Specification	Close Loop	Open Loop		
EGSM	850-900	-139.5@3MHz	-141.7@3MHz	-144.7@3MHz	-97.9@50KHz	0.4°
	DCS/PCS		-137.2~ -139.6@3MHz	-140.5~ -143.1@3MHz	-90.6~ -91.3@50KHz	0.97°~ 1.06°
UMTS	FDD	-120@3MHz	-136.3@3MHz	-140@3MHz	-91.1@50KHz	1.32°
	TDD	-145@20MHz	-145.7@20MHz	-149@20MHz		
WLAN 802.11	a/b/g/n	-102@1MHz	-112.5~ -116.8@1MHz	-113~ -119.1@1MHz	-89~ -95.8@100KHz	1.25° ~ 2.9°
WIMAX 802.16	TDD/FDD	-102@1MHz	-108.8~ -123.6@1MHz	-113~ -123.4@1MHz	-85.1~ -95.8@100KHz	1.25° ~ 3°
Bluetooth	802.15.1	-89@500KHz	-90.3*@500KHz	-112@500KHz	-80*@50KHz	4.87°*
DECT		-131@4.7MHz	-137.9@4.7MHz	-142@4.7MHz	-90.6@50KHz	1.58°
Zigbee	802.15.4	-110@10MHz	-129.3*~ -140.8*@10MHz	-139.1~-148.7@10MHz	-80* ~ -95*@50KHz	1.19°* ~ 4.87°*
UWB	802.15.3a	-100@1MHz	-100.1 ~ -109.8@1MHz	-102 ~ -110.6@1MHz	-84.2 ~ -93.1 @100KHz	2.09° ~ 5.38°
UWB	802.15.3c	-88@1MHz	20G: -97.2, 40G: -91.2 @1MHz	60G: -93.2@1MHz	20G: -75, 40G: -69 @100KHz	1.7pS (Jitter)
Broad-casting	DVB-T/H	-87@10KHz -115@1MHz	-119.9* ~ -134.7*@1MHz	-128.1 ~ -135.8 @1MHz	-91.7* ~ -107.7*@10KHz	0.1°* ~ 0.85°*
Position	GPS	-105@1MHz	-130.7@1MHz	-132.2@1MHz	-91.5@50KHz	1.08°
RFID	UHF	-144@3.6MHz	-144.3@3.6MHz	< -145.7@3.6MHz	-96.2@50KHz	0.3°

*The bias current of Q-VCO is intentionally reduced to save power while keeping sufficient margins for phase noise

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF SDR FREQUENCY SYNTHESIZERS

Ref.	[3]	[5]	[6]	[7]	[8]	[11]	[17]	[18]	This work
Technology	40 nm CMOS	0.18 µm BiCMOS	0.25 µm BiCMOS	90 nm CMOS	0.25 µm BiCMOS	90 nm CMOS	65nm CMOS	65nm CMOS	0.13 µm CMOS
Carrier freq. [GHz]	0.08~12	0.125~32	0.8~1.1, 1.5~2.1 2.3~3.1, 4.7~6.2	1.4/1.75/2/2.19/ 2.3/2.9/3.5/4.38/ 4.7/5.83/7/8.75	0.6~4.6, 5~7 10~14, 20~28	0.8~1, 1.6~2 2.2~2.8, 4.4~5.6	0.01~6.6	0.31~46.5	0.047~10, 19~22, 38~44
Reference freq. [MHz]	40	20	16.38	N/A	25	N/A	36	100	33
10KHz PN (f_c=1.7GHz) [dBc/Hz]	-102.5[1]	-94[1]	-79.8[1]	N/A	-109.9[1]	N/A	-95.1	-106.5[1]	-91~-98[1]
3MHz PN (f_c=1.7GHz) [dBc/Hz]	-132.6[2]	-137.2[1,2]	-138.5	-129.8[2]	-136.5[1,2]	-129.6[1,2]	-135.3	-138.1[1,2]	-139.6
Reference Spur [dBc]	-63	-70.2	N/A	N/A	-70	N/A	-79	NA	-57
Power [mW]	30	703~861	6.2[4]	31	680	60[5]	16~26	36~90	33~83
Core area [mm^2]	0.28	4.4[3]	2.55	0.29	4.8[2]	0.06[5]	0.38	1.82	3.0

1. Normalized to 1.7 GHz from values reported at other carrier frequencies, 2. Normalized to 3 MHz from values reported at other frequency offsets, 3. Area including pads, 4. For VCO only, 5. Power/area of the receiver front-end

44 GHz while achieving a phase noise of −141.7 dBc/Hz (close to −144.7 dBc/Hz at 3 MHz with increasing the switch size) offset from 900-MHz carrier frequency. To the best of our knowledge, it is still the first SDR synthesizer ever reported that fulfills both the frequency and phase noise specifications for existing wireless standards, including the GSM, fast-hopping MB-OFDM UWB, and 802.15.3c standards, with reasonable power consumption and chip area.

REFERENCES

[1] R. Bagheri *et al.*, "An 800-MHz–6 GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[2] V. Giannini *et al.*, "A 2-mm^2 0.1–5 GHz software-defined radio receiver in 45-nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 3486–3498, Dec. 2009.

[3] J. Borremans *et al.*, "A 86 MHz–12 GHz digital-intensive PLL for software-defined radios, using a 6 fJ/step TDC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2116–2129, Oct. 2010.

[4] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1097–1111, May 2014.

[5] S.-A. Yu *et al.*, "A single-chip 125-MHz to 32-GHz signal source in 0.18-μm SiGe BiCMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 598–614, Mar. 2010.

[6] A. Koukab *et al.*, "A GSM-GPRS/UMTS FDD-TDD/WLAN 802.11a-b-g multi-standard carrier generation system," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1513–1521, Jul. 2006.

[7] B. Razavi, "Cognitive radio design challenges and techniques," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, Sep. 2010.

[8] S. A. Osmany *et al.*, "An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1657–1668, Sep. 2010.

[9] S. Pellerano, P. Madoglio, and Y. Palaskas, "A 4.75 GHz fractional frequency divider with digital spur calibration in 45 nm CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 226–227.

[10] K. Chandrashekar, S. Pellerano, P. Madoglio, A. Ravi, and Y. Palaskas, "A 32 nm CMOS all-digital reconfigurable fractional frequency divider for LO generation in multistandard SOC radios with on-the-fly interference management," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 352–354.

[11] J. Borremans *et al.*, "A compact wideband front-end using a single-inductor dual-band VCO in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 2693–2705, Dec. 2008.

[12] S. Rong and H. C. Luong, "Analysis and design of transformer-based dual-band VCO for software-defined radios," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 449–462, Mar. 2012.

[13] S. Rong and H. C. Luong, "A 0.05-to-10 GHz 19-to-22 GHz and 38-to-44 GHz SDR frequency synthesizer in 0.13 μm CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 18–19.

[14] S. Rong and H. C. Luong, "A 1 V 4 GHz-and-10 GHz transformer based dual-band quadrature VCO in 0.18 m CMOS," in *Proc. IEEE CICC*, 2007, pp. 817–820.

[15] H. Samavati, H. R. Rategh, and T. H. Lee, "A 5-GHz wireless LAN receiver front end," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 765–772, May 2000.

[16] J. Lee and H. Wang, "Study of subharmonically injection-locked PLL," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[17] W. Deng *et al.*, "A compact and low-power fractionally injection-locked quadrature frequency synthesizer using a self-synchronized gating injection technique for software-defined radios," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1984–1994, Sep. 2014.

[18] Y. Jun and H. C. Luong, "A 0.37-to-46.5 GHz frequency synthesizer for software-defined radios in 65 nm CMOS," in *Proc. IEEE Symp. VLSIC Dig.*, 2014, pp. 1–2.