A 12b 180MS/s 0.068mm^2 With Full-Calibration-Integrated Pipelined-SAR ADC

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***Abstract*— This paper presents a 12b 180 MS/s 0.068 mm^2 2× time-interleaved pipelined-SAR analog-to-digital converter (ADC) with gain and offset calibrations fully embedded on-chip. The proposed binary-search gain calibration (BSGC) technique corrects the inter-stage gain error caused by the open-loop residue amplifier. The BSGC, fully integrated into the second-stage SAR ADC, contributes to a compact area. We improve the noise performance by implementing a merged-residue-DAC operation in the first-stage ADC. Also, we propose a dual-phase bootstrap technique to improve the sampling linearity in the partial interleaving architecture. The measurement results of the ADC prototype in 65 nm CMOS demonstrate the effectiveness of the proposed calibration through the enhancement of the signal to noise-and-distortion ratio from 51.5 to 60.9 dB at a Nyquist input, leading to a FoM@Nyq of 36.7 fJ/conversion-step.**

***Index Terms*— Analog-to-digital converter (ADC), successive approximation architecture, low power, switched-capacitor circuits.**

I. Introduction

BENEFITS of technology scaling favor the digital signal processing in ADCs, while placing more challenges over the analog circuits due to the decreased supply voltage and device intrinsic gain [1]. Therefore, in recent ADC designs, commonly used digital-assisted techniques compensate the non-idealities in analog circuits, such as the gain error in amplifiers [2], [3], hence allowing relaxed accuracy requirements and optimized power efficiencies. Recently, the digital-assisted pipelined successive approximation register (Pipelined-SAR) ADC emerged as a good candidate to achieve low power and high resolution [4]–[6]. According to a survey of state-of-the-art ADCs with resolution 12-bit and speed 100 MS/s, the Pipelined-SAR ADC achieves the lowest FoM when compared with SAR and pipeline ADC architectures [4]–[10]. To further boost the conversion speed the TI scheme is usually considered, while the spurs due to gain, offset and timing mismatches limit both spurious-free dynamic range (SFDR) and SNDR. The first two terms (spurs from gain and offset) are possible to be efficiently measured and corrected in the digital domain, but the cost of extra power is usually not included in the total ADC power dissipation [11], [12]. The clock skews can be suppressed by timing calibration techniques [13], [14] or avoided by ADC's operation optimization [15], [16] with an achievable accuracy around 9b. The benefit results from the fact that the clock generator can be designed with very low power to satisfy the jitter requirement only.

To further improve the power efficiency, a large number of opamps in pipeline ADCs can be reduced to only one in the two-stage Pipelined-SAR architecture [17]. Also, the 1st-stage SAR quantizes more bits with a low inter-stage gain, resulting in a relatively small opamp's output swing, thus, relaxing opamp's linearity requirement and power consumption. On the other hand, dynamic or open-loop amplifiers with digital calibration techniques have been proposed recently to improve further the ADC power efficiency. Various calibration techniques have been used extensively that exhibit good performance [11], [12], [18]–[22]. Correlation-based methods [18]–[20] measure the gain error by injecting a pseudo-random noise (PN) sequence in the residue path, which sacrifices the signal dynamic range and requires a long convergence time. Statistical-based techniques [12], [21], [22] typically impose stringent constraints on the ADC's input signal for calibration accuracy. The above calibration techniques are usually performed off-chip, while their on-chip implementations require significant area overhead due to the algorithmic complexity. For example, the calibration engine occupies ≈15% of the core chip area as mentioned in [20] and [23], and the required areas for calibration are equal or even larger than the ADC itself as referred in [19] and [22], respectively.

This paper presents a 12-bit 180 MS/s Pipelined-SAR ADC occupying 0.068 mm^2 of die area with on-chip gain and offset calibrations. The proposed BSGC technique corrects the inter-stage gain error due to the use of the open-loop amplifier, which reuses the SAR ADCs in both stages for error measurement and correction. The calibration does not rely on the type of the input signal or the extra signal injected

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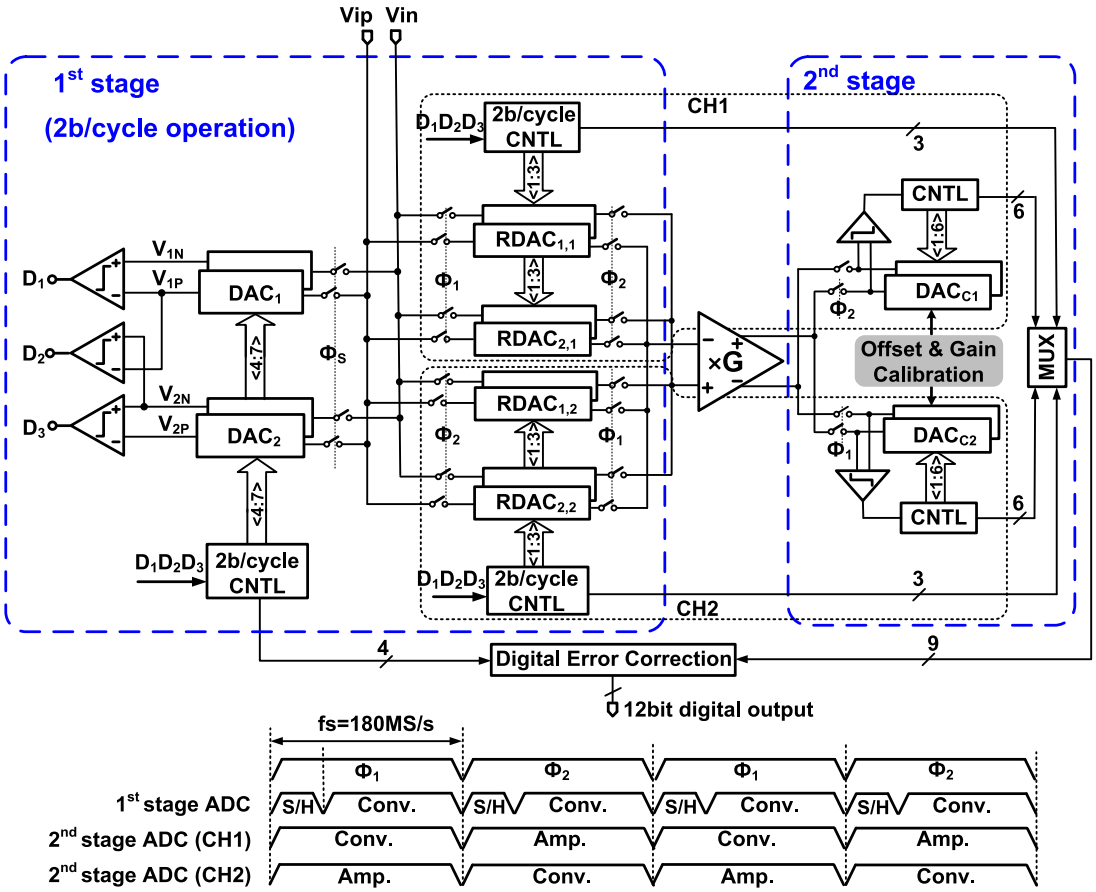


Fig. 1. PI Pipelined-SAR ADC architecture and timing diagram.

during the conversion and we achieve a short calibration time of 128 ns (ADC's start-up time). Since in the PI architecture, the kT/C noise is ultimately determined by the capacitance utilized in the amplification phase rather than the input capacitance [24], in this work, we propose a merged-residue-DAC for a 2b/cycle operation that achieves a better SNR with less design overhead. Moreover, to improve the sampling linearity, we also propose a sampling switch with a dual-phase bootstrapped scheme. We implemented the above-proposed techniques in a 12b 180 MS/s Pipelined-SAR ADC fabricated in 65 nm CMOS. The ADC achieves a SNDR of 60.9 dB @ Nyquist input and consumes 6 mW from a 1.2 V supply, which is equivalent to a FoM of 36.7 fJ/conv.-step.

The organization of the paper is the following. Section II describes the overall ADC architecture and the merged-residue-DAC operation in the 1st-stage. Section III discusses the inter-stage gain error effect and details the implementation of the BSGC technique. Section IV presents the circuit implementation of the main building blocks including the proposed dual-phase bootstrap circuit, the open-loop amplifier, and the comparator design, as well as discusses the layout considerations of the ADC. Sections V and VI show the measurement results and conclusions, respectively.

II. ADC Architecture

Fig. 1 shows the overall PI Pipelined-SAR ADC architecture and its control timing diagram. The 1st-stage utilizes a 7b 2b/cycle SAR ADC operating at a full clock rate of 180 MS/s. By adopting an interpolation technique [25], the 2b/cycle SAR operation is implemented with only two capacitive DACs. Each DAC is composed of a common DAC (DAC_1 & DAC_2) and a ping-pong residue DAC ($RDAC_{1,1}$& $RDAC_{2,1}$ / $RDAC_{1,2}$& $RDAC_{2,2}$). The ping-pong RDACs share the open-loop amplifier for residue amplification. The 2nd-stage utilizes a 2× TI 6b SAR ADC, with each one operating at 90 MS/s. The two stages have one bit overlapping for digital error correction (DEC). The offset mismatches of the 1st [26] and 2nd stage comparators [27], and the stage gain error are all calibrated on-chip. The stage gain error calibration will be introduced in Section III.

When the sampling phase of Channel 1 is enabled ($\Phi_S = 1$, $\Phi_1 = 1$), the input signal is simultaneously sampled onto the top plates of DAC_1 and DAC_2 associated with one pair of the ping-pong RDACs, e.g. $RDAC_{1,1}$ and $RDAC_{2,1}$, In the conversion phase, the coarse 7b (1b+3× 2b/cycle) conversion is performed by the first stage SAR. When the conversion is completed, DAC_1 and DAC_2 are disconnected from their previous TI counterparts and connected to another pair $RDAC_{1,2}$ & $RDAC_{2,2}$ for the next sampling. Meanwhile, $RDAC_{1,1}$ and $RDAC_{2,1}$ re-merge together and connect to the input of the op-amp to perform the residue amplification. In the subsequent pipelined phase Φ_2, the 2nd-stage determines the remaining fine 6b code that

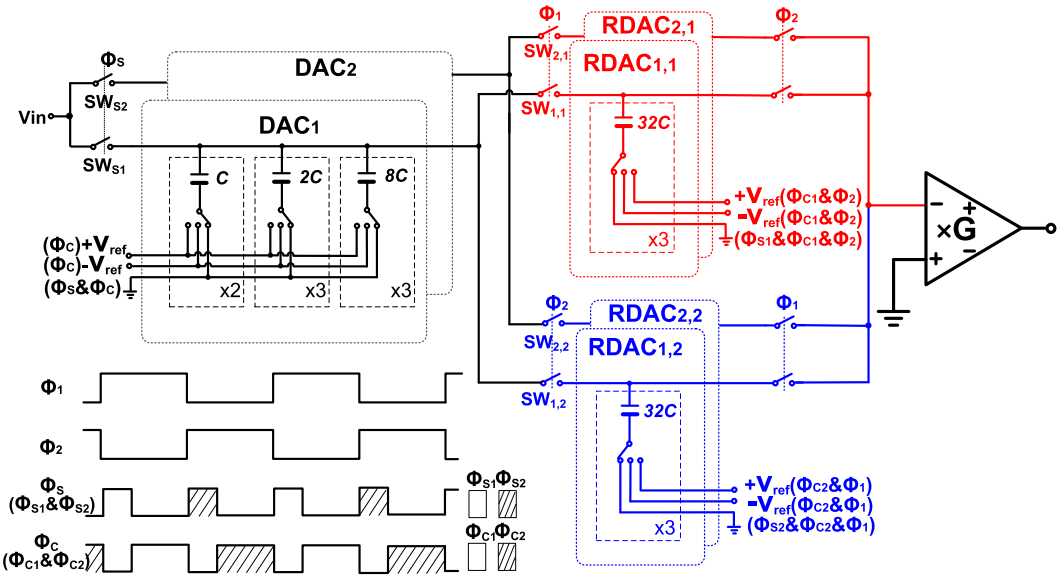


Fig. 2. Implementation of the 1st-stage DAC (single-ended).

is passed to the digital error correction logic for the final 12b output.

Fig. 2 shows the detailed first-stage DAC architecture, with a 7b DAC assigned as a segmented thermometer-code array to simplify the decoding logic. The capacitance ratio in DAC_1 and $RDAC_{1,1}$ is set as 1:3 for two reasons: one is to enlarge the capacitance attached to the amplifier for low noise [24]; the other is to facilitate an energy-efficient 2b/cycle switching operation [28]. The 7b coarse conversion starts with the comparison of the differential inputs for the most significant bit (MSB) by using one of the 3 comparators. If $V_{IN} > 0$, with the conventional switching method, the DAC output should be V_{IN}-1/2V_{REF} by switching the first two "32C"s to -1/2V_{REF}. Then, for the coming 2b comparisons, V_{IN} should be compared with three thresholds, i.e. 1/4V_{REF}, 1/2V_{REF} and 3/4V_{REF}, which is realized by precharging the third "32C" to $\pm$1/2V_{REF} in two pairs of DACs, respectively. Alternatively, by using the pre-charging free switching method [28], the equivalent DAC outputs can be approached by directly switching three "32C" in $RDAC_{1,1}$ and one "32C" in $RDAC_{1,2}$, respectively. Similarly, with the pre-charging operation merged into the bit transition, the remaining 6 bits are resolved in 3 cycles with high energy efficiency [28]. Once the conversion ends, DAC_1 and DAC_2 are released for the next sampling, while $RDAC_{1,1}$ and $RDAC_{2,1}$ that keep the same residue are re-merged and attached to amplifier input for the residue amplification.

The PI scheme reported in [16] avoids the timing skew with the cost of degrading the sampling noise performance, as the amplification capacitance, which ultimately determines the kT/C noise, is only 25% of the input capacitance. In contrast, by adopting the merged-residue-DAC operation, the amplification capacitance that amounts to 75% of the input capacitance improves the SNR by 4.75dB. Thus, this design enables a PI scheme with better noise performance. The total input-referred noise is 135 μV-rms according to the simulation results. With a full-scale of $2V_{p-p}$ this is sufficient for 12b accuracy.

TABLE I
COMPARISON OF FRONT-END DAC ARCHITECTURES IN DIFFERENT ADC DESIGNS

	Input Cap. (C_{in})	Nomi. C_{amp} (C_{amp}/C_{in})	Timing mismatch
This work	C	75%	No
PI Pipelined-SAR [16]	2C	25%	No
TI Pipelined SAR [29]	C	100%	Yes

The 2b/cycle conversion implemented in the 1st-stage achieves higher speed, but it usually demands more than double of the hardware (including capacitance) as required in 1b/cycle conversion. However, this tradeoff can be eased by using the merged-residue-DAC scheme. As listed in Table I, this design allows a 2b/cycle conversion with the input capacitance downsized to the kT/C limitation when compared with the 1b/cycle TI-SAR ADC [29] and meanwhile avoids the timing mismatch due to the PI scheme.

III. Proposed Binary-Search Gain Calibration Technique

The two-stage ADC architecture with an open-loop amplifier for residue amplification suffers from inter-stage gain error, as the gain set by $g_m R_{out}$ fluctuates significantly due to the process variation. Moreover, the top plate parasitic capacitances of the DAC arrays in the 1st- and 2nd- stages also contribute to inter-stage gain error due to the implementations of the top-plate sampling in both stages. The inter-stage gain error causes a full-scale mismatch between the two stages, inducing an overall ADC nonlinearity. Ideally, for a two-stage N-bit pipeline ADC with M-bits resolved in the 1st-stage, the least significant bit (LSB) in the 1st-stage $V_{LSB,1}$ after M-bit quantization is $V_{FS,1}/2^M$, where $V_{FS,1}$ is the full-scale reference of the 1st-stage. Considering that the stage-gain is G and 1-bit redundancy is implemented between the two stages, the full scale of the 2nd-stage ADC $V_{FS,2}$

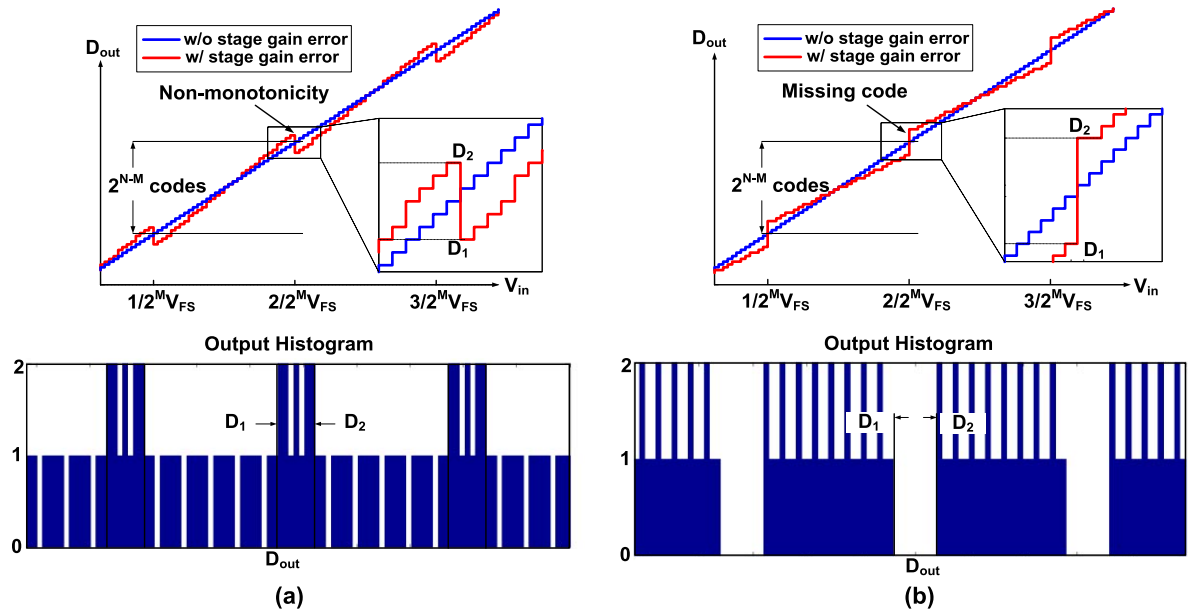


Fig. 3. The Pipelined-SAR ADC transfer curve and code histogram with (a) $GV_{LSB,1} > 1/2V_{FS,2}$ and (b) $GV_{LSB,1} < 1/2V_{FS,2}$.

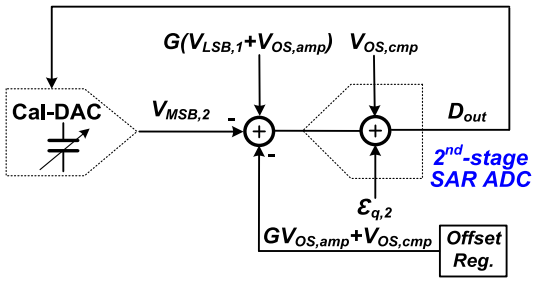


Fig. 4. Signal diagram of the BSGC technique.

should be $GV_{FS,1}/2^{M-1}$. If the reference voltages of the two stages match each other, the MSB of the 2nd-stage ADC $V_{MSB,2}$should be equal to$GV_{FS,1}/2^{M}$, i.e. $GV_{LSB,1}$, with a linear output transfer curve of the ADC, as shown in Fig. 3. However, if the mismatch exists, it causes periodical non-monotonicities or missing codes with an interval of 2^{N-M} codes at the ADC's output as shown in Fig. 3(a) and (b), respectively. The required matching accuracy between the two stages can be derived as,

$$GV_{LSB,1}|\varepsilon_{rms}| < 1/2V_{LSB,2}, \quad (1)$$

where ε_{rms} is the error percentage and $V_{LSB,2}$ is the LSB of the 2nd-stage SAR ADC. As the 2nd-stage quantizes (N-M+1)-bit, $V_{LSB,2}$ is equal to $G/2^{N-M}V_{LSB,1}$. Since the error should be suppressed to less than $1/2V_{LSB,2}$, $|\varepsilon_{rms}| < 1/2^{N-M+1}$. Therefore, the acceptable ε_{rms} in this design is $< \pm 1.5\%$. The inter-stage gain error can be estimated and corrected by the proposed BSGC technique with low digital circuit overhead.

Fig. 4 shows the signal diagram of the proposed BSGC scheme. This concept utilizes the 2nd-stage SAR ADC to quantize the inter-stage gain error and correct it accordingly via a gain-tunable calibration DAC (Cal-DAC). To detect the gain error, the offsets from the amplifier $V_{OS,amp}$ and the 2nd-stage comparator $V_{OS,cmp}$ need to be removed before the gain calibration. We employ a self-embedded offset calibration [27], which reuses the 2nd-stage ADC to measure and subtract the offsets after the sampling phase. Fig. 5 shows the detailed circuit implementation of the BSGC technique. For simplicity, only Channel 1 is shown. The testing signal $V_{LSB,1}$ generated from the 1st-stage DAC, will be amplified Gtimes before the 2nd-stage DAC. As stated above, we expect $GV_{LSB,1}$ to match with$V_{MSB,2}$(generated by the 2nd-stage as described below), the difference between these two voltages represents the inter-stage gain error, which can be quantized to 5-bit digital codes via the 2nd-stage SAR ADC. The calibration logic feeds back the corresponding control logic to the Cal-DAC as shown in Fig. 5. The gain adjustment is binary-approximated, and the minimum step size of the Cal-DAC is $\pm 1/2C$ corresponding to the required accuracy of $\pm 1.5\%$. Fig. 5 also details the control timing diagram of the BSGC scheme. Initially, half of the Cal-DAC is grounded, and the other half is floating. Once the offset calibration finishes, the gain calibration is enabled. The 1st-stage DAC is reset first, and then a testing signal $V_{LSB,1}$ is generated by switching the LSB capacitor to V_{ref}, while keeping the others to *Gnd*. Next, the $V_{LSB,1}$ is amplified by G and sampled onto the top-plate of the 2nd-stage DAC during the amplification phase (Φ_2). When Φ_C starts, the MSB capacitor of the 2nd-stage DAC is switched to *Gnd* to generate a residue of $GV_{LSB,1}$-$V_{MSB,2}$. If $GV_{LSB,1}$-$V_{MSB,2}$>0 (D_1 =1), $V_{FS,2}$ is scaled up by floating an 8C in Cal-DAC$_2$, and if $GV_{LSB,1}$-$V_{MSB,2}$<0 (D_1 =0), $V_{FS,2}$ is scaled down by connecting an 8C in Cal-DAC$_1$ to *Gnd*. The above operation repeats by several times until the inter-stage gain error is suppressed to the required accuracy. The calibration range can cover the gain variation mainly introduced by the open-loop amplifier up to $\pm 50\%$, and based on the binary search algorithm, the gain error is reduced by half in each cycle, so it takes 5 cycles until the gain error is suppressed to the

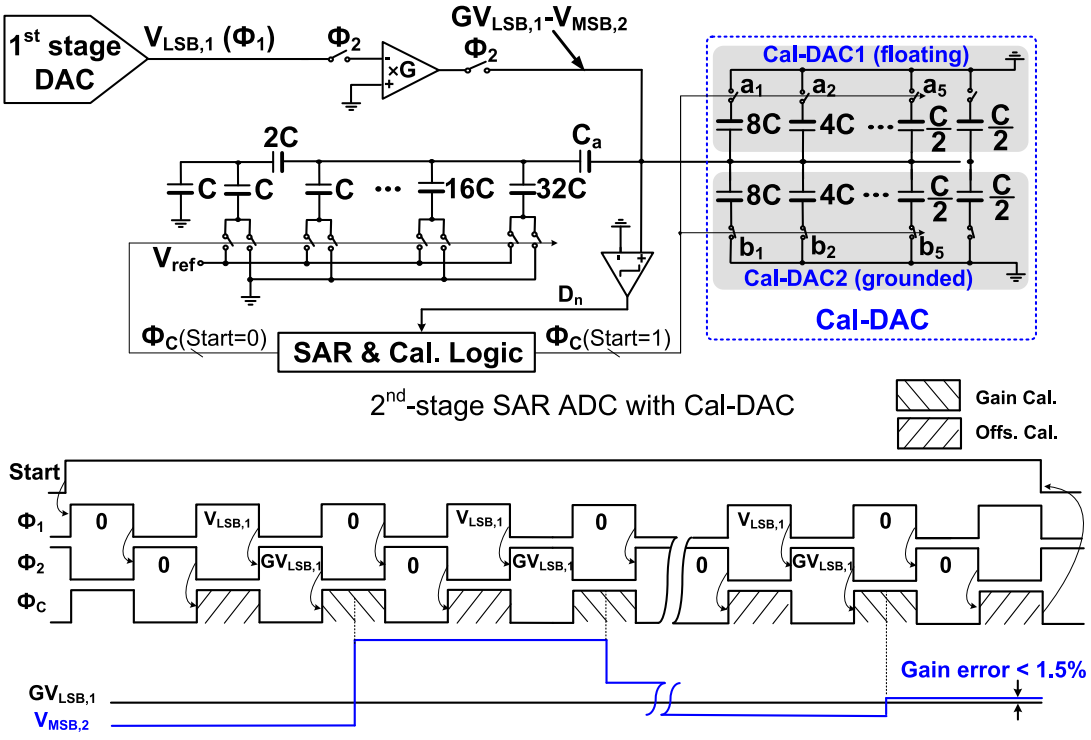


Fig. 5. Circuit implementation of the BSGC technique and its control timing diagram (Only Channel 1 shown).

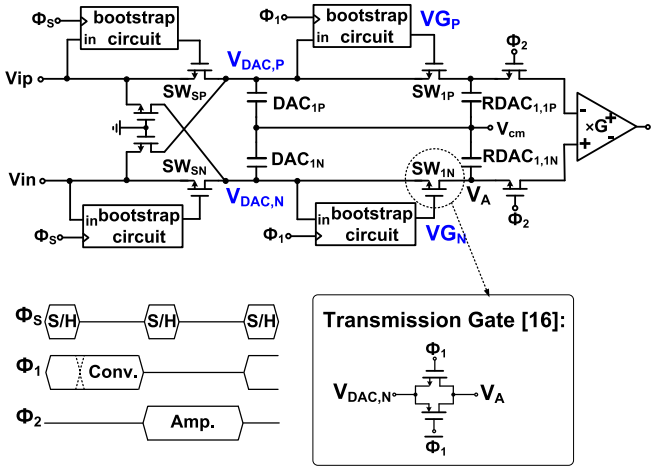


Fig. 6. Sampling front-end with the bootstrapped TI switches.

required accuracy of ±1.5%. The calibration logic integrated into the SAR controller is simple and implemented in a tiny area. Considering the gain mismatch between two channels, the BSGC technique is implemented once for each channel. With both the gain and offset calibrations working in a time-interleaved manner, a total of 23 conversion cycles (≈128 ns) is needed to complete all the calibrations in both channels.

IV. Building Blocks

A. Proposed Dual-Phase Bootstrap Circuit

Fig. 6 shows the implementation of the sampling front-end (For simplicity we describe only one of the differential pairs DAC_1 & $RDAC_{1,1}$ in Fig. 2). We use the cross-coupled technique for the sampling switches to reduce signal feed through from the input to the DAC [30]. In the sampling phase Φ_S, the series-connected switches SW_{SP} and SW_{1P}, SW_{SN} and SW_{1N} are all turned on, which track the input signals at the top plates of the DACs. According to the merged-residue-DAC operation introduced in Section II, the TI switches (SW_{1P} and SW_{1N}) are kept on until the conversion ends. In [16], the TI switch implemented with a transmission gate, had a varying on-resistance causing sampling distortion, and limiting the sampling total harmonic distortions (THD) to only -68 dB according to the simulation results. Therefore, to improve the sampling linearity, the TI-switches need to be bootstrapped during the sampling, as shown in Fig. 6. However, the input of the bootstrap circuit that connects to a high impedance node $V_{DAC,P}$/$V_{DAC,N}$ will cause a problem. It should be noted that in the conventional bootstrap circuit shown in Fig. 7, the drain of M_5 usually connects to the active input source during sampling. However, in this design, as the TI-switch SW_1 needs to be kept on until the coarse conversion finishes, it is necessary to connect to the top-plate of DAC_1 rather than to the input signal. Since the conversion duration is larger than 4 ns and the drain-source voltages of the transistors M_6, M_8, M_{11} and M_{12} are signal-dependent, as listed in Fig. 7, they inject signal-dependent leakage currents to the DAC_1's top-plate and ultimately degrade the overall conversion accuracy. As illustrated in Fig. 7(b), the V_{DAC} that is performing successive approximation, exhibits a voltage drop due to the leakage error, and the maximum residue error can go up to 0.7 mV according to the simulation, which degrades the SNDR to 67 dB. To solve the problem, the TI switch in this work is boosted with the proposed

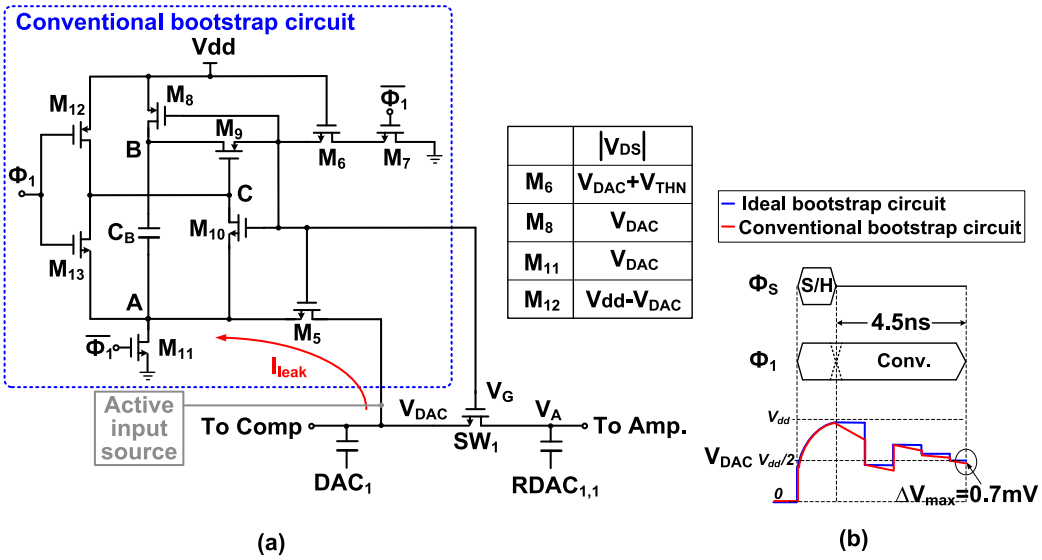


Fig. 7. Conventional bootstrap circuit and the leakage problem. (a) Conventional bootstrap circuit. (b) Voltage drop of V_{DAC} during Φ_1.

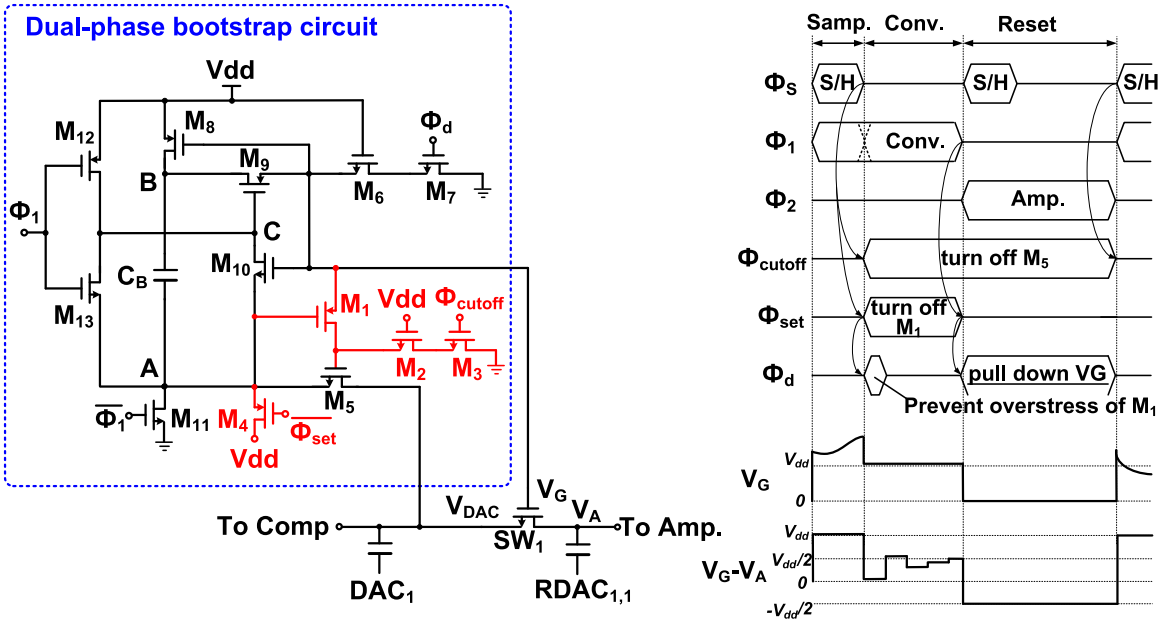


Fig. 8. Proposed dual-phase bootstrap circuit and its timing diagram.

dual-phase bootstrap circuit as shown in Fig. 8. As the TI switch needs to be on during both the sampling and conversion phases, the proposed bootstrap circuit can provide dual gate-voltage-controlling modes ($V_G = V_{in} + V_{dd}$ in the sampling phase; $V_G \approx V_{dd}$ in the conversion phase) and isolate the DAC's top-plate from the bootstrap input to prevent the signal-dependent leakage error. There are 4 transistors M_1-M_4 added to turn off M_5 for the signal isolation. The dual-phase operation of the bootstrap circuit is introduced phase by phase as follows: 1) In the sampling phase ($\Phi_S = 1$ & $\Phi_1 = 1$), the transistors M_3 and M_4 are off, while M_1 is on, which functions as a switch to pass the signal of $V_{in} + V_{dd}$ to the gate of M_5. The V_{GS} of M_1 holds a constant value of V_{dd} to reduce the signal distortion at the gate of M_5; 2) In the conversion phase ($\Phi_S = 0$ & $\Phi_1 = 1$), M_3 pulls down the gate of M_5 to *Gnd* to isolate the bootstrap circuit from the DAC's top-plate. Meanwhile, the node A charges to V_{dd} via M_4 to turn off M_1. As the node B attempts to reach up to $2V_{dd}$, M_1 will be overstressed. Therefore, M_7 is turned on for a short instant (Φ_d) to discharge V_G to a value near V_{dd}; 3) In the remaining part of the phase ($\Phi_1 = 0$), DAC_1 disconnects from $RDAC_{1,1}$ and connects to another TI-RDAC to start a new sampling and conversion. Accordingly, the SW_1 is turned off by pulling V_G down to *Gnd* via M_7.

The bootstrap circuit needs to provide a sufficient V_{GS} to maintain a low on-resistance of the TI switch during the conversion, and the value of V_G is determined by the pulse

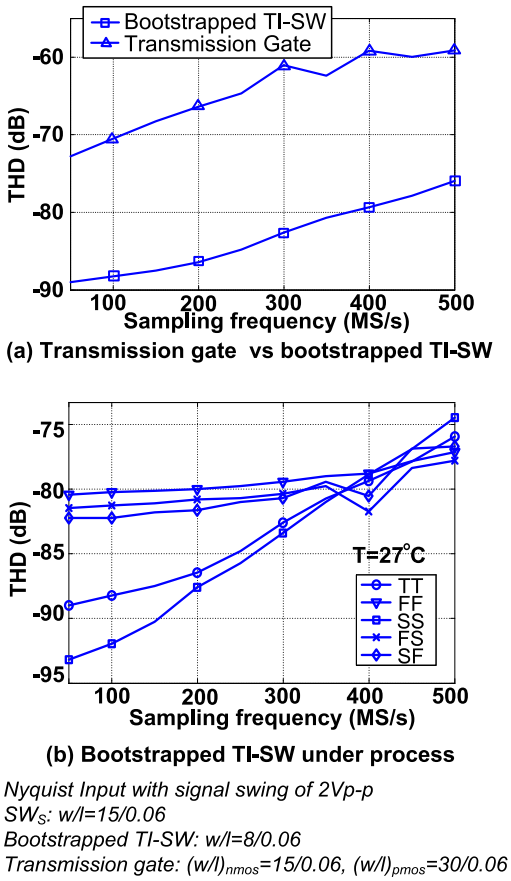


Fig. 9. Sampling distortion performance (a) with transmission gate and bootstrapped TI switch. (b) with bootstrapped TI switch under process.

width of Φ_d. A large boosting capacitor ($C_B \approx 300$fF) is used where a large RC time constant reduces the sensitivity to the variation of time for discharging the output node. Based on the process corner simulation results, the pulse width of Φ_d varies within $\pm 20\%$, leading to a V_G variation of 1.1 ± 0.1V. With the largest time constant corresponding to V_G of 1V in the worst case corner, the 1st stage's DAC output can still settle to the required accuracy of 8b for bit-by-bit SAR sub-ADC decisions and 13b for final residue before amplification.

Fig. 9(a) plots the sampling THDs versus the sampling frequency, where the TI switches use the proposed bootstrapped technique and the transmission gate, respectively. The input frequency is Nyquist, and the input swing is $2V_{p-p}$. The sampling THD in the proposed dual-phase bootstrap technique is at least 14 dB better than in the transmission gate solution. With the proposed bootstrap circuit, the sampling THD under different corners is simulated with the temperature of 27° C, and Fig. 9(b) shows that the sampling THD can achieve $>$-75dB with the sampling frequency up to 500MS/s.

B. Residue Amplifier

The residue amplifier implemented as a differential pair open-loop amplifier achieves low power and wide bandwidth, as shown in Fig. 10. To improve the common-mode rejection ratio (CMRR) and further relax the conversion

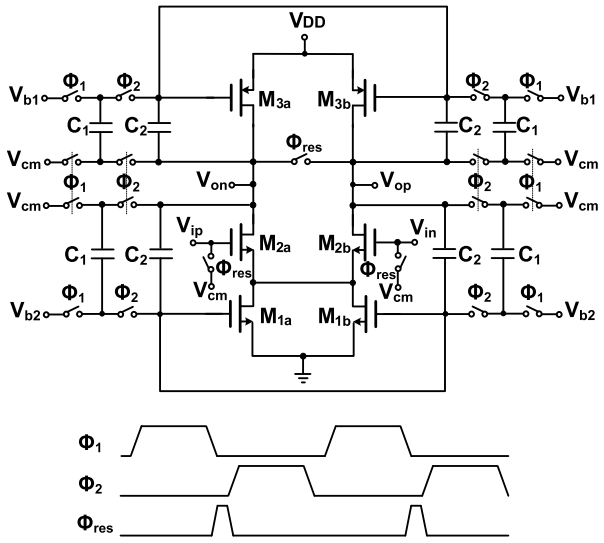


Fig. 10. Residue amplifier circuit schematic and its timing diagram.

accuracy requirement of the 2nd-stage, we designed an open-loop DC gain of 22 dB. The required gain-bandwidth product (GBW) is $>$ 1.5 GHz. Thus, a GBW of 2 GHz leads to 430 μW power dissipation. We used two pairs of dynamic switched-capacitor (SC) common-mode feedback (CMFB) circuits to define well the output common-mode level. The output common-mode (CM) is controlled within (600 ± 10) mV with one CMFB loop, and it can be further stabilized to (600 ± 5) mV with two CMFB loops. Although extra CMFB loop adds the loading of the amplifier, the added loading, i.e. C1+C2=5fF, is almost negligible when compared to the total capacitance of the 2nd-stage DAC and Cal-DAC (Maximum value is up to 200fF). Also, the SC-CMFB does not dissipate DC static power, and the amplifier occupies only a very small portion of core ADC area as shown in Fig. 13, then, the extra CM loop consumes a negligible area budget. Both input and output have reset switches to remove the memory effect. The time constant of the reset switch on-resistance and the input parasitic capacitance is 40 ps, thus the reset duration is set to be 400 ps to reset well the amplifier input parasitics. Although the gain established by $g_m R_{out}$ suffers from significant process variations, it can be corrected by the proposed gain calibration. The input of amplifier is a 7b residue in the coarse sub-ADC quantization, which has a swing of ± 7 mV. The input is multiplied by a gain of 22dB, leading to an output swing of ± 88 mV. By inputting a sinusoidal wave with an amplitude of 7mV, the worst case of THD is -42dB based on a 50-run Monte-Carlo simulation result, which still can satisfy the 6b linearity requirement for the amplifier.

C. Comparator Designs

The comparators used in the 1st-stage are differential pair dynamic comparators, with offset calibrated by adjusting the differential currents with an extra input pair [26].

For a normal SA conversion, the 2nd-stage SAR ADC quantizes 6-bit, while the SAR ADC converts 2 additional bits during the offset calibration. Since the accuracy of the offset and the gain calibrations depends on the comparison

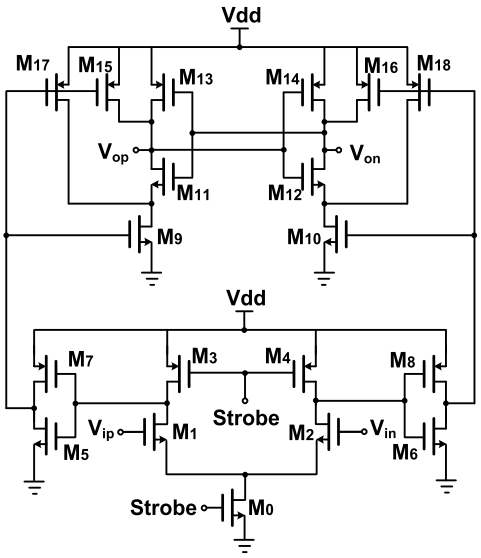


Fig. 11. Circuit implementation of the 2nd-stage comparator.

accuracy at the 2nd-stage, we use a low-noise three-stage dynamic comparator [31], with the circuit schematic shown in Fig. 11. The comparator incorporates a dynamic preamplifier, an inverter, and a regenerative latch. During the reset phase (Strobe=0), with the preamplifier switched-off, and the transistors M_5 and M_6 charged by M_3 and M_4; M_{15}-M_{18} turn on to reset the output nodes (V_{op} and V_{on}) to V_{dd}. When the regeneration phase starts (Strobe=1), the input difference is successively amplified by the preamplifier and the inverter, and then passed to the output latch stage for decision-making. With the inverter inserted between the input and output stages, the gain before the regenerative latch is improved by 12 dB, achieving an equivalent 1σ input-referred noise of 880 μV, which is sufficient for the offset calibration scheme.

D. Layout Considerations

In the Pipelined-SAR ADC fabricated in 65-nm 1P7M CMOS, with the conversion accuracy in the 1st-stage relaxed to 8b, the matching of the DAC needs to be accurate to ensure the overall ADC precision. In this design, we adopt a unit capacitor of 5.5 fF in both stages, which uses a custom-designed fringe structure (2 μm×2.4 μm) with the metal layer 1-5. Fig. 12 shows the layout of the 1st-stage DAC. Since the two channels share the $DAC_1$and DAC_2, we placed them separately on the right-hand side. The ping-pong RDACs ($RDAC_{1,1}$ & $RDAC_{2,1}$ / $RDAC_{1,2}$& $RDAC_{2,2}$) are laid together to perform the merging operation. To reduce the bandwidth mismatch between two channels we centered the dual-phase bootstrap circuits and the input path in the middle. The master sampling clock (Φ_S) has less coupling with the input signal path and is routed symmetrically to the main bootstrapped circuit for the shared DAC_1 and DAC_2. Benefitting from the partial interleaving operation [16] the design is not sensitive to the timing mismatches. Therefore, the routings of the bootstrap circuit clock paths (described in Fig. 8) to the two TI channels are not symmetrical.

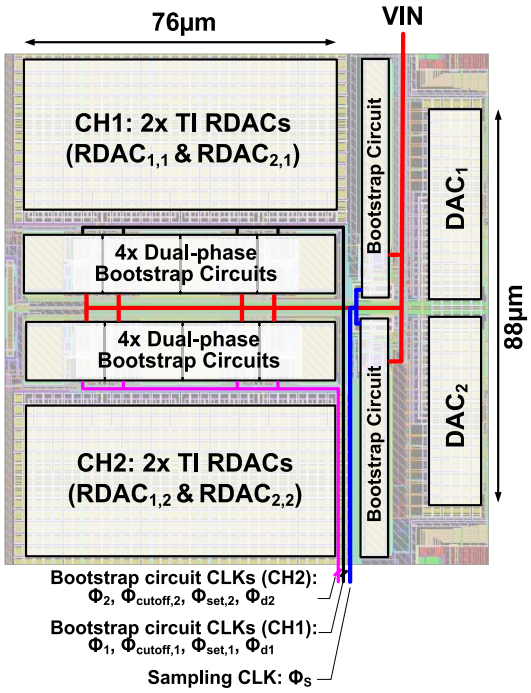


Fig. 12. Layout of the 1st-stage DAC.

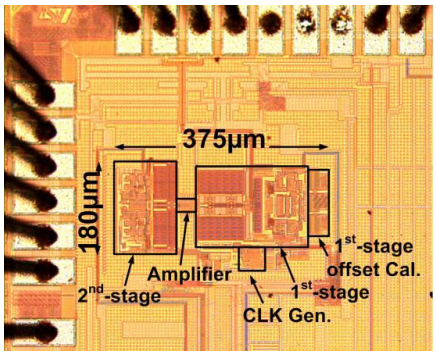


Fig. 13. Die photo.

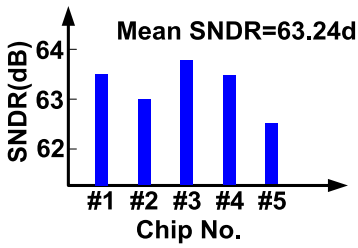
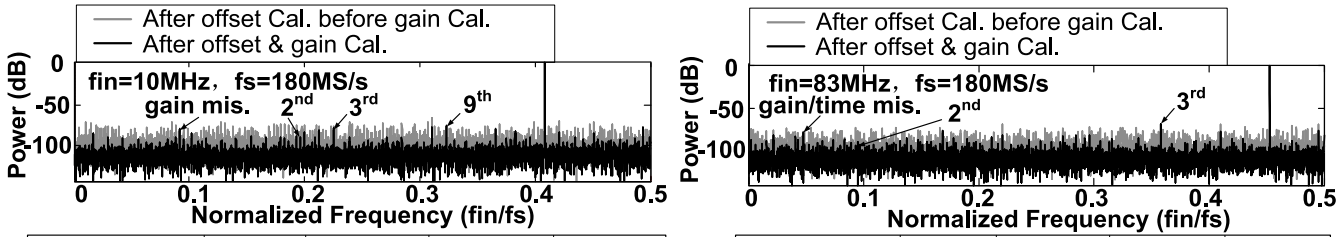


Fig. 14. Measured SNDR of 5 chips @ fin=10MHz, fs=180MS/s.

V. Experimental Results

Fig. 13 shows the die photo of the ADC, where the core occupies 0.068 mm^2 including all the calibration circuits. This design didn't implement the input and reference buffers.

The supply voltage is 1.2 V for both analog and digital, with the reference voltages of 1.1 V and 0 V generated externally. Fig. 14 shows the measured SNDR of 5 chips @



	SNR (dB)	SFDR (dB)	SNDR (dB)	THD (dB)
Before gain Cal.	51.53	65.27	51.27	-63.42
After gain Cal.	64.5	76.3	63.8	-72.3

	SNR (dB)	SFDR (dB)	SNDR (dB)	THD (dB)
Before gain Cal.	51.74	66.11	51.5	-65
After gain Cal.	62.6	67.17	60.92	-65.72

Fig. 15. Measured FFT of the digital output decimated by 25.

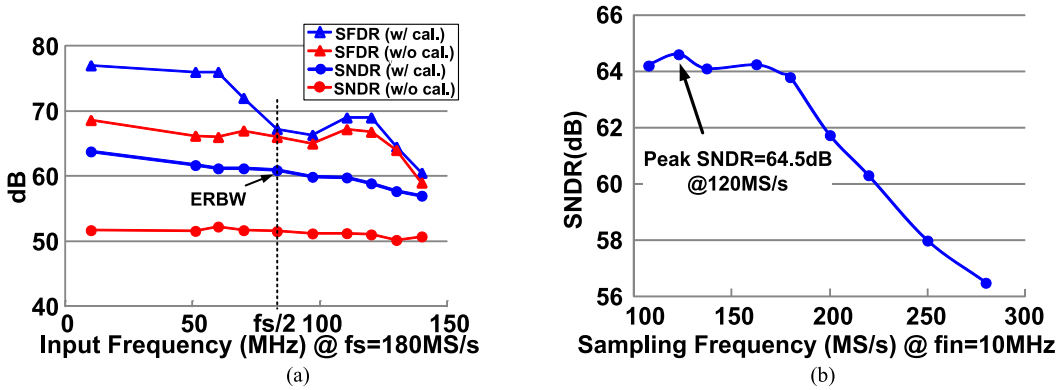


Fig. 16. Measured dynamic performances. (a) SNDR/SFDR vs. input. (b) SNDR vs. clock frequency.

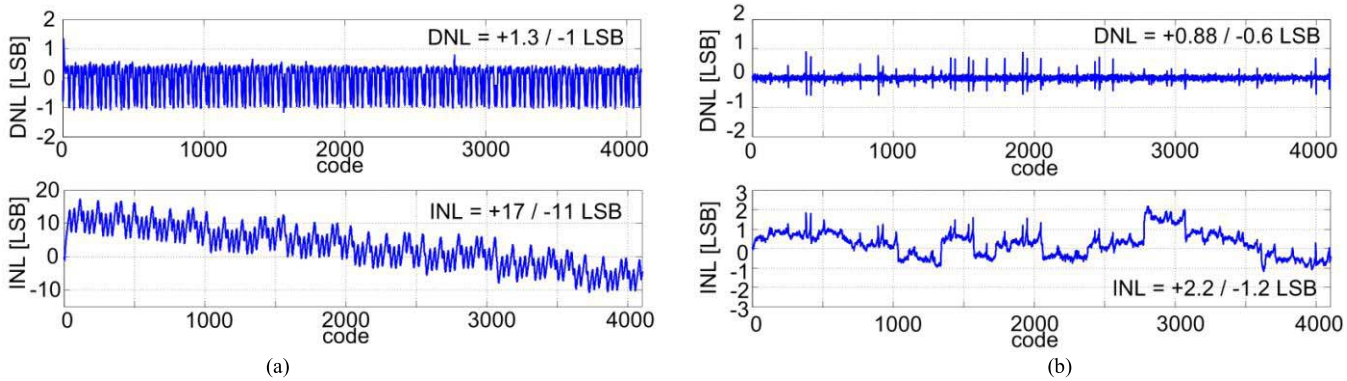


Fig. 17. Measured DNL and INL (a) before, and (b) after stage-gain calibration.

DC input, with an average SNDR of 63.24 dB. To demonstrate the effectiveness of the gain calibration, Fig. 15 shows the measured FFTs before and after gain calibration @ DC and near Nyquist input frequencies, respectively. With a DC input the inter-stage gain error due to the utilization of the open-loop amplifier causes a bunch of spurs spreading among the whole spectrum. Such spurs limit the SNDR and SFDR to 51.3 dB and 65.2 dB, respectively. After calibration, with the spurs suppressed, there is an improvement of the SNDR and SFDR to 63.8 dB and 76.3 dB, respectively. The SNDR drops by nearly 3 dB with a Nyquist input, mainly limited by the clock jitter. The spur due to gain mismatch decreases to -78.5 dB @ DC input, which demonstrates the effectiveness of the BSGC calibration. By adopting the merged-residue-DAC operation, the achieved SNR @DC input is 64.5 dB, which is 8 dB better than that reported in [16] with total input capacitance maintaining the same. The design also shows immunity to the timing mismatch, where the spur maintains -77 dB @ Nyquist input. Figs. 16 and 17 plot the measured dynamic performances. The SNDR is > 60 dB as the input frequency goes up to 100 MHz. The 3rd harmonic dominates the SFDR @ Nyquist input. The ADC achieves a peak SNDR of 64.5 dB @ 10MHz input and fs=120 MS/s. Fig. 17 depicts the measured static performances with and without the gain calibration. Based on the measurement, the DNL before calibration has a systematic comb-like pattern due to a large

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	[4] VLSI'14	[5] VLSI'14	[6] VLSI'14	[7] VLSI'13	This Work
Architecture	Pipelined-SAR	Pipelined-SAR	Pipelined-SAR	Pipeline	Pipelined-SAR
Technology (nm)	28	40	65	65	65
Resolution (bit)	14	12	12	12	12
Sampling Rate (MS/s)	200	160	210	200	180
Supply Voltage (V)	0.9	1.1	1	1.2	1.2
Power (mW)	2.3	4.96	5.3	11.5	6 (Cal. power included)
SNDR@Nyq (dB)	65	65.3	60.1	57.6	60.92
SNDR@DC (dB)	70	66.5	63.48	65	63.8
FoMw@Nyq (fJ/conv.-step)	7.9	20.7	30.3	92.8	36.7
FoMw@DC (fJ/conv.-step)	4.4	17.7	20.7	39.6	26.3
Area (mm^2)	0.1	0.042	0.48	0.26	0.068 (Cal. logic included)
Onchip Cal.	No	No	No	No	Yes
Cal. Time	15us (3k cycles/per channel)	0.11s (17M cycles)	–	–	128ns (23 cycles)

number of missing codes, which are periodic and have an interval near 2^5 codes. Also, the INL exhibits a slope-down pattern indicating that the intrinsic conversion nonlinearity relevant to stage gain error depends on the use of the open-loop amplifier. When the calibration is active, all the missing codes in DNL disappear, and the INL improves to less than 2.2 LSB.

The total power consumption of the ADC including the calibration circuit is 6 mW, where the analog and digital powers are 2.8 mW and 3.2 mW, respectively. The FoM @DC and @Nyq at 180 MS/s are 26.3 fJ/conv.-step and 36.7 fJ/conv.-step, respectively. Table I summarizes the performance of this work. Comparing it with the state-of-the-art high-speed pipeline and Pipelined-SAR ADCs, this design achieves a competitive conversion accuracy and FoM with all the calibrations on-chip. The achieved die area including the calibration is still better than [4], [6], [7]. The other works all need post signal processing to fix the gain and offset errors, which requires extra power and area.

VI. CONCLUSIONS

This paper presented a full-calibration-integrated 12-bit 180 MS/s Pipelined-SAR ADC fabricated in a 65 nm CMOS technology. The merged-residue-DAC operation enables a PI scheme without the degradation of sampling noise performance. The dual-phase bootstrap technique improves the sampling and conversion linearity in partial interleaving operation. Moreover, the correction of the gain error induced by the open-loop amplifier with binary-search gain calibration, leads to a short calibration time, wide error coverage range and high accuracy with a small area. This work implements all the calibrations on-chip and achieves a SNDR of 60.9 dB @Nyquist input with 6 mW of power dissipation and a compact area of 0.068 mm^2.

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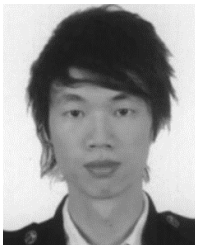

Chi-Hang Chan (S'12–M'15) was born in Macao, China, in 1985. He received the B.S. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2008, and the M.S. and Ph.D. degrees from the University of Macau, Macao, China, in 2012 and 2015, respectively. He was an Intern with Chipidea Microelectronics (currently Synopsys, Macao, during his bachelor's studies. He currently serves as a Research Assistant Professor with the University of Macau. His current research interests include Nyquist ADC, mixed signal circuits, comparator offset calibration, and Flash and Multi-bit SAR ADC. He received the Chipidea Microelectronics Prize and the Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level), in 2012 and 2011, respectively. He also received the Macau FDCT Award for Technological Invention (2nd class) and the Macao Scientific and Technological Research and Development for Postgraduates Award (Ph.D. Level) in 2014 for outstanding Academic and Research achievements in Microelectronics. He was a recipient of the 2015 Solid-State-Circuit-Society (SSCS) Pre-doctoral Achievement Award. He was also a co-recipient of the 2011 ISSCC Silk Road Award and the Student Design Contest Award in A-SSCC 2011.

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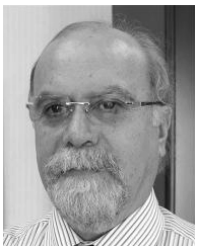

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He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and the IEEE Macau Joint-Chapter on CAS/COM from 2005 to 2008 [2009 World Chapter of the Year of IEEE CASS]. He was the Vice President for the Region 10 of the IEEE CASS from 2009 to 2011, and the Vice President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (T-CAS II): EXPRESS BRIEFS from 2010 to 2013, nominated Best Associate Editor of T-CAS II, from 2012 to 2013. He was also a member of the IEEE CASS Fellow Evaluation Committee from 2013 to 2014, and CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS) - Director of the IEEE. He was the General Chair at the IEEE Asia-Pacific Conference on Circuits and Systems - APCCAS 2008 and the ACM/IEEE Asia South Pacific Design Automation Conference - ASP-DAC'2016. He is currently a Nominations Committee Member of IEEE CASS. He received two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.