Digital 2-/3-Phase Switched-Capacitor Converter With Ripple Reduction and Efficiency Improvement

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***Abstract*— This paper presents a digitally controlled 2-/3-phase 6-ratio switched-capacitor (SC) dc-dc converter with low output voltage ripple and high efficiency. To achieve wide input and output voltage ranges, six voltage conversion ratios are generated with only two discrete flying capacitors by using both 2- and 3-phase operations. An adaptive ripple reduction scheme is proposed to achieve up to four times reduction in the output voltage ripple. The complexity of controller design is reduced by using digital synthesis, and the technique is scalable with process. Fast loop response is achieved by using synchronized hysteretic control. The SC converter was fabricated in a 0.13-μm CMOS process. It can deliver a maximum power of 250 mW to an output of 0.5–3 V with a wide input voltage range of 1.6–3.3 V. Compared to an SC converter with only 2-phase operation, the maximum efficiency improvement is 20%. The converter achieves a peak efficiency of 91%.**

***Index Terms*— Adaptive ripple reduction, dc-dc converter, digitally controlled, efficiency improvements, 2-/3-phase, 3-phase, SC converter, switched-capacitor (SC), voltage conversion ratio, voltage regulator.**

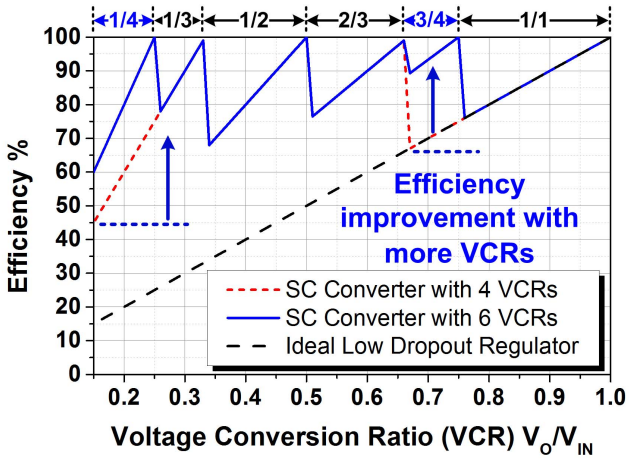

Fig. 1. Theoretical efficiency comparison of SC converter with four and six VCRs versus ideal low dropout regulator.

I. Introduction

THE rising market of Internet-of-Everything (IoE) and wearable devices has great demands for power management ICs. Some of the applications are powered by harvested energy such as photovoltaic, piezoelectric, thermoelectric, and RF sources [1]. A high-efficiency power converter is usually needed to regulate the harvester's source voltage. For low-power applications ranging from 10 to 250 mW, very small capacitors and integrated capacitor array of multilayer ceramic capacitors with very small footprint can be used, and in handling the same power, the cost of ceramic capacitors is lower than that of a power inductor. Hence, switched-capacitor (SC) power converters are preferred over inductor-based switching converters as they do not need bulky and costly power inductors.

Fully-integrated SC converters with on-chip capacitors are becoming popular in recent years [2]–[7]. However, SC converters using on-chip capacitors have two limitations. First, standard bulk CMOS processes have low capacitance density and hence low energy density, limiting the power density of SC converters [3], [4]. Special technologies and processing steps have been developed to increase the capacitance density by using exotic capacitor technologies such as deep-trench capacitors [5] and ferro-electric capacitors [6] at an increased processing cost. Second, the core transistors of an advanced process such as sub-65-nm CMOS cannot handle high input voltage directly, and stacking techniques with auxiliary rails [3], [7], I/O devices [8], or some designated voltage conversion ratios (VCRs) [4], [7], [9] may have to be used. For an energy harvesting system, the source voltage could vary drastically according to environmental conditions [10], and a power converter with a wide source voltage range is needed. To address the above concerns, we proposed a SC converter that uses an off-chip integrated capacitor array that only requires small area and cost overhead to handle wide voltage range, deliver moderately high power, and reduce the system cost [11].

The design of SC converters with off-chip capacitors faces two major challenges. First, the power conversion efficiency (PCE) is related to the number of VCRs. Fig. 1 shows the theoretical efficiency of an SC converter with 4 or 6 VCRs versus that of an ideal low dropout regulator. With two extra VCRs (3/4× and 1/4×), the efficiency at certain V_{IN} can be improved by around 20%. Thus, to obtain a high overall efficiency, many VCRs are needed [12], [13]. A gear-box technique was proposed in [12], and 3 on-chip capacitors were used to realize 4/5× and 2/3×. The area overhead was

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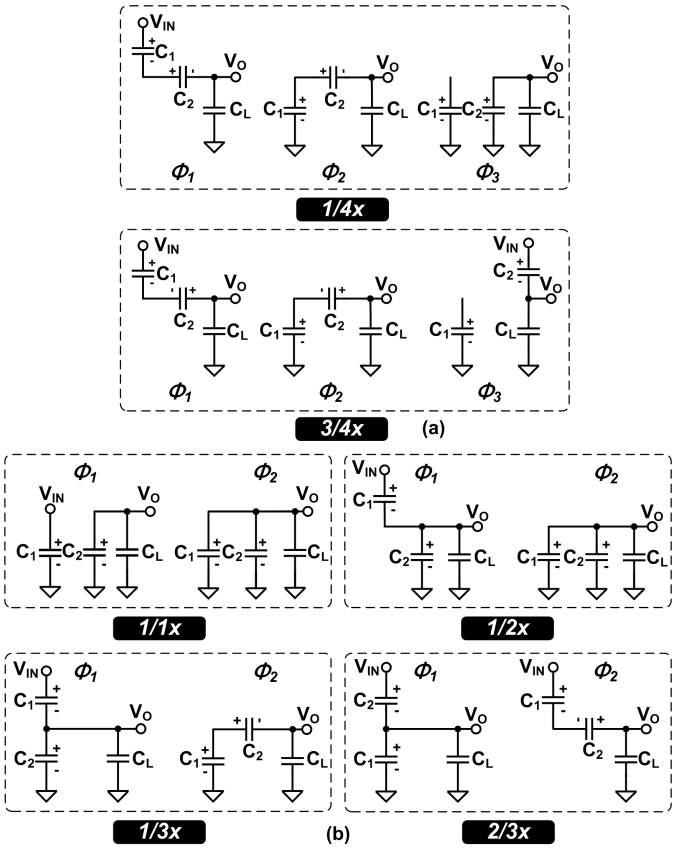

Fig. 2. Operating principle of 6-ratio configurations. (a) Topologies operating in 3-phase mode. (b) Topologies operating in 2-phase mode.

reduced by using the same connection for the capacitors and the switches in phase 1. In [13], a gear-train topology was investigated and 5 off-chip capacitors were used to construct 4 stacked power stages that realize 24 VCRs. However, the increased output impedance due to stacking too many transistors in series limits the load current capability. Moreover, 2-phase operation restricts the number of VCRs that could be realized. Now, one off-chip flying capacitor needs two IC pins, and more VCRs need more flying capacitors that increase both the volume and cost. Hence, commercial products usually use two flying capacitors to minimize the pin count and only have 2–3 VCRs such as 2/3×, 1/2×, and 1/3× [14]–[16]. Consequently, the challenge is to realize more VCRs with fewer flying capacitors.

Second, large voltage ripples on the power rails in general degrade the performance of noise-sensitive loads. Although this side effect could be canceled in particular when the loading is a digital circuit and its behavior could be programmed to adapt to the ripple voltage [17]; however, it may not be feasible for applications other than digital. To reduce the voltage ripple, multiphase interleaving techniques have been investigated [18]–[20] and commonly used in both step-up and step-down SC converters [21]–[23]. However, high-power applications use discrete capacitors, and they cannot be split into smaller capacitors to realize multiphase interleaving. Modulating the capacitance [24] could reduce the voltage ripple by suppressing extra charge being delivered to the outputs, but again

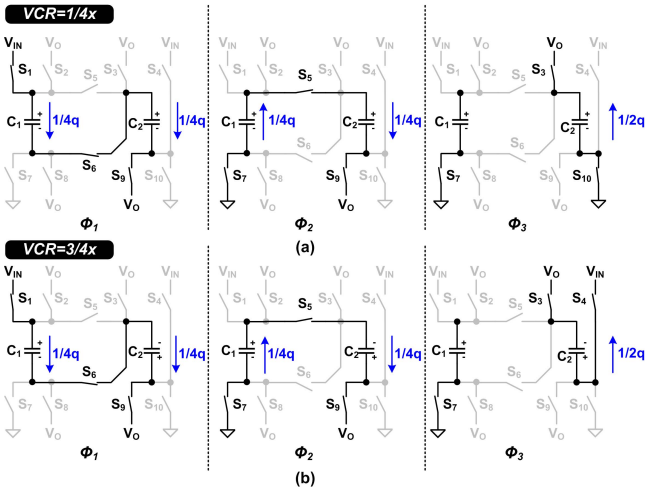

Fig. 3. Detailed operation principles of the 3-phase. (a) 1/4× mode. (b) 3/4× mode.

this method is not feasible for discrete capacitors. Analog approaches that tune the on-resistance of switches [25], [26] are not preferred for a digitally controlled SC converter. Cascading a post regulator [27], on the other hand, would degrade the overall efficiency.

To tackle the above two issues, this paper proposes a digital 2-/3-phase SC converter with improved efficiency and reduced voltage ripple over wide input and output voltage ranges. This paper is organized as follows. Section II discusses the principle of 2-/3-phase operation and analyses the performance. Section III introduces the scheme of digital ripple voltage reduction. Section IV presents the design of the proposed SC converter, including its architecture, design considerations, and circuit implementation. Measurement results are shown in Section V, followed by concluding remarks.

II. 2-/3-Phase Topological Analysis

A. Theoretical Limit of 2-Phase Operation

Most SC converters use a 2-phase clock, and the number of VCRs is limited by the number of flying capacitors [28], [29]. For example, with two flying capacitors, the realizable step-down VCRs are only 1×, 2/3×, 1/2×, and 1/3× only. More VCRs need more flying capacitors, at the cost of two pins per capacitor plus more complicated power-switch configurations, and thus a higher system cost.

An alternative method to realize more VCRs using the same number of flying capacitors is to use multiphase operation, which has been employed in realizing step-up VCRs [30], [31] to extend the output voltage with a very high VCR. It was applied to step-down SC converter in [32] to generate a very low voltage to power up energy-efficient digital circuits in the subthreshold region. To add no additional flying capacitors, 3-phase operation is especially suitable for SC converters whose volumes are limited by packaging and external components. In this paper, we discover more 3-phase topologies and combine them with those in [32] to fully utilize the flying capacitors, and achieve a higher average efficiency over the input and output voltage ranges.

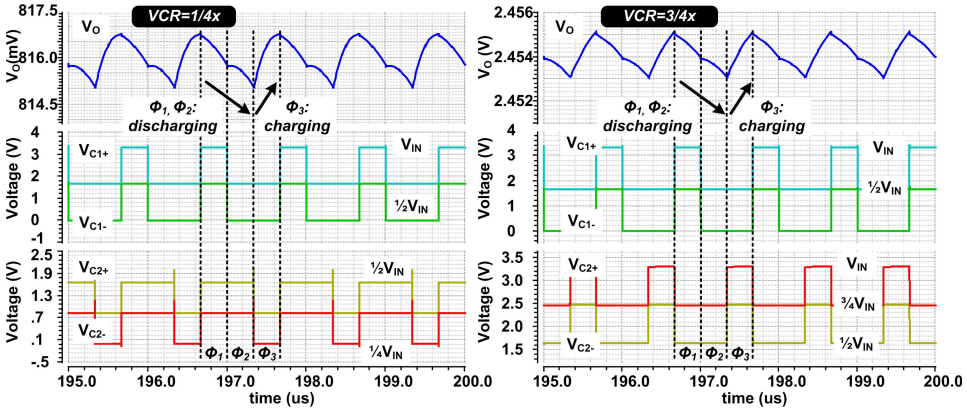

Fig. 4. Simulated steady state waveforms of output voltage V_O and top and bottom plates of flying capacitors (C_1 and C_2) with $I_O = 10$ mA.

B. 3-Phase Operation Using Two Flying Capacitors

We propose to use two flying capacitors C_1 and C_2 to generate six VCRs. Fig. 2 shows the phase-by-phase connections of C_1 and C_2 and the load capacitor C_L (at V_O) by the switches. Fig. 2(a) shows how 1/4× and 3/4× are realized using 3-phase operation, and Fig. 2(b) shows how 1/1×, 2/3×, 1/2×, and 1/3× are realized using 2-phase operation. By monitoring V_O/V_{IN} the appropriate VCR in maximizing the theoretical PCE will be used. As 2-phase operations are well known, we mainly focus on 3-phase operations. The ideal V_O/V_{IN} at zero load current is considered. Fig. 3(a) shows the case of realizing VCR = 1/4×. In Φ_1, C_1 and C_2 are connected in series between V_{IN} and V_O, and

$$\Phi_1 : V_{IN} = V_{C2} + V_{C1} + V_O. \tag{1}$$

In Φ_2, C_1 is connected to ground, and the positive nodes of C_1 and C_2 are connected together with C_2 stacking on top of V_O, yielding

$$\Phi_2 : V_{C1} - V_{C2} = V_O. \tag{2}$$

In Φ_3, C_1 is left floating and C_2 is discharged in parallel with C_L, and obviously

$$\Phi_3 : V_{C2} = V_O. \tag{3}$$

By solving (1) to (3), we obtain that $V_O = 1/4V_{IN}$.

For the 3/4× mode, Φ_1 and Φ_2 operations are identical to those of the 1/4× mode. In Φ_3, C_1 is left floating, and the positive node of C_2 connects to V_{IN} and the negative node to V_O. Hence, we have

$$\Phi_1 : V_{IN} = V_{C1} - V_{C2} + V_O \tag{4}$$

$$\Phi_2 : V_{C2} + V_{C1} = V_O \tag{5}$$

$$\Phi_3 : V_{IN} - V_{C2} = V_O. \tag{6}$$

Solving (4) to (6) gives $V_O = 3/4V_{IN}$. Note that in Φ_3, C_1 is floating and does not engage in charge transfer. As large values can be used for the off-chip capacitors, the output impedance is low even for the floating phase of C_1, which will be derived in the following sections.

Charge transfer can be traced by using the charge balance law [33]. Let the total charge delivered to C_L (V_O) in one cycle be q. In Φ_1, C_1 and C_2 are charged up by V_{IN}, and $1/4q$ is delivered to V_O. In Φ_2, C_1 discharges the charge of $1/4q$ to C_2, which is then delivered to V_O. In Φ_3, C_1 is floating with no charge transfer, but for C_2, the accumulated $1/2q$ is discharged to V_O. The ratios of the charge transferred in each element (capacitor or switch) to the total charge delivered to the output could be used to obtain the topological factors in Section IIC. Fig. 4 shows the simulated steady state waveforms

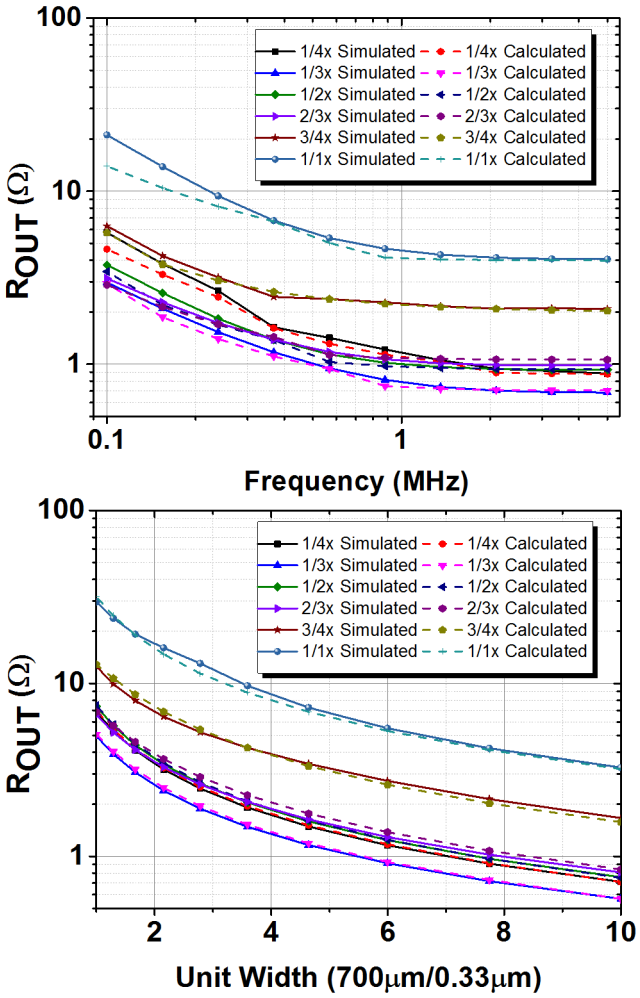

Fig. 5. Simulated and calculated output resistance versus frequency and unit width of transistor under six VCRs.

TABLE I
SUMMARY OF EQUIVALENT OUTPUT IMPEDANCE OF SIX VCRS

VCRs	K_C	R_{SSL}	K_S	R_{FSL}
1/1x	1	$\frac{1}{C_{fly} f_{sw}}$	8	$8R_{ON}$
3/4x	$\frac{1}{4}$	$\frac{1}{4C_{fly} f_{sw}}$	$\frac{7}{4}$	$\frac{7}{4}R_{ON}$
2/3x	$\frac{2}{9}$	$\frac{2}{9C_{fly} f_{sw}}$	$\frac{14}{9}$	$\frac{14}{9}R_{ON}$
1/2x	$\frac{1}{4}$	$\frac{1}{4C_{fly} f_{sw}}$	2	$2R_{ON}$
1/3x	$\frac{2}{9}$	$\frac{2}{9C_{fly} f_{sw}}$	$\frac{14}{9}$	$\frac{14}{9}R_{ON}$
1/4x	$\frac{1}{4}$	$\frac{1}{4C_{fly} f_{sw}}$	$\frac{7}{4}$	$\frac{7}{4}R_{ON}$

of the output voltage and the top- and bottom-plate voltages of C_1 and C_2 when $V_{IN} = 3.3$ V and $I_O = 10$ mA. The voltage swings show that the dc voltages across C_1 and C_2 after balancing are 1/2 V_{IN} and 1/4 V_{IN}, respectively. As a summary, benefited by 3-phase operations, 6 VCRs are generated by using only two flying capacitors.

C. Output Impedance Analysis

In order to explore the power losses of all VCRs, in this section, we investigate the charge redistribution loss, the conduction loss, and the equivalent output resistance of the 2-/3-phase SC converter. In [34], the SC converter could be modeled as an ideal dc voltage source with a finite output resistance, and a more complete model with multiple operating phases could be found in [35]. The equivalent output resistance R_{OUT} can be calculated by combining the slow-switching-limit (SSL) resistance R_{SSL} due to charge redistribution and the fast-switching-limit (FSL) resistance R_{FSL} due to the switch resistance, given by

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{7}$$

$$R_{SSL} = K_C \frac{1}{C_{fly} f_{SW}} \tag{8}$$

$$R_{FSL} = K_S R_{ON} \tag{9}$$

where K_C and K_S are topological factors determined by summing the charge vectors, C_{fly} is the value of the flying capacitor, f_{SW} is the switching frequency, and R_{ON} is the turn-on resistance of switches.

The topological factors K_C and K_S can be calculated as [28]

$$K_C = \sum_{i \in \text{caps}} \sum_{j=1}^{n} \frac{[a_{c,i}(\Phi_j)]^2}{2} \tag{10}$$

$$K_S = \sum_{i \in \text{switches}} \sum_{j=1}^{n} \frac{[a_{r,i}(\Phi_j)]^2}{D_j} \tag{11}$$

where $a_{c,i}(\Phi_j)$ is the capacitor charge vector of capacitor C_i in phase Φ_j, and $a_{r,i}(\Phi_j)$ is the switch charge vector of switch R_i in phase Φ_j.

Let the duration of each phase be equal, then (11) can be reduced to (12a) for 2-phase VCRs and (12b) for 3-phase VCRs, respectively

$$K_{S,\text{2-phase}} = 2 \sum_{i \in \text{switches}} [a_{r,i}(\Phi_j)]^2 \tag{12a}$$

$$K_{S,\text{3-phase}} = 3 \sum_{i \in \text{switches}} [a_{r,i}(\Phi_j)]^2. \tag{12b}$$

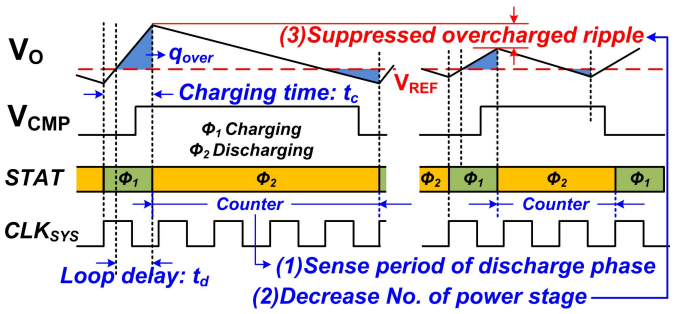

Fig. 6. Concept of proposed ripple reduction scheme.

Now, charge vectors can be determined by inspecting the charge flow in all the phases. For the 1/4× mode, the charge vectors of capacitors $a_{c,i}(\Phi_j)$ can be written below, and different from 2-phase operation, the calculation involves three vectors

$$a_c(\Phi_1) = \left[\frac{1}{4} \quad \frac{1}{4}\right] \tag{13a}$$

$$a_c(\Phi_2) = \left[-\frac{1}{4} \quad \frac{1}{4}\right] \tag{13b}$$

$$a_c(\Phi_3) = \left[0 \quad \frac{1}{2}\right]. \tag{13c}$$

Referring to Fig. 3(a), the switch charge vector $a_{r,i}(\Phi_j)$ of transistors (S_1–S_{10}) can be obtained as

$$a_r(\Phi_1) = \left[\frac{1}{4} \quad 0 \quad 0 \quad 0 \quad 0 \quad \frac{1}{4} \quad 0 \quad 0 \quad \frac{1}{4} \quad 0\right] \tag{14a}$$

$$a_r(\Phi_2) = \left[0 \quad 0 \quad 0 \quad 0 \quad \frac{1}{4} \quad 0 \quad \frac{1}{4} \quad 0 \quad \frac{1}{4} \quad 0\right] \tag{14b}$$

$$a_r(\Phi_3) = \left[0 \quad 0 \quad \frac{1}{2} \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad \frac{1}{2}\right]. \tag{14c}$$

By substituting (13a) to (13c) and (14a) to (14c) into (10) and (12b), the topological factors can be calculated. After applying this method to all six VCRs, the impedance vectors can also be calculated. Table I summarizes the parameters of the six conversion ratios. An interesting observation is that R_{SSL} and R_{FSL} of the 1/4× mode are the same as those of the 3/4× mode, because the charge vectors of the two flying capacitors have the same values. After getting R_{SSL} and R_{FSL}, R_{OUT} could be obtained by (7), and the power losses including charge redistribution loss and conduction loss can be calculated from

$$P_{LOSS} = R_{OUT} I_O^2. \tag{15}$$

Fig. 5 shows the calculated and simulated output impedances with respect to frequency and unit-size transistor (=700 μm/0.33 μm), respectively. The simulated results fit the calculated results very well in general. The mismatch

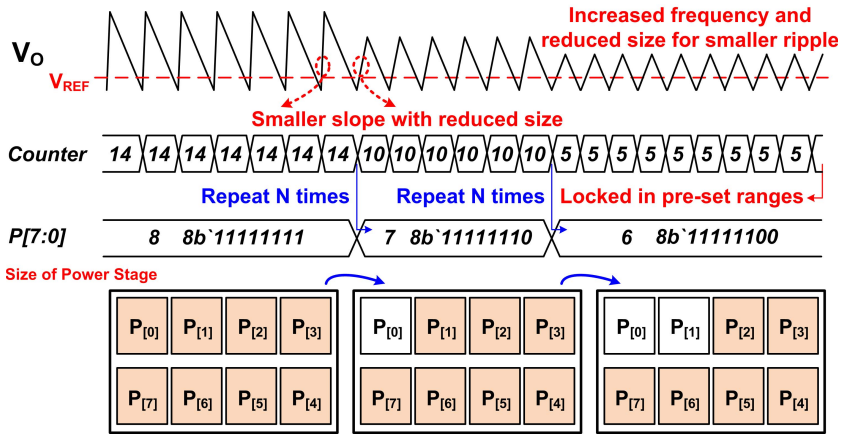

Fig. 7. Timing diagram of operation procedure.

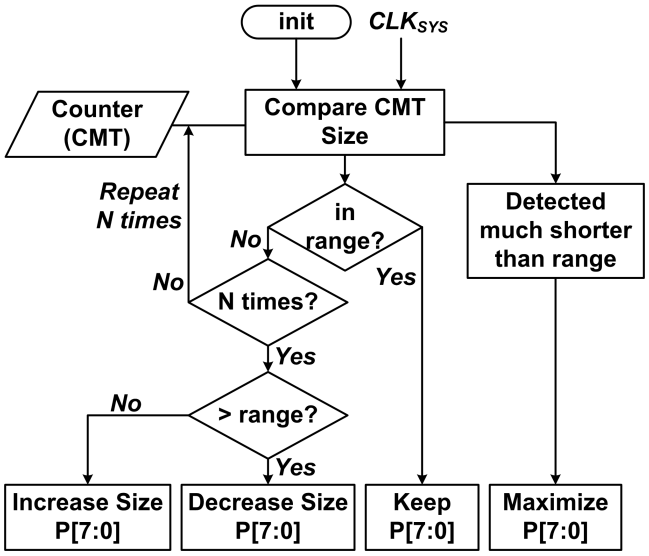

Fig. 8. Digital logic flow of adaptive ripple reduction.

between the calculated and simulated $R_{\rm OUT}$ is due to the non-idealities in practical implementation. For example, the model is inaccurate when the output has ripples [36]. Besides, ideal duty cycles of 50% and 33.3% are used in the calculation, but these values are smaller in simulations due to the switching dead-times.

From Table I and Fig. 5, we learn that $R_{\rm OUT}$ of 3-phase modes are of the same range as those of the 2-phase modes, hence, both the current driving capability and PCE are not affected. $R_{\rm OUT}$ of the 1/1× mode and 3/4× mode are larger because equal sizing was adopted for an easy layout, and thus the PMOS switches have larger turn-on resistance than the NMOS switches.

III. Digital Adaptive Ripple Reduction

An SC converter may suffer from large voltage ripples, if the charge delivered to the outputs is not well controlled. To reduce the voltage ripple of an SC converter, multiphase interleaving that results in ripple cancellation was investigated in [18]–[20] and has been commonly used [21]–[23]. Modulating the capacitance [24] reduces the voltage ripple by suppressing extra charge being delivered to the outputs. Both techniques rely on using on-chip capacitors that could be split into smaller capacitors. For large power applications that use discrete capacitors, tuning the on-resistance is easier to be realized. In [25], a three-stage amplifier is used to drive the power transistors, and the on-resistance is adjusted through changing the gate voltages. In [26], both gate-voltage and transistor-size modulations were used. For a digital SC converter, tuning the gate voltage of transistors needs analog circuits and is not preferred. Hence, in our design, transistor-size modulation was used. The concept of the proposed light-load ripple reduction scheme is shown in Fig. 6. Basically, the charging and discharging phases of an SC converter are controlled by a hysteretic comparator. Ideally, when V_O is larger than the reference voltage $V_{\rm REF}$, the comparator output should become high, and the SC converter should instantaneously change to the discharging phase. However, there is loop delay (t_d) due to the comparator and the power stage, delaying the phase transition. In such case, an excess charge of $q_{\rm over}$ will be overcharging the output capacitor, and results in a higher output voltage ripple that is derived as

$$\Delta V_O \propto \frac{q_{\rm over}}{C_L} \propto \left(\frac{V_{\rm ON}}{R_{\rm ON}} - I_O\right)\frac{t_d}{C_L} \tag{16}$$

where $V_{\rm ON}$ is the averaged voltage across the turn-on resistors connecting the flying capacitors to C_L, and is different for different VCRs. $R_{\rm ON}$ and C_L are the turn-on resistance and loading capacitor, respectively. In the hysteretic control, $((V_{\rm ON}/R_{\rm ON}) - I_O)$ is the charging slope and is always larger than zero. The charging slope is larger when I_O is smaller, and the converter has larger ripple at light load. Based on (16), reducing the delay (t_d) or increasing $R_{\rm ON}$ and C_L can help reducing the voltage ripple.

Loop delay is inherent to the system and shortening it requires power. Moreover, it varies with process, voltage, and temperature (PVT) conditions. Controlling the delay precisely by a digital compensation loop is complicated. Therefore, for a digital SC converter using discrete capacitors, tuning the size of power switches is a more feasible way to reduce ΔV_O.

In order to achieve ripple reduction under most conditions, our proposed method senses the loading condition and adjusts

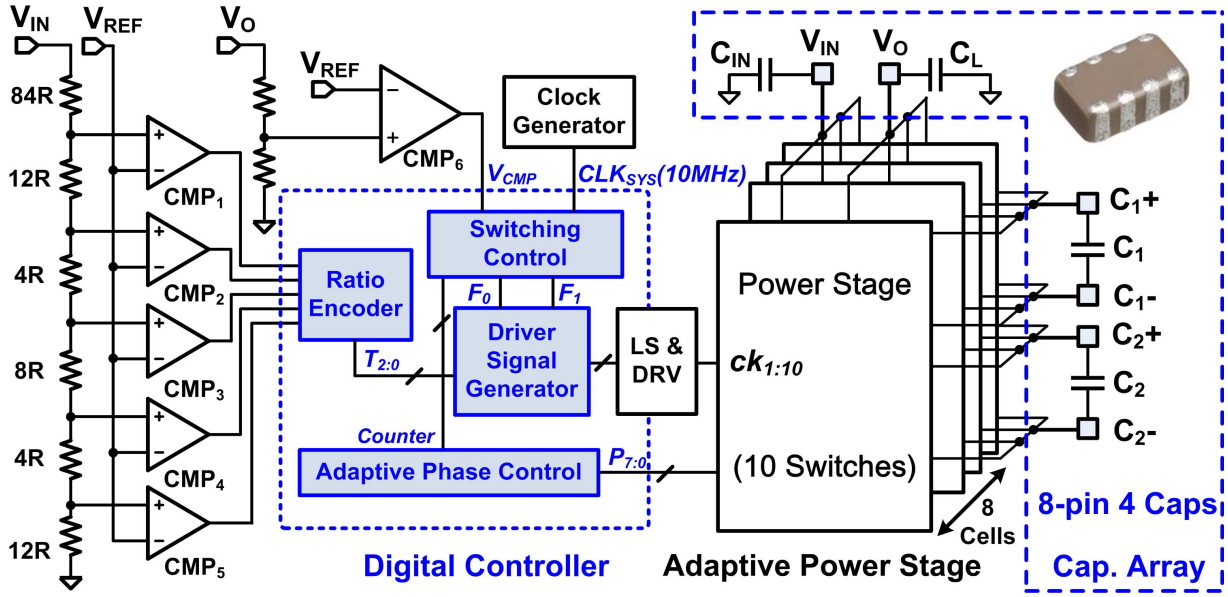

Fig. 9. System architecture of proposed 2-/3-phase SC converter.

TABLE II
CLOCK SELECTION OF THE SWITCH LOGICS WITH VCRs

Clocks/VCRs	1/1x	2/3x	1/2x	1/3x	3/4x	1/4x
ck_1 (S_1)	Φ_1	Φ_2	Φ_1	Φ_1	Φ_1	Φ_1
ck_2 (S_2)	Φ_2	Φ_1	Φ_2	0	0	0
ck_3 (S_3)	1	Φ_1	1	Φ_1	Φ_3	Φ_3
ck_4 (S_4)	0	Φ_1	Φ_1	0	Φ_3	0
ck_5 (S_5)	0	0	0	Φ_2	Φ_2	Φ_2
ck_6 (S_6)	0	Φ_2	0	0	Φ_1	Φ_1
ck_7 (S_7)	1	Φ_1	Φ_2	Φ_2	$\Phi_{2,3}$	$\Phi_{2,3}$
ck_8 (S_8)	0	0	Φ_1	Φ_1	0	0
ck_9 (S_9)	0	Φ_2	0	Φ_2	$\Phi_{1,2}$	$\Phi_{1,2}$
ck_{10} (S_{10})	1	0	1	Φ_1	0	Φ_3

the output impedance to limit the extra charge. As shown in Fig. 6, a counter in the digital controller detects the duration of the discharging phase. If it is longer than the preset range, the controller will decrease the size of the power switches, and the rising slope in the next charging phase will be reduced. In this way, the portion of the output voltage that is higher than V_{REF} will be smaller, yielding a suppressed overcharged voltage ripple.

Fig. 7 is a timing diagram example that illustrates the ripple reduction and power stage adjustment process. Initially, the power switches have a full size of 8. Due to the intrinsic loop delay, the power stage cannot be changed to the discharging phase immediately, and the large charging slope results in a large output voltage ripple. The digital counter senses that the discharging period is 14 cycles of the system period, which is larger than the preset range. In the next step, the controller decreases the size of the power switches by 1 bit, resulting in a smaller charging slope. However, one step adjustment is not enough. The process will continue until the duration of the discharging duration is within the preset range. Size adjustment is activated only after the discharging duration has been out of range N times (N is chosen to be 2^6), as detected by a counter to avoid false triggering. Finally, the size of the power switches is locked when the discharging duration is within 5–7 cycles of the system clock period, which results in a higher switching frequency and smaller ripple for V_O.

The logic flow of adaptive ripple reduction is shown in Fig. 8. After initialization, a counter always keeps monitoring the duration of the discharging phase, and N cycles of the system clock is set as a comparison duration. After one comparison period, the value of the counter will be compared with the preset threshold value. If the counter value is larger than the threshold value, the size of the power stage will be increased. On the contrary, if the counter value is smaller, the size of the power stage will be decreased. The size will keep unchanged when the counter value is within the preset range.

To avoid a large droop when light load changes to heavy load, especially when the size of the power stage is small due to the ripple reduction scheme, the following mechanism is installed. When light load suddenly changes to heavy load, the output voltage will drop because there is not enough current delivered to the output capacitor. This will result in a very short discharging phase and the counter will detect that the value is much shorter than the heavy load detection threshold value (1–2 cycles of system clock). In this case, the power-stage size will change to maximum to restore the output voltage.

IV. CONVERTER DESIGN AND IMPLEMENTATION

A. System Architecture

Fig. 9 shows the system architecture. It consists of ratio encoding comparators (CMP_{1-5}), a hysteretic comparator (CMP_6), a digital controller, level shifters, gate drivers, and

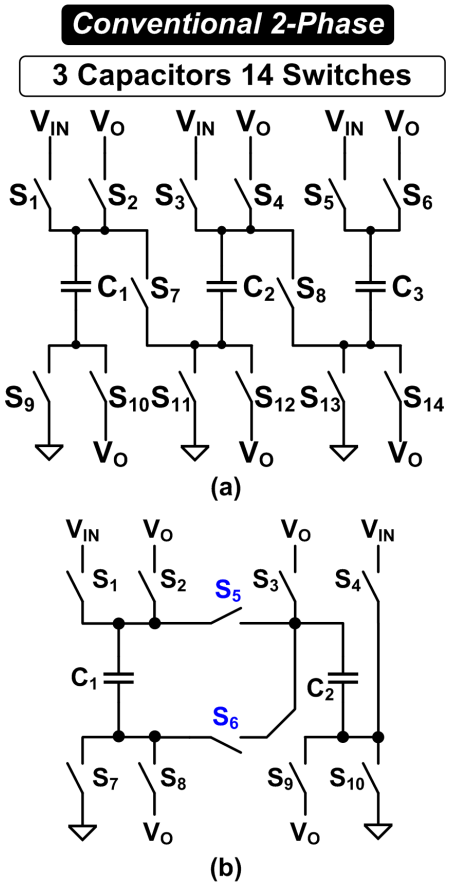

Fig. 10. Configuration of switches and flying capacitors of (a) conventional 2-phase SC converter and (b) proposed switch reduction scheme for 2-/3-phase SC converter.

power stages. To determine the V_O/V_{IN} ratio, V_{IN} is compared to V_{REF} by $CMP_{1\text{-}5}$ and the code $T_{2\text{-}0}$ indicating VCR is issued by the ratio encoder. The driver signal generator then issues the driving signals $ck_{1\text{-}10}$ to provide on/off sequences for the power switches. Instead of manually designing the logic blocks, digital synthesis is adopted to reduce design complexity and accelerate the design speed.

The power stage is split into eight cells and each cell can be adaptively enabled or disabled by the signal $P_{7\text{-}0}$. In such a way, the size of the power switches is adjusted by the adaptive phase controller according to the load current, thus reducing the output voltage ripple especially at light load. The input, output and two flying capacitors are implemented by one 4×1 μF capacitor array [37], and the volume is 40% smaller than using four discrete capacitors.

B. Power Stage

The number of switches is optimized for achieving the six reconfigurable VCRs. Fig. 10(a) shows a conventional 2-phase implementation of the 6 VCRs using 3 flying capacitors and 14 switches. By using 3-phase operation, only two flying capacitors (C_1 and C_2) are needed. To reduce the number of power switches, a switch reduction scheme is proposed in Fig. 10(b): when connecting C_1 to C_2, only the positive plate of C_2 is connected together with C_1, and the negative plate of

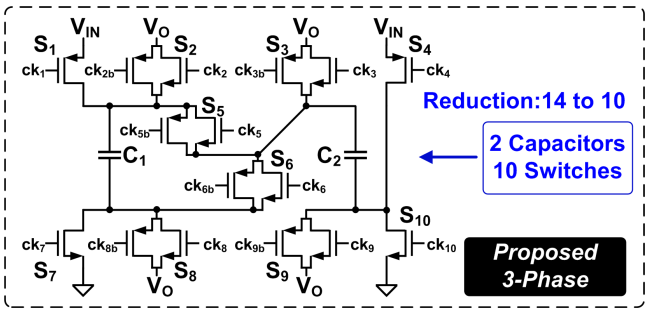

Fig. 11. Power stage implementation of proposed 2-/3-phase SC converter.

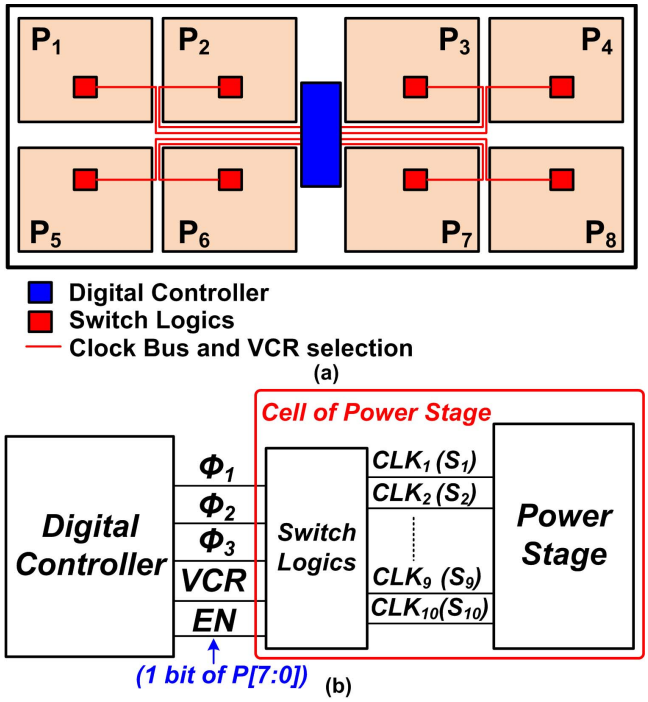

Fig. 12. (a) Layout floorplan of power cells and clock buses. (b) Switch logics.

C_2 is connected to V_O, V_{IN}, and GND. In this way, only two switches (S_5 and S_6) are needed. Therefore, the power stage of the proposed SC converter only needs two flying capacitors and ten power switches, and silicon area reduction of around 28.5% compared to the conventional 2-phase SC converter is achieved, if the size of the power transistors is the same.

Fig. 11 shows the transistor-level implementation of the power stage. To cater for a wide output voltage range, the switches $S_{2\text{-}3}$, $S_{5\text{-}6}$, and $S_{8\text{-}9}$ that connect to V_O are implemented with complementary devices (C-switches). The switches that connected to V_{IN} (S_1 and S_4) and GND (S_7 and S_{10}) are implemented by PMOS and NMOS transistors, respectively. The signals $ck_{1\text{-}10}$ are generated by the digital controller and buffered by the level-shifters and predrivers. To enable digital adaptive ripple reduction, the power stage is split into eight power cells with the same configuration. The detail will be introduced in the following section.

As the polarity of C_2 may change in different configurations, therefore, C_2 should not be an electrolytic capacitor but a

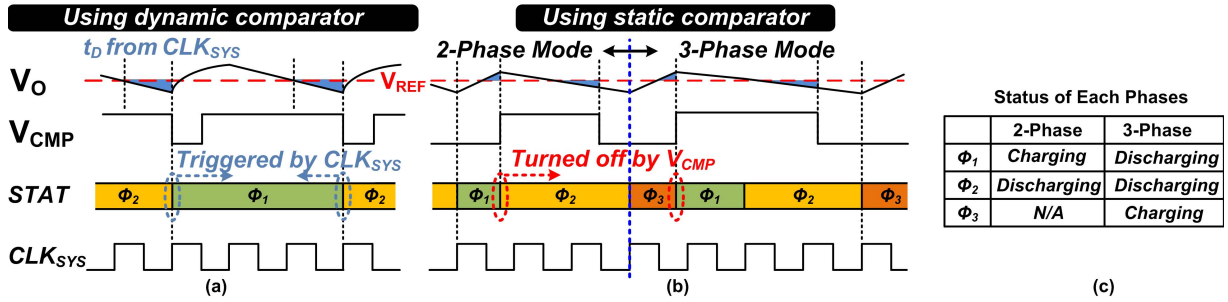

Fig. 13. Timing diagram of synchronized hysteretic control by using (a) dynamic comparator, (b) static comparator, and (c) status of each phases.

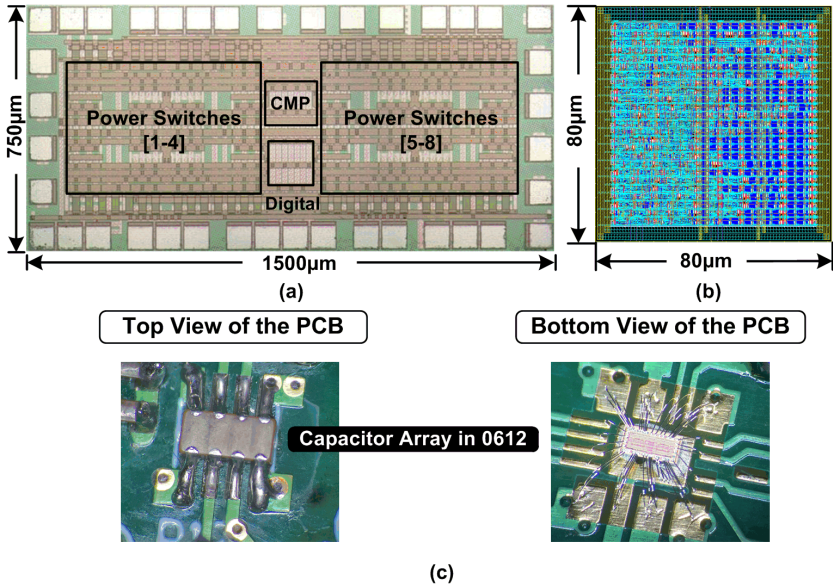

Fig. 14. (a) Chip micrograph, (b) layout of synthesized digital controller, and (c) top and bottom views of PCB for measurement with capacitor array in 0612 packing.

nonpolarized ceramic capacitor. Short bond-wires and small packages are preferred because the capacitors then have lower equivalent series resistance and inductance to reduce the glitches. Moreover, voltage coefficient has to be considered, such that a sufficiently large capacitance is ensured when a high dc voltage is applied.

C. Adaptive Power Cells for Ripple Reduction

The layout floor plan is shown in Fig. 12(a). All power cells are identical. The turn on/off signals of the power cells use thermometer code, and there is only 1-bit change of power cells during the transition. As such, potential glitches due to reconnecting the power cells are minimized. To eliminate phase mismatch during clock distribution, the H-tree structure is employed, as shown in Fig. 12(a). The three clock phases (Φ_1, Φ_2, and Φ_3), the VCR selection signals and the enable signal EN are generated in the digital controller and then distributed by clock buses.

The block diagram of switch logic is shown in Fig. 12(b). The logic that determines the clocks for each transistor is placed locally close to each power cell. The dead-time generation circuit is used to prevent shoot-through current and is placed locally at the power cell. Table II lists the clock selection of each transistor (S_1 to S_{10}) under different VCRs. For example, when VCR = 1/4×, transistors S_1, S_6 and S_9 will be turned on in Φ_1; S_5, S_7 and S_9 will be turned on in Φ_2; S_3, S_7 and S_{10} will be turned on in Φ_3; and S_2, S_4 and S_8 will be kept off. The selection logic is synthesized by standard digital cells.

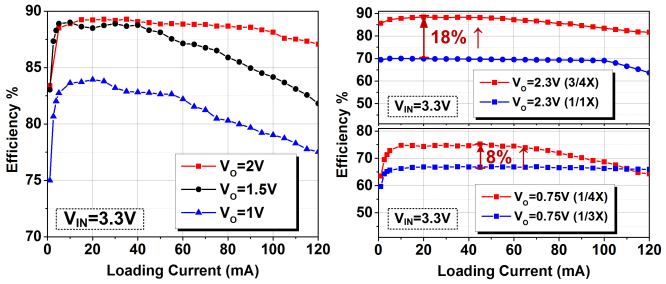

Fig. 15. Measured efficiency of the proposed SC converter versus loading current.

D. Digital Controller

The digital controller consists of the adaptive ripple reduction circuit (discussed in Section III) and the switching controller, to be discussed below. Fig. 13 shows the synchronized

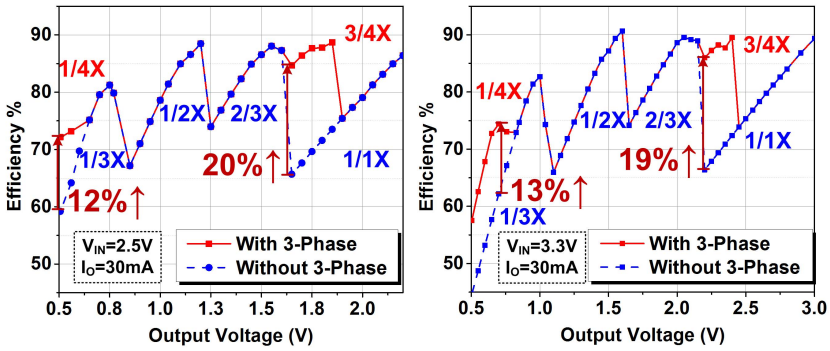

Fig. 16. Measured efficiency of the proposed SC converter versus output voltages.

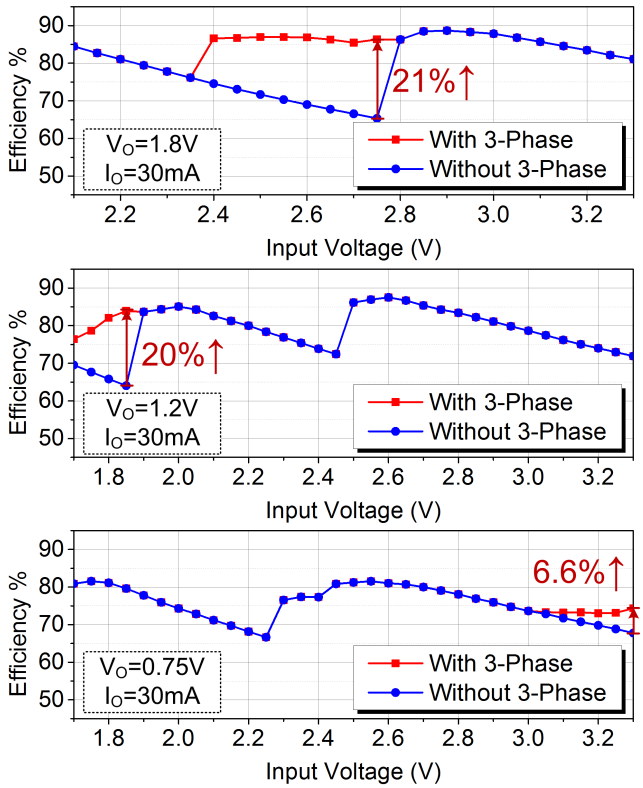

Fig. 17. Measured power efficiency versus input voltage.

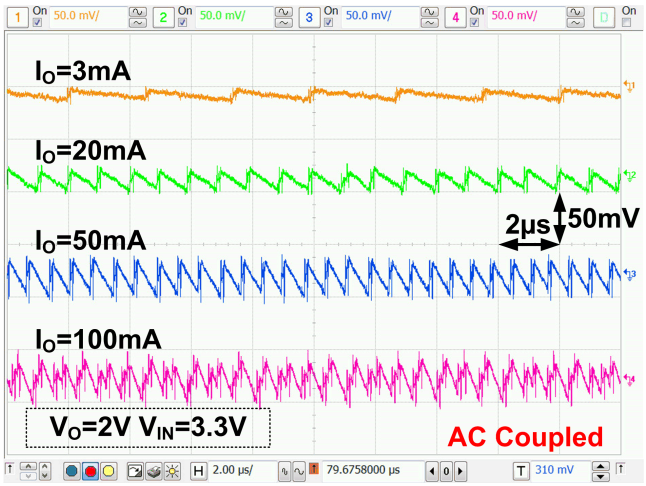

Fig. 18. Measured steady state waveform of output ripple voltage.

hysteretic control that is used to achieve voltage regulation and fast response. The single boundary is set by V_{REF}, representing the designed output voltage level. In [8] and [38], when the comparator detects that V_O is lower than V_{REF}, the SC converter will switch to the next clock phase to recharge the output capacitor. A dynamic comparator that consumed no quiescent current was used, and triggered by a high-frequency system clock. The power consumption is low but the drawback is that it needs system clock to trigger the boundary violation detection, meaning that the phase switching could not be triggered immediately when V_O is lower than V_{REF} (in Fig. 13(a)). When the system frequency is high, the delay could be small. However, our design uses a 10-MHz system clock. In the worst case, a delay of 100 ns is needed before the system clock could trigger to flip the dynamic comparator. Therefore, the delay may bring extra charge to the output and result in large voltage ripple.

In this design, to avoid the extra voltage ripple after V_{CMP} turns high, synchronized hysteretic control is used. The system clock is set at 10 MHz, generated by an on-chip ring oscillator. At 10 MHz, the speed requirement of the comparator is not as critical as that in [38], and a static comparator (CMP_6) with a quiescent current of 12 μA is used instead of a dynamic one, as shown in Fig. 13(b). The turn-on of the charging phase is triggered by the system clock, while the turn-off is triggered by the comparator. Hence, the delay due to the mismatch of the system clock can be eliminated. Then, by employing the proposed adaptive ripple reduction technique described in Section III, the undesired voltage ripple caused by loop delay caused by the static comparator, digital logic, level shifters, and power stages could be reduced.

Fig. 13 also shows the status of each phase in the 2-/3-phase mode. For 2-phase mode VCRs, Φ_1 and Φ_2 are interchangeable. We may define the charging phase as Φ_1 and the discharging phase as Φ_2. For 3-phase mode VCRs, refer to the sequence in Fig. 3. In Φ_3, the output capacitor receives more charge than in Φ_1 and Φ_2. From the perspective of the output capacitor, V_O falls in Φ_1 and Φ_2, and will rises in Φ_3. Hence, Φ_1 and Φ_2 are defined as the discharging phases, and

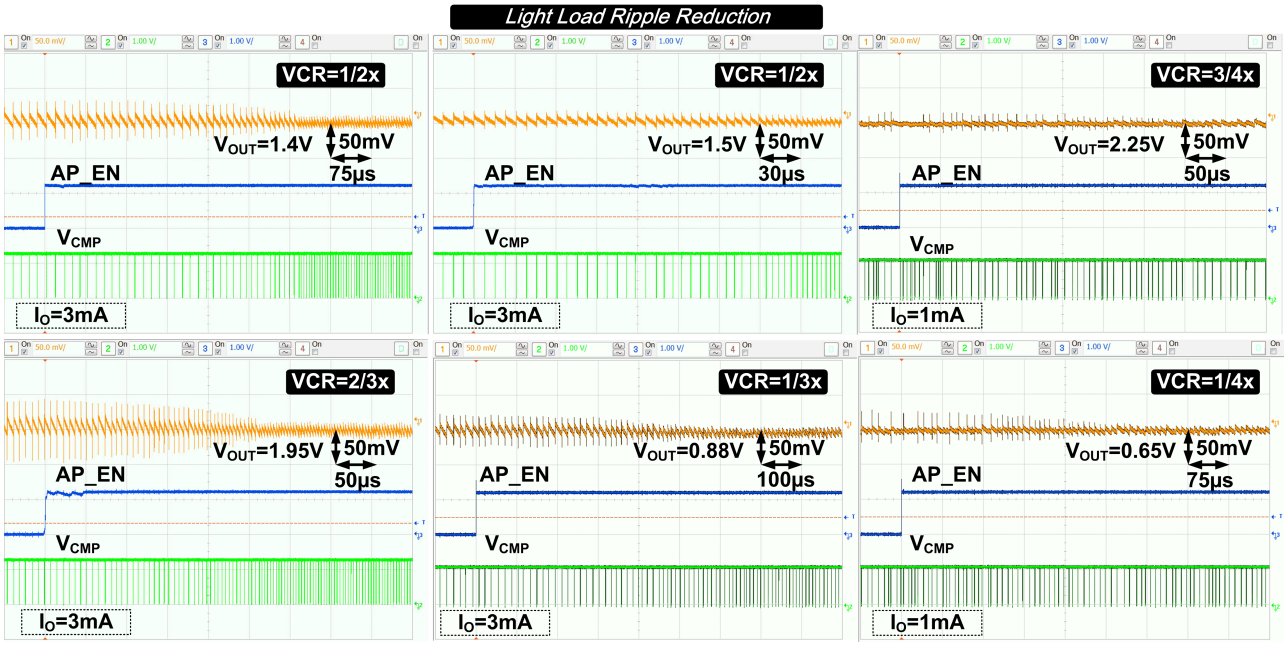

Fig. 19. Measured waveforms of light load ripple reduction under different VCRs.

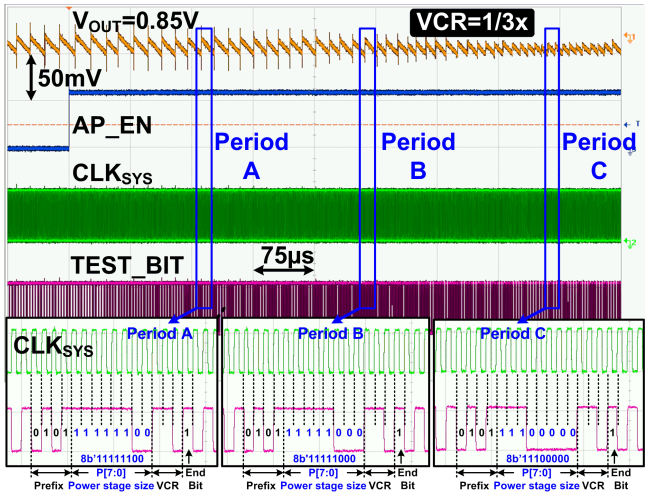

Fig. 20. Measured waveforms of ripple reduction procedure and the outputs of testing data.

Φ_3 is defined as the charging phase. For design simplicity, the transition between Φ_1 and Φ_2 is triggered by the system clock.

V. Measurement Results

The proposed SC converter was fabricated in a 0.13 μm bulk CMOS process. Fig. 14(a) shows the chip micrograph with a total area of 750 μm $\times$ 1500 μm, including power switches, comparators, digital controller and decoupling capacitors. The layout of the fully synthesized digital controller with an area of 80 μm $\times$ 80 μm is shown in Fig. 14(b), and the printed circuit board (PCB) setup with the 0612 capacitor array is shown in Fig. 14(c). The capacitor array is on the top of the PCB and the chip is bonded on the bottom, and they occupied almost the same PCB area. The 4 $\times$ 1 μF capacitor array is mounted on the top side of the PCB, and the test chip is wire-bonded on the bottom side. The four capacitors are the two flying capacitors and the input and output decoupling capacitors. Other capacitors are used for testing purposes.

Fig. 15 shows the measured efficiency versus the load current. This design achieved a moderately high load current capability of 120 mA in all 6 modes. The measured peak efficiency was 91% when $V_{\rm IN}$ = 3.3 V and I_O = 30 mA. The results with and without the 3-phase modes are shown for comparison. When V_O = 2.3 V, by using the 3-phase 3/4$\times$ mode instead of the 2-phase 1/1$\times$ mode, the converter achieved up to 18% efficiency improvement. When V_O = 0.8 V, it also achieved up to 8% efficiency improvement by using the 3-phase 1/4$\times$ mode rather than the 2-phase 1/3$\times$ mode.

The measured efficiency with respect to the output voltage is shown in Fig. 16. It shows that efficiency improvements of 13% and 20% were obtained when the converter worked in the 1/4$\times$ and 3/4$\times$ modes, respectively. Fig. 17 plots the efficiency versus the input voltage, and shows efficiency improvement when the 3-phase modes were used instead of the 2-phase modes. Benefited from 3-phase modes, the average efficiency improvements over the entire input voltage range when V_O = 1.8, 1.2, and 0.75 V were 5.4%, 1.7%, and 0.6%, respectively. When $V_{\rm IN}$ = 3.3 and 2.5 V, the average efficiency improvement over the output range was 3.4%. Moreover, with two additional VCRs, the SC converter achieved a wide output voltage range of 0.5 to 3 V with an input voltage of 1.6 to 3.3 V.

The measured output voltage ripple at different loading currents is shown in Fig. 18. By activating the ripple reduction scheme, the measured ac coupled voltage ripples were all lower than 50 mV for I_O ranged from 3 to 100 mA. Fig. 19 shows the effectiveness of the ripple reduction scheme, which is enabled by the adaptive-phase-enable signal *AP_EN*. Before *AP_EN* was enabled, large ripples and glitches around 100 mV can be observed due to the parasitic inductance

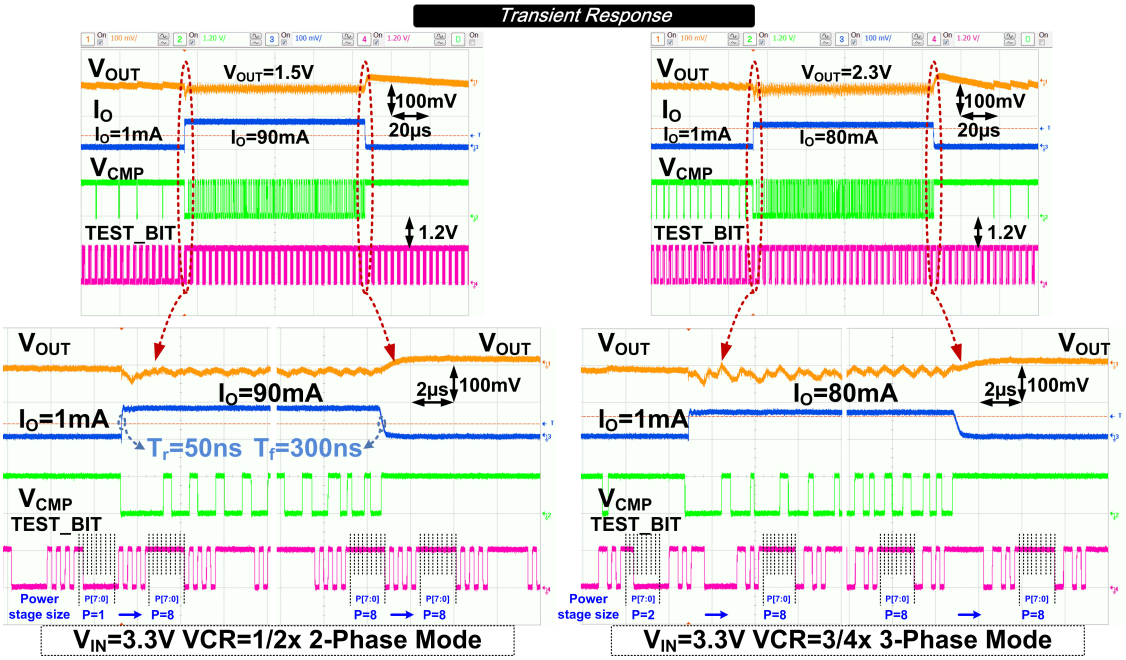

Fig. 21. Measured waveforms of transient response.

TABLE III

PERFORMANCE COMPARISON WITH STATE-OF-THE-ART SC CONVERTER WORKS

Work	[14] LM2770	[15] LTC1503	[16] TPS60500	[13] VLSIC`15	[22] JSSC`17	[32] ISSCC`15	[30] ISSCC`14	This work
Technology	N/A	N/A	N/A	0.25 μm	65 nm	65 nm	0.16 μm	**0.13 μm**
Topology	Step-Down SC	Step-Down SC	Step-Down SC	Step-Down SC	Step-Down SC	Step-Down SC	Step-Up SC	**Step-Down SC**
Ideal VCRs	2/3x, 1/2x, 1/3x	1/1x, 2/3x. 1/2x	1/1x, 2/3x, 1/2x, 1/3x	24 Ratios	3/4x, 2/3x, 1/2x	1/3x, 1/4x	6x	**1x, 3/4x,2/3x, 1/2x,1/3x, 1/4x**
# of VCR	3	3	4	24	3	2	1	**6**
# of C_{fly}	2	2	2	4	3	2	3	**2**
V_{IN}	2.7-5.5V	2.4-6V	1.8-6.5V	2.5-5V	1.6-2.2V	1.5-2.5V	3.3V	**1.6-3.3V**
V_O	1.2V, 1.5V	1.8V, 2V	0.8-3.3V	0.2-2V	0.6-1.2V	0.4-0.7V	16V	**0.5-3V**
V_O/V_{IN} Range	Fixed V_O	Fixed V_O	53.19%	36%	27.3%	12%	Fixed V_O	**75.7%**
η_{peak}	85%	90%	90%	95.5%	80%	79.5%	70.3%	**91%**
$P_{OUT,MAX}$	250mW	200mW	625mW (1/1x) 255mW (others)	186mW	152mW	26mW	160mW	**250mW**
Active Area	N/A	N/A	N/A	3.47mm^2	0.844mm^2	0.425mm^2	1.65mm^2	**1.125mm^2**
Passive Type	2× 1μF 2× 10μF	2× 1μF 2× 10μF	1× 1μF 1× 4.7μF 2× 10μF	1× 4.7μF 4× 2.2μF	On-Chip	On-Chip	On-Chip 2× 1μF 1× 220nF 1× 100nF	**1× Cap Array with 4× 1μF**
Passive Volume	5.1mm^{3*}	6.72mm$^{3\#}$	7.312mm$^{3\#}$	1.5mm$^{3\#}$	N/A	N/A	1.1mm$^{3\#}$	**2.566mm^3 (0508) 6.912mm^3 (0612)$^+$**

*: Estimated by using 0603 (1.6mm × 0.8mm × 1mm) multi-layer ceramic capacitors.
#: Extracted from official recommended demonstration boards and measurement results by using 0402 [13] and 0201 [30] multi-layer ceramic capacitors.
+: Extracted from measurement results.

of bond-wires and PCB traces. After *AP_EN* was enabled, the voltage ripple was significantly reduced. As high as four times ripple reduction was achieved from 90 to 20 mV for $I_O = 3$ mA and $V_O = 1.95$ V. The ripple reduction was also effective in other conditions, also listed in Fig. 19.

To observe the status of the registers in the digital controller and help debugging during the measurement, a design for test (DFT) module was implemented. Parallel to series conversion was done to reduce the number of monitoring pins. The data of the registers indicating the VCR used and the power stage size (P[7:0]) were read out through the single *TEST_BIT* pin. The sequence of the testing output is initialized by the prefix bits *4b′ 0101*, followed by the size of the power stage and the code of VCR, and terminated by the end bit *1b′ 1*. Fig. 20 shows the measured procedure of ripple reduction. From period-A to period-C, the size of the power stage was

decreased from $8b'$ *11111100* to $8b'$ *11100000* after (*AP_EN*) was triggered.

The measured transient response waveforms of $V_O = 1.5$ V (in 2-phase mode) and 2.3 V (in 3-phase mode) are shown in Fig. 21. Due to the hysteretic control, when the load current switched from 1 to 90 mA and 1 to 80 mA, ΔV_{OUT} was around 50 mV and the recovery time was less than 500 ns. No obvious over-shoot or under-shoot was observed. To restore current deliverability, the power stage was fully turned on once a heavy load was detected.

Table III summarizes the performance comparison with state-of-the-art works. Compared to commercial products [14]–[16] with off-chip capacitors delivering similar output power with the same number of flying capacitors, this work achieved more VCRs and hence improved efficiency. Moreover, this work delivered more power using fewer flying capacitors and achieved a wider $V_{\mathrm{O}}/V_{\mathrm{IN}}$ range than the recursive SC converter of [13]. Compared with integrated 2-phase [22] or 3-phase [30], [32] SC converters, the proposed SC converter achieved a wider operating voltage range. As discrete flying capacitors with larger value are used, this work also achieved a higher output power with higher PCE.

VI. Conclusion

In this paper, a 2-/3-phase 6-ratio SC dc-dc converter is proposed. The 3-phase operation is proposed and analyzed to achieve two more VCRs than the conventional 2-phase SC converter. The achieved maximum available output voltage range over the input voltage range is up to 75.8%, and the PCE was improved by as high as 20% compared to 2-phase SC converters.

A digital adaptive ripple reduction scheme is also introduced to reduce the output voltage ripple by as much as four times at light load. This converter is implemented in a 0.13 μm bulk CMOS technology and is capable of operating at a wide input range of 1.6–3.3 V and a wide output range of 0.5–3 V with 91% peak efficiency and delivers a maximum power of 250 mW.

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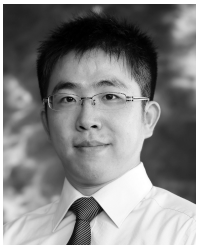

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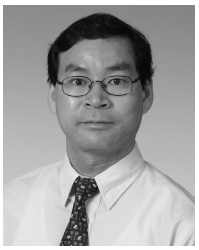

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