Frequency-bandwidth-tunable powerline notch filter for biopotential acquisition systems

C.-T. Ma, P.-I. Mak, M.-I. Vai, P.-U. Mak, S.-H. Pun, W. Feng and R.P. Martins

Presented is a novel powerline notch filter embeddable into a chopper-stabilised instrumentation amplifier for biopotential measurements. The frequency-translation property of the chopper enables the powerline notching to be indirectly implemented by two resonant zeros around the chopper frequency, resulting in substantial silicon area savings. Transistor-level implementation in 90 nm CMOS using a pseudo-*LC* circuit topology with *Q*-enhancement demonstrates 50 to 60 Hz frequency tunability, 25/41 dB powerline rejection at 5/30 Hz bandwidth, and 1000× relaxation of time constant under a 4 kHz chopper frequency.

Introduction: Lessening the measurement cost of biopotential signals such as the electroencephalogram (EEG), electrocardiogram (ECG), and electromyogram (EMG) against various contaminating signals has driven the development of performance-intensive low-power CMOS biomedical monitoring systems [1]. The dominant contaminating signals sophisticating the design of the front-stage instrumentation amplifier (IA) are the transistor flicker noise, and the powerline interference located at 50 or 60 Hz that are geographically dependent. Chopper stabilisation [2] has been the technique embedded into the IA for eliminating the flicker noise (and also the DC-offset), whereas the powerline interference has been conventionally tackled by exploiting a separate powerline notch filter [3]. This powerline notch filter unavoidably calls for extra power and silicon area. Moreover, if the notch filter is directly implemented by on-chip inductor-capacitor (*LC*) resonances, the area overhead will be huge for realising the required time constant.

In this Letter we propose a powerline notch filter that can be embedded into the chopper-stabilised IA. The frequency-translation property of the chopper significantly helps relaxing the filter's time constant, while the pseudo-*LC* quality-factor (Q)-enhanced circuit topology realises a frequency-bandwidth-tunable notch; all of which are demanding features of portable biomedical acquisition systems.

Architecture: Fig. 1 shows the block diagram and the schematic of the proposed powerline notch filter. The input chopper modulator (M_{IN}) will first frequency-translate the input biopotential signal, together with the powerline interference (assumed at 50 Hz) from spectrum S_1 to S_2, where the chopper frequency is set to an optimised 4 kHz [1]. Accounting the upper and lower sidebands of the powerline interference, it will be split into two components located at 3.95 and 4.05 kHz. Rejecting them at these higher frequency locations reduces the required time constant for building the notch. The output chopper modulator (M_{OUT}) will frequency-translate both the signal and powerline interference back to the baseband after simple lowpass filtering (spectrum S_3 to S_4). The final response will be a single notch at 50 Hz as expected (S_5).

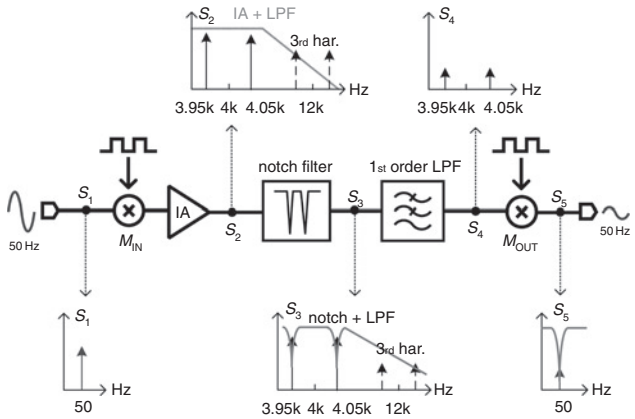

Fig. 1 *Block diagram of a chopper-stabilised IA with embedded powerline notch filter*

Circuit implementation: The associated implementation is constituted by two pseudo-inductor-C_1 notches with Q-enhancement and frequency-bandwidth tunability as shown in Fig. 2, where the schematic of *notch*$_2$ (the same as *notch*$_1$) is omitted for brevity. With the frequency-translation method, the values of capacitor C_1 can be reduced by more than 1000× when compared with a direct method. The *Q*-enhancement circuit is based on a cross-coupled transistor pair for building negative impedance; it cancels the excessive impedance of the pseudo-*L*. Since the powerline frequency is geographically dependent (50 or 60 Hz), and the passives integrated on-chip can vary with the integration process, it is design convenient to externalise the capacitor C_2 and adopt a variable resistor R (based on a triode-region transistor) for frequency tuning. The overall *s*-function governing the notch filter is given by

$$G(s) = \frac{s^2 + s(\alpha/C_1C_2R) + \omega_{n1}^2}{s^2 + s[\alpha/C_1C_2(R + r_o) - \omega_{n2}/Q] + \omega_{n2}^2} \tag{1}$$

where

$$\alpha = (C_1 + C_2 - C_1 gm_x R) \tag{2}$$

$$Q = C_1 r_o \tag{3}$$

$$\omega_{n1}^2 = (gm - gm_x)/C_1C_2R \tag{4}$$

$$\omega_{n2}^2 = (gm - gm_x)/C_1C_2(R + r_o) \tag{5}$$

r_o is the output resistance of the input source follower; gm and gm_x are the transconductances of M_A and M_x, respectively. According to (1), α should be neutralised to maximise the *Q*-factor of the notch. Note that r_o can be made sufficiently large to suppress the overshoot and result in a better *Q*, but the location of the pole and zero in (1) will further separate with each other and the notch bandwidth will be enlarged. A simple way to overcome this drawback is to maximise the resistance of R, thereby pushing ω_{n1} closer to ω_{n2}.

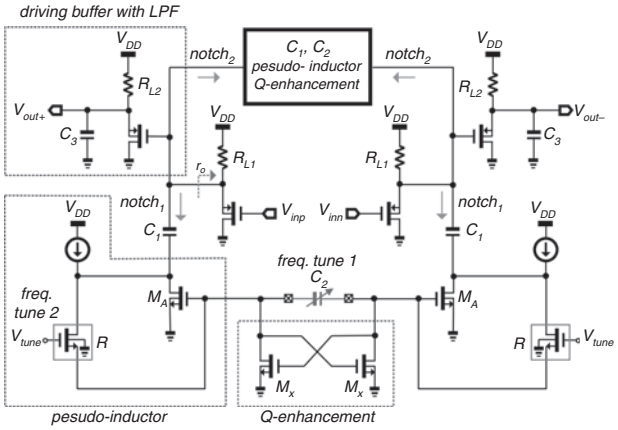

Fig. 2 *Schematic of proposed powerline notch filter*

The *Q*-factor of the notch is susceptible to the odd-harmonic-mixing problem induced by the square-wave-like chopper functions toggling between 1 and −1 at chopper frequency. To minimise this effect, the −3 dB bandwidth of the IA is set to the chopping frequency whereas a resistor-capacitor (*RC*) lowpass filter (LPF) is added at the output driving buffer to realise overall two first-order LPFs. The overall notch rejection $G_{n,wLPF}$ accounting all odd harmonics is given by

$$G_{n,wLPF} = \left(|A_{-1}|\angle\phi_{-1} + \sum_{n=1}^{\infty}\frac{1}{2n+1}|A_{2n+1}|\angle\phi_{2n+1}\right) \times \left(|A_1|\angle\phi_1 + \sum_{n=1}^{\infty}\frac{1}{2n+1}|A_{2n+1}|\angle\phi_{2n+1}\right) \times \frac{1}{\left(\sum_{\substack{n=1\\n=odd}}^{\infty}1/n\right)^2} \tag{6}$$

where n is an integer, $|A_{-1}|\ \angle\phi_{-1}$ and $|A_1|\ \angle\phi_1$ are the rejection gain and phase at the notching frequency. According to (6), the improvement

of the notch rejection offered by the LPF G_{imp} can be calculated,

$$G_{imp} = G_{n,wLPF} - G_{n,w/oLPF} = \frac{(|A_{-1}|\angle\phi_{-1} + |A_1|\angle\phi_1)\Delta_{n,odd} + \Delta^2_{n,odd}}{\left(\sum_{\substack{n=1\\n=odd}}^{\infty} 1/n\right)^2} \quad (7)$$

where

$$\Delta^2_{n,odd} = \left(\sum_{n=1}^{\infty} \frac{1}{2n+1}|A_{2n+1}|\angle\phi_{2n+1} - \sum_{n=1}^{\infty} \frac{1}{2n+1}\right)$$

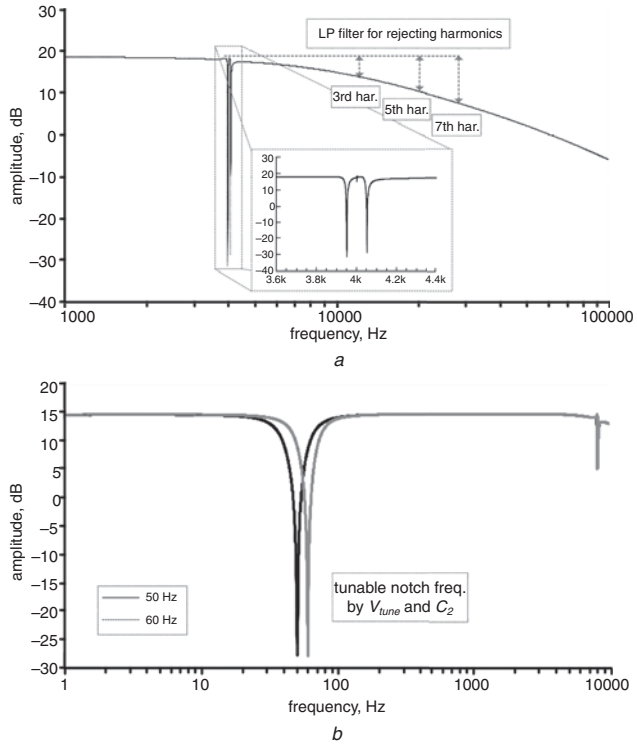

Fig. 3 *Simulated frequency responses of chopper notch filter*

a Before demodulation
b After demodulation

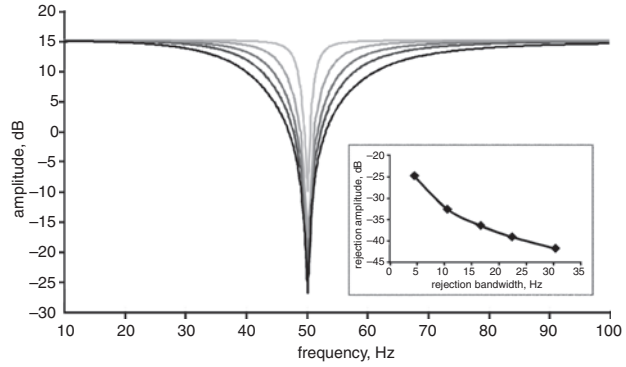

Fig. 4 *Simulated rejection gain-bandwidth characteristic by varying R_{L1}*

Simulation results: The powerline notch filter embedded into a chopper-stabilised IA was implemented using a 90 nm CMOS process with both thick- and thin-oxide transistors. The frequency responses of the filtering mechanism before and after demodulation are illustrated in Figs. 3*a* and *b*, respectively. Two zeros suppress the two fundamental harmonics of the powerline interference (Fig. 3*a*), whereas the two first-order LPFs reject the remaining odd harmonics. The demodulated frequency response will be a single zero at 50 Hz (Fig. 3*b*), or at 60 Hz via tuning of V_{tune} and C_2. The achieved notch rejection is more than 40 dB in both the 50 and 60 Hz cases. This single-order notching has the intrinsic advantage of no passband ripple. Moreover, in order to extract the biopotential signal within the notch frequency band with higher precision, the rejection can be traded with the notch bandwidth, which shows a range of 5 to 30 Hz and a notch deepness of 25 to 41 dB by tuning R_{L1}, as shown in Fig. 4. The power consumption subject to the value of R_{L1} ranges from 57 to 75 μW at 3 V.

Conclusion: A novel powerline notch filter embeddable in the IA for rejecting the powerline interference has been presented. Capacitor area for realising the notch's time constant is reduced by 1000× by utilising the frequency-translation property of the chopper stabilisation, which has been the technique of flicker-noise reduction, but is now extended to reject also the powerline interference fully within the IA. Simulation results validate the feasibility of the circuit in a mainstream 90 nm CMOS process.

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