Analysis of Common-Mode Interference and Jitter of Clock Receiver Circuits With Improved Topology

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***Abstract*— This paper presents an analysis based on the impulse sensitivity function to precisely characterize and estimate the jitter caused by the common-mode interference (CMI). Unlike the conventional common-mode rejection ratio concept, the proposed method considers the CMI jitter in a transient rather than in an ac perspective. Inspired by the analytical results, we propose a clock receiver circuit (CRC) based on the self-bias amplifier topology. The accuracy of the analysis and the efficiency of the proposed CRC are verified both in simulations and measurements. A 1-GS/s ADC was fabricated in 65-nm CMOS containing simultaneously three CRCs, including an inverter-chain, a differential amplifier and the proposed structure, serving as the sampling clock. Both simulation and measurement results show a good agreement with the presented analysis. The proposed CRC achieves a 30-fs$_{rms}$ jitter with a 620-μW power at 1.2 V supply. With a similar CMI rejection and random jitter performance, the proposed CRC exhibits a 20-fold power reduction when compared with the state-of-art designs.**

***Index Terms*— Low clock jitter circuit, ISF, self-bias.**

I. Introduction

NEXT generation wireless and wireline communication systems require a high -speed and -precision clock for their analog-to-digital converters (ADCs). While toward higher sampling rate, the jitter of the sampling clock can limit the achievable SNR of the ADC. For instance, the SNRs of the ADCs presented in [1] and [2] are both degraded by more than 6 dB at their Nyquist input rate due to the jitter from the sampling clock. Besides, it can be found in the state-of-the-art ADC survey [3] that the SNDR of all reported ADCs is bounded by a root-mean-square (rms) jitter of 100 fs and mostly below 1 ps as shown in Fig. 1. This boundary is not only applicable for high-speed implementations but also valid for high-resolution designs, where the ADCs with SNDR larger than 80 dB are all bounded by 1 ps$_{rms}$ jitter.

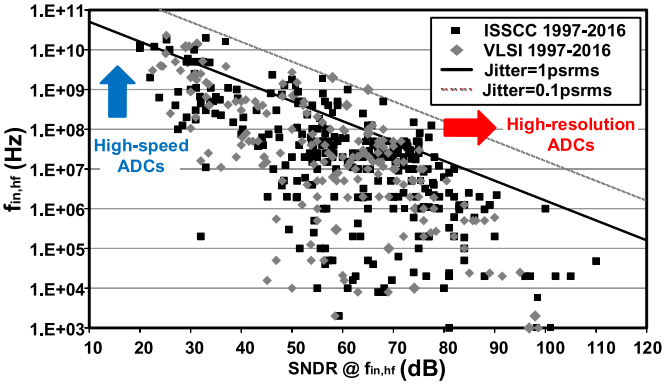

Fig. 1. SNR degradation due to jitter as a function of input frequency.

Theoretically, for each decade increased of rms jitter, the SNR of the ADC decays 20 dB; therefore, a low jitter clock source is extremely important for high performance ADC designs. In general, the sampling clock of the ADCs can be either from the on-chip PLL [1], [2] or an off-chip clock source, and obtained from a crystal oscillator or a signal generator. In the first scenario, the jitter is dominated by the on-chip PLL, and the clock receiver circuit design can be relaxed due to the low-pass filtering effect from the PLL on the reference clock. While the low jitter PLL designs have been well studied in [4] and [5], we consider and analyze in this paper a second scenario, which is applicable to implementations with IPs integrated in wireless communications [6], [7] or used for testing [8].

A high purity off-chip sinusoidal clock signal can be generated by band-pass filtering a sine-wave from a signal generator achieving a jitter less than 30 fs$_{rms}$ [7]. However, both on-chip and off-chip noise as well as their interference can introduce a large jitter to the clock source of ADCs. The overall jitter of the sampling clock can be classified as deterministic or random. The deterministic jitter is mainly caused by the supply noise, environmental coupling noise and bouncing between the on-chip and off-chip grounds. Approaches, such as deep

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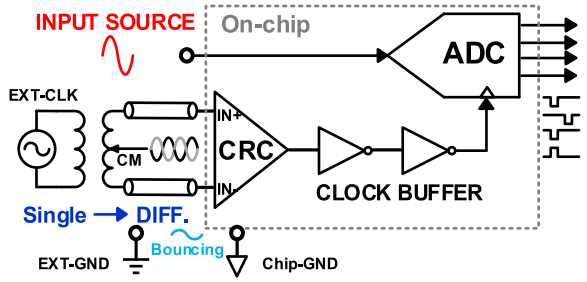

Fig. 2. Scheme of a clock generation/receiver system for high-speed ADCs.

n-well isolation, LDO, power supplies separation and supply decoupling for clock distribution circuits [7], can be adopted to suppress the deterministic jitter. On the other hand, the common-mode interference (CMI) from the bouncing between the on-chip and off-chip grounds also can induce significant jitter to the clock source which cannot be suppressed by the methods mentioned above. Hence, the CMI rejection is a critical design consideration for CRC designs and the reason for the focus of this work. We will show in Section II that a large rms jitter can be induced by a small CMI with a clock receiver circuit (CRC) based on an inverter chain. Thus, even though the inverter can consume very low power, it is difficult for the inverter-based CRC with a single-ended clock input to achieve an rms jitter less than 100 fs. To achieve an extremely low jitter, conventional approaches use a differential amplifier to convert the differential sine-wave clock input to a single-ended square-wave signal which can suppress common-mode voltage fluctuations. Common-mode interference is mainly composed by the noise coupled to the common-mode node of the Balun and bouncing between the on-chip and off-chip grounds, which can be illustrated with the block diagram of Fig. 2.

To obtain a low jitter sampling clock for the ADCs, both deterministic and random jitter are critical. The random jitter can be suppressed by increasing the current to obtain a sharper transition slope [9]. With a traditional differential amplifier, the literature shows that it consumes around 30 mA of current in 0.35 μm BiCMOS process to achieve 50 fs_{rms} jitter [7] whose power is 2-fold higher than the state-of-the-art ADC requiring this jitter specification. Although many design methods and circuits based on different types of differential amplifier have been proposed to lower the random jitter as well as the power consumption [8], [10], [11], the progress is still very limited and the power consumption is not acceptable for present highly effective state-of-art ADCs.

Besides, unlike traditional differential amplifiers used to tackle a small signal in a linear time-invariant (LTI) system, the amplifier utilized in the CRC is driven by a clock signal with a large swing, and its circuit states vary with time. Therefore, the common-mode rejection ratio (CMRR), obtained from the LTI, fails to characterize the common-mode rejection effect of these circuits. Though measurement results in [6]–[8] support a good common-mode suppression for their CRCs based on the differential amplifier topology, a theoretical study that can quantify the jitter caused by the common-mode noise, was not yet developed.

This paper introduces a numerical method, based on the impulse sensitivity function (ISF) [12], to quantify the deterministic jitter caused by the CMI. Unlike the conventional CMRR approach, the present scheme can precisely estimate the CMI jitter based on its time-variant response characteristic. Motivated by the analysis, we propose a self-bias topology based CRC that achieves sub-50fs jitter and consumes 20-fold less power than state-of-art designs while simultaneously maintaining a good common-mode noise suppression. Furthermore, we analyze the constraint of the differential amplifier (diff-amp) based CRCs for achieving low power consumption with low random jitter. It can be recognized that there exists a tradeoff between deterministic and random jitter in conventional approaches. We will verify the present method and analysis through simulations and measurements with three CRC topologies, including an inverter chain, a differential amplifier and the proposed structure. Moreover, we will integrate the three CRCs with a 1 GS/s SAR ADC in 65nm CMOS. Both simulation and measurement results show a good agreement with our analysis, confirming the effectiveness of the proposed CRC.

The paper is organized as follows. Section II describes the characterization of the deterministic jitter caused by CMI with ISF. Section III proposes a CRC based on ISF analysis. Section IV compares the random jitter performance among two types of widely adopted CRCs and the proposed structure. Section V shows the measurement results, and finally Section VI summarizes the results of the proposed CRCs.

II. Charaterization of CMI Jitter by ISF

In a standalone ADC testing, an off-chip sinusoidal signal is often adopted as the clock source for the ADC due to its single harmonic characteristic. However, a sinusoidal signal is vulnerable to the interference and noise because of its slow slope when compared with a square-wave signal. Therefore, a CRC is used to convert the sinusoidal input into a square-wave clock signal for the ADC's sampling network. A strong CMI rejection is necessary for the CRC in order to suppress the noise and interference between on-chip and off-chip interface. In this section, we analyze first the CMI rejection of a diff-amp and an inverter based CRC.

A. Conventional LTI Approach and Disagreement

Linear time-invariant analysis is fundamental in analog circuit design, but its application is limited to linear time-invariant systems. For oscillators and amplifiers driven by a clock signal with large swing they are time-varying in nature according to the clock phases. This can be shown with the following analysis. For example, a differential amplifier with the topology of Fig. 3 (a) can be easily designed with a CMRR over 28 dB in 65nm CMOS when both inputs are biased at mid-supply. By applying the CMRR concept, the deterministic jitter due to CMI can be obtained by converting a common-mode into a differential interference and then dividing the differential error voltage by the slope of the differential input clock as indicated in (1) and (2),

$$CMRR = 20\log_{10}\left(\frac{A_d}{|A_{cm}|}\right) \tag{1}$$

$$\sigma_{cm,rms} = \frac{10^{-\frac{CMRR}{20}} \cdot A_{cm,noise,rms}}{2\pi f_{clk} \cdot \frac{1}{2}A_{clk,p2p}} \tag{2}$$

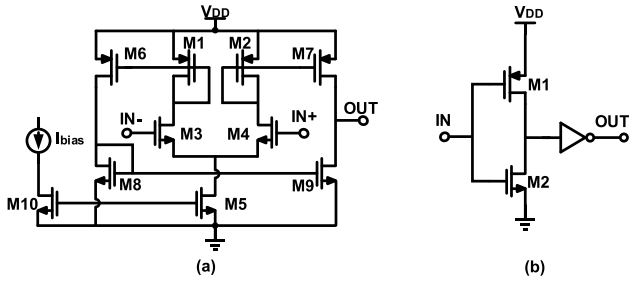

Fig. 3. Traditional clock receiver circuits: (a) differential amplifier (b) inverter chain.

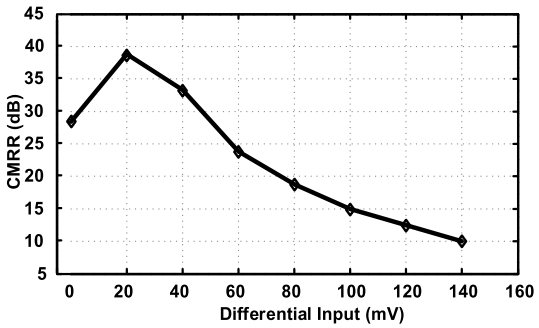

Fig. 4. Simulated CMRR under various differential input voltages.

where A_d is the differential gain, A_{cm} is the common-mode gain, $A_{cm\_noise,rms}$ represents the rms magnitude of the common-mode noise, $A_{clk,p2p}$ is the peak-to-peak amplitude of the input clock signal and f_{clk} is the clock frequency. Then, we can compare the results from (1) and (2) through simulations. Based on the setup in Fig. 2 and adopting the differential amplifier in Fig. 3 (a) (designed with CMRR over 28 dB) as the clock receiver circuit, a sinusoidal interference with an amplitude of 20 $mV_{p\text{-}p}$ is applied to the common-mode node of the differential clock input. According to (1)-(2), the computed jitter is around 37 fs_{rms} under a differential input clock frequency of 1 GHz with a signal amplitude of 2.4 $V_{p\text{-}p}$. Nevertheless, more than 170 fs_{rms} jitter is obtained from *Spice* simulations, which is much larger than the calculated result. Such a large disagreement is mainly due to the variation of the CMRR when the voltage difference between the inputs becomes large. As the transistor enters triode region because of a large output swing, a smaller effective output impedance results in a smaller differential gain. Meanwhile, the asymmetrical transconductance between the input transistor pair causes a larger common-mode gain. Since the adopted diff-amp experiences a rail-to-rail variation during the clock receive process, it is inaccurate to estimate the jitter caused by CMI in a specific biasing point. On the other hand, the CMRR of the diff-amp is varying with the input voltage as the simulated result of Fig. 4 shows. To simulate the CMRR we use an AC analysis setting both inputs at a mid-supply voltage and applying a constant differential voltage to the inputs. With the differential input voltage changing from 20 to 140 mV, the CMRR varies from 40 to 10 dB, dropping significantly with a large differential input as it induces a smaller differential gain and a larger common-mode gain.

B. Converting CMI to Jitter With ISF

From the previous analysis, it can be concluded that the conventional CMRR study cannot accurately estimate the jitter caused by the CMI. As the CMRR of the CRCs varies in time due to the large input swing, it can be inferred that it would be difficult to quantify the jitter caused by the CMI with LTI modeling methods. Alternatively, the CMI jitter can be analyzed by a large signal analysis method similar to a VCO [13], with the operations of the transistor divided into different regions. While for the CMI and noise, which have a relative small signal amplitude when compared with the clock, the linear characteristic is maintained during the clock propagation. Therefore, it can be still considered as a linear time-varying system. Compared with the LTI modeling and large signal analysis [13], the LTV analysis is a simple, insightful and accurate method, when the CMI is small compared to the input clock signal and this is true in all practical applications.

Basically, ISF is a periodic function with 2π characteristic of a linear time-variant (LTV) system. Hence, once both ISF and CMI are known, the deterministic jitter can be estimated accurately by the integral of the CMI and ISF. The ISF can be obtained either by simulations or calculations [12], and we adopt here the former. In the simulation setup, a small common-mode impulse in various phases is injected to the differential clock input and the jitter is measured at the mid supply point. The ISF can be calculated as:

$$ISF(\omega_0\tau) = \frac{\Delta t}{V_{inj}(\tau)\cdot t_{inj}} \tag{3}$$

where Δt is the timing error at the crossing point caused by the injected impulse, ω_o is the angular frequency of the clock, τ is the time when the impulse is injected, V_{inj} is the amplitude of the impulse and t_{inj} is the impulse width. Fig. 5 plots the simulated ISF curves for the differential amplifier and the inverter chain (Fig. 3 (a) and (b)). Once we obtain the ISF of the CMI, the deterministic jitter due to CMI can be given by,

$$jitter_{CMI} = \int_0^{t_{edge}} ISF(\omega_0\tau)CMI(\tau)d\tau \tag{4}$$

$$jitter_{CMI,rms} \approx ISF_{int}CMI_{rms} \tag{5}$$

where, $jitter_{CMI}$ is the CMI jitter in one transition interval, t_{edge} is the clock transition time for rising or falling edge of the output clock, $CMI(\tau)$ is the common-mode interference, ISF_{int} is the integral of the ISF and CMI_{rms} is the rms value of the CMI. The jitter of the clock signal due to CMI in one transition interval can be computed with (4). Besides, when the period of CMI is much larger than the non-zero interval of ISF, the rms jitter can be estimated as (5). According to (4), the jitter of the sampling clock is the integral of the product of ISF and CMI functions. It can be noticed in Fig. 5 (a) that the ISF integrated value of the inverter is much larger than that of the diff-amp, resulting in a larger rms jitter caused by CMI. From the ISF plot, it can be also found that only the CMI in the transition region of the clock signal can cause jitter where the clock signal shows a zero-sensitivity to the CMI before and after the transition region (Fig. 5(b)). Noted that the time span of the transition region is equal to t_{edge} in (4).

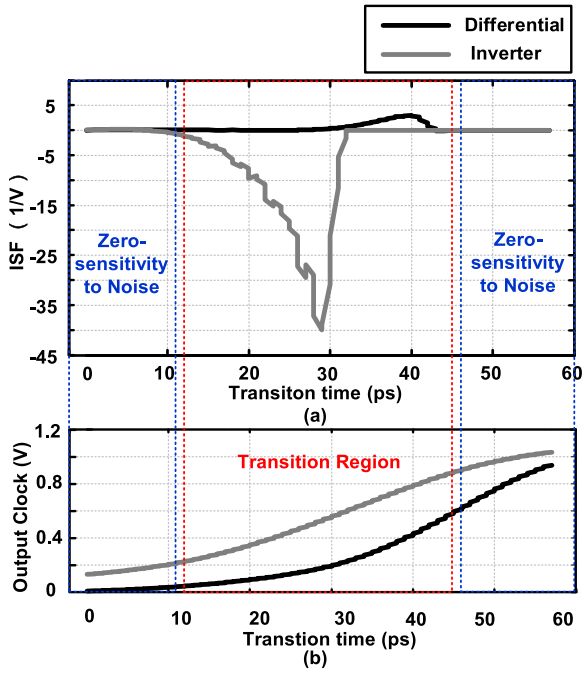

Fig. 5. (a) ISF and (b) output of diff-amp and single inverter as CRC.

This happens because the output node of either the differential amplifier or the inverter is in a very low impedance when its voltage is near supply or ground, thus noise cannot affect the crossing point of the clock. On the other hand, the output node is at a high impedance when the output clock signal is in the transition region, such that the noise can accumulate causing subsequently the jitter.

C. Verification of ISF Through Simulation

In order to verify the accuracy of the ISF for jitter estimation due to the CMI, we compare the calculated and simulated jitter for a traditional differential amplifier and inverter, based on common-mode interferences with various peak-to-peak amplitudes (2-16 mV) and frequencies (10-200 MHz). As Fig. 6 (a) and (b) show, the jitter caused by CMI is independent of the interference frequency but linearly proportional to its amplitude. The estimated jitter results according to (5) agree closely with the simulated where the small differences are due to the simulation accuracy constraint.

D. Comparisons of CMI Jitter Between the Inverter and the Differential Amplifier

With only an inverter between the off-chip and on-chip interface, any off-chip noise coupled to the sinusoidal clock signal directly causes jitter to the sampling clock without any suppression. A CMI with 2 $mV_{p\text{-}p}$ can introduce jitter around 200 fs_{rms} according to the simulated results of Fig. 6. For a diff-amp based CRC, the environmental noise is coupled to both differential clock signals as a common-mode noise, such that the noise can be partially cancelled. The differential amplifier uses its own common-mode rejection nature to suppress the CMI jitter by lowering its sensitivity to interferences, which can be considered as a static method. However, such suppression method requires a static charging and discharging

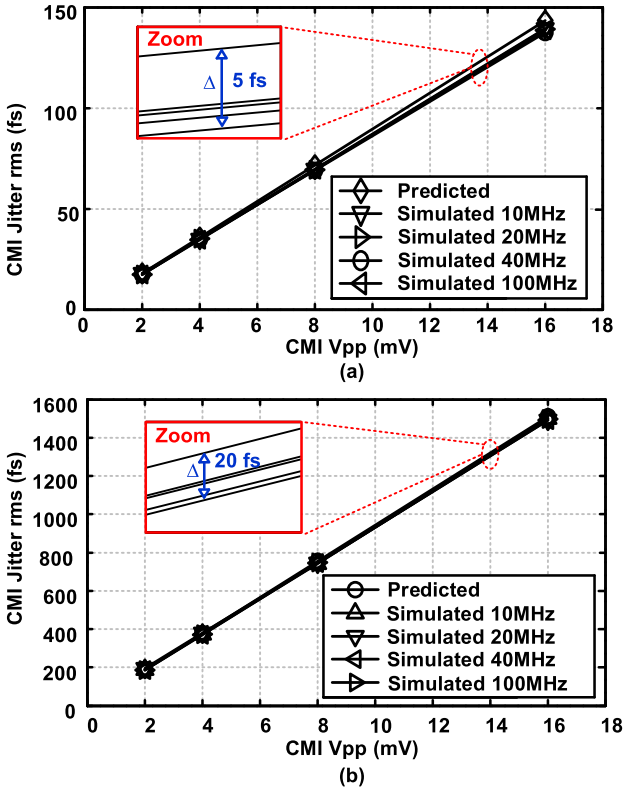

Fig. 6. Predicted jitter and simulated jitter for (a) diff-amp and (b) inverter.

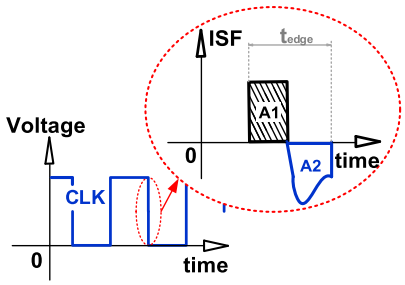

Fig. 7. High CMI suppression ISF.

current which degrades the random jitter performance which will be described in detail in Section IV. Such a characteristic implies a design tradeoff between the deterministic and random jitter in the above clock receiver topologies. In the following section, we propose a clock receiver circuit which can relieve such a tradeoff.

III. Proposed Clock Receiver With Strong CMI Rejection Circuit Based on ISF Analysis

A. Proposed Clock Receiver Circuit Based on ISF

Previously, the diff-amp based CRC has shown a strong CMI suppression by keeping the amplitude of the ISF small. However, it can be recognized from (4) that this is not the only valid approach. The CMI rejection indeed relies on the integral rather than the amplitude of the ISF. Assuming a circuit can obtain an ISF, as shown in Fig. 7, during the clock transition time (t_{edge}), although the amplitude of the ISF is large, the circuit can still possess a strong CMI rejection, as its integral

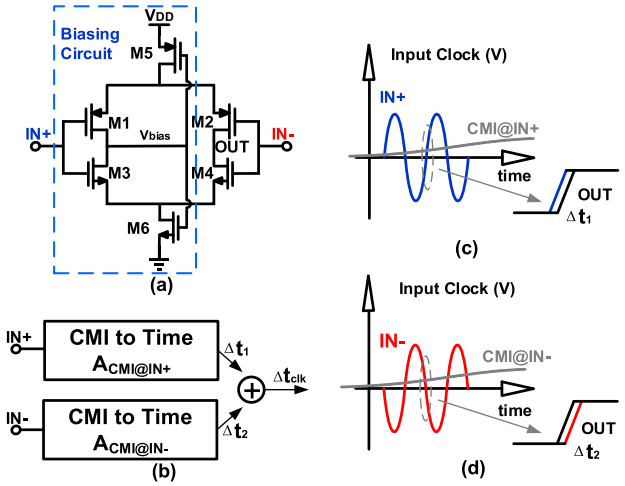

Fig. 8. Proposed CRC based on self-bias amplifier and circuit operations.

is small. Theoretically, the jitter caused by CMI can be zero when the shaded areas A1 and A2 are identical.

In order to realize a CRC with an ISF similar to Fig.7, the circuit has to operate differentially and show a complementary sensitivity to the CMI over the clock transition. The self-bias amplifier, shown in Fig. 8 (a), can satisfy both requirements mentioned above, and we will discuss the circuit operations next in Section B. It has been initially proposed in [14] to enhance input common-mode range and gain. Fig. 9 plots the ISFs of both the self-bias and the diff-amp based CRC for comparison. With the self-bias amplifier as CRC, a complementary ISF can be obtained. Although the ISF of the self-bias amplifier has a larger magnitude than the diff-amp, its integral is smaller.

For the self-bias amplifier, the ISF is complementary within a very short interval, and it will cancel out all the noise from the low to high frequency except the period of the noise close to the transition interval of the ISF. The effective interval of the ISF for different types of amplifier is only around 20 ps_{rms} according to simulations, which is dependent on the transition time of the rising and falling edge of the output clock. When the rising/falling time of the output clock is shorter, the transition region shrinks accordingly, contributing to achieve a smaller CMI jitter as the integral time t_{edge} is reduced in (4). While the CMI jitter in the inverter CRC decreases proportionally with the input slope, the diff-amp and self-bias CRCs do not possess such a characteristic as they have an inherenent CMI rejection.

B. CMI Rejection of Self-Bias Amplifier Based CRC

The self-bias amplifier (Fig.8 (a)) possesses the Class B properties of the CMOS inverter since there is an embedded inverter which consists of M2 and M4. Compared to an inverter, there is a biasing circuitry composed by M1, M3, M5 and M6. The output is an inverted and amplified version of IN−, and its transition current depends on the biasing circuits. The operation of the self-bias CRC can be described as follows. When the input clock signal IN+ is rising, M1 and M3 act as a push-pull amplifier, amplifying its input IN+ and CMI with reversed polarity at node V_{bias}, which

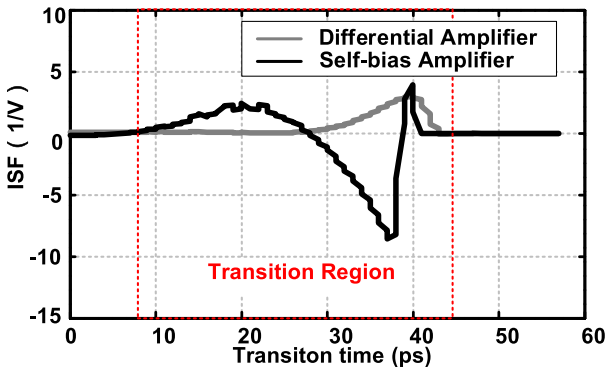

Fig. 9. ISF of diff-amp and self-bias amplifier.

also serves as an adaptive biasing voltage for the current sourcing and sinking transistors M5 and M6, forming another push-pull amplifier, therefore the CMI associated with IN+ is reversed twice at the output (OUT). On the other hand, the CMI associated with IN− is only amplified and reversed once at OUT by M2 and M4. Then, the CMI from IN+ and IN− can cause an opposite time drift Δt at OUT, resulting in a CMI jitter reduction. As shown in Fig.8 (b), the conversion gain of CMI-to-time drift from IN+ and IN− to OUT are denoted as $A_{CMI@IN+}$ and $A_{CMI@IN-}$, respectively, where they are not inherently identical due to its asymmetrical circuit operations. On the other hand, it is not necessary to be symmetric as the CMI rejection only relies on the integral of the ISF in our proposed CRC. While for the CMI rejection optimization, $A_{CMI@IN+}$ and $A_{CMI@IN-}$ should be designed as close as possible, to cancel out both Δt_1 and Δt_2, which can be accomplished by the ISF manipulation techniques introduced next.

For instance in Fig. 8 (c) and (d), a positive CMI is coupled to the differential input pair when IN+ is rising and IN− is falling. Such CMI can be considered as constant in a short transition interval. The CMI associated with IN+ decreases the biasing voltage of M5 and M6, which leads to an earlier rising transition at the output node (OUT) when compared with its ideal value. Such time drift caused by CMI at two input nodes IN+ and IN− results in a leading time error Δt_1 and a lagging time error Δt_2 at the output of the CRC, respectively. The two errors can be partially canceled out, thereby the CMI jitter can be reduced.

C. Optimization of CMI Rejection by ISF Manipulation

An approximate zero mean ISF of the proposed CRC is obtained by controlling the conversion gain $A_{CMI@IN+}$ and $A_{CMI@IN-}$, which is known as the ISF manipulation technique similar to what [15] and [16] present for VCO designs. In the proposed self-bias CRC ISF's integral can be minimized by manipulating the positive and negative areas of the ISF in the transition region in Fig.7. When the CMI-to-time conversion gain associated with IN+ ($A_{CMI@IN+}$) increases, the positive area of the ISF will also grow, vice-versa for negative area with $A_{CMI@IN-}$. Fig. 10 shows the ISFs of the self-bias CRC with three different sizes of M1 and M3 in order to demonstrate the ISF manipulation. Compared to the ISF_1, where all the devices (M1, M2, M3, M4) are sized with identical W and L,

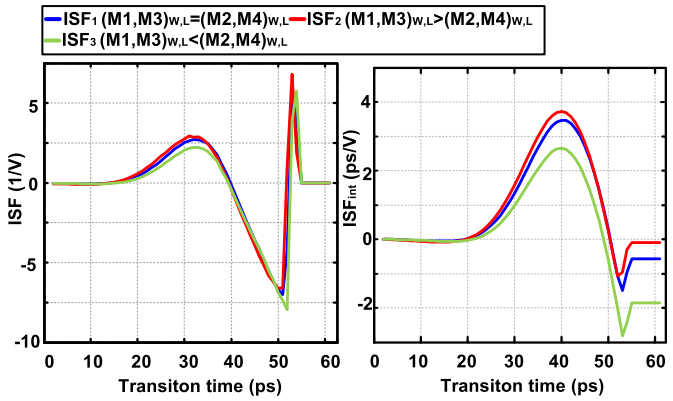

Fig. 10. ISF manipulation of minimizing integral area.

ISF_2 obtains a larger positive area by enhancing both W and L of the device M1 and M3, whose transconductance is maintained with increased impedance for larger L, resulting in a larger $A_{CMI@IN+}$. Similarly, shrinking the W and L of M1 and M3 can enlarge the negative area as it is the case of ISF_3. The integrals of ISF_1, ISF_2, and ISF_3 are 5:1:15, where the ISF manipulation can effectively change the ISF integral. Hence, the approximate zero mean ISF can be obtained by ISF manipulation.

D. Simulation and Comparison

When the CMI period is much larger than the non-zero interval of the ISF, the integral of the ISF determines the CMI jitter according to (5). With the simulated ISF in Fig. 5 and Fig. 9, their integrals can be calculated by integrating ISF over the transition region, and it indicates that the proposed self-bias amplifier based CRC is around 7 dB and 27 dB better than diff-amp and inverter, respectively, in terms of CMI rejection.

Besides, the ISF for different CRCs can vary with process. Fig. 11 shows 200-run Monte-Carlo simulations with both global and local variations to demonstrate the process influence. In the simulation, a CMI of a 20.1 MHz and 20 $mV_{p\text{-}p}$ sinusoidal signal is injected into the CRCs. The mean values are 74 and 173 fs_{rms} and the standard deviations (SD) are 29 and 19 fs_{rms} for the self-bias amplifier and the diff-amp, respectively. For the proposed CRC, the conversion gains of the CMI from both inputs to the time drift at the CRCs' output ($A_{CMI@IN+}$ and $A_{CMI@IN-}$) vary under process variations. As mentioned in Section III-B, the proposed CRC possesses an asymmetrical signal path from IN+ and IN− to the output (OUT). The total gain from IN+ to OUT is composed of two stages (M1 and M3, M5 and M6), while the gain from IN− is only obtained from a single stage (M2 and M4). Due to such a characteristic, the process variations cause different gain variations and result in different integrals of ISF which affect the jitter performance of the proposed CRC. The results verify the effectiveness of the CMI cancellation mechanism introduced previously and the proposed CRC can achieve better CMI rejection than the traditional differential amplifier over process variations.

IV. Analysis of Random Jitter

The detailed analysis of random jitter of an inverter chain can be found in [9]. Random jitter analysis of the differential

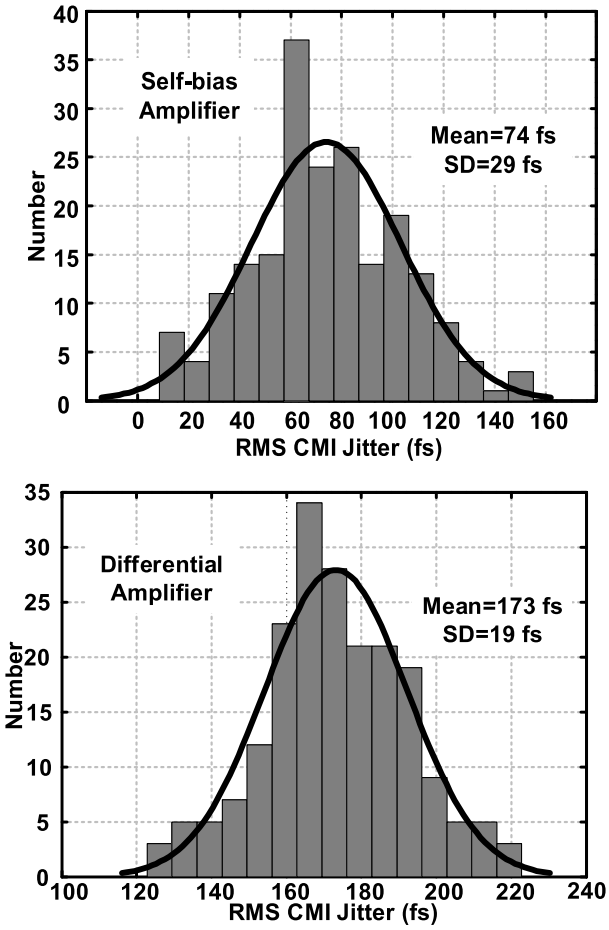

Fig. 11. RMS CMI jitter histogram from Monte-Carlo simulations.

amplifier is similar to the frequency divider in [17]. In this section, we present a qualitative analysis which shows that a much larger power is required to achieve the same random jitter in the diff-amp based CRC when comparing it with the inverter-chain and the self-bias amplifier topologies.

A. Introduction of Random Jitter

A clock signal propagating over active circuit devices can be contaminated by noise and leads to jitter. Such jitter is random and mainly caused by the thermal and flicker noise from all devices in the clock path. According to the definition in [18], the random jitter can be computed by (6),

$$Jitter_{\text{rms}} = \frac{v_{n,rms}}{Slope} \tag{6}$$

where $v_{n,rms}$ is the rms value of the noise voltage sampled at the crossing point and *Slope* is the slope at the crossing point. From (6), we can conclude that a smaller random jitter can be achieved by lowering the magnitude of the noise voltage or increasing the slope of the clock signal. However, it requires a larger power consumption for a steeper slope [9], and its efficiency can be degraded by the self-load of the devices too.

B. Qualitative Analysis of Random Jitter of CRCs

From the previous analysis, a static current is required in the diff-amp based CRC in order to achieve a good CMI rejection. However, such current not only causes a large power

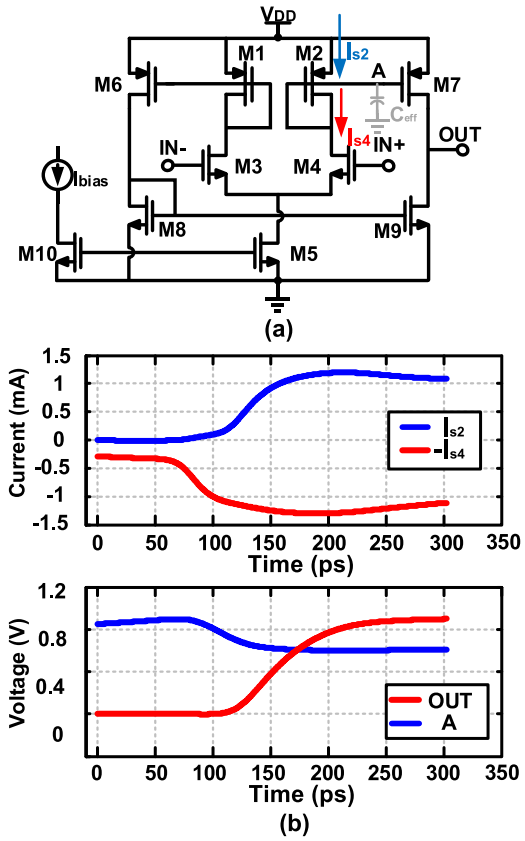

Fig. 12. (a) Redraw of diff-amp with current flow (b) plot of transient signal.

consumption but also introduces a large random jitter which can be explained next. Without loss of generality, assuming that the output voltage is switching from low to high at the output (OUT) of the diff-amp we can draw Fig.12 (a). During the switching, the gate voltage of M7 (node A) is pull-down. However, the static charging current I_{s2} slows down its transition slope. As shown in Fig.12 (b), when the signal at A is falling, M2 is on and I_{s2} is charging the effective capacitance at A, resulting in a slower transition slope. The transition slope can be computed as (7),

$$Slope_{\mathrm{A}} = \frac{-I_{s4} + I_{s2}}{C_{eff}} \tag{7}$$

where $Is2$ and $Is4$ are the current through M2 and M4 respectively and C_{eff} is the effective capacitance at A. Meanwhile a noise current is also introduced by thermal noise and flicker noise from M2. According to (6), the static current of the differential amplifier slows down the transition slope and introduces more noise, resulting in larger random jitter at A that will propagate to the output (OUT), because the output stage is driven by the signal at A.

In terms of an inverter chain (Fig. 3 (b)), assuming the output node is switching from low to high, the input clock signal shuts off the PMOS (M1), when it crosses the threshold voltage of M1, and negligible current is sourced from M1. Hence, the transition slope does not slow down. Moreover, there is negligible thermal noise current from M1 during the switching. Consequently, the inverter can achieve a much smaller random jitter than the diff-amp when their power

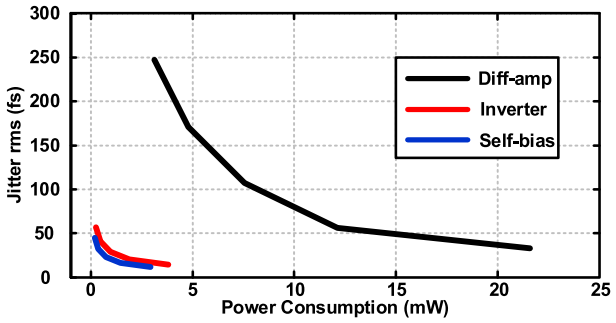

Fig. 13. Power consumption and jitter in various CRCs.

consumptions are the same. Similarly, for the self-bias amplifier (Fig. 8 (a)), when the output node is switching from low to high, IN+ is at a high voltage level, which shuts off M1 and M6 and turns on M5. During this period, the self-bias amplifier react as an inverter; therefore, it can achieve a similar random jitter performance as the inverter.

Nevertheless, the inverter-based CRC suffers from the deterministic jitter caused by CMI, which aggravates the overall jitter performance. On the other hand, the self-bias amplifier can achieve a good CMI suppression consuming no static current, and it can obtain a good power efficiency with low overall jitter when acting as a CRC.

C. Simulation Results for Power and Jitter in Three Types of Clock Receiver Circuits

Based on the same simulation setup (power supply 1.2V) and differential input clock signal (1 GHz with 2.4 $V_{p\text{-}p}$) for the self-bias and diff-amp CRCs, and singled-end (1 GHz with 1.2 $V_{p\text{-}p}$) for the inverter CRC, we can compare the jitter performances of three types of CRCs. *SPECTRE* PSS+Pnoise simulations are performed in 65 nm CMOS to quantify the clock jitter of these three CRCs. The random jitter can be obtained under various power consumptions, with the variation of the bias voltage of the diff-amp, and the sizing of the inverter and the self-bias amp. The simulation results in Fig. 13 show that a lower jitter can be achieved by these three types of CRCs with a larger power consumption due to the faster switching slope. These results also comply with the analysis in [9], where the rms jitter is inversely proportional to the square root of the amplitude of the charging and discharging current. Based on this, the self-bias can achieve 30 fs_{rms} with 560 μW power consumption, and the inverter 45 fs_{rms} with 540 μW, while the differential amplifier consumes more than 13 mW to reach 50 fs_{rms}. Both inverter-based and self-bias amplifier based CRCs are able to attain a smaller random jitter and lower power consumption than the diff-amp. Such results also comply with our qualitative random jitter analysis. Besides, the self-bias has less supply bounce than the differential amplifier due to less current required for the same random jitter performance.

V. Measurement Setup, Results and Comparison

A. Measurement Setup for Jitter Sampling Clock Circuit

In order to verify the correctness of the proposed analysis and the effectiveness of the CRCs, we implemented the

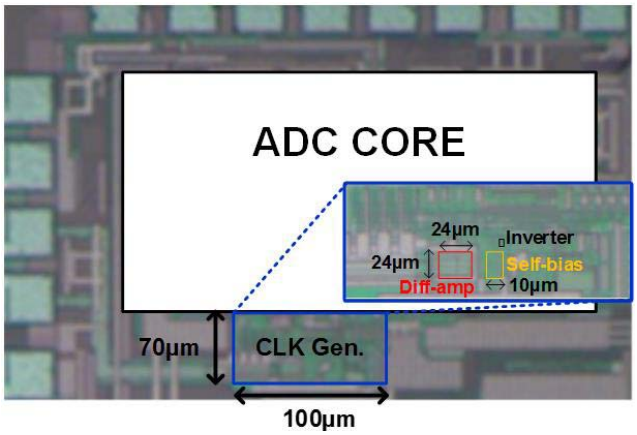

Fig. 14. Chip microphotograph.

above discussed three clock receiver topologies, including the inverter, the differential amplifier and the proposed self-bias amplifier, through the fabrication in 65 nm CMOS along with a 1 GS/s SAR type ADC, as illustrated by the microphotograph in Fig. 14. The areas of the CRCs are 24 μm×24 μm, 10 μm×24 μm and 3 μm×3 μm for the Diff-amp, the self-bias and the inverter, respectively.

The eye diagram can provide histogram information which is helpful in identifying the contribution of the deterministic and random jitter [19]. However, it is quite difficult to perform an eye diagram measurement with our target jitter performance ($\sim$130f_{ms}). With such low jitter, any extra circuits can induce significant additional noise which affects the measurement accuracy. Therefore, we adopted a different approach in our measurement which estimates the jitter of the sampling clock from the SNR of the ADC. When switching to different CRCs via an on-chip multiplexer we can obtain the jitter from each topology. The relationship between the jitter and SNR of ADCs has been well studied. Estimating the jitter of the sampling clock by measuring the SNR of ADCs with varying input signal frequencies is also a very reliable evaluation. This scheme is also less sensitive since it mostly relies on the ADC's digital output.

We measured a single channel ADC (with a similar architecture of [20]) under different input frequencies from 100 MHz to $\sim$6 GHz for different CRCs. It is worth noting that serious harmonic distortion is induced due to the limited bandwidth of the sampler circuit at high input frequency. However, we only measure the SNR for the jitter calculation which excludes the effect of the harmonic distortion; therefore, the results are still reliable. The harmonic distortions caused by the insufficient bandwidth in the sampler are not considered in the SNR measurement. It is also expected that the SNR of the ADC would be mainly limited by the clock jitter under a high frequency input; therefore, the amount of jitter in each CRC can be estimated by the SNR degradation trend across different input frequencies. Besides, we injected a sine-wave signal with different frequencies (200 KHz to 1 MHz) and amplitude (1 mV to 8 mV) to the common-mode node of the differential sampling clock source. By measuring the spur due to the common-mode injection from three clock receiver circuits at the ADC's output spectrum, we can verify the CMI rejection performance.

For a fair comparison of jitter performance, three CRCs use the same power supply, while the power consumption of each CRC cannot be measured separately. In order to obtain the power consumptions of different CRCs, the differential amplifier is turned off by pulling down the bias voltage of the tail current transistor. Hence the power of the diff-amp CRC can be measured by the difference between these two setups. Based on the power consumed by the differential amplifier, the power consumption of the self-bias and the inverter CRCs can be estimated by a ratio with the diff-amp CRC. The sampling clock is a differential input clock signal (1 GHz with 2.4 $V_{p\text{-}p}$) for the self-bias and diff-amp CRCs, and single-ended (1 GHz with 1.2 $V_{p\text{-}p}$) for the inverter CRC. The rising/falling time (10% to 90% of the clock signal) is around 296 ps.

B. Measurement Theory and Simulation Results

Based on the frequency scalability, the total noise of an SAR type ADC (n_{tot}^2) can be mainly categorized by: i) the noise independence of the input signal frequency, including KT/C noise from the sample and hold circuit, quantization noise and comparators noise ($n_{indep\_f}^2$), and ii) the noise square that proportionally increases with the input frequency mainly caused by the jitter of the sampling clock (n_{samp}^2), as given by (8),

$$n_{tot}^2 = \mathrm{n}_{samp}^2 + \mathrm{n}_{indep\_f}^2 \tag{8}$$

The noise power caused by the jitter of the sampling clock in the ADC can be calculated as (9),

$$\mathrm{n}_{samp}^2 = \left(2\pi f_{in} \frac{\mathrm{A}_{input}}{\sqrt{2}} \sigma_{samp}\right)^2 \tag{9}$$

where, f_{in} is the input frequency, A_{input} is the input signal amplitude and σ_{samp} is the rms jitter of the sampling clock.

The total rms jitter of the sampling clock is caused by the CMI (σ_{CMI}^2) and supply interference (σ_{supply}^2), the jitter from the input signal and clock generator ($\sigma_{sig\_gen}^2$), and also from the sampling clock buffers ($\sigma_{clk\_buf}^2$) and the CRC (σ_{CRC}^2), which can be obtained as,

$$\sigma_{\mathrm{samp}} = \sqrt{\sigma_{sig\_gen}^2 + \sigma_{clk\_buf}^2 + \sigma_{CRC}^2 + \sigma_{CMI}^2 + \sigma_{supply}^2} \tag{10}$$

According to the simulations, $\sigma_{CRC} =\sim 50$ $\mathrm{fs_{rms}}$, $\sigma_{clk\_buf} = \sim 75$ $\mathrm{fs_{rms}}$, $\sigma_{sig\_gen} =\sim 70$ $\mathrm{fs_{rms}}$, while σ_{supply} is negligible due to a good isolation and a well decoupled network. On the other hand, σ_{CMI} cannot be accurately obtained through simulation because of its dependence on the PCB ground bouncing condition. The calculated total clock jitter is around 120 $\mathrm{fs_{rms}}$ based on the above simulation results (without CMI). The final SNR of the ADC can be expressed by,

$$\mathrm{SNR}_{ADC} = 10\log_{10}\left(\frac{\frac{1}{2}\cdot A_{input}^2}{n_{tot}^2}\right) \tag{11}$$

where A_{input} is the input amplitude, and n_{tot}^2 is the total noise power. When the input frequency is low, the SNR is

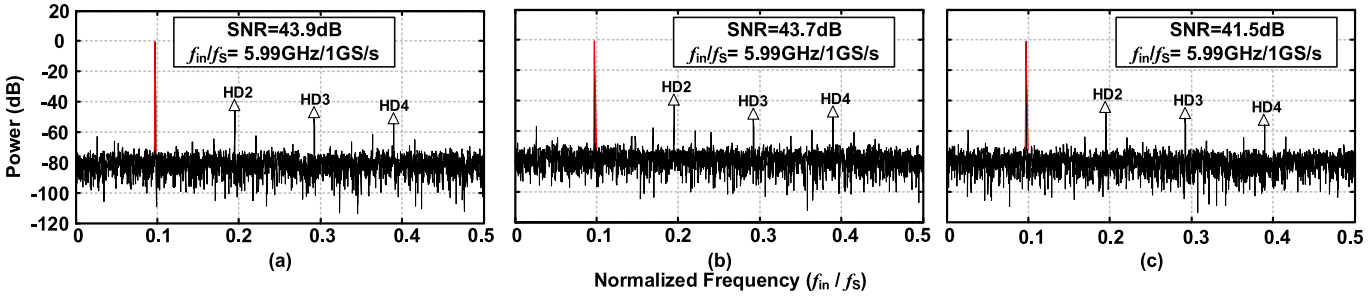

Fig. 15. FFT plots of three types of CRCs with 5.99 GHz input frequency: (a) Self-bias (b) Diff-amp (c) Inverter.

dominated by $n^2_{indep\_f}$ as n^2_{samp} is small. Once the input frequency increases, the SNR drops as n^2_{samp} increases. To compensate the roll-offs due to the limited bandwidth of the sampler, we increased the input amplitude to normalize the ADC's output range at each input frequency. At high input frequencies, the output-code-swing drops significantly under a full-swing ADC input amplitude which is determined at a low frequency. By compensating the actual roll-off of the sampler with increased input amplitude, we manage to keep the output-code-swing constant in each SNR measurement under different input frequencies. With the measured SNR, the clock jitter can be estimated from (8) ∼ (11). For the CMI rejection measurements, when we inject a sine-wave interference at the common-mode node of the differential sampling clock source, a spur in the FFT spectrum will appear. The ratio of the signal to the spur caused by the CMI is measured accounting for the CMI rejection of the CRCs.

C. Measurement Results

Fig 15 illustrates the measured FFT plots of the ADC with three types of CRCs at an input frequency (f_{in}) around 6 GHz. The SNRs are 43.9 dB, 43.7 dB and 41.5 dB for self-bias, diff-amp inverter CRC, respectively. Since the clock jitter only raises the noise floor of the spectrum, the SNRs do not include harmonic distortion from 2 (HD2) to 10 (HD10). Fig.16 presents the measured SNRs with input signal frequency varying from 100 MHz to 6 GHz. The SNRs of the three CRCs drop with the increase of the input signal frequency. The SNR is dominated by $n^2_{indep\_f}$ at low frequency. With an input frequency of 100 MHz and amplitude A_{input} of 250 mV, the measured SNR is close to 49 dB for the three types of CRCs. Minor differences in the SNRs, at the low frequency input, among the CRCs are caused by the variations of the measurement conditions, which do not reflect the jitter performance of the proposed CRC as the SNR is dominated by other noise sources from the ADC.

The total noise power n^2_{tot} can be calculated with (11) which is equal to the $n^2_{indep\_f}$ (as n^2_{samp} is negligible with low input frequency). When the input frequency raises to around 6 GHz, n^2_{samp} contributes with significant noise power and $n^2_{indep\_f}$ remains the same. Hence, n^2_{samp} can be calculated with (8). Table I depicts the calculated noise power based on the measured SNR of the ADC.

According to (9), the calculated jitter is around 135 fs_{rms} for CRCs based on the diff-amp and the self-bias amplifier.

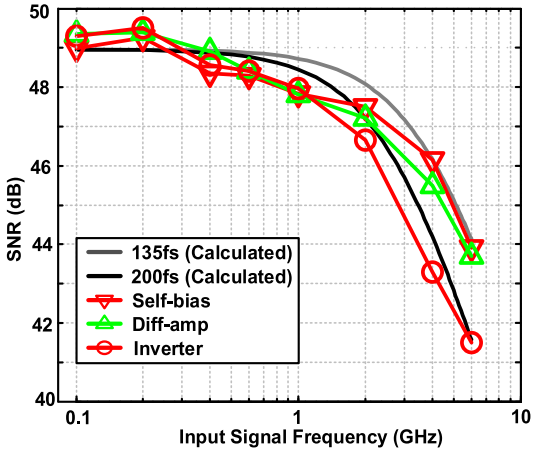

Fig. 16. SNR measurements for 3 types of CRCs.

TABLE I
NOISE POWER CALCULATION RESULTS

Input Frequency	Measured SNR	n^2_{tot}	$n^2_{indep\_f}$	n^2_{samp}
100 MHz	~49 dB	0.39 μV^2	0.39 μV^2	~177 pV^2
6 GHz	~44 dB	1.24 μV^2	0.39 μV^2	0.85μV^2

Similarly, the calculated jitter is around 200 fs_{rms} for the CRC based on the inverter. The poor CMI rejection of the inverter CRC is verified by the experiment with CMI injection. This setup is reliable since three CRCs are designed with the same random jitter performance and the measurement conditions are exactly the same, including the input signal of the ADC, the sampling clock source and the supply decoupling. Therefore, we can conclude that the large disagreements between the simulated and the measured jitter for the inverter CRC are caused by the CMI. The CMI results in 66% larger jitter than the simulation for the inverter CRC, eventually leading to a much larger measured jitter when comparing it with other two CRCs. Besides, with over 20 dB better CMI rejection than that of the inverter CRC, the CMI only causes negligible effect (at most 1%) on the jitter performance of the diff-amp and the self-bias CRCs.

A common-mode sine-wave with different amplitudes (from 1 - 8 mV), and various frequencies, including 200 KHz, 600 KHz, 1 MHz, is injected to the differential sampling clock sources and the spur caused by the CMI is measured.

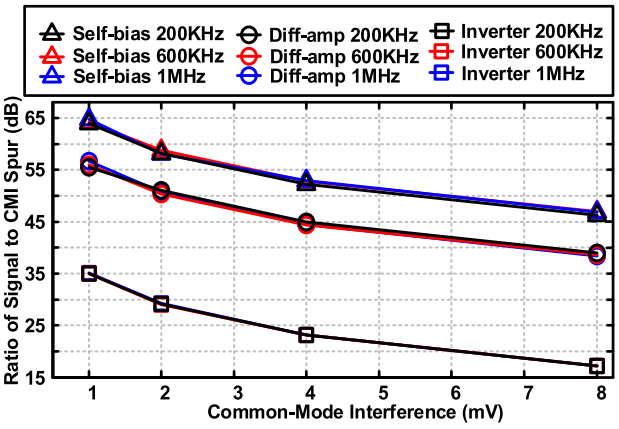

Fig. 17. CMI rejection measurements for 3 types of CRCs.

In Fig. 17, the measured signal to CMI spur ratio for the 3 types of CRCs shows that the ratio is independent of the CMI frequency, which complies with the presented ISF analysis. Besides, the signal to CMI spur ratio decreases by 6 dB when the amplitude of the CMI is doubled during the measurement. Hence the amplitude of the spur caused by CMI is linearly proportional to the amplitude of the CMI, which also agrees with our analysis. The clock receiver of the self-bias amplifier shows around 8 dB and 28 dB better CMI rejection than those of the differential amplifier and the inverter, respectively, under the same measurement conditions. The measurement results comply with the ISF simulation results with approximately 1 dB error in the CMI rejection.

The measured power consumption is around 10.5 mW for the diff-amp CRC, which is only 5% different from the simulation (11 mW). The estimated power consumptions are 620 μW and 240 μW for the self-bias and the inverter CRCs, respectively.

VI. Conclusions

This paper presented a numerical method to precisely characterize the jitter caused by CMI. The measurement results comply with the predicted CMI suppression with only around 1 dB disagreement. Inspired by the proposed analysis, a low jitter CRC topology was proposed with efficiency verified by the measurement of a 1 GS/s SAR-type ADC. The proposed clock receiver circuit shows an 8 dB better CMI suppression and a 20-fold reduction in power consumption, when compared with the diff-amp CRC, while achieving a sub-50 fs_{rms} jitter.

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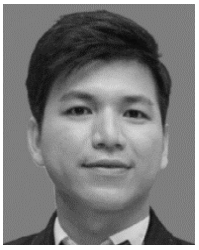

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In 2001, he co-founded Chipidea Microelectronics, Ltd., Macau, as the Engineering Director, and the corporate VP-IP Operations Asia Pacific for devoting in advanced AMS Semiconductor IP product development since 2003. The company was acquired in 2009 by the world leading EDA & IP provider Synopsys Macau Ltd. He is also the Corporate Senior Analog and Mixed-Signal Design Manager and the Site General Manager.

He has authored or co-authored over 140 publications, and four books in Springer and China Science Press in the area of VHF SC filters, analog baseband for multi-standard wireless transceivers, and very high-speed TI ADCs. He co-holds ten U.S. patents.

Dr. U received ~30 research and academic/teaching awards. He is a co-recipient of the 2014 ESSCIRC Best Paper Award. He is also the advisor for ~30 various international student paper award recipients, such as SSCS Pre-Doc Achievement Award, the ISSCC Silk-Road Award, the A-SSCC Student Design Contest, the IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, and PRIME. He received the 2012 IEEE SSCS Outstanding Chapter Award, as the Macau founding Chairman. First time from Macau, he received the Science and Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010 and the State S&T Progress Award in 2011. He also received the Macau S&T Invention and Progress Award in 2012 and 2014. In recognition of his contribution in academic research and industrial development, he received the Honorary Title of Value by the Macau SAR Government in 2010. He was also elected as the Scientific Chinese of the Year 2012.

He is currently the Founding Chairman of the IEEE SSCS and the Chairman of the CAS/COMM Macau chapter. He is appointed as a member of the S&T Commission of China Ministry of Education. He was the IEEE SSCS Distinguished Lecturer (2014–2015) and a A-SSCC 2013 Tutorial Speaker. He has also been with technical review committee of various IEEE journals, such as JSSC, TCAS, and TVLSI. He was the Program Committee/Chair of the IEEJ AVLSIWS, the IEEE APCCAS, ICICS, PRIMEAsia, and the IEEE ASP-DAC'16. He is currently a TPC of ISSCC, A-SSCC, and RFIT, an Analog Sub-Committee Chair of VLSI-DAT, and an Editorial Board Member of the Journal AICSP.

Rui P. Martins (M'88–SM'99–F'08), born in April 30, 1957, received the Bachelor (5-years), the Masters, and the Ph.D. degrees, as well as the *Habilitation* for Full-Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively. He has been with the Department of Electrical and Computer Engineering (DECE) / IST, TU of Lisbon, since October 1980.

Since 1992, he has been on leave from IST, TU of Lisbon (now University of Lisbon since 2013), and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he is currently a Chair-Professor since August 2013. In FST he was the Dean of the Faculty from 1994 to 1997 and he has been Vice-Rector of the University of Macau since 1997. From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as Vice-Rector (Research) until August 31, 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and has supervised (or co-supervised) 40 theses, Ph.D. (19) and Masters (21). Co-authored: 6 books and 12 book chapters; 25 Patents, USA (23) & Taiwan (2); 400 papers, in scientific journals (126) and in conference proceedings (274); as well as other 62 academic works, in a total of 505 publications. He was a co-founder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001/2002, and created in 2003 the ANALOG AND MIXED-SIGNAL VLSI RESEARCH LABORATORY of UM, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director.

Prof. Rui Martins is an *IEEE Fellow*, was the Founding Chairman of IEEE Macau Section (2003-2005), and IEEE Macau Joint-Chapter on Circuits and Systems (CAS) / Communications (COM) (2005-2008) [*2009 World Chapter of the Year* of *IEEE CASS*]. He was the General Chair of 2008 IEEE Asia-Pacific Conference on CAS - *APCCAS'2008*, and was the Vice-President for the Region 10 (Asia, Australia and the Pacific) of *IEEE CAS Society* (2009-2011). Since then, he was Vice-President (World) Regional Activities and Membership of IEEE CAS Society (2012-2013), and Associate Editor of IEEE TRANSACTIONS ON CAS II: Express Briefs (2010-2013), nominated *Best Associate Editor of T-CAS II* for 2012 to 2013. Plus, he was a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS) - Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference - *ASP-DAC'2016* and received the *IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award 2016*. He was a Nominations Committee Member of *IEEE CASS* (2016) and is currently the Chair of the *IEEE CASS* Fellow Evaluation Committee (Class 2018). He is now the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference - ASP-DAC'2016. He was the recipient of 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In July 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.