15-nW Biopotential LPFs in 0.35-μm CMOS Using Subthreshold-Source-Follower Biquads With and Without Gain Compensation

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***Abstract*—Most biopotential readout front-ends rely on the g_m-C lowpass filter (LPF) for forefront signal conditioning. A small g_m realizes a large time constant ($\tau = C/g_m$) suitable for ultra-low-cutoff filtering, saving both power and area. Yet, the noise and linearity can be compromised, given that each g_m cell can involve one or several noisy and nonlinear V-I conversions originated from the active devices. This paper proposes the subthreshold-source-follower (SSF) Biquad as a prospective alternative. It features: 1) a very small number of active devices reducing the noise and nonlinearity footsteps; 2) No explicit feedback in differential implementation, and 3) extension of filter order by cascading. This paper presents an in-depth treatment of SSF Biquad in the nW-power regime, analyzing its power and area tradeoffs with gain, linearity and noise. A gain-compensation (GC) scheme addressing the gain-loss problem of NMOS-based SSF Biquad due to the body effect is also proposed. Two 100-Hz 4th-order Butterworth LPFs using the SSF Biquads with and without GC were fabricated in 0.35-μm CMOS. Measurement results show that the non-GC (GC) LPF can achieve a DC gain of -3.7 dB (0 dB), an input-referred noise of 36 $\mu\mathrm{V_{rms}}$ (29 $\mu\mathrm{V_{rms}}$), a HD3@60 Hz of -55.2 dB (-60.7 dB) and a die size of 0.11 $\mathrm{mm^2}$ (0.08 $\mathrm{mm^2}$). Both LPFs draw 15 nW at 3 V. The achieved figure-of-merits (FoMs) are favorably comparable with the state-of-the-art.**

***Index Terms*—Biomedical, biopotential, body effect, CMOS, gain compensation, harmonic distortion, lowpass filter, MOSFET, source follower, subthreshold, time constant, transconductor.**

I. Introduction

EXTREMELY-LOW-POWER analog circuits continue to play a key role in wearable or implantable biomedical devices to achieve maximum battery life [1], or to become completely autonomous via energy harvesting [2]. A number of nW-class analog circuits have been reported, such as the operational amplifier [3], the power management unit [4], the sigma-delta modulator [5], the energy harvesting unit [6], the sensor interface [7] and the voltage [8]. They, in conjunction, exhibit high potential for bringing down the power consumption of emerging bioelectronics. However, existing biopotential acquisition systems still consume power in the range of tens to hundreds of μW [9], [10].

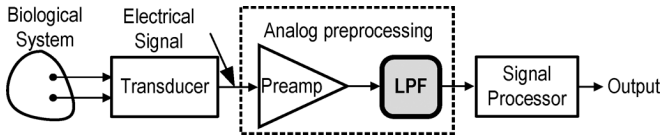

Fig. 1. Block diagram of a general purpose biopotential signal acquisition system.

This work focuses on the nW-class lowpass filter (LPF) in biopotential acquisition systems (Fig. 1), which should be able to handle different bio-signals such as ECG, EEG and ECoG (typically from 0.1–100 Hz). A LPF with a bandwidth from a few Hz to hundreds of Hz has been widely adopted for signal conditioning [11], and a high dynamic range (DR) is essential to enhance the signal resolution. Given the linearity specification, the power and area should be optimized with the $\mathrm{DR} = 20\log(\mathrm{v_{in.\,max}}/\mathrm{v_{n.rms}})$, where $\mathrm{v_{in.max}}$ is the maximum amplitude of the input signal; and $\mathrm{v_{n.rms}}$ is the input-referred noise (IRN) voltage. High linearity is also required to minimize the harmonic distortion (HD). Notice that as the LPF is not a standalone component but embedded in the signal processing chain, system level co-designing can be practiced to achieve system power optimization. As shown in Fig. 1, the LPF's driving capability can be evaluated by the input capacitance of the subsequent signal processor (typically headed by a data converter with [5]), which can be co-designed to achieve the required LPF performances.

Biopotential LPFs were widely based on the transconductor-capacitor (g_m-C) topology [12, ch. 13], [13]. A very small g_m (a few nA/V) yields a small bandwidth, being highly efficient in terms of power and area. The linearity and noise, however, are still moderate, as each g_m cell fundamentally involves one or several noisy and non-linear V-I and I-V conversions with MOSFETs. Hence, the reported g_m-C LPFs still consume significant power for improved DR and linearity: 10 μW for a 60-dB DR and -60-dB HD3 in [11], 11 μW for a 57-dB DR and a -61.5-dB HD3 in [14], and 0.453 μW for a 50-dB DR and -49-dB HD3 in [15].

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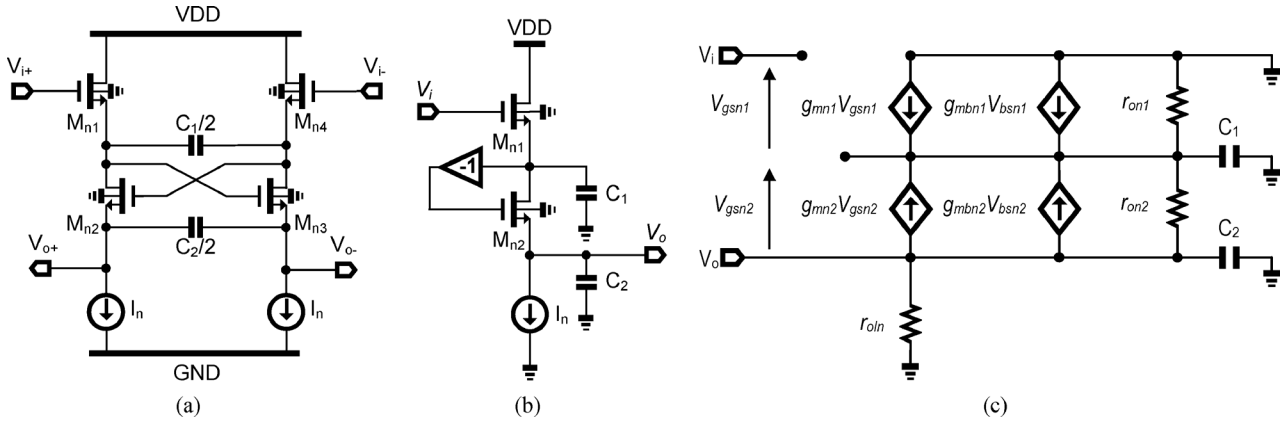

Fig. 2. (a) Non-GC NMOS-based SSF Biquad. (b) The single-ended equivalent circuit and its (c) small-signal equivalent circuit.

This paper proposes the subthreshold source follower (SSF) as a promising sub-cell for nW-class biopotential filtering. The theoretical details of SSF Uniquad are omitted here for brevity, and can be found in [16], [17]. Unlike the prior works that were mainly focused on the saturation-region operation of source followers (e.g., [18]), this paper reveals its properties under a nA bias current, and proposes a gain-compensation (GC) scheme to alleviate the gain-loss problem of NMOS-based SSF Biquad due to the body effect. The SSF Biquad can be extended to synthesize a high-order LPF via cascading. The theory and the effectiveness of the GC are validated by both simulations and measurements.

This paper is organized as follows: Section II studies the SSF Biquad and proposes a GC scheme to improve the SSF Biquad performance. Section III describes the experimental results. Section IV draws the conclusions.

II. SSF Biquad

A. NMOS-Based SSF Biquad

The schematic of a NMOS-based SSF Biquad is depicted in Fig. 2(a). It differentially consists of four MOSFETs ($M_{\rm n1}$-$M_{\rm n4}$), two current sources ($I_{\rm n}$) and two floating capacitors (C_1 and C_2). No common-mode feedback (CMFB) is entailed as each inner node can be well-defined, which will be explained in detail in Section II-B. To simplify the theoretical analysis, a single-ended equivalent, as shown in Fig. 2(b), is employed. Its operating principle shows that the positive feedback from the drain of $M_{\rm n2}$ to its gate realizes a complex pole, sharpening the stop-band attenuation. The loop gain after breaking the positive feedback at the gate of $M_{\rm n2}$ is inherently less than one (i.e., no instability issue).

1) I/O Transfer Characteristic: Fig. 2(c) shows the small-signal equivalent circuit of such a Biquad including the finite output resistance of all transistors and the body effect (for generality, no deep n-well is assumed). $g_{\rm mbn1,2}$ ($g_{\rm mn1,2}$) denotes the bulk (gate) transconductances of $M_{\rm n1}$ ($M_{\rm n2}$); $V_{\rm gsn1,2}$ ($V_{\rm bsn1,2}$) is the gate-source (bulk-source) voltage; $r_{\rm on1}$, $r_{\rm on2}$ and $r_{\rm oIn}$ are the output resistances of $M_{\rm n1}$, $M_{\rm n2}$ and the bias current source, respectively. Assuming that all transistors feature the same transconductance (i.e., g_m) given by $I_{\rm n}/nU_{\rm T}$, where n is the subthreshold slope factor (~ 1.5) and $U_{\rm T}$ is the thermal voltage ($\sim 26\,{\rm mV}$ at room temperature), and the effect of bulk-transconductances and finite output resistances are ignored, the Biquad shows the following characteristics [18]: DC gain $(A) = 1$; cutoff frequency $(\omega_0) = g_m/\sqrt{C_1C_2}$ and pole quality factor $(Q) = \sqrt{C_2/C_1}$. However, the body effect is not negligible for the case of long channel-length devices and subthreshold circuits design. With the bulk transconductance taken into account, the s-domain transfer function is given by

$$H(s) = \frac{-\frac{g_{\rm mn1}g_{\rm mn2}}{g_{\rm msn2}+g_{\rm msn2}}}{s^2\frac{C_1C_2}{g_{\rm msn1}g_{\rm msn2}} + s\frac{C_1g_{\rm msn2}+C_2(g_{\rm msn1}-g_{\rm mn2})}{g_{\rm msn1}g_{\rm msn2}} + 1} \quad (1)$$

where $g_{\rm msn1,2} = g_{\rm mn1,2} + g_{\rm mbn1,2}$ is the source transconductance; From (1) the new expressions of the DC gain, cutoff frequency and pole quality factor are dependent on the body effect

$$A = \frac{g_{\rm mn1}g_{\rm mn2}}{g_{\rm msn1}g_{\rm msn2}},$$
$$\omega_0 = 2\pi f_0 = \frac{\sqrt{g_{\rm msn1}g_{\rm msn2}}}{\sqrt{C_1C_2}},$$
$$Q = \frac{\sqrt{g_{\rm msn1}g_{\rm msn2}}\sqrt{C_1C_2}}{C_1g_{\rm msn2} + C_2(g_{\rm msn1} - g_{\rm mn2})}.$$

Obviously the DC gain is no longer unity and is given by $1/(1+\eta)^2$, where $\eta = g_{\rm mb}/g_m$ is the body effect trans-conductance ratio in the range of 0.2 to 0.5. Thus, the achievable DC gain should be between -3.2 to -7 dB in practice. This gain loss is critical as it will degrade the IRN. Both ω_0 and Q can be adjusted by tuning the bias current (i.e., the transconductances) to compensate for process variation, temperature and parasitic effects, realizing the desired frequency response.

2) Linearity: The linearity analysis is based on the equivalent circuit depicted in Fig. 3(a). The composite input signal consists of a DC bias voltage $V_{\rm IQ}$ and an AC signal $v_{\rm i}$, which is converted into current $I_{\rm D1}$ via $M_{\rm n1}$. With the voltage through C_1 as $V_{\rm x}$, it will be composed of a DC component $V_{\rm XQ}$ and an AC signal $v_{\rm x}$. After passing through the feedback network, the gate voltage of $M_{\rm n2}$ is defined by $V_{\rm g2} = V_{\rm XQ} - v_{\rm x}$, which is converted into current $I_{\rm D2}$ via $M_{\rm n2}$. The output signal $V_{\rm o}$ consists of a DC voltage $V_{\rm OQ}$ and an AC signal $v_{\rm o}$. $M_{\rm n1}$ and $M_{\rm n2}$ conduct the summed current of $I_{\rm D1} = I_{\rm D2} + i_{\rm nc1}$ and $I_{\rm D2} = I_{\rm n} +$

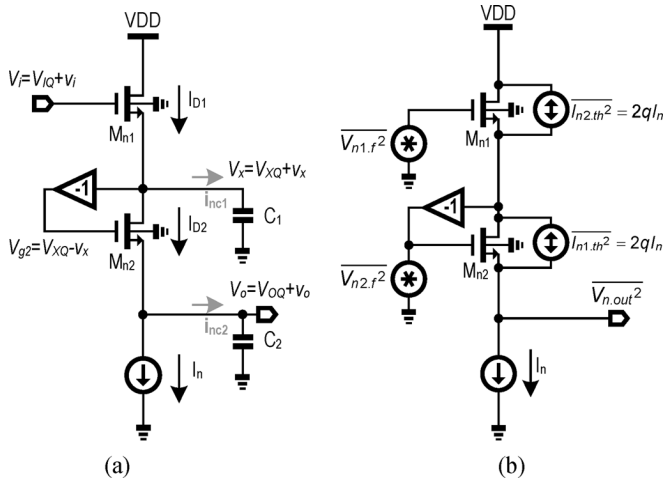

Fig. 3. Equivalent circuits. (a) Linearity analysis. (b) Noise analysis.

i_{nc2}, respectively, where I_{n} is the DC bias current. $i_{\mathrm{nc1,2}}$ is the frequency-dependent current via the capacitive loads $C_{1,2}$. The linearity performance is evaluated by analyzing the 3rd-order harmonic distortion (HD3) (i.e., even-order terms are ignored as the Biquad is practically differential). In order to obtain the input-output function of the Biquad filter, we established firstly the relationship between V_{i} and V_{x}, then derived the function between V_{x} and V_{o}. The detailed derivation can be found in [16] and is omitted in this article for brevity. The nonlinearities stem from the body effect due to the bulk modulation of the threshold voltage and the frequency-dependent effect through the capacitive item. According to the knowledge of power series expansion for HD3 calculation in [19], the HD3 of SSF Biquad is simplified as follows:

$$\begin{aligned}
&HD3\\
&\approx \left\{ \frac{-\frac{\gamma}{16}\left(a^{-5}+b^{-5}\right)-\frac{\gamma^2}{32ab}\left(a^{-2}+b^{-2}\right)^2}{4\left[1+\frac{\gamma}{2}\left(a^{-1}+b^{-1}\right)\right]^4} \right.\\
&\quad \left. + \frac{\frac{1}{6(nU_{\mathrm{T}})^2}\left(c^4+d^4+2c^3d+2cd^3-6c^2d^2-2c^3-2d^3\right)}{4[1+c+d]^4} \right\} v_{\mathrm{i}}^2\\
&a=\sqrt{2\Phi_{\mathrm{F}}+V_{\mathrm{OQ}}},\\
&b=\sqrt{2\Phi_{\mathrm{F}}+V_{\mathrm{XApx}}-V_{\mathrm{OQ}}}\\
&c=\frac{j\omega(C_1-C_2)nU_{\mathrm{T}}}{I_{\mathrm{n}}+j\omega C_1(V_{\mathrm{XApx}}-V_{\mathrm{OQ}}-V_{\mathrm{XQ}})},\\
&d=\frac{j\omega C_2 nU_{\mathrm{T}}}{I_{\mathrm{n}}}
\end{aligned} \tag{2}$$

with

$$\begin{aligned}
V_{\mathrm{XApx}} = 2V_{\mathrm{XQ}} - V_{\mathrm{t0.n}} - \gamma\left(\sqrt{2\Phi_{\mathrm{F}}+V_{\mathrm{OQ}}}-\sqrt{2\Phi_{\mathrm{F}}}\right)\\
-nU_{\mathrm{T}}\ln\left\{\frac{I_{\mathrm{n}}}{\left[2n\mu C'_{\mathrm{ox}}U_{\mathrm{T}}^2\left(\frac{W}{L}\right)\right]}\right\}
\end{aligned} \tag{2a}$$

where V_{XApx} represents the intermediate term in the 1st order approximation of V_{x} and is expressed with the zero-bias threshold voltage $V_{\mathrm{t0.n}}$, the body-effect coefficient γ, the Fermi level Φ_{F}, the carrier mobility μ and the gate oxide capacitor per unit area C'_{ox}, as shown in (2-a). In (2), the cross-product terms are omitted since they are much smaller than other terms, and it can be observed that there are two non-ideal terms that contribute to distortion. The first term, which is frequency independent and is caused by the body effect of M_{n1} and M_{n2}, is a function of the DC operating point, while the second term varies with frequency. At ultra-low frequency (approaching DC), the nonlinearity arising from the body-effect is pronounced, and the distortion is reduced with a higher DC level. When the frequency increases, the frequency-dependent effect becomes more pronounced as more AC current passes through the capacitive load. With such insights, the linearity can be optimized by minimizing the parameters c and d of the second term in (2). Instead of improving the linearity by enlarging the bias current at the expense of increased power, it can be shown that the frequency-dependent distortion can be optimized by choosing the value of C_2 to be close to half of C_1. The frequency-dependent term should dominate the overall linearity to be explained in Section II-D. Further improvements in linearity can be achieved via reducing C_1 and C_2 at the expense of increased noise. Since the quality factor (Q) is directly determined by the capacitance ratio, special considerations should be taken to balance the linearity and Q when cascading the Biquads for a high-order LPF in practice.

3) Noise: Fig. 3(b) is used for noise analysis. Both flicker and thermal noises are considered. $\overline{I^2_{\mathrm{n1,2.th}}}$ denotes the squared noise current of $M_{\mathrm{n1,2}}$; $\overline{V^2_{\mathrm{n1,2.f}}}$ are the squared noise voltages. The total IRN density is given by

$$\begin{aligned}
\overline{V^2_{\mathrm{n.in}}} = \frac{2qI_{\mathrm{n}}}{g^2_{\mathrm{mn1}}}\left(1+\frac{g^2_{\mathrm{msn1}}}{g^2_{\mathrm{msn2}}}\right)\\
+\frac{K_{\mathrm{F0}}}{{C'_{\mathrm{ox}}}^2 f^{\mathrm{AF}}}\left(\frac{1}{(WL)_1}+\frac{g^2_{\mathrm{msn1}}}{(WL)_2 g^2_{\mathrm{msn2}}}\right)
\end{aligned} \tag{3}$$

where q is electron charge; K_{F0} is the flicker noise factor for subthreshold operation, and AF is the flicker noise exponent. As ultra-low-power circuits require a large gate area for the MOSFETs, the flicker noise can be suppressed effectively. The dominant noise source should be the thermal noise when the bias current is extremely low. The thermal noise after integrated over the passband and assuming $g_{\mathrm{msn1}} = g_{\mathrm{msn2}}$, is given by

$$\overline{V^2_{\mathrm{n.in.int}}} = \frac{8nkT}{\sqrt{C_1C_2}} \tag{4}$$

where k is Boltzmann's constant and T is the absolute temperature. It is clear that the noise can only be reduced by increasing the capacitance (i.e., a tradeoff between area, linearity and noise).

4) Simulation Validation: In order to confirm the above analysis, the schematic shown in Fig. 2(a) was simulated in AMS 0.35-μm 2P4M CMOS process with SPECTRE as the simulator. The process parameters for hand calculation are listed in Table I. C_1 and C_2 were set as 20 pF and 10 pF, respectively. The bias current is 280 pA so as to realize the desired cutoff at

TABLE I
PROCESS PARAMETERS FOR HAND CALCULATION

NMOS process parameters In AMS 0.35 μm 2P4M CMOS Process	Typical value
Body factor γ	0.58 √V
Fermi potential (Φ_F)	0.7 V
Subthreshold slope factor (n)	1.5
Thermal voltage (U_T)	0.026 V (room temperature)
Carrier mobility (μ)	370 cm²/Vs
Gate oxide capacitance (C'_{ox})	7.6 fF/um²
Threshold voltage for long-channel ($V_{t0,n}$)	0.46 V
Thermal-noise energy (kT)	4.142×10-21 VA /Hz

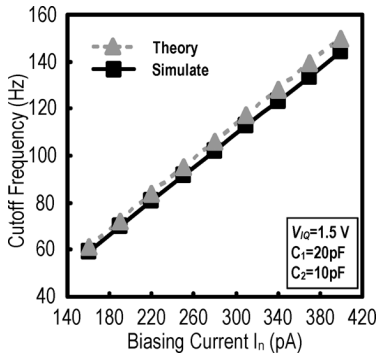

Fig. 4. Cutoff frequency versus the biasing current $I_{\rm n}$.

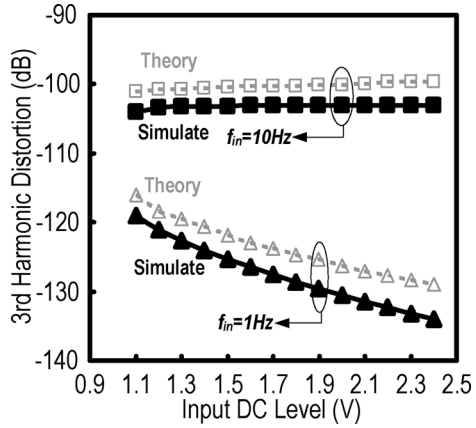

Fig. 5. HD3 versus input dc level at 50-$\mathrm{mV_{p-p}}$ input for both $f_{\rm in} = 1$ Hz and $f_{\rm in} = 10$ Hz.

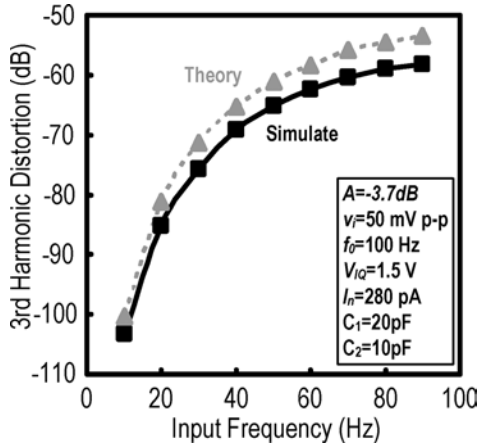

Fig. 6. HD3 versus input frequency at 50-$\mathrm{mV_{p-p}}$ input and 1.5-V input DC voltage.

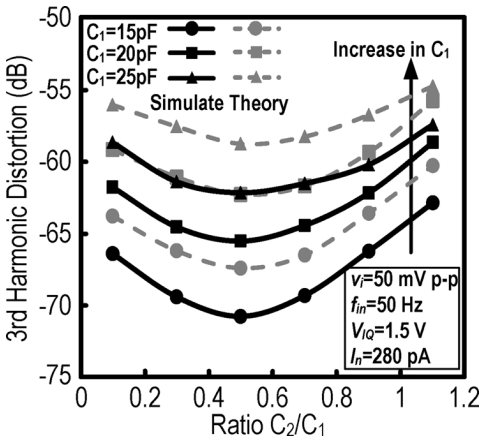

Fig. 7. HD3 versus the capacitance ratio of C_2/C_1 for different C_1 at 50-Hz 50-$\mathrm{mV_{p-p}}$ input.

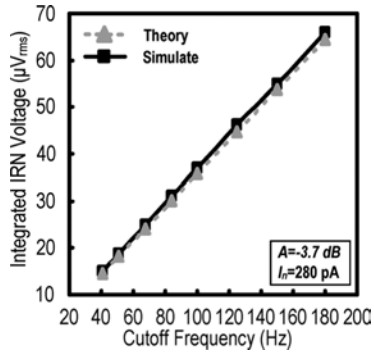

Fig. 8. Integrated IRN voltage for different cutoffs.

100 Hz. All the transistors were biased in the subthreshold region with equal W/L aspect ratio of 10/50 (μm). As plotted in Fig. 4, the cutoff frequency is almost linearly increased with the bias current. The linearity performance is evaluated based on the theoretical analysis from (2) and illustrated in Figs. 5–7. For low-frequency range test the input signal was set to 1 Hz such that the frequency-dependent distortion components can be neglected. With the input DC level swept from 1.1 to 2.4 V, the HD3 of the filter excited by a sinusoidal input with 50 $\mathrm{mV_{pp}}$ is shown in Fig. 5. The distortion is reduced with an increase in DC level as expected. For comparison, the HD3 with the input frequency of 10 Hz against different DC levels is plotted. The distortion is immune to the variation of the DC level, showing that the frequency-dependent term dominates the overall linearity. Fig. 6 shows the HD3 with respect to different input frequency in the passband. The linearity is progressively deteriorated when the signal frequency goes up. This confirms that the in-band linearity is mainly affected by the frequency-dependent effect. The calculated values using (2) are well consistent with the simulation results. Fig. 7 describes the HD3 versus the capacitance ratio of C_2/C_1 for different C_1. The optimum C_2/C_1

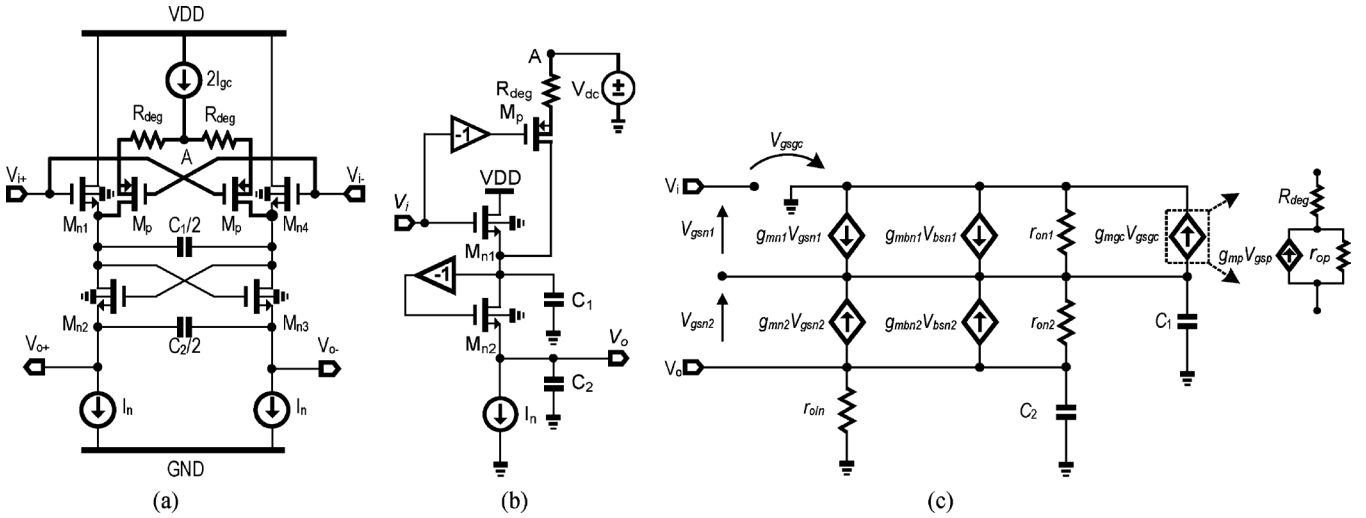

Fig. 9. (a) GC NMOS-based SSF Biquad. (b) The single-ended equivalent circuit and its (c) small-signal equivalent circuit.

for low distortion is around 0.5, when C_1 increases, the distortion becomes more pronounced. This validates the optimized strategy in choosing C_1 and C_2 to achieve low distortion. The noise against different cutoff frequencies is illustrated in Fig. 8. The cutoff frequency is swept by scaling the capacitances C_1 and C_2 simultaneously while keeping the same bias current. It is obvious that the relationship between the cutoff frequency and the integrated IRN voltage is almost linear, which agrees well with (4).

B. GC NMOS-Based SSF Biquad

Due to the body effect, the NMOS-based SSF Biquad suffers from gain-loss that can degrade the IRN when cascaded with other blocks. In this section, we describe a GC scheme constructed by a cross-connected differential pair $M_{\rm p}$ to provide an extra gain path to solve the problem. As shown in Fig. 9(a), the GC circuitry is biased with the current source $I_{\rm gc}$ and the source-degenerated resistor $R_{\rm deg}$ is utilized to leverage the gain-linearity tradeoff. The simplified single-ended equivalent circuit is depicted in Fig. 9(b), in which node A is the virtual ground.

1) I/O Transfer Characteristic: Similar to the analysis given in Section II-A, the small-signal model of the GC SSF Biquad is shown in Fig. 9(c). Here, $g_{\rm mn1}$ is always smaller than $g_{\rm mn2}$. The ideal parameters for the Biquad are: $A = 1 + g_{\rm mgc}/g_{\rm mn1}$, $\omega_0 = \sqrt{g_{\rm mn1}g_{\rm mn2}}/\sqrt{C_1C_2}$ (or written as $\sqrt{(I_{\rm n}-I_{\rm gc})I_{\rm n}}/\left(nU_{\rm T}\sqrt{C_1C_2}\right)$) and $\mathrm{Q} = \sqrt{g_{\rm mn1}g_{\rm mn2}C_1C_2}/\left[C_1g_{\rm mn2}+C_2(g_{\rm mn1}-g_{\rm mn2})\right]$. $g_{\rm mgc} = g_{\rm mp}/\left(1+g_{\rm mp}R_{\rm deg}\right)$ is the equivalent transconductance of the GC circuitry, where $g_{\rm mp}$ denotes the transconductance of $M_{\rm p}$. When the body effect is included, the transfer function is given by

$$H(s) = -\frac{\frac{(g_{\rm mn1}+g_{\rm mgc})g_{\rm mn2}}{g_{\rm msn1}g_{\rm msn2}}}{s^2\frac{C_1C_2}{g_{\rm msn1}g_{\rm msn2}} + s\frac{C_1g_{\rm msn2}+C_2(g_{\rm msn1}-g_{\rm mn2})}{g_{\rm msn1}g_{\rm msn2}} + 1} \tag{5}$$

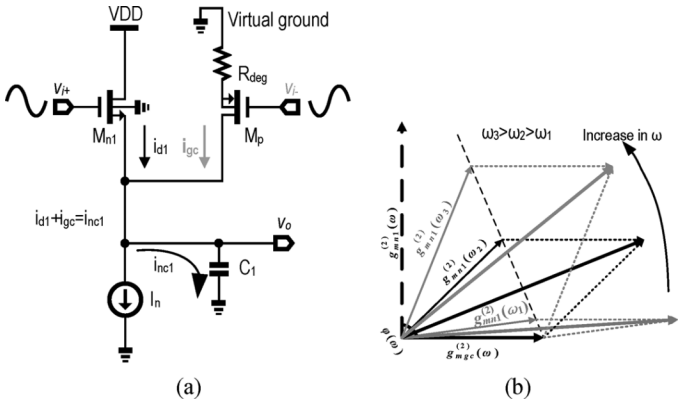

Fig. 10. (a) Equivalent circuit for linearity analysis. (b) Effect of distortion cancellation.

and the DC gain by

$$= \frac{(g_{\rm mn1}+g_{\rm mgc})g_{\rm mn2}}{g_{\rm msn1}g_{\rm msn2}}. \tag{5a}$$

By designing $g_{\rm mgc} \approx g_{\rm mbn1} + g_{\rm mbn2}$, a unity DC gain compensating the gain-loss induced by the body effect can be achieved. Due to the reduction of current through $M_{\rm n1}$, the cutoff frequency is also reduced. Consequently, smaller capacitance values can be used to maintain the same bandwidth and Q, and a smaller die size can be achieved. Due to the increase in DC gain, the overall IRN will not be sacrificed because of the smaller capacitor size. This issue will be discussed in Section III-C.

C. Linearity

The circuit representation shown in Fig. 10(a) is utilized to analyze the linearity. A differential signal $v_{\rm i}$ is converted into an AC current $i_{\rm d1}$ via $M_{\rm n1}$ and the current $i_{\rm gc}$ via $M_{\rm p}$. The AC current though the capacitor C_1, denoted as $i_{\rm nc1}$, is frequency dependent. For transistors $M_{\rm n1}$ and $M_{\rm p}$, we obtain $\mathrm{i_{d1}} = 2n\mu C'_{\rm ox}U_{\rm T}^2(W/L)_1 \cdot \exp\left(\hat{v}_{\rm i}/nU_{\rm T}\right)$ and $\mathrm{i_{gc}} = 2n\mu C'_{\rm ox}U_{\rm T}^2(W/L)_{\rm p} \cdot \exp\left(\hat{v}_{\rm i}/nU_{\rm T}\right)$, where $\hat{v}_{\rm i}$ is the

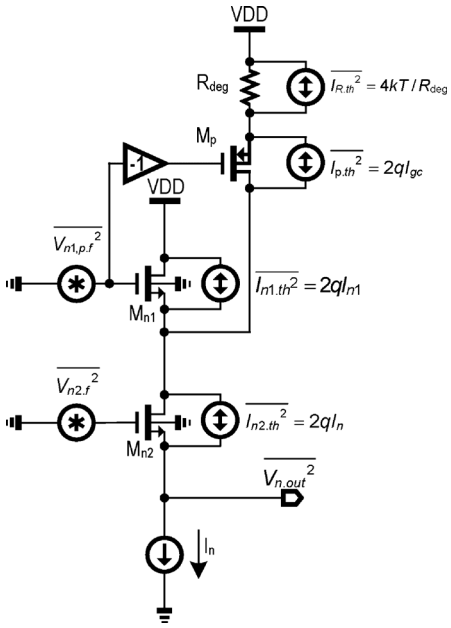

Fig. 11. Equivalent circuit for noise analysis.

amplitude of the input signal. The current can be expressed as the sum of the linear and non-linear components given by: $\mathrm{i}_{\mathrm{d1}} \approx g_{\mathrm{mn1}}\hat{v}_{\mathrm{i}} + (1/2!)g_{\mathrm{mn1}}^{(1)}\hat{v}_{\mathrm{i}}^2 + (1/3!)g_{\mathrm{mn1}}^{(2)}\hat{v}_{\mathrm{i}}^3$ and $\mathrm{i}_{\mathrm{gc}} \approx g_{\mathrm{mgc}}\hat{v}_{\mathrm{i}} + (1/2!)g_{\mathrm{mgc}}^{(1)}\hat{v}_{\mathrm{i}}^2 + (1/3!)g_{\mathrm{mgc}}^{(2)}\hat{v}_{\mathrm{i}}^3$. The linear components, $g_{\mathrm{mn1}}\hat{v}_{\mathrm{i}}$ and $g_{\mathrm{mgc}}\hat{v}_{\mathrm{i}}$, realize the GC operation. The nonlinear components $(1/3!)g_{\mathrm{mn1}}^{(2)}\hat{v}_{\mathrm{i}}^3$ and $(1/3!)g_{\mathrm{mgc}}^{(2)}\hat{v}_{\mathrm{i}}^3$ determine the linearity as a result of the differential topology. The summation of the two terms should be in a vector form as there exists magnitude and phase differences between the ac currents i_{d1} and i_{gc}, which are sensitive to the bias current. In our design, the bias currents are properly chosen to obtain an almost constant magnitude and phase V-I conversion for M_{p} over the band of interest. For M_{n1}, with an increase of input frequency, the distortion will increase (i.e., $(1/3!)g_{\mathrm{mn1}}^{(2)}\hat{v}_{\mathrm{i}}^3$ goes up) according to (2), and the phase given by $\varphi(\omega) = -\tan^{-1}(\omega C_1/g_{\mathrm{mn1}})$ will approach $-90°$. The mechanism of harmonic cancellation for various input frequencies is illustrated in Fig. 10(b). The magnitude after vector sum first decreases from ω_1 to ω_2, and then goes up from ω_2 to ω_3. Thus, minimum harmonic distortion can be obtained at an optimum spot frequency ω_2. This optimum frequency for low distortion can be adjusted by tuning the bias current. The GC scheme, thus, also exhibits the additional beneficial feature of harmonic cancellation.

1) Noise: The noise analysis circuit for the GC scheme is shown in Fig. 11. $\overline{I_{\mathrm{R.th}}^2}$ ($\overline{I_{\mathrm{p.th}}^2}$) denotes the noise current of R_{deg} (M_{p}); $\overline{V_{\mathrm{n1.p.f}}^2}$ denotes the summed flicker noise voltage of M_{n1} and M_{p}. The total IRN, with contributions from the thermal noise of M_{n1} and M_{n2}, the thermal noise of R_{deg} and M_{p}, and the summed flicker noise of M_{n1}, M_{n2}, and M_{p}, is defined as (6).

$$\overline{V_{\mathrm{n.in}}^2} = \frac{2q\left(I_{\mathrm{n}} - I_{\mathrm{gc}}\right){g_{\mathrm{mn2}}}^2 + 2qI_{\mathrm{n}}{g_{\mathrm{msn1}}}^2}{{g_{\mathrm{mn2}}}^2\left(g_{\mathrm{mn1}} + g_{\mathrm{mgc}}\right)^2} + \frac{2qI_{\mathrm{gc}} + 4kTR_{\mathrm{deg}}g_{\mathrm{mp}}^2}{\left(g_{\mathrm{mn1}} + g_{\mathrm{mgc}}\right)^2\left(1 + g_{\mathrm{mp}}R_{\mathrm{deg}}\right)^2} + \frac{K_{\mathrm{F0}}}{C_{\mathrm{ox}}'^2 f^{\mathrm{AF}}} \cdot \left[\frac{1}{(WL)_1} + \frac{{g_{\mathrm{msn1}}}^2}{(WL)_2\left(g_{\mathrm{mn1}} + g_{\mathrm{mgc}}\right)^2} + \frac{1}{(WL)_{\mathrm{p}}}\right] \tag{6}$$

The dominant thermal noise is integrated over the passband of $\sqrt{(I_{\mathrm{n}} - I_{\mathrm{gc}})I_{\mathrm{n}}}/\left(nU_{\mathrm{T}}\sqrt{C_1C_2}\right)$, expressed as

$$\overline{V_{\mathrm{n.in.int}}^2} = \frac{4nkT\left(\sqrt{\frac{I_{\mathrm{n}}}{I_{\mathrm{n}} - I_{\mathrm{gc}}}} + \sqrt{\frac{I_{\mathrm{n}} - I_{\mathrm{gc}}}{I_{\mathrm{n}}}}\right) + 4kT|A-1|\sqrt{\frac{I_{\mathrm{n}}}{I_{\mathrm{n}} - I_{\mathrm{gc}}}}}{A^2\sqrt{C_1C_2}} \tag{7}$$

where $A = 1 + g_{\mathrm{mgc}}/g_{\mathrm{mn1}}$. Also, notice that

$$\frac{I_{\mathrm{n}}}{I_{\mathrm{n}} - I_{\mathrm{gc}}} = \frac{I_{\mathrm{n1}} + I_{\mathrm{gc}}}{I_{\mathrm{n1}}} = \frac{g_{\mathrm{mn1}} + g_{\mathrm{mp}}}{g_{\mathrm{mn1}}}. \tag{8}$$

To achieve improved power and area efficiency, $g_{\mathrm{mp}}R_{\mathrm{deg}} < 1$ is desirable. As a result, $g_{\mathrm{mgc}} \approx g_{\mathrm{mp}}$, and $I_{\mathrm{n}}/(I_{\mathrm{n}} - I_{\mathrm{gc}}) \approx A$. Consequently, (7) can be rewritten as

$$\overline{V_{\mathrm{n.in.int}}^2} = \frac{4nkT\left(\frac{\sqrt{A}+1}{\sqrt{A}}\right) + 4kT|A-1|\sqrt{A}}{A^2\sqrt{C_1C_2}}. \tag{9}$$

It can be observed that the IRN voltage is reduced with an increase in gain, and the noise contribution of its subsequent blocks can also be suppressed. The improvement will be more noticeable when the design is extended to a higher order as in the fabricated prototypes to be described later. From the above analysis, the GC current and the degenerated resistor should be well designed based on the tradeoff among DC gain, linearity and noise.

2) Simulation Validation: A GC SSF Biquad with a 100-Hz cutoff frequency was designed to validate the above analysis. The bias current I_{n} was set to be 200 pA and I_{gc} was properly chosen to be 80 pA to achieve a unity gain. All the transistors were subthreshold-biased with an equal $(W/L)_{\mathrm{n}}$ of 10/50 (μm) and $(W/L)_{\mathrm{p}}$ of 100/10 (μm). The source-degenerated resistor of 100 MΩ is implemented by using subthreshold transistors to save area. The capacitance values of C_1 and C_2 were set as 10.6 pF and 8 pF, respectively. Fig. 12 shows the enhancement of the DC gain with the increase of the GC current I_{gc}, and simulated results are based on the DC gain obtained from (5-a). The theoretical curve is related to the term $\left(1 + g_{\mathrm{mgc}}/g_{\mathrm{mn1}}\right)/(1+\eta)^2$. The unity gain location is at $I_{\mathrm{gc}} = 80$ pA. The relationship between the cutoff frequency and I_{gc} is illustrated in Fig. 13, with $\omega_0 = \sqrt{g_{\mathrm{msn1}}g_{\mathrm{msn2}}}/\sqrt{C_1C_2}$. With an increase of I_{gc}, the current through M_{n1} is reduced for the same I_{n}. This reduces g_{mn1} and hence the cutoff frequency. Fig. 14 shows the simulated HD3 for different input frequencies, which features a V-shape, and the optimized frequency for low-distortion, which can be adjusted by bias current tuning, is

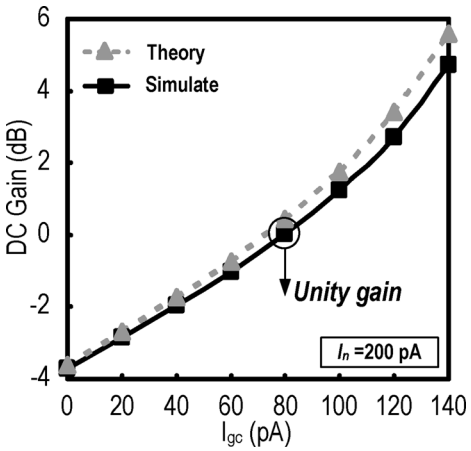

Fig. 12. DC gain against gain-compensated current $I_{\rm gc}$.

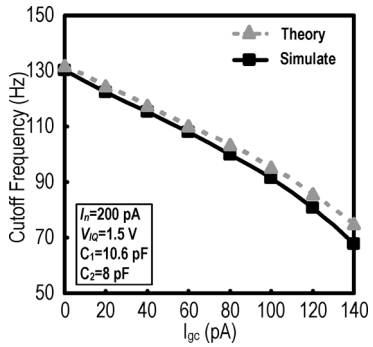

Fig. 13. Cutoff frequency versus gain-compensated current $I_{\rm gc}$.

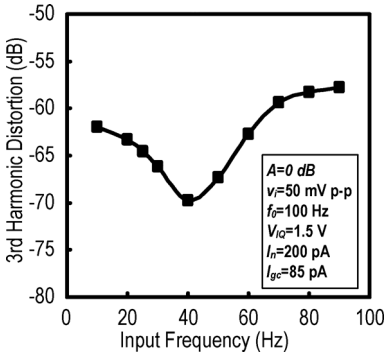

Fig. 14. HD3 for different input frequencies.

~ 40 Hz. The noise voltage over the passband against $I_{\rm gc}$ is described in Fig. 15. It is observed that the integrated IRN voltage is reduced with higher $I_{\rm gc}$, (i.e., more DC gain), corresponding well to (7).

III. Cascaded SSF Biquard Implementation

To demonstrate the applicability of SSF for LPF design, two 4th-order 100-Hz-bandwidth LPFs using Butterworth approximation were designed for ECG monitoring application with a bandwidth of 0.1–100 Hz [20]. For a filter-order greater than two, a cascade of NMOS- and PMOS-based SSF Biquads is necessary to match their bias voltages. The first design is a non-GC NMOS-based SSF Biquad followed by a PMOS one (Fig. 16). The second design is a GC NMOS-based SSF Biquad followed by a PMOS one (Fig. 17). As the body effect in the PMOS-based

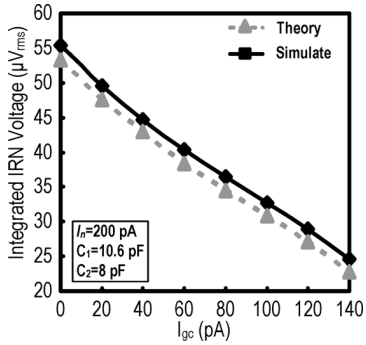

Fig. 15. Integrated IRN voltage against gain-compensated current $I_{\rm gc}$.

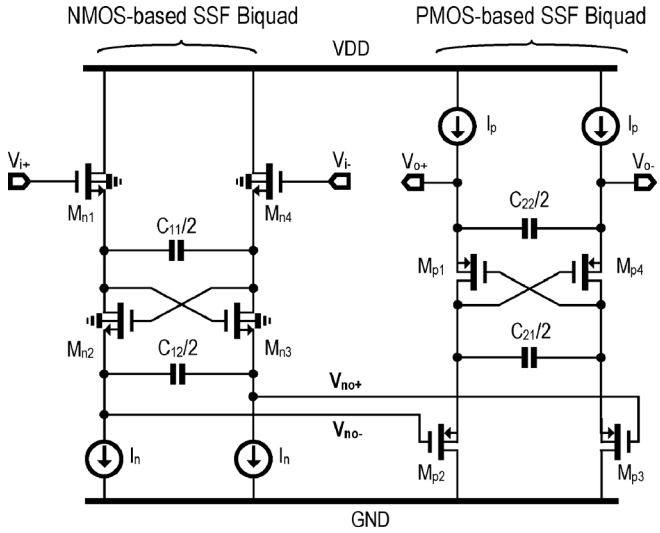

Fig. 16. Fabricated 4th-order non-GC LPF using SSF Biquads.

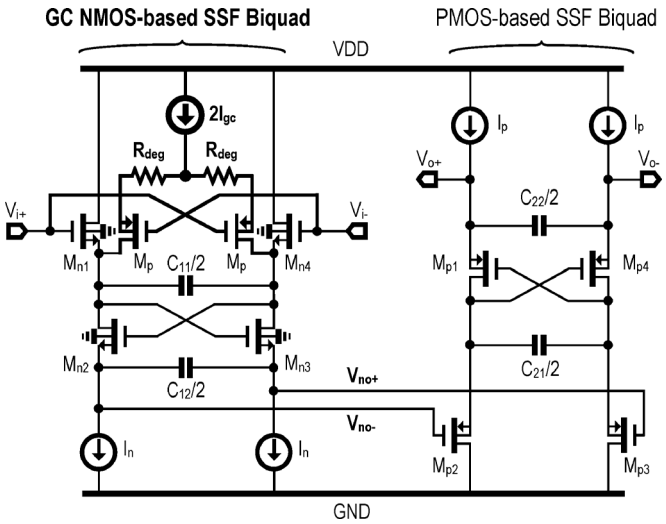

Fig. 17. Fabricated 4th-order GC LPF using SSF Biquads.

Biquad is avoided, no gain compensation is necessary. For the cascaded Biquads, each Biquad should be optimized individually for overall filter optimization in terms of Q and bandwidth. Since the capacitance size can help to reduce the noise and nonlinearity but penalize the power and area, the sizing of the load

TABLE II
SIMULATED RESULTS WITH VARIATIONS OF MISMATCH AND PROCESS, SUPPLY VOLTAGE, TEMPERATURE AND BIAS CURRENT FOR NON-GC AND GC LPFS

	Non-GC LPF					GC LPF				
	Mismatch and Process (100-runs)	Supply voltage (2.7-3.3 V)	Temp. (0-70 °C)	Bias current (±5 %)	Mismatch between I_n pairs (±3 %)	Mismatch and Process (100-runs)	Supply voltage (2.7-3.3 V)	Temp. (0-70 °C)	Bias current (±5 %)	Mismatch between I_n and I_{gc} (±3 %)
DC gain (dB)	-3.72± 0.11	-3.716±0.001	-3.71 ± 0.1	-3.716±0.002	-3.716±0.001	0.16±0.23	0.038±0.004	0.07±0.08	0.038±0.005	0.16±0.14
CM Voltage (V)	1.563±0.078	1.575±0.0002	1.577±0.037	1.576±0.001	1.575±0.001	1.571±0.085	1.579±0.0002	1.569±0.039	1.579±0.0008	1.574±0.0005
Bandwidth (Hz)	99.9±10.4	99.8±0.6	98.7±9.2	99.8±4.2	100.1±1.8	100.1±11.2	100.2±0.8	98.6±9.8	100.3±5.3	100.3±0.8
Offset (mV)	0.04±1.96	0	0	0	0.09±1.01	0.02±2.08	0	0	0	0
Noise (μV)	31.1±1.8	30.9±1.2	30.9±1.5	31.13±0.01	31.2±0.6	24.5±1.6	24.2±1.3	24.1±1.5	24.57±0.02	24.28±0.14
HD2 (dB) @ f_{in}=40 Hz	-91.6±11.6	-92.2±0.6	-92.6±1.5	-91.8±1.9	-90.1±10.9	-86.3±10.9	-86.6±0.6	-86.9±2.3	-86.3±1.8	-86.7±3.2
HD3 (dB) @ f_{in}=40 Hz	-62.4±2.9	-62.3±0.5	-63.6±2.3	-62.3±0.7	-62.4±0.5	-51.8±2.5	-51.8±0.7	-52.7±1.6	-51.4±0.6	-51.8±0.6

capacitance must follow an optimization process. The capacitors for the first stage Biquad are chosen to be large enough for reduced noise, while those for the second stage are optimized for low distortion to account for the extra loading capacitances for pads and external test buffers. Moreover, the Q should be balanced as well in the cascaded Biquads. The total capacitances for the first and second LPFs are 59.2 and 49.6 pF, respectively.

A. Mismatch and Process Variation

As component mismatches can lead to DC offset and linearity degradation, transistors with a longer channel length are more favored to improve the matching, which also befits the ultra-low-bias-current nature of our LPFs. Symmetrical layouts with the common-centroid technique also enhanced the matching.

To study the effect of various non-idealities, the simulated variations of different filter parameters under (1) mismatch and process; (2) supply voltage variation; (3) temperature variation; (4) bias current with $\pm 5\%$ variation; and (5) bias current with $\pm 3\%$ mismatch are quantitatively given in Table II. As expected the bandwidth has a strong relationship with the transconductances and capacitances. The DC gain variation of the GC LPF is as high as 0.23 dB, which is mainly due to the variation of the pseudo-resistors. The impact of matching-induced offset on the linearity, evaluated by the HD2, is also noticeable. However, the HD3 is still dominant.

For the effect of non-ideal current sources, we adjust the bias current $I_{\rm n}$ (in Fig. 16) with a variation of $\pm 5\%$ for non-GC LPF, and $I_{\rm n}$ and $I_{\rm gc}$ (in Fig. 17) simultaneously with the variation of $\pm 5\%$ for GC LPF. From Table II, one can observe that this effect causes large variation in the filter bandwidth, but has negligible effects on the DC gain and CM voltage. We have also simulated the effect of $\pm 3\%$ bias current mismatch between the $I_{\rm n}$ pairs in non-GC LPF, and $I_{\rm n}$ and $I_{\rm gc}$ in GC LPF. For the non-GC LPF, an increase in offset is observed due to the mismatch in the differential input pair, and degradation in HD2 results. For the GC LPF, there is an observable effect on the DC gain as a result of non-ideal gain compensation.

In both of our proof-of-concept prototypes, capacitor arrays covering a gain range of $\pm 12\%$ with a 4-bit digital word for manual filter bandwidth tuning are designed. For the GC LPF, we also need an external manual calibration of the voltage-controlled pseudo-resistor (nominal 100 $\mathrm{M\Omega}$) to set the DC gain to the expected value. The required tuning range to cover the DC gain variation of ± 0.23 dB due to process and mismatch in Table II is $\pm 47\%$, which corresponds to a control voltage range from 1.21 to 1.26 V. Of course, in practice, a bandwidth calibration loop such as the amplitude tracking technique [21] should be adopted. It is to quantize the LPF output's amplitude using a low-power amplifier and an asymmetric comparator. Then, a digital controller can be used to vary the tuning parameters (e.g., capacitor banks) until the maximum quantized amplitude is found, which corresponds to the desired bandwidth. Note that a stable Q for each Biquad requires a concurrent tuning of its two capacitors.

B. Filter Drivability

When the LPFs are to drive an A/D converter, they should fulfill the corresponding settling requirement to achieve less than 0.5 LSB tracking error [22], which can be achieved via adding an output buffering stage. For a typical pre-amplified ECG signal with a 100-Hz bandwidth and a 50-$\mathrm{mV_{pp}}$ amplitude, an A/D resolution of approximately 50 $\mu\mathrm{V/LSB}$ is generally required, resulting in a sampling capacitor size of ~ 6.6 pF to limit the thermal noise level to less than 0.5 LSB at room temperature. The required buffer bandwidth should be ~ 7 times to that of the signal bandwidth to achieve 0.1% settling. From simulations, a source follower with a power budget of ~ 1 nA is capable to fulfill such a requirement.

C. Experimental Verification

Fabricated in a standard 0.35-μm CMOS process, the active areas are 0.11 $\mathrm{mm^2}$ (non-GC LPF) and 0.08 $\mathrm{mm^2}$ (GC LPF) as shown in the die photo of Fig. 18. Both are designed for the same power of 15 nW including the bias circuit using a 3-V battery. The bias currents are generated externally. For the filter without GC, $I_{\rm n} = 600$ pA is injected externally and mirrored on chip for $I_{\rm p}$. For the filter with GC, $I_{\rm n} = 500$ pA and 2 $I_{\rm gc} = 360$ pA are provided externally. Around 6 nW is consumed by the front

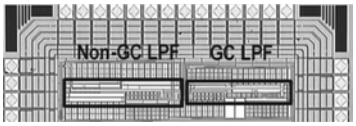

Fig. 18. Chip photo of the two LPFs using SSF Biquads with and without GC.

TABLE III
COMPONENT PARAMETERS OF THE TWO FABRICATED LPFS

	Non-GC LPF		GC LPF	
Components	1st Stage	2nd Stage	1st Stage	2nd Stage
I_n (pA)	600	1000	500	1000
I_{gc} (pA)	N/A	N/A	180	N/A
W/L of $M_{n1\text{-}4}$ (μm)	10/50	N/A	10/50	N/A
W/L of $M_{p1\text{-}4}$ (μm)	N/A	15.5/50	N/A	15.5/50
W/L of M_p (μm)	N/ A	N/A	40/4	N/A
R_{deg} (MΩ) [1]	N/A	N/A	~100	N/A
$C_{12}/2$ (pF)	16	N/A	9.3	N/A
$C_{22}/2$ (pF)[2]	N/A	8.8	N/A	8.8
$C_{11}/2$ (pF)	16.4	N/A	13.5	N/A
$C_{21}/2$ (pF)	N/A	18	N/A	18

[1] emulated by subthreshold transistors with W/L=2/20 (μm) and the resistance is voltage controlled.
[2] exclude the capacitance of pad and input capacitance of buffer

stage, and 9 nW by the back stage. The component parameters for the two LPFs are summarized in Table III.

As SSF Biquads are utilized to achieve ultra-low power consumption, the output common-mode (CM) voltage (designed to be 1.575 V), which is determined by the gate-source voltage $V_{\rm GS}$ of the transistors, is process dependent. As this CM voltage variation may cause possible reliability issue, careful common-centroid layout is practiced to alleviate this issue. Measurement results show that the worst case variation of the output DC level for 10 chips is less than 40 mV, which will not affect the overall performance of the filter. Notice that no on-chip buffers are included to facilitate the tesing, and the LPFs are designed to drive an off-chip commercial buffer [23] directly, which offers sufficiently high input impedance ($5\ \mathrm{T\Omega}||4\ \mathrm{pF}$) and low noise (0.3 to 0.1 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$ in the 10 to 100-Hz range) in all the experiments. With an estimated pad and PCB loading of 2 pF, the capacitve load of the LPF is up to 6 pF which has been accounted for in C_{22} (Figs. 16 and 17) to obtain the desired cutoff frequency.

The measured and simulated results of the first non-GC LPF are plotted and compared. Fig. 19(a) shows the gain response which exhibits a DC gain of $-3.8\,\mathrm{dB}$. With the bias current variation of $\pm 5\%$, the DC gain and bandwidth varies by 0.002 dB and 4.8 Hz, respectively. Fig. 19(b) plots the IRN voltage density (the noise contribution of the test buffer is de-embedded), and the estimated integrated IRN voltage over the passband is 36 $\mu\mathrm{V_{rms}}$ (simulation is 31 $\mu\mathrm{V_{rms}}$). The linearity was assessed by measuring the HD3 against the input frequencies with a 50-$\mathrm{mV_{p-p}}$ single-tone output, as depicted in Fig. 19(c), which is obtained via averaging the results from 10 chips to assure the

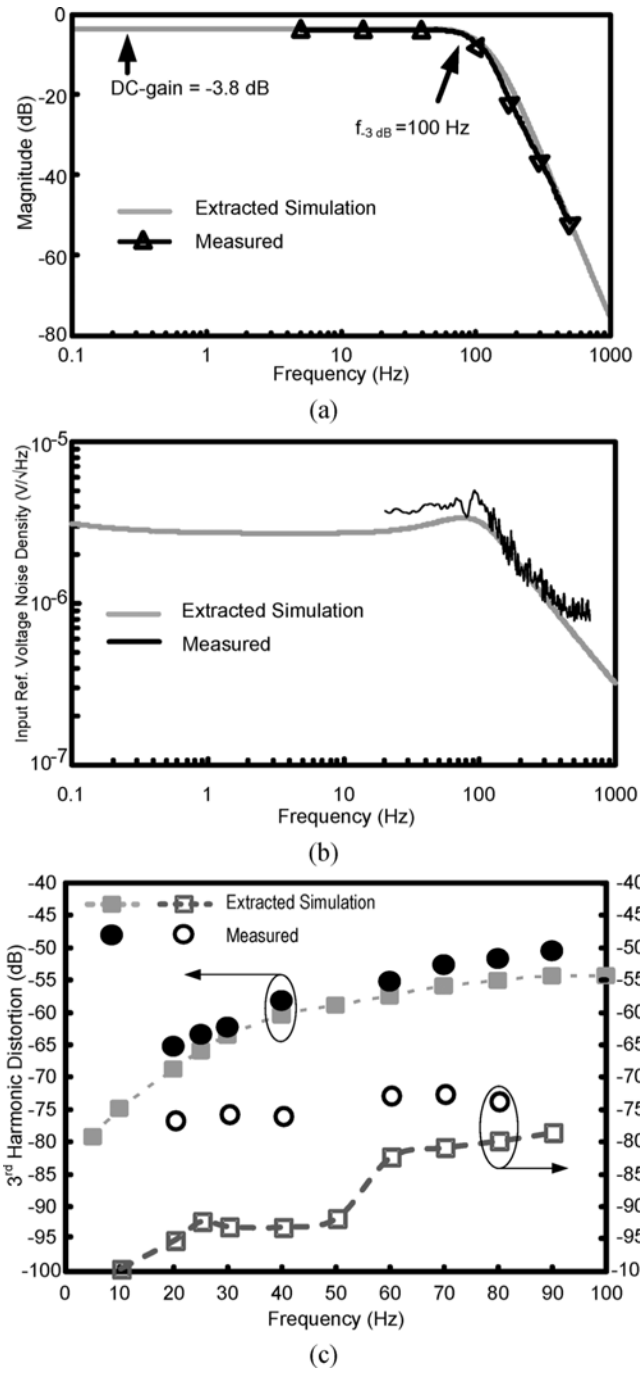

Fig. 19. Measured and simulated performances of the non-GC LPF. (a) Magnitude response. (b) Noise response. (c) HD_3 and HD_2 against different input frequencies for a 50-$\mathrm{mV_{p-p}}$ sinusoid output.

accuracy with a standard deviation of 2.12 dB. The HD3 increases with the input frequency which is consistent with the analysis given in Section II-B. The result at 50 Hz is omitted as the powerline interference is picked up by the equipments. The HD3 is $-55.2\ \mathrm{dB}$ when the input is at 60 Hz. The DR is 66.7 dB. HD2 is also plotted to illustrate the matching performance of the filter. The matching-induced offset leads to an increment of HD2 for the fully differential topology. The DC offset is 0.08 mV for 15 chips with a standard deviation of

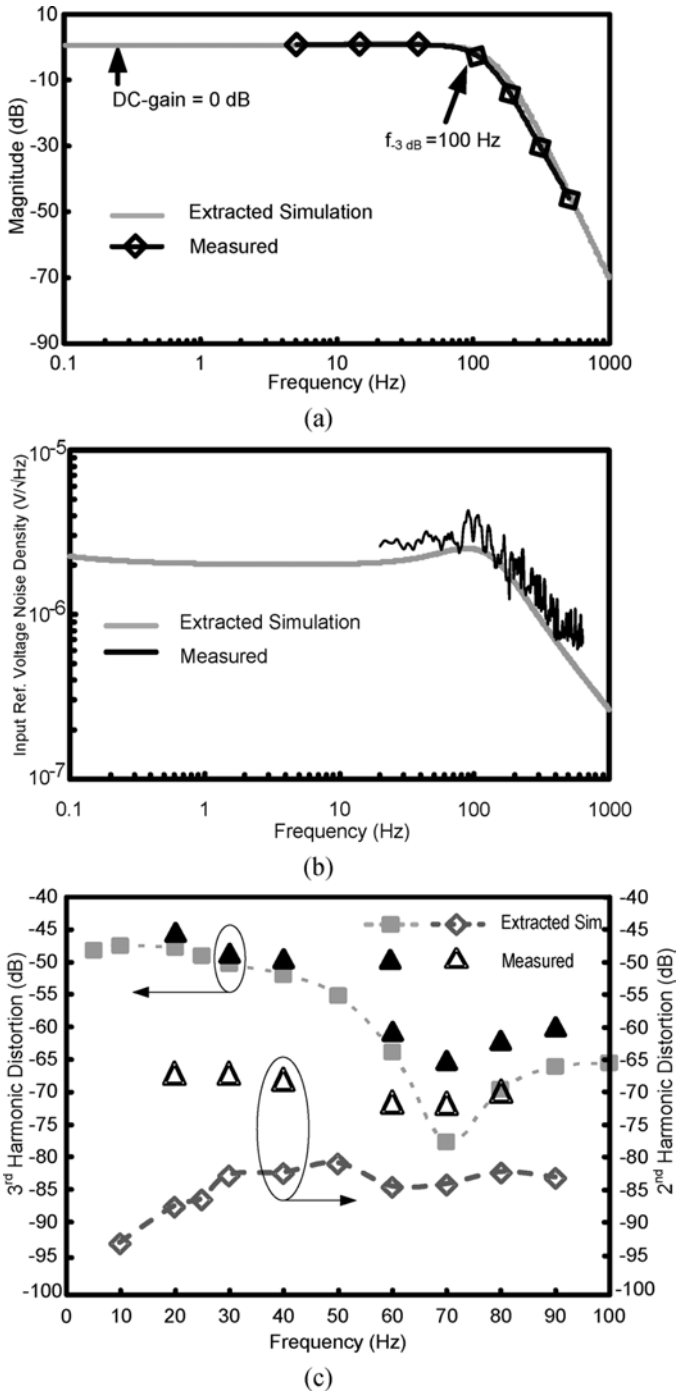

Fig. 20. Measured and simulated performances of the GC LPF. (a) Magnitude response. (b) Noise response. (c) HD_3 and HD_2 against different input frequencies for a 50-$\mathrm{mV_{p-p}}$ sinusoid output.

1.1 mV. The HD2 is below -70 dB for different input frequencies in the passband.

Fig. 20 shows a similar set of results for the GC LPF. The gain response is plotted in Fig. 20(a), where the DC gain is recovered to around 0 dB. The DC gain and bandwidth varies by 0.008 dB and 5.7 Hz, respectively, with the bias current variation of $\pm 5\%$. Fig. 20(b) describes the input IRN density, and the estimated integrated IRN voltage over the passband is 29 $\mu\mathrm{V_{rms}}$ (simulation

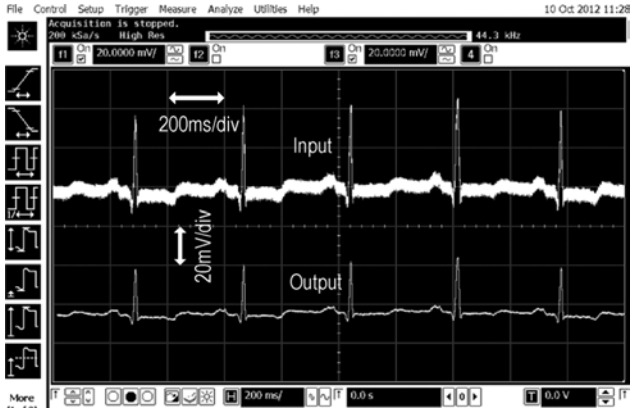

Fig. 21. Arrhythmic ECG signals before and after filtering (non-GC LPF).

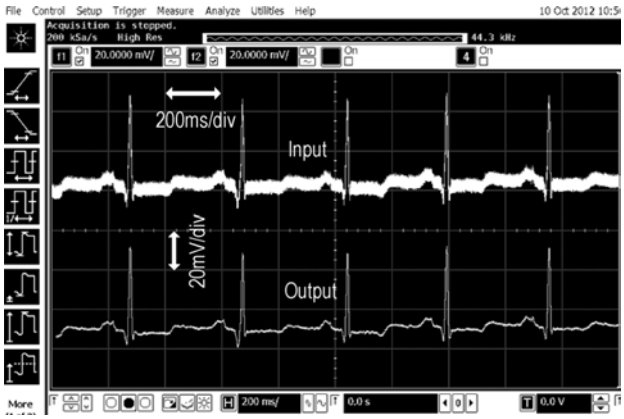

Fig. 22. Arrhythmic ECG signals before and after filtering (GC LPF).

is 24.6 $\mu\mathrm{V_{rms}}$), which is improved by 24% even with smaller capacitances when compared with the non-GC LPF. This derives from the gain enhancement of the first stage, with the suppression of the noise contribution of the second stage. The linearity performance is plotted in Fig. 20(c), which is also obtained via averaging the results from 10 chips with a standard deviation of 1.86 dB. When the input frequency is at 60 Hz or above, the HD3 is improved by > 5.5 dB, when compared with the non-GC Biquad. The V-shaped curve appears close to the frequency of 70 Hz matching fairly with the theory and simulation (Fig. 14). The DR seems smaller (1.9 dB) than the non-GC, but this is due to the improved passband gain to ensure the comparison is at an equal output swing of 50 $\mathrm{mV_{pp}}$. The measured HD2 is shown in Fig. 20(c). It is worse than that of the non-GC LPF due to the extra mismatch induced by the GC unit. The DC offset is 0.06 mV for 15 chips with a standard deviation of 1.1 mV.

To demonstrate the functionality of the LPFs, an arrhythmic ECG signal is captured before and after the filtering as shown in Fig. 21 (non-GC LPF) and Fig. 22 (GC LPF). The input signal constructed from [24] is amplified to be 50 $\mathrm{mV_{pp}}$, and is superimposed by a 10-$\mathrm{mV_{pp}}$ out-band (300 Hz) sinusoid signal. It shows that the latter can be suppressed adequately to improve the signal quality.

Benchmarking with the works [14], [15], [25], [26] targeting a similar bandwidth in Table IV, both the GC and non-GC LPFs

TABLE IV
SUMMARY AND BENCHMARK WITH PRIOR ARTS

	ACSP'05 [14]	TBIOCAS'09 [15]	EL'10 [25]	TBIOCAS'10 [26]	This Work	
					Non-GC LPF	**GC LPF**
VDD	± 1.5 V	1 V	1 V	1.8 V	**3 V**	**3 V**
CMOS Technology	0.35 µm	0.18 µm	0.18 µm	0.18 µm	**0.35 µm**	**0.35 µm**
Filter Order (Topology [a])	5 (S)	5 (D)	4 (D)	9(S)	**4 (D)**	**4 (D)**
BW	37 Hz	250 Hz	732 Hz[b]	3 KHz	**100 Hz**	**100 Hz**
Integrated IRN voltage	243 μV_{rms}	<340 μV_{rms}	50 μV_{rms}	~564 μV_{rms}[c]	**36 μV_{rms} (0.1 to 100 Hz)**	**29 μV_{rms} (0.1 to 100 Hz)**
HD3	-61.5 dB @ f_{in}=8 Hz v_{out}=50 mV_{p-p}	-49 dB @ f_{in}=50 Hz, v_{out}=9.43 mV_{p-p}	<-40 dB @ f_{in}=700 Hz, v_{out}= N/A	<-38.4 dB @ f_{in}= 1 KHz, v_{out}=40 mV_{p-p}	**-55.2 dB** @ f_{in}=60 Hz, v_{out}=50 mV_{p-p}	**-60.7 dB** @ f_{in}=60 Hz, v_{out}=50 mV_{p-p}
DR	57 dB	50 dB	55 dB	34 dB	**66.7 dB**	**64.8 dB**
Power	11 µW	0.453 µW	14.4 nW	360 nW	**15 nW**	**15 nW**
DC Gain	~0 dB	-10.5 dB	-6 dB	~0 dB	**-3.7 dB**	**0 dB**
Active Area	0.25 mm^2	0.13 mm^2	0.13 mm^2	0.03 mm^2	**0.11 mm^2**	**0.08 mm^2**
FoM	1.04 x 10^{-9}	7.25 x 10^{-12}	0.89 x 10^{-13}	3.9 x 10^{-13}	**5.62 x 10^{-13}**	**5.79 x 10^{-13}**

a (S): Single-ended, (D): Differential.
b Center frequency of the bandpass filter.
c Calculated according given input range and DR.

exhibit superior performances in terms of the Figure-of-Merit (FoM) defined as [27]

$$FoM = \frac{P}{N \cdot f_{\rm c} \cdot DR} \tag{10}$$

where P is the filter power consumption, N is the order, $f_{\rm c}$ is the cutoff frequency (exception for the center frequency in [25]), and DR is the dynamic range. Lower FOM figures indicate better filter performance. This work measures comparable FoM with the state-of-the-art.

IV. CONCLUSIONS

Ultra-low-power analog circuits will continuously open up new prospects for bioelectronics. This research work was focused on the nW-class filtering revealing the valuable properties of the SSF Biquad. It decouples better the linearity and noise from the power and area than the widely used g_m-C topology. The gain-loss problem of NMOS-based SSF Biquad due to the body effect has been addressed via the proposed GC scheme. Two 4th-order LPFs with and without GC verified the theory. The GC LPF shows improved DC gain and lower IRN over the non-GC structure. Both LPFs exhibit favorable power and area efficiencies as well as comparable FoM with respect to the state-of-the-art. Subsequently, further research under development is the design of a sub-μW biopotential readout front-end using nW-class instrumentation amplifier and analog-to-digital converter. The future work includes the implementation of automatic tuning and on-chip biasing to improve the practicality of our current prototype.

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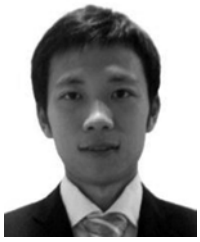

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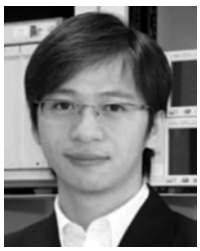

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