A 0.19 mm^2 10 b 2.3 GS/s 12-Way Time-Interleaved Pipelined-SAR ADC in 65-nm CMOS

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***Abstract*— This paper presents a 2.3 GS/s 12-way time-interleaved pipelined-SAR ADC achieving 1.1 GHz input bandwidth with 47.4 dB signal-to-noise distortion ratio (SNDR). Here, we propose a hierarchical interleaving with passively shared sub-sampling front-end to eliminate the timing skews, thus avoiding the timing calibration for design simplicity as well as better area and power efficiency. To provide a fast signal transfer with good power efficiency to the sub-ADCs, the power and bandwidth trades off by using the passive sharing or active buffers are analyzed according to our developed mathematic model. The analysis is based on two scenarios: noise and matching limited sampling. Moreover, we propose a *boosting-capacitor-sharing* technique to enhance the compactness of the time-interleaved bootstrapped sampling front-end, which is particularly critical when omitted the time calibration in this design. Measurement results on a 65 nm CMOS prototype operated at 2.3 GS/s and 1.2 V supply show 31 mW total power consumption with a SNDR of 47.4 dB @Nyquist leading to a FOM of 69 fJ/conv.step.**

***Index Terms*— Time-interleaved ADC, sampling front-end design, passive sharing, pipelined-SAR ADC, switch bootstrap technique.**

I. Introduction

RECENT radio applications and next generation mobile communication system call for low-power, high-speed (multi-GS/s) and mid-resolution (∼10 bit) *analog-to-digital converters* (ADCs). Recently, several multi-GHz ∼10 bit ADCs have been reported [1]–[6], in which the skew calibrated *time-interleaved* (TI) *successive approximation register* (SAR) ADC [1]–[3] achieves the best *Figure-of-Merit* (FoM). SAR ADCs [7]–[9] exhibit excellent power efficiency due to its simple architecture. However, when used as a sub-ADC its sequential conversion feature exhibits speed limitation especially in medium to high resolution converters. To achieve GHz sampling rates usually it requires larger number of TI channels demanding heavy calibration efforts to correct the skew, gain and offset mismatches [1]–[3]. The extraction of time errors becomes much more complex, as it is signal dependent and the other circuit non-idealities would affect the calibration accuracy, i.e., the gain and offset errors that must be suppressed to a sufficiently low value. The time calibrated TI-SAR ADC [3] achieves near 48 dB *signal-to-noise distortion ratio* (SNDR) at >1 GHz bandwidth. However, once the power and area from the digital overhead are included, it becomes less attractive. To interleave a large number of sub-ADCs without timing calibration implies typically the need of buffers [5], [6], [10]. The hierarchical interleaving of a few *sample & holds* (S/Hs) with multiplexed buffer-ADC units [5] optimizes the clocking, bandwidth and linearity, whereas the buffers consume large static power and induce offset and gain errors. This scheme achieves 1.25 GHz input bandwidth with a SNDR of 48.5 dB consuming hundreds of mW dominated by the buffers and the calibrations. The *master-slave* (MS) [11] avoiding time calibration and buffers exhibits excellent power efficiency for an 11-bit level, which achieves comparable SNDR with those of the time-calibrated TI-SAR ADCs [1], [2] at near a 500 MHz input bandwidth. However, targeting for the GHz range bandwidth demands an increased number of sub-ADCs. The flatting interleaving of many sub-ADCs in the back-end induces a significant bandwidth mismatch and signal feedthrough, therefore, the solution so far has been limited to low resolution [12], [13] mostly in the advanced SOI technology node.

This paper presents a 12-way TI pipelined-SAR ADC in 65 nm CMOS that achieves a 2.3 GS/s sampling rate and a SNDR of 47.4 dB @Nyquist input. We employ several techniques to achieve the specification: i) the hierarchical interleaved sampling front-end implements MS S/Hs with ping-pong passive sharing for sub-sampling, providing a fast signal transfer to sub-ADCs and good signal isolation. It effectively suppresses the interleaving spurs below −64 dB at the Nyquist input without any time calibration; ii) bootstrap circuits for sub-sampling switches use a BCS technique to improve the compactness of the sampling network. Moreover, the power dissipation by sub-sampling with passive sharing or buffer are

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analyzed with our developed model, where the former demonstrates better power efficiency for targeted sampling accuracy under both noise and matching limited scenarios. Fabricated in 65 nm CMOS the prototype achieves 50.5 dB SNDR @DC input with a compact area of 0.19mm^2 including the reference decoupling capacitance and the offset calibrations.

This paper is organized as follows. Section II discusses the design trade-offs between direct and MS sampling, and analyzes and compares the power efficiency of the sub-sampling network, categorized as voltage-based by using active buffers or charge-based by passively sharing. Section III introduces the proposed sampling front-end design, which is followed by the ADC architecture and the circuit implementations in sections IV and V, respectively. Finally, we report the measurement results and draw the conclusions.

II. Passively Shared & Buffered Sub-Sampling Comparison

There are two voltage-based time interleavers: 1) direct sampling (DS) [1]–[3] and 2) MS sampling [11]–[14] as shown in Fig. 1(a) and (b), respectively. The direct sampling minimizes the resistance in the input path to the sampling capacitor, where the input signal goes through only one of the switches (S_1 to S_{N1}) and is tracked onto its T/H capacitor (C_S) in the corresponding channel. The sampling *bandwidth* (BW) in the 1st hierarchy is determined by $2\pi/R_{on}C_S$, where R_{on} is the switch on-resistance. Timing mismatch (or known as periodic timing-skew) in time-interleaved systems refers to the mismatch in the sampling instant inside the individual channel, originated from the inaccurate sampling clock edges (ϕ_1 to ϕ_{N1} in Fig.1(a)) derived from by the mismatch in the clock generation paths. Timing mismatches are difficult to compensate due to its signal-dependent dynamic nature, and complex algorithms are generally required to calibrate the timing mismatch in the digital domain leading to a large digital area and power consumption. The SNDR due to timing mismatch can be calculated as [15]:

$$SNDR = 20\log\left(\frac{1}{2\pi f_{in}\sigma_t}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \quad (1)$$

where σ_t and f_{in} represent the standard deviation of the timing mismatch and the input frequency. M is the number of TI channels. From (1) it is evident that the performance of the DS with timing mismatch degrades as the input signal frequency increases, e.g. to achieve 62dB SNDR, with M of 12 and f_{in} of 1.1GHz, the σ_t needs to be suppressed to less than 120 fs that can constitute a main design challenge. The timing calibrations [1]–[3] are investigated to improve the ADC performance using DS, which either draws a large digital overhead and power consumption to fix the error at the background [1] or faces accuracy limitation affected by other circuit non-idealities such as offset and gain mismatches [1]–[3]. The MS sampling avoids the time-skews by using a master switch in series connection with interleaving switches, which aligns the TI clocks to the full speed of the master clock. Assuming the master and TI switches are designed with the same R_{on}, its BW compared with DS is reduced by half. As shown in Fig.1(b) the sampling instant is determined by ϕ_0 only, the required clock jitter for target same specification as DS is 70 fs. The time skews for TI clocks (ϕ_1 to ϕ_{N1}) are quite relaxed, where more than 50 ps latency between the falling edges of master and TI clocks is sufficient to guarantee the required accuracy.

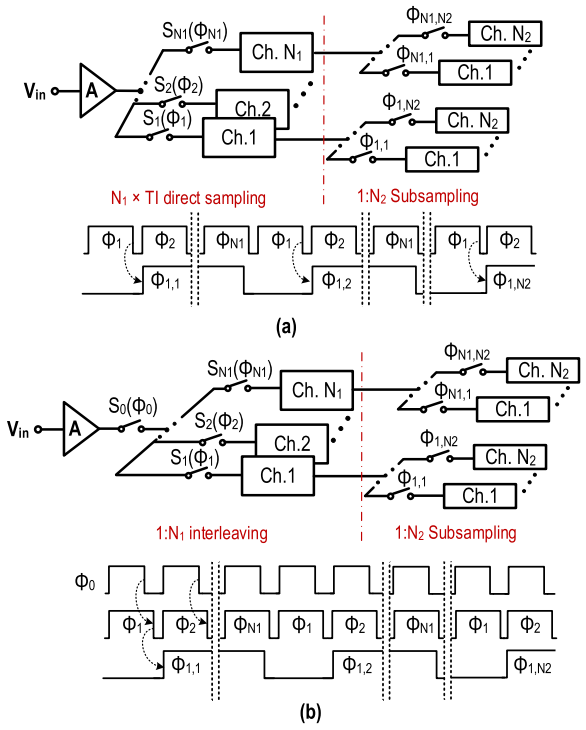

Fig. 1. Voltage-based sampling network (a) direct sampling with subsampling. (b) MS sampling with subsampling.

To enable a high interleaving factor for high speed ADC design, the subsampling technique is usually utilized at the 2nd hierarchy that can be categorized as voltage-based by using active buffers [6], [13] or charge-based by passively sharing the signal with the sub-ADCs [12] in this work. The aim of this section is to analyze and compare the power efficiency of voltage- and charge-based sub-sampler with given specifications. The models derived here relate the buffer's power dissipation to the analog input BW under a specified available track time on the sampling capacitor. We quantified the sampling capacitance for two scenarios: kT/C noise and matching limited designs.

The overall sampling can be divided into two phases: 1) tracking the input; 2) transferring the input to the sub-ADC (sub-ADC sampling). For phase 1 as depicted in Fig. 2 the MS sampling is used to avoid time mismatches, where C_p and C_S are the routing parasitic and sampling capacitance in one of the sub-channels, respectively. The RC network in the tracking phase is equivalent to the 2nd order RC filter, where $R_{on,0}$ and $R_{on,1}$ are the on-resistances of the switches. $C_{p,N1}$ and $R_{out,0}$ model the sum of routing parasitics from the sub-channels and the output impedance of the front-end input buffer, respectively. The sub-ADC's sampling either using the passive sharing or active buffer are exhibited in Fig. 3(a) and (b), respectively. Obviously, excluding the

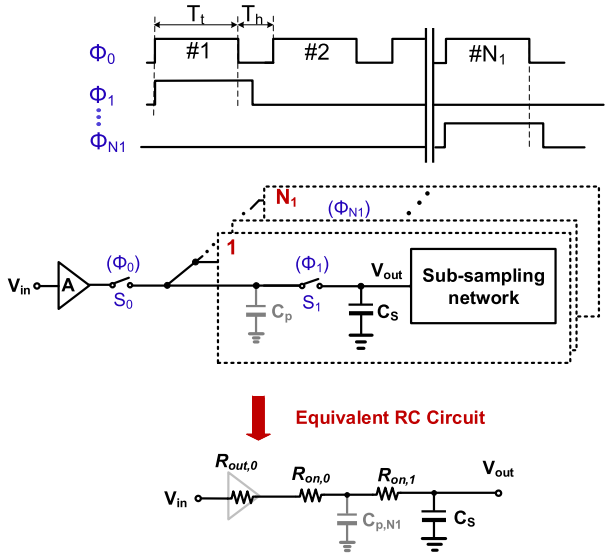

Fig. 2. MS S/H sampling network at the 1st hierarchy and its RC equivalent circuit in the tracking phase.

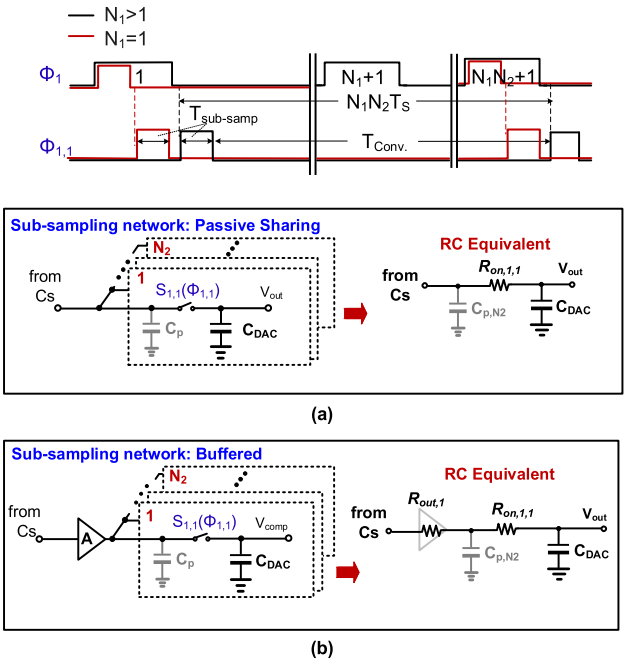

Fig. 3. (a) Sub-sampling with passive sharing and its 1st order RC equivalent (b) Sub-sampling with active buffer and its 2nd order RC equivalent.

power from the clock buffers, the passive-shared sub-sampling can provide a fast signal delivery for the sub-ADCs without extra power dissipation, while the signal loss degrades the *signal-to-noise ratio* (SNR). For the buffered sub-sampling, the source-follower topology is generally used [6], [14] for better BW leading to less signal attenuation than its counterpart but the buffers consume static power. To relax its power and BW trade-off, the number of sub-ADCs often needs to be increased.

Firstly, we discuss the noise limited sampling where the sampling capacitor is determined by the kT/C noise. To match the ADC's specification in this design, the sampling front-end is designed for a 10 bit ADC with a sampling rate of 2.3 GS/s. Therefore, the targeted sampling total-harmonic-distortion (THD) is set at 62 dB under a signal swing of 1.4 V_{p-p}. For the buffered sub-sampling, assuming that the signal attenuated by the buffers in each hierarchy is -2 dB. To satisfy the 10b kT/C noise, C_S and the sub-DAC (C_{DAC}) need to be designed with values not smaller than 54 fF and 84 fF, respectively. In the passive sharing C_{DAC} must be larger than 214 fF for the same SNR. The routing parasitics C_p is set as 5 % of its sampling capacitance, therefore, $C_{p,N1}$ rises linearly with the number of sub-channels. According to the tracking-mode in Fig.1 the transfer function of the 2nd order RC circuit can be derived as (2), as shown at the bottom of this page where C_{Sum} is the sum of the sampling capacitors after the activated demux switch. The passive sharing structure of Fig. 3(a) includes C_S and the total routing parasitics ($C_{p,N2}$) from C_S to $N_2\times$ sub-ADCs, while in the buffered sub-sampling $C_{p,N2}$ is isolated by the buffer. With passive sharing, the best SNR can be achieved by setting the ratio of C_{Sum} and C_{DAC} to 1:1, if the total capacitance is fixed. The time constant τ can be obtained as (3), as shown at the bottom of this page For n bit accuracy, the required tracking time T_t is

$$T_t = k\tau, \tag{4}$$

where the time constant k should be (5), as shown at the bottom of this page.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{[sR_{on2}C_{Sum}+1][sC_{p,N1}(R_{out1}+R_{on1})+1]+s(R_{out1}+R_{on1})C_{Sum}}, \tag{2}$$

$$\tau = \frac{1}{2}\left[\left(R_{out,0}+R_{on,0}\right)\left(C_{Sum}+C_{p,N1}\right)+R_{on,1}C_{Sum}+\delta\right]$$
$$\delta = \sqrt{\left[\left(R_{out,0}+R_{on,0}\right)\left(C_{Sum}+C_{p,N1}\right)+R_{on,1}C_{Sum}\right]^2-4R_{on,1}C_{p,N1}C_{Sum}\left(R_{out,0}+R_{on,0}\right)} \tag{3}$$

$$k \geq (n-1)\ln 2+\ln\left[\frac{\left(R_{out,0}+R_{on,0}\right)\left(C_{Sum}+C_{p,N1}\right)+R_{on,1}C_{Sum}}{\delta}+1\right]. \tag{5}$$

TABLE I
DEVICE PARAMETERS FOR NOISE AND MATCHING LIMITED CASES

	$R_{on,0}$ (Ω)	$R_{on,1}$ (Ω)	$R_{on,1,1}$ (Ω)	Buffered Sub-sampling				Passive-sharing Sub-Sampling	
				1st hierarchy		2nd hierarchy			
				C_{Sum1} (fF)	$C_{p,N1}$ (fF)	C_{Sum2} (fF)	$C_{p,N2}$ (fF)	C_{Sum} (fF)	$C_{p,N1}$ (fF)
Noise limited	5	11	11	54	5%xN1x C_{Sum1}	84	5%xN2x C_{Sum2}	214	5%xN1xC_{Sum}x (1-5%xN2)
Capacitor matching limited				400		400		400	

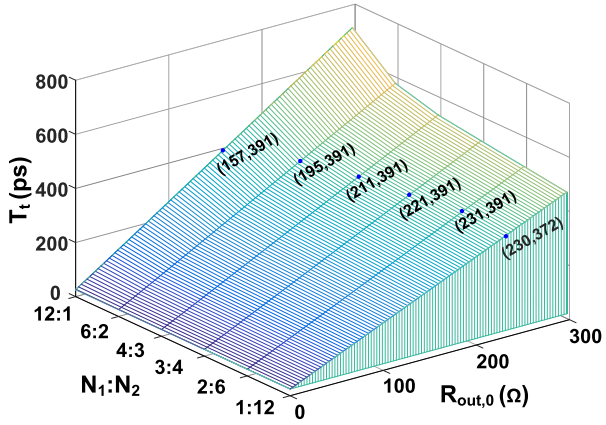

Fig. 4. T_t vs. $R_{out,0}$ under different combinations of N_1 and N_2 for passive sharing.

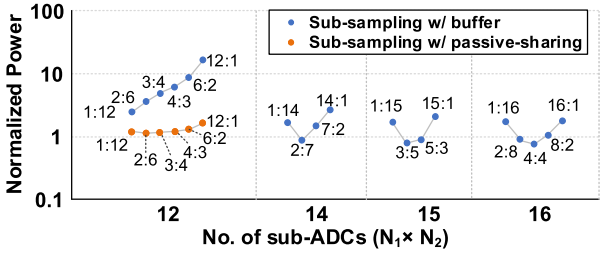

Fig. 5. Power dissipation in a noise limited scenario under different combinations of N_1 and N_2 by using passive-sharing and buffered sub-sampling.

Through (3)-(5) we can easily obtain the function of $T_t = f(R_{out,0})$, while the power dissipation from the front-end buffer is correlated with $R_{out,0}$and can be calculated as

$$P_{buff} = V_{DD} \cdot \left(\frac{I_D}{g_m}\right) \cdot \frac{1}{R_{out,0}}, \tag{6}$$

where V_{DD} is the supply voltage of the buffer, g_m is the MOS device's transconductance, and I_D/g_m is its transconductance efficiency whose value depends on the biasing condition and the inversion level [16], [17]. Since P_{buff} is inversely proportional to $R_{out,0}$, previous inverse function: $R_{out,0} = f(T_t)$ is required. However, such inverse function is difficult to be derived as $f(R_{out,0})$ is quite complicated. Instead, if here some design parameters (listed in Table I) in this work are substituted into $f(T_t)$, such as the switch's on-resistance ($R_{on,0} = 5.5\Omega$ and $R_{on,1} = 11\Omega$) and the total capacitance in each hierarchy ($C_{p,N1} = 5\%N_1C_S$ and $C_{p,N2} = 5\%N_2C_{DAC}$, where N_1 and N_2 are the number of channel in the 1st and 2nd hierarchy, respectively), we can plot $R_{out,0}$ versus T_t under different combinations of N_1 and N_2. Fig. 4 shows the plot for passive sharing. In each case $R_{out,0}$ always corresponds to a specified T_t, implying the buffer's power dissipation can be calculated with a known value of T_t.

The available tracking time $T_t$depends on the number of TI channels assigned in the 1st hierarchy, i.e. N_1. Assuming the sub-ADC operates synchronously with a maximum conversion rate of 500 ps/bit, and according to the timing diagram in Fig. 2 and Fig. 3, the 10-bit conversion must be completed within $N_1N_2T_S$ (the period of $\phi_{1,1}$). Therefore, it requires at least a number of 12 ($N_1 \times N_2$ =12) TI sub-ADCs for 2.3 GS/s. With passive sharing, the signal transferred from C_S to C_{DAC} is power-free and experiences a 1st order RC settling, which requires less than 20 ps for a 10-bit accuracy with the $R_{on1,1} = 5.5\Omega$. Thus, only the front-end buffer contributes the overall power. The tracking (T_t) and holding (T_h) time allocation under different N_1 can be optimized to

$$\begin{cases} T_t : T_h = 6:1, & N_1 = 1 \\ T_t : T_h = 9:1, & N_1 > 1. \end{cases} \tag{7}$$

If there is no interleaving at the 1st hierarchy (N_1 =1), the front-end and sub-ADC's sampling cannot occur concurrently, where C_S must be released out before next incoming sampling, reducing the available tracking duration. Once N_1 is set >1, the sub-ADC's sampling can be processed simultaneously with the front-end sampling, maximizing the tracking duration. Thus, the ratio of T_t and T_h can be optimized. For a specified T_t defined in (7) we can find the corresponding $R_{out,0}$ under different combinations of N_1 and N_2 as highlighted in Fig. 4. Therefore, the power dissipation according to (6) by using passive sharing can be plot in Fig. 5. The case with higher power consumption occurs at N_1: N_2@ 12 : 1, as the parasitic $C_{p,N1}$is maximized. Though N_1: N_2@ 2 : 6 obtains the best power efficiency, it requires one C_S to be shared by a large number of sub-ADCs, increasing the routing complexity. This issue in the sub-ADC built with the SAR unit becomes more critical, where typically the sampling capacitor is a DAC for 10 bit quantization containing at least 512 capacitive units. Even though the total capacitance is

TABLE II
TIME ALLOCATION IN BUFFERED SUB-SAMPLING

	N_1=1	N_1>1
$T_t : T_h$	1 : 1	9 : 1
$T_{h,Cs}$	T_h	$(N_1\text{-}1)T_S$

designed for a minimum kT/C requirement, the binary array and connections still occupy a large area. Flatting interleaving with many of them at the back-end originates substantial area expansion, ultimately leading to significant interconnection mismatch between the C_S and each sub-DAC. Considering the layout symmetry, here, N_2 is set as 2, while the number of sub-sampling units at the 1st hierarchy would rise. As C_S is a large unit rather than a DAC array, it costs less area overhead and layout complexity. Therefore, the routing can be optimized easily to reduce the mismatches.

Unlike the passive-sharing, to provide a fast signal transfer to the sub-ADCs the power burden from an active buffer would be extremely high. By increasing the number of sub-ADCs, additional buffering time can be provided to each sub-channel to relax the buffer's BW. Table II lists the time allocation in each hierarchy with different values of N_1, where $T_{h,Cs}$ is the hold time on C_S. When N_1 is equal to 1, the front-end sampling and the sub-ADC's sampling needs to be performed separately with each occupying 0.5 T_S for BW optimization. The tracking time can be extended to 0.9 Ts at $N_1>1$.

Fig.6 presents the $R_{out,0}$ from the front-end buffer versus different T_t and N_1, where the corresponding power dissipation can be obtained. The sub-ADC's sampling duration ($T_{t,sub}$) is determined by $Min\left(T_{h,Cs}, N_1N_2T_S - T_{Conv}\right)$, where T_{Conv} is the conversion time in the sub-ADC. The 2nd term represents the available sampling time provided by the back-end quantizer. The buffered sub-sampling network can also be modeled as a 2nd-order RC filter as shown in Fig. 3(b). Similarly, Fig.7 plots the corresponding $R_{out,1}$ for the required settling accuracy under a different sub-sampling time $T_{t,sub}$ and a number of sub-channels N_2. According to the plot we can obtain the power dissipation from the sub-sampling buffers. Both of the front-end and the sub-sampling buffers contribute the total power dissipation. With different combinations of N_1 and N_2 the power for the buffered sub-sampling scheme is also shown in Fig. 5. Comparing two schemes with 12 sub-channels, the buffered sub-sampling demonstrates poorer power efficiency due to stringent buffers' BW requirements. Traded with the increasing the number of sub-ADCs ($N_1\times N_2>12$), its power efficiency becomes better, but it also rises up the power budget for back-end quantizer. Besides, we found that N_1 equal to 1 or $N_1\times N_2$ demonstrate worse power efficiency, because the front-end buffer dominates the overall power dissipation due to less tacking time or maximized parasitics. Although the passive sharing requires a 4-fold larger sampling capacitor for the same SNR, to achieve fast signal transfer, it still exhibits better power efficiency than its counterpart. However, the signal loss in the passive sharing also increases the noise requirement for the back-end quantizer which needs to invest more power to compensate it. The trade-off can

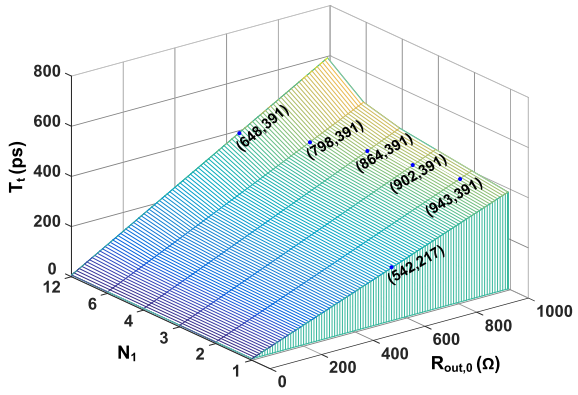

Fig. 6. T_t v.s. $R_{out,0}$ from the front-end buffer under different N1 in buffered sub-sampling, plotting the cases in 12 sub-channels in Fig.5.

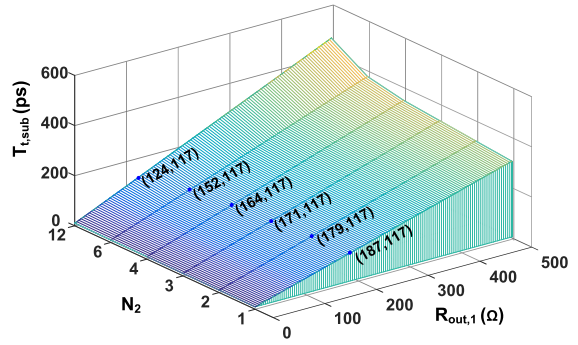

Fig. 7. $T_{t,sub}$ v.s $R_{out,1}$ from the sub-sampling buffer under different N_2, plotting the cases with 12 sub-channels in Fig.5.

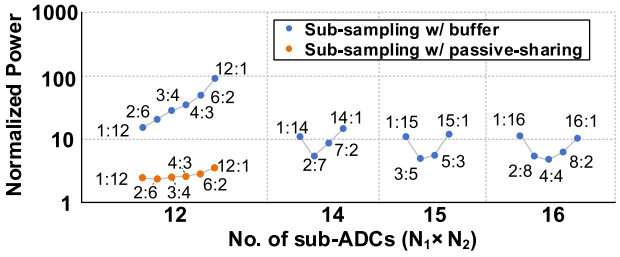

Fig. 8. Power dissipation in the capacitor matching limited scenario under different combinations of N_1 and N_2 by using passive sharing and buffered sub-sampling.

be balanced by carefully designing the back-end sub-ADC, i.e., implementing the quantizer with residue amplification, such as a pipelined-SAR architecture [18], which can achieve better power efficiency than a pure SAR ADC [21], especially for high resolution.

Secondly, we discuss the capacitor matching limited scenario. Assuming the two schemes target for the same sampling accuracy of 62 dB, we implement in this design the same C_{DAC} and C_S, e.g., 400 fF, for matching purpose. The other parameters remain unchanged as in the previous analysis. Fig. 8 illustrates the comparisons in terms of power consumption between the two schemes, where the passive sharing

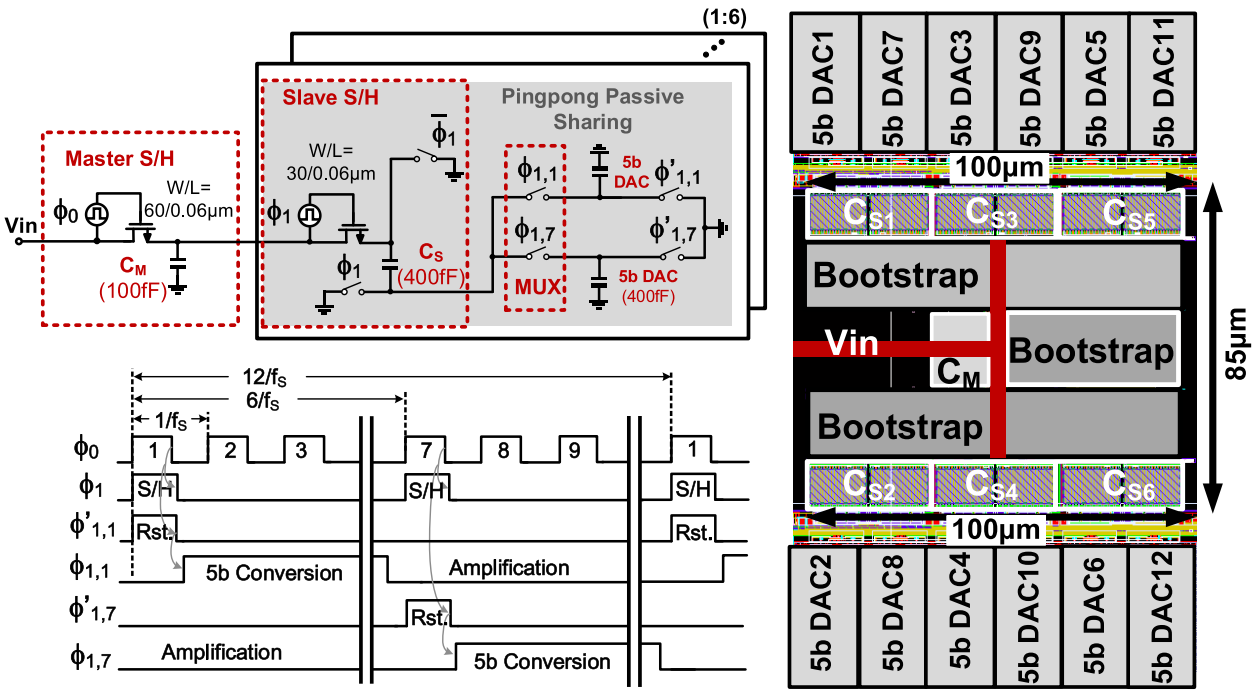

Fig. 9. (a) Proposed sampling network and its timing diagram; (b) Layout design of the proposed sampling network.

scheme reveals at least a 28 % better power advantage than all the cases with buffered sub-sampling.

III. Proposed MS S/Hs With Passively Shared Sub-Sampling

Fig. 9(a) depicts the sampling network containing MS S/Hs based on the bootstrapped switched-capacitor topology. The input signal is 1.4 V_{p-p} differentially and a 50Ω termination resistor is placed on-chip to match the signal source impedance. A MS sampling is used to avoid time skews and the 1st hierarchy contains 6× sub-S/H units. The design synchronizes the sampling time instants according to a 2.3 GHz clock (ϕ_0) which suppresses time mismatch without the need of a low skew clock or time-calibration. Two sub-ADCs shares one sub-S/H unit where the signal passes passively through a mux to the 5b DAC in the sub-ADC. During the sampling phase ($\phi_0 = \phi_1 = \phi_{1,1} = 1$) both C_M and C_S track V_{in}, while the DAC in the sub-ADC-1 is reset to Gnd. Before the sub-ADC starts the conversion,$\overline{\Phi_1}$ and $\phi_{1,1}$ are set to high. Thus, the sampled signal is shared passively from the bottom-plate of C_S to the DAC. $\overline{\Phi_1}$ and $\phi_{1,1}$ are kept high until the 5b conversion completes, which significantly reduces the signal-dependent charge injection and clock feedthrough from the mux as the residue is close to common mode voltage (V_{cm}) at the end of the conversion. After the conversion the sub-channel 1 amplifies the residue to the 2nd stage, meanwhile the MS S/Hs together with sub-channel 7 start the next incoming sample. The bottom-plate sharing [12] provides a good signal isolation to sub-ADCs, whereas it requires a large number of sampling switches. In this design the passive sharing is achieved at the bottom of the sub-S/H capacitor and the top-plate of the sub-DAC, which decouples the sub-DAC from the master S/H with less design complexity. Another benefit is associated with the layout that can be very compact thus reducing the interconnection mismatch and gradient effect. As shown in Fig. 9(b) the area of the MS S/Hs is only 0.0085 mm^2 achieved by two key factors. Firstly, the number of sub-S/Hs is halved when compared with the sub-ADCs. Secondly, C_S is a large single unit of 400 fF rather than a binary-weighted array, which occupies only 1/3 of the area of the 5-bit DAC designed with similar capacitance.The passive sharing potentially causes the gain mismatch among the sub-ADCs; therefore, the back-end sub-ADC is implemented with a pipelined SAR architecture where the sampling capacitance contains less number of units leading to a small area overhead. The symmetrical interconnection between the sub-S/H and its sub-DACs counterparts suppress the gain spurs below −67 dB, according to measurement results. To compensate the signal loss due to passive sharing a power efficient pipelined SAR architecture is implemented for back-end quantization. Consequently, under a signal swing of 1.4 V_{p-p}, this work still achieves a SNDR of 50.5 dB at a low input frequency. The ratio between C_S and DAC is designed with 1:1, thus, the signal full-scale of the sub-ADCs is ∼0.7 V_{p-p} after passive sharing. The total input capacitance is 500 fF including C_M and C_S only. Further, providing an input signal swing higher than the supply rail of the ADC is highly desirable in a sub-micron technology as the shrinking of the device intrinsic gain and supply level increase the design difficulties to meet a high resolution target. Therefore, the general solution to obtain good sampling SNDR is to use multiple supply levels for different building blocks [19], [20], e.g. the input buffer usually designed with much high supply level (3.3V) can offer a signal swing larger than the supply rail (1.2V) of the

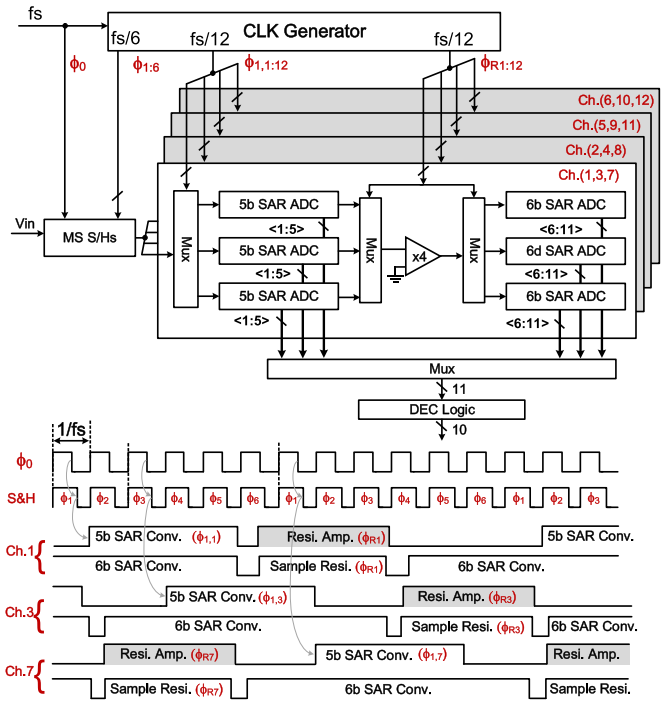

Fig. 10. Overall ADC architecture and its timing diagram.

back-end ADC. The input buffer is necessary not only for buffering the signal to ADC but also providing good signal isolation for the front-end analog circuitries to avoid the kick-back from the sampling switch.

IV. ADC Architecture

Fig. 10 shows the overall ADC architecture, consisting of proposed sampling front-end followed by 12-way TI sub-ADCs. Each channel operates at near 192 MS/s for an aggregating 2.3 GS/s. The MS S/Hs output is passed through a MUX to the corresponding sub-ADC for 10 bit quantization. The sub-ADC is implemented with a two-stage pipelined-SAR architecture [18]. The 1st stage resolves the coarse 5 bit and then the residue is amplified by 4 to the 2nd stage, which determines the fine 6 bits. Two stages have 1 bit overlapping for digital error correction (DEC) to relax the comparison and offset accuracy in the 1st stage. For power and area efficiency the Op-Amps are fully utilized, each of which is shared by 3 sub-ADCs according to their time allocation for residue amplification. Consequently, the overall ADC requires only 4 Op-Amps for total 12 sub-channels.

V. Circuit Implementations

A. Boosting Capacitor Sharing Technique

The slave switches are also bootstrapped for better sampling bandwidth and linearity, but the boosting capacitor has a large area overhead. Fig. 11 shows the design of the bootstrapped circuit for the slave switches. The boosting capacitor and its reset circuit are shared among the channels for layout compactness. To implement this M1, M2 and M4 are added to control the gate of M3. When channel-1 is activated to track

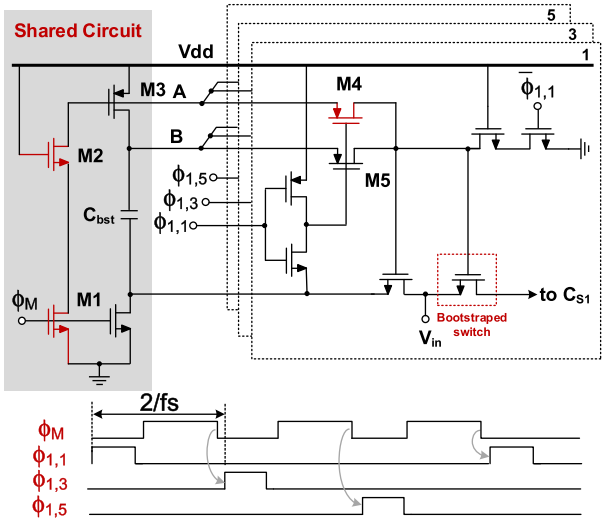

Fig. 11. Bootstrap design for the slave switches using the proposed boosting capacitor sharing technique.

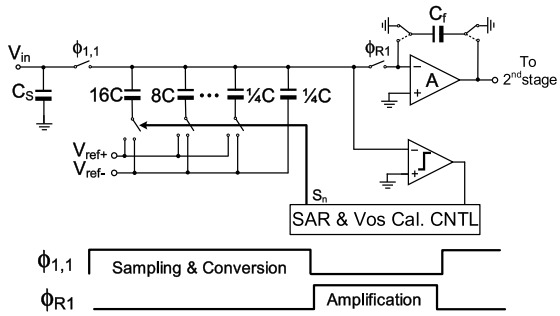

Fig. 12. The 1st stage sub-SAR ADC.

the input ($\phi_M = 0$, $\phi_{1,1} = 1$), M4 and M5 are both enabled, which disables M3 and provides a level shift of $V_{dd}+V_{in}$ to the gate of the slave switch. After the tracking phase ϕ_{M1} goes high, the gate voltage of M3 is pulled down to Gnd that resets the boosting capacitor to V_{dd}. The transistor M2 avoids the overstress of M1. According to the time slot the odd and even phases share one boosting capacitor, respectively. The boosting capacitor C_{bst} is implemented with a large unit of 400 fF. The proposed scheme saves two C_{bst} units achieving 50 % area reduction when compared with the conventional structure.

B. 1st & 2nd -Stage ADC Designs

The 1st stage SAR ADC is shown in Fig. 12, which consists of a 7-bit binary-weighted DAC array, a comparator and an Op-Amp for residue amplification. The 1st stage determines the coarse 5 bits. The extra 2-bit implemented in the DAC are for compensation of the offset; therefore, its matching accuracy is not necessary to attain the full resolution. The sampling capacitor Cs passively shares the input signal (V_{in}) to the DAC, and it is kept connected to V_{cm} to serve as a capacitive-divide of the reference voltages during the conversion. Once a 5-bit residue is generated, the offset code will be firstly subtracted via the DAC to guarantee the residue within ±tLSB/2 of the 1st stage that is ±15.6 mV. Then, with the

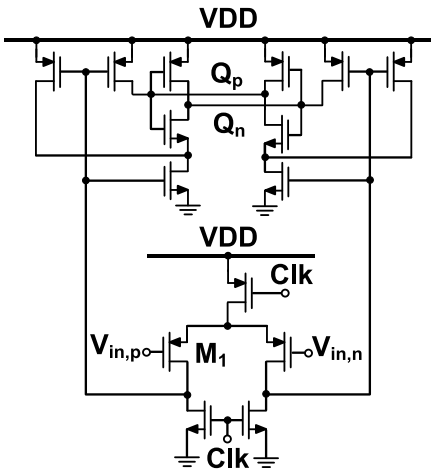

Fig. 13. Schematic of dynamic comparator.

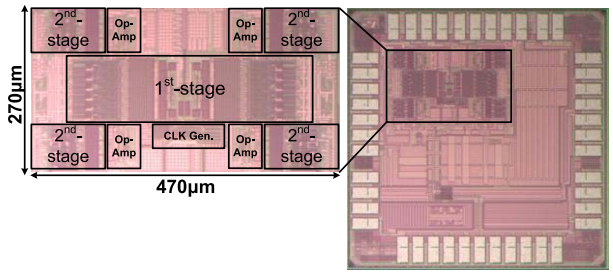

Fig. 14. Die microphotograph of the ADC.

amplification phase Φ_{R1} enabled it will amplify the residue to the 2nd stage SAR ADC. The switchback switching [8] is used that requires two reference voltages V_{ref+} and V_{ref-} setting as 1 and 0 V, respectively. The unit capacitance is 11 fF resulting in the total capacitance of 352 fF.

The Op-Amp is implemented with low power requirements, which adopts a telescopic topology with gain-boost [21]. It achieves a sufficient DC gain of 66 dB and a GBW of 2 GHz for the design requirements (at TT corner and 27 ^{o}C).

Since the 1st stage quantizes 5-bit, the residue would be within $1/2^5 V_{FS}$. With the stage-gain of 4 and 1 bit overlapping between two stages, the full-scale of the 2nd stage should be $1/2^2$ V_{FS}. We use a similar capacitive attenuator as in [22] to scale down the reference. Two stages share the same reference voltages, generated externally with 800 pF on-chip decoupling capacitor consuming an area of $\approx$0.06 mm^2. A smaller unit capacitor of 3 fF is used in the 2nd stage DAC, and its output equivalent capacitance as the loading of the Op-Amp is 138 fF.

C. Comparator Design

Since SAR ADCs in both stages are used to quantize the offsets during the calibration period, the calibration accuracy depends on the resolution of the comparator. Both stages engage a double-tail dynamic comparator [23], [24] (Fig.13) achieving low noise with good power efficiency. The input-referred noise voltages of the comparator in the 1st and the 2nd stages are 1.9 and 0.8 mV$_{rms}$, respectively. Thanks for the redundancy and stage gain their accuracies are sufficient for the quantization, but the offset calibration accuracy is still limited by the comparator noise as the offset is measured only once. The voting scheme is an effective solution to further reduce the offset spurs while it calls for additional digital power and area overhead.

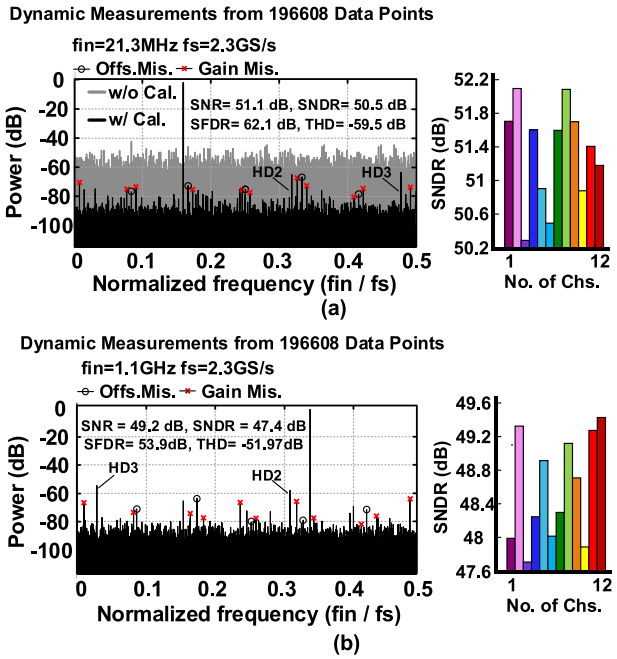

Fig. 15. Measured FFTs from 196608 data outputs and decimated by 125; (a) without offset calibration and with offset calibrations @f_{in} = 21.3 MHz; (b) with offset calibration @Nyquist input.

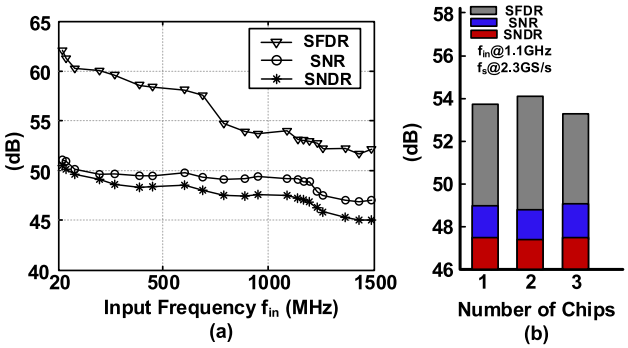

Fig. 16. (a) Measured dynamic performance vs. input frequency; (b) Multi-samples measured @Nyquist input frequency.

VI. Measurement Results

The ADC was fabricated in a 1P7M 65 nm CMOS process and Metal-oxide-Metal (MOM) capacitors. Fig. 14 shows the die photograph of the design; the ADC core occupies 0.13 mm^2 (270 μm $\times$ 470 μm) with the offset calibrations introduced in section IV. Fig. 15 (a) illustrates the measured output spectrums @ 21.3 MHz input frequency before and after offset calibrations as well as the SNDRs of the total 12 channels. The offset mismatches at the 1st stage cause a large residue error which results in the SNDR of only 21 dB. After

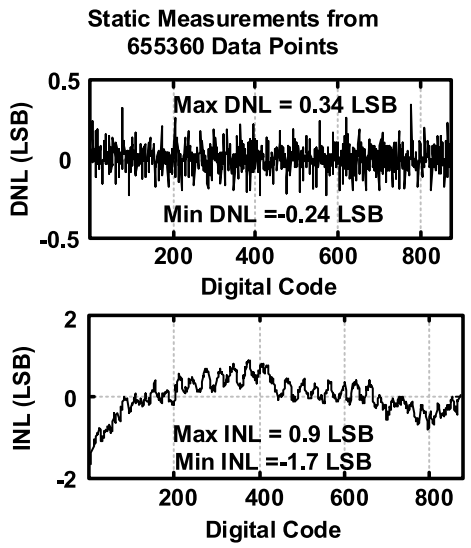

Fig. 17. Measured static performance after offset calibration.

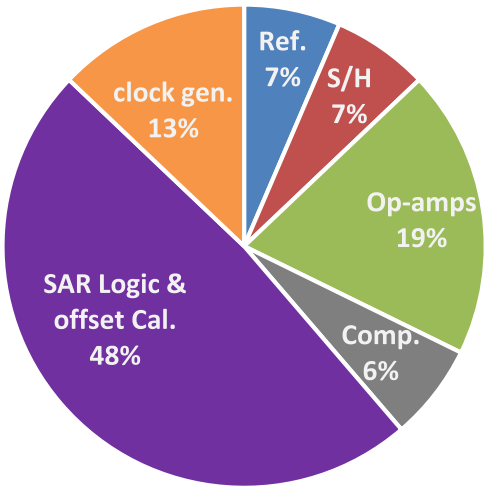

Fig. 18. Simulated power breakdown of the ADC.

offset calibrations the ADC resumes to its normal operation, achieving a SNDR of 50.5 dB. The 3rd harmonic limits the *spurious-free dynamic range* (SFDR) to 62.1 dB partially contributed by the sampling distortion in the sub-S/Hs. The spurs due to gain and offset mismatches are below −67 dB. The average SNDRs of the total 12 channels is 51.3 dB. Fig. 15(b) plots the output spectrum @Nyquist input and the corresponding SNDRs of 12 channels. The achieved SNDR is 47.4 dB. The 3rd harmonic dominates the SFDR and the spurs due to bandwidth/time mismatch are below −64 dB. Fig. 16 plots the swapping of the input frequency and the measured performance of multi-samples @Nyquist input. According to simulation we design the clock to be 150 fs_{rms} that will limit the SNR of our ADC to ∼54 dB at 1.5 GHz input. Since the measured SNR is lower than the expectation, it implies that other circuit non-idealities dominate the performance. An estimation of the total sampling jitter is 500 fs_{rms}. Fig. 17 shows the static performance after offset calibration, with the *differential-nonlinearity* (DNL) and *integral-nonlinearity* (INL) compensated within 0.34 LSBs and 1.7 LSBs, respectively. The power consumption is 31 mW at a 1.2 V supply, including 12 mW analog power from the sampling front-end, Op-Amps and comparators and 19 mW digital power from the SAR logic, calibration and clock generator. Fig.18 illustrated the power breakdown according to simulations. The ADC achieves a FoM of 49 and 69 fJ/conversion-step @ DC and Nyquist input, respectively. Table III shows a performance summary and benchmark with state-of-the-art ADCs with > 2 GS/s conversion rate and similar resolution. This work achieves a comparable SNDR with less calibration overhead, leading to a compact area of 0.19 mm^2 with on-chip calibration and decoupling capacitor for the reference. When compared with the time calibrated TI-SAR ADC [3], this work still reaches a comparable conversion accuracy and FoM under a smaller input swing.

TABLE III
BENCHMARK WITH STATE-OF-THE-ART WORKS

	ISSCC' 11 [5]	VLSI' 12 [3]	ISSCC' 13 [6]	ISSCC' 15 [4]	This Work
Architecture	TI SAR	TI SAR	TI SAR	TI PSAR	TI PSAR
Technology (nm)	65	65	65	28	65
Resolution (bit)	10	10	11	10	10
fs (GS/s)	2.6	2.8	3.6	5	2.3
fin (GHz)	1.3	1.4	1	2.35	1.1
Supply (V)	1.2/1.3/1.6	1.2	1.2/2.5	1	1.2/1
SNDR (dB)	48.5	48.2	50	46	47.4
Area (mm^2)	5.1	0.18	7.4	0.45	0.19*
Power (mW)	480	44.6	795	150	31
FoM_{Walden} (fJ/c)	851	76	862	96	69
Time Cal.	No	Yes	No	Yes	No
Gain Cal.	Yes	Yes	Yes	Yes	No
Offset Cal.	Yes	Yes	Yes	Yes	Yes
Cal. On-chip	Yes	No	Yes	No	Yes

*** including the reference decoupling capacitance and offset calibrations**

VII. CONCLUSION

This work reports a 2.3 GS/s 10-bit 12-way TI ADC in 65nm CMOS technology with all calibrations on-chip. The proposed MS S/H with passively shared sub-sampling obtains fast signal transfer to back-end sub-channels and good signal isolation. The proposed hierarchical sampling and boosting capacitor sharing technique achieves layout compactness that can effectively suppress the skew mismatches. The mathematic model demonstrates also a better power efficiency of the passive-sharing when compared it with the active buffer in both noise and matching limited designs. Combining all these circuit solutions the ADC achieves 47.4 dB SNDR at Nyquist input when operating at 2.3 GHz sampling rate.

REFERENCES

[1] N. Le Dortz *et al.*, "A 1.62 GS/s time-interleaved SAR ADC with digital background mismatch calibration achieving interleaving spurs below 70 dBF," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 386–387.

[2] S. Lee, A. P. Chandrakasan, and H. S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.

[3] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW time-interleaved ADC achieving 50.9 dB SNDR and 3 dB effective resolution bandwidth of 1.5 GHz in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 971–982, Apr. 2013.

[4] M. Brandolini *et al.*, "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.

[5] K. Doris, E. Janssen, C. E. Janssen, A. Zanikopoulos, and G. van der Weide, "A 480 mW 2.6 GS/s 10b time-interleaved ADC with 48.5 dB SNDR up to Nyquist in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2821–2833, Dec. 2011.

[6] E. Janssen *et al.*, "An 11 b 3.6 GS/s time-interleaved SAR ADC in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 464–466.

[7] Y. Zhu *et al.*, "A 10-bit 100 MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[8] G. Y. Huang, S.-J. Chang, C.-C. Liu, and Y.-Z. Lin, "10-bit 30-MS/s SAR ADC using a switchback switching method," *IEEE Trans. Very Large Scale Integr. (TVLSI) Syst.*, vol. 21, no. 2, pp. 584–588, Mar. 2012.

[9] C.-C. Liu, C.-H. Kuo, and Y.-Z. Lin, "A 10 bit 320 MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20 nm CMOS," *IEEE J. SolidState Circuits*, vol. 50, no. 11, pp. 2645–2654, Nov. 2015.

[10] S. M. Louwsma, A. J. M. van Tuijl, M. Vertregt, and B. Nauta, "A 1.35 GS/s, 10 b, 175 mW time-interleaved AD converter in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 778–786, Apr. 2008.

[11] Y. Zhu, C.-H. Chan, S.-P. U, and R. P. Martins, "An 11 b 900 MS/s time-interleaved sub-ranging pipelined-SAR ADC," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 211–214.

[12] S. Le Tual, P. N. Singh, C. Curis, and P. Dautriche, "A 20 GHz-BW 6 b 10 GS/s 32 mW time-interleaved SAR ADC with master T&H in 28 nm UTBB FDSOI technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 382–383.

[13] L. Kull *et al.*, "A 90 GS/s 8 b 667 mW 64× interleaved SAR ADC in 32 nm digital SOI CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 378–379.

[14] L. Kull *et al.*, "Implementation of low-power 6–8 b 30–90 GS/s time-interleaved ADCs with optimized input bandwidth in 32 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 636–649, Mar. 2016.

[15] M. Gustavsson, *CMOS Data Converters for Communications*. Boston, MA, USA: Kluwer, 2000.

[16] T. Sundstrom, B. Murmann, and C. Svensson, "Power dissipation bounds for high-speed Nyquist analog-to-digital converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 3, pp. 509–518, Mar. 2009.

[17] B. Murmann, P. Nikaeen, D. J. Connelly, and R. W. Dutton, "Impact of scaling on analog performance and associated modeling needs," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2160–2167, Sep. 2006.

[18] Y. Zhu, C.-H. Chan, S.-W. Sin, S.-P. U, R. P. Martins, and F. Maloberti, "A 50-fJ 10-b 160-MS/s pipelined-SAR ADC decoupled flip-around MDAC and self-embedded offset cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2614–2626, Nov. 2012.

[19] A. M. A. Ali *et al.*, "A 14 Bit 1 GS/s RF sampling pipelined ADC with background calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, Dec. 2014.

[20] S. Devarajan *et al.*, "A 12 b 10 GS/s interleaved pipeline ADC in 28 nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 288–289.

[21] J. Zhong, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "Thermal and reference noise analysis of time-interleaving SAR and partial-interleaving pipelined-SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2196–2206, Sep. 2015.

[22] Y. Zhu, C.-H. Chan, S.-P. U, and R. P. Martins, "An 11 b 450 MS/s three-way time-interleaved subranging pipelined-SAR ADC in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1223–1234, Feb. 2016.

[23] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE ASSCC*, Nov. 2008, pp. 269–272.

[24] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 314–315.

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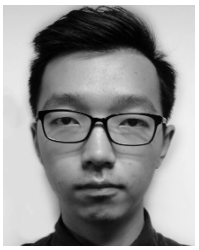

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Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's (five years), master's, and Ph.D. degrees, and the Habilitation degree for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively. He has been with the Department of Electrical and Computer Engineering, IST, TU of Lisbon (from 2013 the Universidade de Lisboa), since 1980.

Since 1992, he has been on leave from the IST, Universidade de Lisboa, and is also with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair-Professor since 2013. In FST, he was the Dean of the Faculty from 1994 to 1997 and he has been a Vice-Rector of the UM since 1997. In 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as a Vice-Rector (Research) until 2018. Within the scope of his teaching and research activities he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 44 theses, Masters (21), and Ph.D. (23). He has co-authored seven books and 11 book chapters; 30 Patents, USA (28) & Taiwan (2); 430 papers, in scientific journals (140) and in conference proceedings (290); and other 63 academic works, in a total of 541 publications. He was a Co-Founder of Chipidea Microelectronics (Macao) [now Synopsys] in 2001 and 2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the First in Engineering in Macao), being its Founding Director.

Prof. Rui Martins was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, in 2010, being the only Portuguese Academician living in Asia. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. He was the Founding Chairman of both the IEEE Macau Section (2003–2005) and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (2005–2008) [2009 World Chapter of the Year of the IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS–APCCAS'2008, and was a Vice-President for Region 10 (Asia, Australia, and the Pacific) of IEEE CASS (2009–2011). Since 2011, he was a Vice-President (World) Regional Activities and Membership of the IEEE CASS (2012–2013), and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS (2010–2013), nominated as a Best Associate Editor of T-CAS II for 2012 to 2013. Plus, he has been a member of the IEEE CASS Fellow Evaluation Committee (2013, 2014, and 2019), and CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–the Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference–ASP-DAC'2016 and received the IEEE Council on Electronic Design Automation Outstanding Service Award 2016. He was a Nominations Committee Member of the IEEE CASS (2016–2017) and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In representation of UM was one of the Vice-Presidents (2005–2014) and the President (2014–2017) of the Association of Portuguese Speaking Universities.