A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration

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***Abstract*— This paper presents a 2× time-interleaved 7-b 2.4-GS/s 1-then-2 b/cycle SAR ADC in 28-nm CMOS. The process-voltage-temperature sensitivity of a multi-bit SAR architecture has been improved by the proposed 1-then-2 b/cycle scheme with background offset calibration. With the pre-charge reduction scheme, the traditional large switching energy and time consuming pre-charge operation have been removed, which simultaneously enables a simple control logic without the need of a V_{cm} voltage. Besides, a background offset calibration is implemented on chip which does not involve any extra phase or calibration input signal. Its operation is well embedded within the 1-then-2 b/cycle architecture, thus leading to a very minimal modification of the ADC core. With an improved fringing DAC structure and a high-speed dynamic logic circuit, a single-channel ADC can work at 1.2 GS/s under a 0.9-V supply. Using two-way time interleaving, the prototype samples at 2.4 GHz and consumes 5-mW power including the on-chip background offset calibration. It exhibits a 40.05-dB SNDR at Nyquist, leading to a Walden FoM of 25.3 fJ/conversion step. Measurement results show that the SNDR of the ADC can be kept above 38 dB at 2 GS/s under a wide range of temperature, supply, and input common-mode variation.**

***Index Terms*— 1-then-2 b/cycle SAR ADC, analog-to-digital conversion, background offset calibration, multi-bit/cycle SAR ADC, time interleaving.**

I. Introduction

MODERATE resolution above gigahertz ADCs is in high demand for wireless communications and Ethernet networks. They often require an ADC with more than 6-b ENOB at Nyquist, sampling at over 1 GHz, consuming low power and occupying a small chip area. Besides, such type of ADCs are often adopted for highly time interleaving [1] where its immunity to process-voltage-temperature (PVT) variation becomes a critical concern. Conventionally, flash ADCs are applicable for this range of specifications. With a time-based folding technique in the advanced technology node, Miyahara *et al*. [2] achieves a Walden FoM of 206 fJ/conversion step at 2.2 GS/s. However, the design of moderate resolution comparator becomes challenging in fine technology nodes, thus architectures with massive comparators like flash ADCs are less attractive. Even targeting for a 6-b ENOB, the noise from the comparator still needs to be carefully addressed due to the reduction of intrinsic gain and supply voltage. This makes the size of the comparators being undesirably enlarged and eventually increases the power consumed by the high-speed clock network.

Some reported speed enhancement techniques, such as comparator interleaving [3] and multi-bit per cycle conversion scheme [4]–[6], allows a single-channel SAR ADC targeting to such specifications while simultaneously maintaining its superior energy efficiency. The multi-bit SAR ADC relies on its parallelism to speed up the conversion and resolve more than 1 b in each comparison. Therefore, the same bit resolution can be achieved with fewer comparisons when comparing it with the 1 b/cycle scheme. This relaxes the size scaling (for speed) of the comparators, consequently saving power. On the other hand, the extra hardware and operation phase can lead to diminished returns. First, the multi-bit SAR ADC has more than one DAC and requires a pre-charge operation to generate different reference levels for the comparison, which increases the burden of the reference buffers and logic complexity, leading to a higher PVT sensitivity on the conversion speed. In [5], the multiple reference levels are generated through a dedicated DAC where the subtraction is accomplished with an additional input pair transistor in the comparator. These not only induce extra mismatch between the DACs but also add noise in the comparator. Second, the offset among the comparators requires calibration running in the background in order to keep track of the VT variations. Consequently, the actual benefits of the conventional multi-bit SAR ADC become very minor.

In this paper, we address the above issues through the utilization of different techniques under the scope of a 1-then-2 b/cycle SAR architecture [7]. We remove all the pre-charge phase and operation with the proposed pre-charge reduction scheme (PRS). It can be realized by a very simple logic without the need of a V_{cm} voltage and achieves a >40% reduction on the maximum and average switching energy

Manuscript received July 26, 2017; revised September 29, 2017 and November 27, 2017; accepted December 7, 2017. Date of publication January 18, 2018; date of current version February 21, 2018. This work was supported in part by NSFC under Grant 61604180, in part by Macau Science and Technology Development Fund under Grant 117/2016/A3, and in part by the University of Macau under Research Grant MYRG2015-0086-AMSV. This paper was approved by Associate Editor Jeffrey Gealow. *(Corresponding author: Chi-Hang Chan.)*

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Digital Object Identifier 10.1109/JSSC.2017.2785349

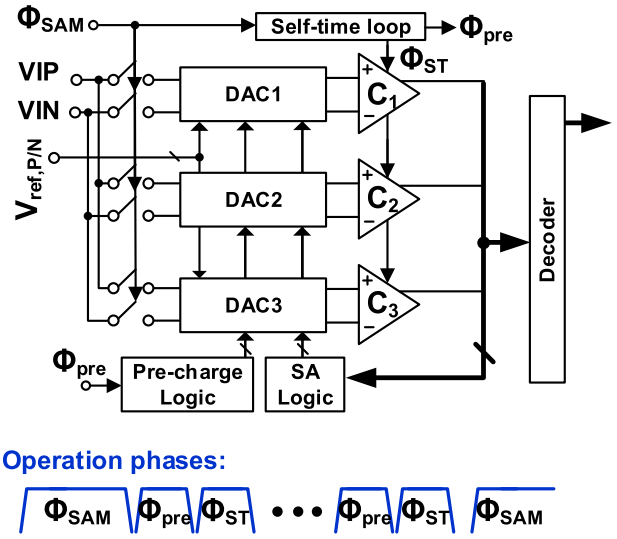

Fig. 1. Conventional 2 b/cycle block diagram and operation phases.

when comparing it with the conventional V_{cm}-based multi-bit switching technique [8]. Besides, we introduce a background offset calibration whose operation is well embedded with the proposed architecture. It does not require any extra calibration signal and phase for sensing the offset, and runs synchronously with the SAR conversion in the background. We applied all the above techniques in the proposed 1-then-2 b/cycle SAR architecture to obtain a 7-b two-way interleaved ADC in 28-nm CMOS. The prototype achieves 2.4 GS/s with a 0.9-V supply exhibiting an SNDR above 40 dB at Nyquist input. The power consumption is only 5 mW including the background offset calibration, resulting in a Walden FoM of 25.3 fJ/conversion step. The organization of the remaining part of this paper is as follows. Section II presents a brief review and discussion on PVT sensitivity of a conventional multi-bit SAR ADC. Section III introduces the proposed 1-then-2 b/cycle SAR ADC. Section IV describes the switching method and the energy, then comparing them with the conventional approach. Section V discusses the background offset calibration technique and Section VI details the circuit and DAC structures. Section VII reports the measured results and finally we draw conclusions in Section VIII.

II. Background and PVT Sensitivity Analysis of Multi-Bit SAR ADCs

A. Conventional Multi-Bit SAR ADC Architecture

Fig. 1 illustrates the block diagram of the conventional 2 b/cycle SAR ADC and its operation phases. It consists of three comparators (C_1–C_3), three DAC arrays, a 2 b/cycle SA logic, a pre-charge logic, a self-time loop, a sampling front end, and a decoder. The operation phases are: sampling (Φ_{SAM}), pre-charging (Φ_{pre}), and decision (Φ_{ST}). Since each comparison resolves 2 b, two reference voltages need to be generated through the DAC_1 and DAC_3 during Φ_{pre}, which together with DAC_2 produce the residual voltages according to comparators' decisions at Φ_{ST}. The pre-charge phase (Φ_{pre}) in the conventional multi-bit operation leads to extra time (in the DAC settling and logic), hardware and power overhead. Such overheads not only degrade the conversion efficiency and speed but also render the architecture to be more sensitive to PVT variations because of additional phases and logic operations. Besides, parallel conversion requires multiple comparators, resulting in offset mismatch. To save power, one can apply calibration techniques [5], [6]; however, they often work in the foreground which does not tolerate VT variations in deep sub-micrometer technologies even in moderate resolution designs. While background offset calibrations require extra hardware [9] or operation phases [3], they also degrade the conversion efficiency.

B. Synchronous Versus Asynchronous and PVT Variation

The SA loop in the multi-bit SAR ADCs is often synchronous [4], [6]. Even though an asynchronous architecture [10] can be obtained by sensing multiple comparators' output, it does not exhibit much benefit as it can be shown next. Considering the 2 b/cycle scheme with three comparators, the best time saving condition is at a peak input value (V_{FS}). The saving of the conversion time can be expressed by

$$\left.\frac{T_{asyn,2b}}{T_{syn,2b}}\right|_{best} = \frac{\frac{n}{2}\cdot \ln V_{FS} - \sum_i^{n/2-1} \ln 2^{2i} V_{LSB}}{\frac{n}{2}\cdot \ln \frac{V_{FS}}{V_{LSB/2}}} \approx 0.57 \quad n = 6, 8 \ldots \quad (1)$$

where V_{FS} is the full swing of the ADC and n is the number of bits resolution. While the savings are slightly worse than the 1 b/cycle asynchronous scheme, it still achieves a >40% speed enhancement on the conversion time. However, it is obviously too optimistic just to consider the best case scenario. Each comparator corresponds to a set of different input values in the worst case situation, where the inputs make the residual voltage having alternative polarities in each comparison. The critical input for comparators C_1, C_2, and C_3 are around $-1/4$ V_{FS}, $\pm 1/8$ V_{FS} and $+1/4$ V_{FS}, respectively. The time saving can be determined by

$$\left.\frac{T_{asyn,2b}}{T_{syn,2b}}\right|_{worst} = \frac{\ln \frac{V_{FS}}{1.5V_{LSB}} + \ln \frac{V_{FS}}{2.5V_{LSB}} + \cdots \ln \frac{V_{FS}}{\max(1/(4\cdot 2^n), 0.5V_{LSB})}}{\frac{n}{2}\cdot \ln \frac{V_{FS}}{V_{LSB/2}}} \approx 0.81 \quad \text{where } n = 6, 8 \ldots \quad (2)$$

The derivation procedure of (1) and (2) is similar to [10] while here we consider the 2 b/cycle operation. The saving in the worst case for the asynchronous operation is less than 20%. It is worth highlighting as well that the probability of the comparators to encounter the worst case is around 3 times higher in the 2 b/cycle than in the 1 b/cycle, which makes the result in (2) more reliable. The extra logic controls and routing for the three comparators' outputs also lead to less savings. Plus, when considering the timing overhead from the pre-charging and sampling, the actual speed improvement will be very minimal.

For low-power operation, rather than utilizing a high-speed clock, the synchronous loop can be implemented by a self-time loop [11]. The interval between each phase would be controlled by a delay unit which drifts under PVT variations.

Such drift can be as large as 60% based on the simulation with the adopted technology, eventually slowing down the ADC according to its number of operation phases. Furthermore, even a 2 b/cycle SAR ADC only requires $n/2$ comparisons to accomplish n-bit, its total number of operation phases are n, which is the same as an n-bit 1 b/cycle SAR ADC, due to the extra pre-charge phases. This not only slows down the ADC but also induces a higher penalty under PVT variations.

C. Resolution Versus VT Variation

Unlike the interleaving SAR ADC, the offset voltage among comparators in the multi-bit SAR ADC causes large missing codes which cannot be recovered at the digital backend. Such offset either needs calibration or enlarging the size of the comparator to mitigate it. However, increasing the device size is very inefficient as it only has a square-root improvement on the mismatch voltage while proportionally raising the power consumption, thereby the digital calibrations [5], [12] would be a better choice as it mostly consumes dynamic power and scales with the technology. While contemplating a wide range of temperature and supply variation (±10%), the offset of the comparator can vary significantly and affect the performance of the ADC even when targeting a moderate ENOB (6–7 b). The offset mismatch of a transistor pair arises mainly from three parts which are the threshold, the current factor, and I_d/g_m mismatches [13]. While the temperature and voltage dependence of the threshold and current-factor mismatches is little [14] due to their highly technology-dependent characteristics, mismatch from the I_d/g_m has a dominated effect under VT variations. Fig. 2(a) shows ten Monte Carlo simulation results of the offset from the adopted comparator under −45 °C to 125 °C temperature variation, using 25 °C as a reference. The temperature drift coefficient is around 110 μV/°C with a small sizing comparator. The maximum drifted offset voltage can be as large as 20 mV which exceeds half LSB of 5-b resolution with a V_{FS} of 0.9 V. Fig. 2(b) illustrates the simulation results with ±10% supply voltage variation, using 0.9 V as a reference. The drifted offset is larger than half LSB of 7 b. Therefore, the offset needs to be calibrated in the background to keep track of VT variations in this design.

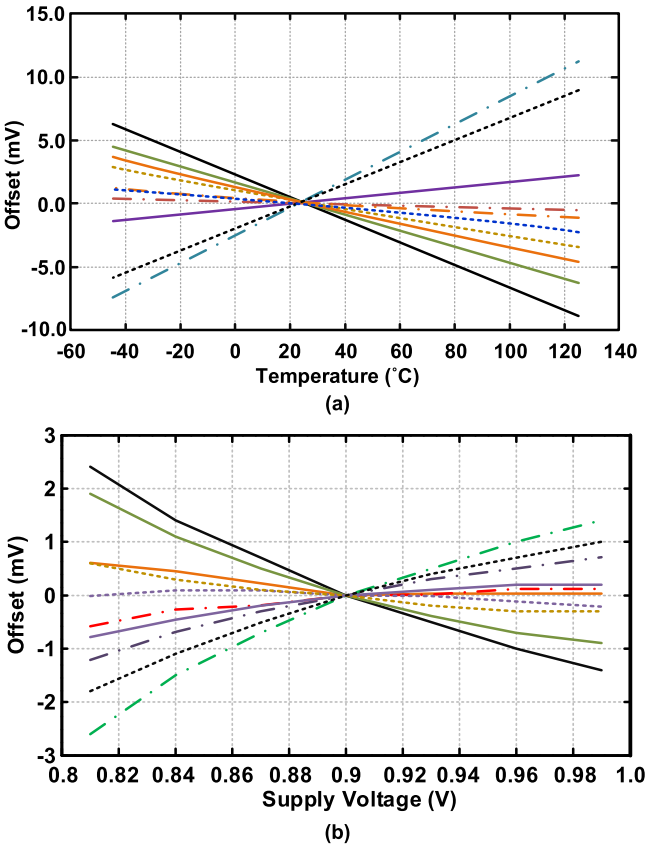

Fig. 2. Monte Carlo simulation of drifted offset. (a) Under temperature variation using 25 °C as a reference. (b) Under supply voltage variation using 0.9 V as a reference.

III. Proposed 1-Then-2 b/Cycle SAR ADC Architecture

Here, we propose a 1-then-2 b/cycle SAR architecture with background offset calibration to address the previous referred issues. Fig. 3 illustrates the block diagram of the 1-then-2 b/cycle SAR ADC. It consists of two DAC arrays, three dynamic comparators, an SAR logic, bootstrapped sampling front end, decoder, dynamic shift register, and background offset calibration circuit. Worth noting that is the fact that the hardware is the same as in the 2 b/cycle SAR architecture although the operations are different. Unlike the conventional multi-bit SAR ADC, the first comparison happens right after the sampling (Φ_{SAM}) without pre-charging. Even though it only gives 1-b resolution, three comparators are triggered at the same time which facilitates the background offset calibration. After the first comparison, the ADC resumes to 2 b/cycle operation and the 1-b decision controls the

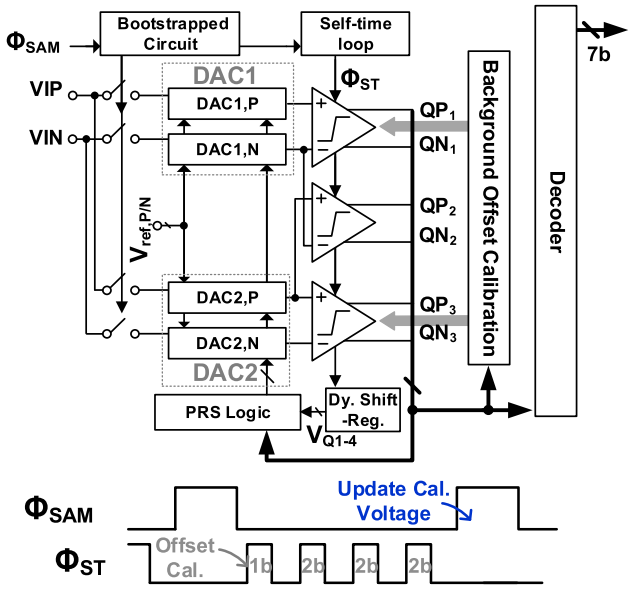

Fig. 3. Proposed 1-then-2 b/cycle architecture and its timing diagram.

DACs to generate a multi-bit residue (including the necessary reference charging). The second comparison resolves 2 b and a total four comparisons result in a 7-b resolution in this architecture. Furthermore, all the pre-charge operations in the conventional approach are eliminated and only the necessary charging are performed in the proposed PRS, which allows the 1-then-2 b/cycle architecture to have only $n/2 + 1$ operation phases for n-bit design. The PRS will be detailed in the

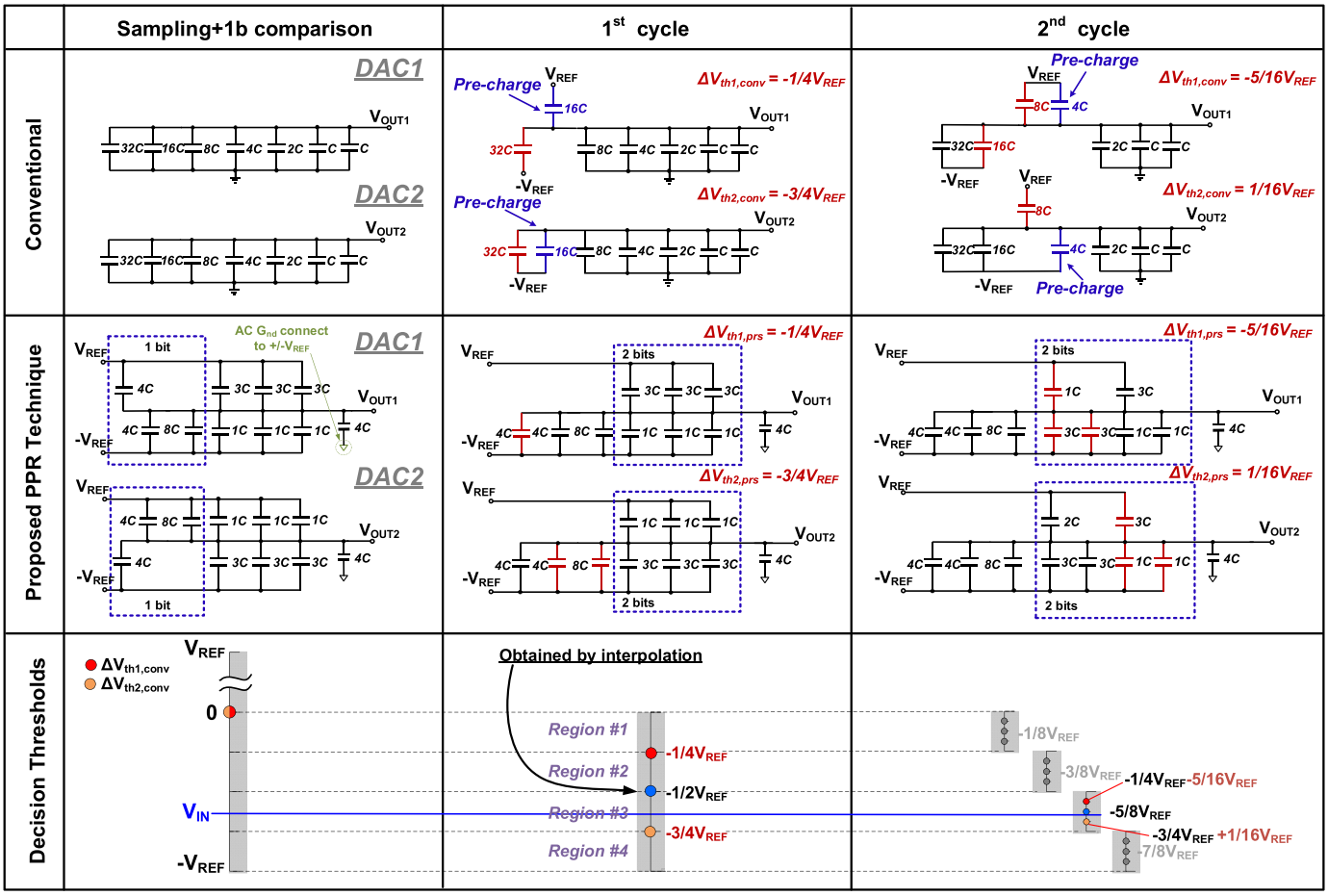

Fig. 4. First 3-b switching operation of DAC1 and DAC2 with conventional $V_{\rm cm}$-based switching and PRS switching.

following. All comparators' outputs are consequently decoded through the decoder to obtain a binary output. The background calibration senses the comparators' outputs during the first comparison and adjusts their offsets during the upcoming sampling phase.

IV. Switching Methods

A. Conventional Multi-Bit SAR Switching Methods

The conventional multi-bit SAR ADC requires a pre-charge phase to generate the reference voltage for the subsequent comparisons [4], [8]. In the first pre-charging, half of the capacitance in the DACs needs to charge/discharge to $V_{{\rm ref},P}/V_{{\rm ref},N}$ which potentially causes a large reference ripple and DNL errors at the transitions. Besides, the pre-charge phase is designed in a synchronous mode, which must happen after the comparison in order to prevent disturbing the current decision. Hence, enough timing margin needs to be left that makes the design being even more sensitive to the PVT variation. To remove these constraints, we propose two techniques. First, a 1-then-2 b operation removes the 1st pre-charging by directly comparing the inputs for the MSB decision. Second, we explore a pre-charge reduction scheme (PRS) that merges the necessary charging operation into the current decisions, thus avoiding the pre-charge activity for the next cycle.

In order to show the effectiveness and explain the PRS, we compare it with a conventional $V_{\rm cm}$-based multi-bit switching [8] in the first 3-b operations. In the example shown in Fig. 4, both schemes applied only after the first 1-b comparison (1-then-2 b operation), where the single-ended equivalent operation of both DACs is also illustrated. Conventionally in the $V_{\rm cm}$-based switching, the bottom plates of both DACs are set to a common-mode level ($V_{\rm cm}$) during the sampling. Since the sampled input $V_{\rm IN}$ is located at Region #3 and below the current decision threshold "0," the MSB's capacitor ($32C$) in both DACs is discharged to $-V_{\rm REF}$, while the MSB/2 capacitor ($16C$) in two DACs is pre-charged/discharged to $\pm V_{\rm REF}$ accordingly which sets the decision thresholds for the next cycle. Obviously, there exists an unnecessary switching for generating the decision threshold $\Delta V_{\rm th1,conv}$ in the 1st cycle as the same value can be obtained simply by discharging a $16C$ to $-V_{\rm REF}$. Then in the 2nd cycle, a $16C$ and $8C$ are switched according to the 2-b decisions. Afterward, a $4C$ is pre-charged, which shifts the thresholds for the next 2 b to Region #3, resulting in $\Delta V_{\rm th1,conv}$ and $\Delta V_{\rm th2,conv}$ being equal to $-5/16$ and $1/16$ $V_{\rm REF}$, respectively. It can be noticed that the $V_{\rm cm}$-based multi-bit switching [8] performs a trial-and-error procedure similar to the conventional 1 b/cycle SAR switching [15] as it processes the pre-charging regardless of the input value.

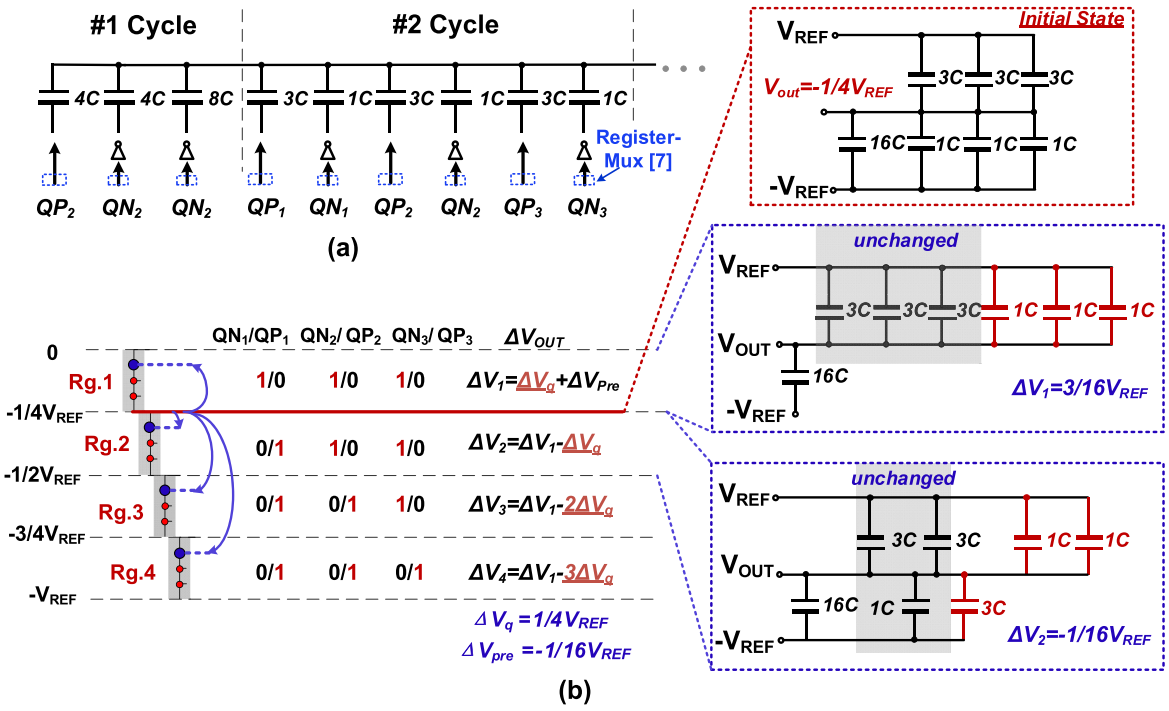

Fig. 5. (a) Control logics for the PRS. (b) Merged and shifted operation example.

B. Pre-Charge Reduction Scheme

Unlike just merging the DAC switching and pre-charging into one single logic operation in [6], we introduce a pre-charge reduction (PRS) scheme which enables simple logic operation and removes unnecessary pre-charging operation. The operation of our proposed PRS is also illustrated in Fig. 4, where each bit capacitors are split into several segments and controlled separately. In the sampling, a certain sequence is set at the bottom plate of the two DACs with $\pm V_{\mathrm{REF}}$. By splitting the MSB into two $4C$ and one $8C$, which are controlled by the complementary outputs of the current decision, the same decision thresholds can be achieved without any unnecessary switching. In this example, only an $4C$ is discharged to $-V_{\mathrm{REF}}$ to generates $\Delta V_{\mathrm{th1,prs}}$ of $-1/4V_{\mathrm{REF}}$, while others keep unchanged. In the 2nd cycle, the 2-b capacitors are split into three pairs of $1C/3C$ segment which are controlled by the current three complementary decisions from the comparators, respectively. Similarly, only the current bits' decisions are involved to obtain the same threshold as the conventional counterparts in the 2nd cycle (Fig. 4). Therefore, the operation of PRS is a pure decision based.

The DAC is rearranged in $2^{n-1}, 3 \times (2^{n-3}), 3 \times 2^{n-5}, \ldots, 4 \times 2^{0}$ and segmented by $2^{n-3}, 2^{n-5}, 2^{n-7}, \ldots, 0$, respectively (where n is the bit resolution), to enable the proposed switching method. Fig. 5(a) shows (part of) the control logics of the $\mathrm{DAC}_{1,p}$. It is worth mentioning that the output of the comparators can directly control the DACs without extra decoding logic. The only circuit inserted in the critical path is a multiplexer-embedded dynamic register (register mux) [7] which consumes a very small amount of power and works at high speed. We use the operation of the 2nd cycle in the previous example (Fig. 4) to explain how the pre-charging can be merged into a single decision-based switching operation as depicted in Fig. 5. Recalled that the initial threshold is set to $-1/4$ V_{REF} in the 1st cycle by discharging the MSB capacitors to $-V_{\mathrm{REF}}$. If the QN_{1-3} are all "1," implying that the input is located in the Region #1, only the 1C in the three segments are charged up to V_{REF}, resulting in a voltage change ΔV_1 of 3/16 V_{REF}. Indeed, the value is the summation of the minimum quantization step in the current cycle (ΔV_q) and the pre-charge step for the next cycle (ΔV_{Pre}), where they are 1/4 V_{REF} and $-1/16$ V_{REF}, respectively, in this case. As if there are a different between QN_{1-3} (case in Regions #2–#4), the output (V_{out}) is shifted down by a step of ΔV_q accordingly. With such merged and shifted operations, the generation of ΔV_{Pre} is embedded into a single switching, thus removing the extra pre-charge phase. Moreover, the operation is fully differential that guarantees a constant common-mode level and no V_{cm} is needed.

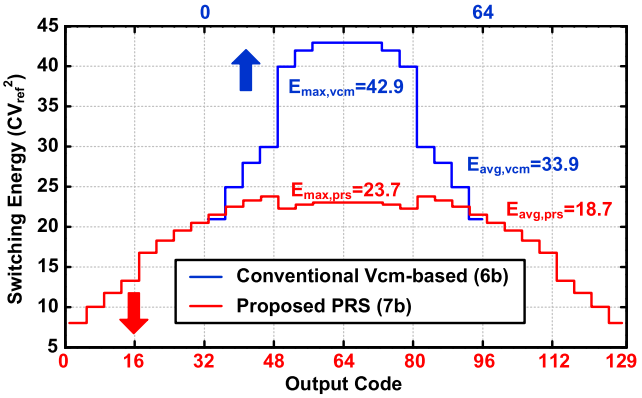

Fig. 6. Comparison of the switching energy between a conventional V_{cm}-based and the proposed PRS.

C. Switching Energy

The switching energy waste in pre-charge operation indeed is negligible in the high-speed designs. On the other hand, the reference and settling errors especially at the MSBs' transitions are critical which need additional time or power to suppress. The V_{cm}-based [8] switching energy can be categorized in two parts which are from the pre-charging and the residue switching. While pre-charging performs independently of the input, it consumes a constant energy (E_{pre}) of $1+\sum_{i}^{n/2-1} 2^{(n-2i+1)}CV_{ref}^2$ (where n is the bit resolution) in each output code. Such energy becomes an overhead from the multi-bit SAR ADC when compared with 1 b/cycle. The average switching energy of an n-bit multi-bit SAR with V_{cm}-based switching can be expressed as

$$E_{avg,vcm} = 2^{n-3} + \frac{1}{2^n}\sum_{i}^{n/2-1} 2^{(2n-4i-3)}(14\times 4^i - 17)CV_{ref}^2 \quad \text{where } n = 2,4,6\ldots \tag{3}$$

For a 6-b case ($n = 6$), the conventional switching is about $34CV_{ref}^2$ where more than 50% of energy is occupied by E_{pre}. It is worth noting that E_{pre} enlarges the maximum switching energy which eventually requires a more power-hungry reference buffer [4]. On the other hand, all the pre-chargings are removed with the proposed PRS. The average switching energy can then be given by

$$E_{avg,prs} = \frac{1}{2^n}\sum_{i}^{(n-1)/2-1} 2^{(2n-4i-4)}(12\times 4^i - 21)CV_{ref}^2 \quad \text{where } n = 3,5,7,\ldots \tag{4}$$

It can be recognized from (3) and (4) that the multi-bit V_{cm}-based switching is valid only for an even bit resolution while PRS only for an odd-bit resolution with $n > 1$. In order to make a fair comparison, we normalize the total C to $32C$ (total C in this design) in both methods and compare a 6-b V_{cm}-based with PRS in 7 b. Fig. 6 shows the energy comparison of these two methods. Both the maximum and average switching energy have been reduced by more than 45% in our scheme.

V. Background Offset Calibration

In Section II-B, we have shown that the offset of the comparator is necessary to be calibrated in the background even when targeting for low resolution but a wide range of VT variations. However, background calibrations often require an extra phase of operation and/or altering the sampling network [3], inducing certain overheads for high-speed design. In this paper, we proposed a background calibration that relieves the above drawbacks.

A. Calibration Concept, Characteristic, and Convergence

The calibration consists of two parts including the decision alignment logic and the offset adjustment circuits as depicted in Fig. 7. Our calibration shares the same general concept with [16] where it tries to equalize the offset of the comparators by aligning their decisions under the same input voltage. However, the comparators in [16] align to an additional

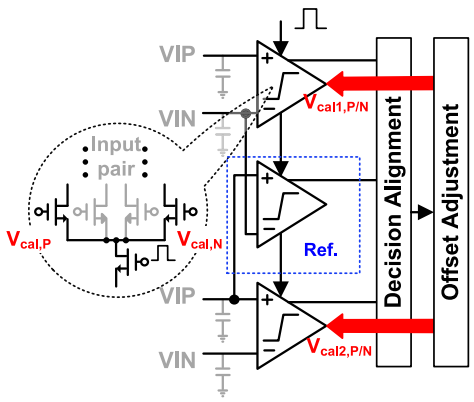

Fig. 7. Calibration concept and setup.

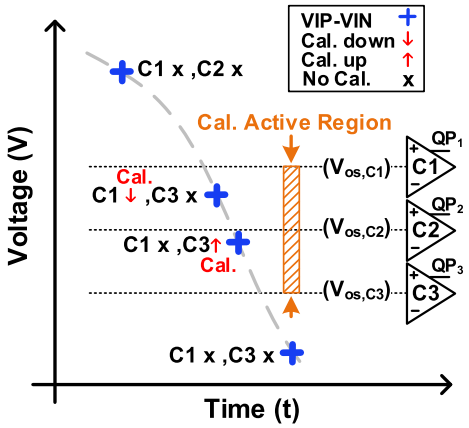

Fig. 8. Calibration characteristic and input range limitation.

reference comparator which induces extra hardware overhead and a more complex clocking. The calibration accuracy can also affect by the clocking nonalignment and not all the comparators are calibrated in background. Unlike [16], our scheme does not call for additional comparator and clocking design overheads. Recalling here during the first comparison, the inputs of all the three comparators are the same, thus their outputs can be used to determine whether offset mismatches exist among the comparators. Even though the first comparison only resolves 1 b, there is no reason to gate the clock signal of other two comparators since it causes diminished returns on speed and power with extra control logic and circuit complexity. Therefore, these extra decisions are considered being obtained with a very low cost. During the calibration, one comparator serves as an offset reference for its two counterparts, which also helps for saving one calibration set. The offset adjustment is done in the analog domain by controlling an extra calibration pair of transistors parallel to the input in the comparators.

Even though the calibration scheme can be embedded in the ADC operation with the inherent benefits mentioned before, it also relies on certain boundary conditions of the input signal. The input requirement can be well explained by Fig. 8 which shows how the calibration reacts under different inputs. If the input voltage (ΔV_{in}) is larger or smaller than all the offset of comparators C_1–C_3 ($V_{os,C1-C3}$), it gives no valid info for the calibration since the comparators have the same decision

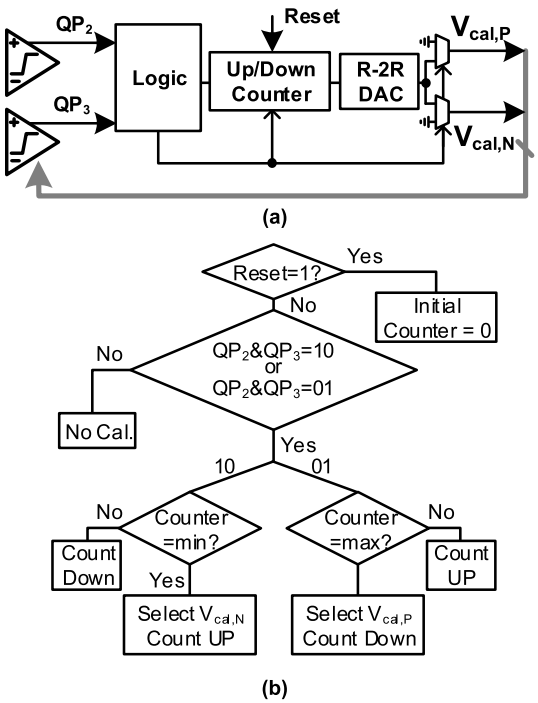

Fig. 9. (a) Block diagram and (b) logic flow of the proposed calibration scheme (shown only for comparator $C3$).

($QP_1 = QP_2 = QP_3$) even when they contain different offset voltages. If ΔV_{in} is between the $V_{\text{os},C1}$ and $V_{\text{os},C2}$, or $V_{\text{os},C2}$ and $V_{\text{os},C3}$, then $QP_1 \neq QP_2$ or $QP_2 \neq QP_3$, the calibration will adjust the offset of $C1$ or $C3$ toward the reference comparator $C2$, respectively. It can be observed that the active region is equal to $|V_{\text{os},C1} - V_{\text{os},C2}| + |V_{\text{os},C2} - V_{\text{os},C3}|$. With a large offset mismatch, the calibration will be triggered more often thus consuming larger power in average. On the other hand, after the offset between $C1$ and $C2$ as well as $C2$ and $C3$ are calibrated within 1/2 LSB, the calibration will be activated very rarely to save power. Therefore, the power of the calibration circuit is inversely proportional to the amount of offset mismatches and no extra controls are required for tracking the drifted offset.

Unlike [17] and [18], the calibration feedback is done in real time without any statistical computation. With a 7-b DAC, the maximum required number of samples for convergence is 128. The convergence will be slowed down as the calibration proceeds as less inputs falls between the mismatched offsets. Enough margins must left to account for the calibration step voltage and comparator noise as the feedback is in real time [19]. We limit their error less than 1/4 LSB in this design. It is also worth noting that one limitation of the proposed algorithm is that it relies on the ADC input that falls in between the mismatched offsets. However, as our ADC targets for systems with digital communication, the input signal is often busy across the full swing.

B. Logic Flow and Implementation

Fig. 9(a) illustrates the calibration block diagram for comparator $C3$. It consists of a calibration logic, an up/down counter, a single-ended R-2R DAC and a multiplexer (MUX). Fig. 9(b) shows the flowchart of the calibration controller for $C3$. During the 1st comparison, the calibration logic checks whether the decision of the calibrating comparators (QP_2 and QP_3) has any discrepancy. If $QP_2 = QP_3$, then no calibration is performed as there is no valid information (as explained before). If $QP_2 \neq QP_3$, depending on QP_2 and QP_3 to be "10" or "01," the calibration logic will check whether the counter is at minimum or maximum value, respectively. For "10" case, if the counter is at a minimum value, the calibration logic will select the calibration voltage output at $V_{\text{cal},N}$ through the multiplexer and imposes that the counter will count up. On the other hand, if the counter is not at a minimum value, the logic will select $V_{\text{cal},P}$ and let the counter count down. While for "01" case, a similar operation is performed with reversed counting and calibration voltage polarity.

With the MUX and the 6-b R-2R DAC, there is a maximum of 128 calibration steps where the calibrating offset polarity (MSB) is controlled by the MUX and the 6-b LSBs are accomplished by the R-2R DADC. It is worth noting that even though the R–2R DAC produces a monotonic calibration step voltage, its non-idealities cause nonuniform steps. Therefore, a small step size is chosen in order to leave enough margin to achieve our target calibration accuracy. We size the calibration pair with a 30-fold attenuation factor to the input pair in the comparator in order to use a large step voltage for calibration. With an ideal $\sim$14 mV step voltage, the calibration range is $\pm$20 mV after taking the non-ideality of the R-2R DAC into account, which can cover the three sigma comparator offsets in a wide range of PVT variations. Besides, the calibration voltage only updates during the sampling period in order to prevent any interference during the conversion and the calibration reference voltage is settled within 750 ps. The unit R is $\sim$10 kΩ. The power of the R-2R DAC is code dependent where a 6-b DAC consumes a maximum current at code 21 and 43. Their power consumption is $\sim$63 μW from a 0.9-V reference. The total power consumption of the calibration circuit is $<$300 μW when the offset is well calibrated. The active area is 0.0017 mm^2.

VI. Circuit Implementation and DAC Structure

A. Dynamic Shift Register

The shift register (SR) in the SAR ADC provides the indication of the working cycle which controls the SA logic to propagate the comparators' decisions to the DAC. As the critical signal path does not pass through the SR, the speed is usually not a concern. On the other hand, it typically consumes a significant amount of power as it comprises n numbers of D-flip-flop (D-FF) for n-bit cycling. For low-power considerations, we replace the power-hungry static D-FF by a switched-capacitor-based dynamic register (SCDR) as shown in Fig. 10(a). The dynamic SR is triggered by the comparator clock Φ_{ST} which is generated by a self-time loop (Fig. 3) with similar implementation in [11]. The operation of the dynamic shift register can be explained by Fig. 10(b). When reset $= 0$, the internal nodes, A and B, of all the SCDRs are reset to G_{nd} and V_{dd}, respectively, which discharges VQ_{1-4} to Gnd. During reset $= 1$ the Φ_{ST} signal initially changes from G_{nd}

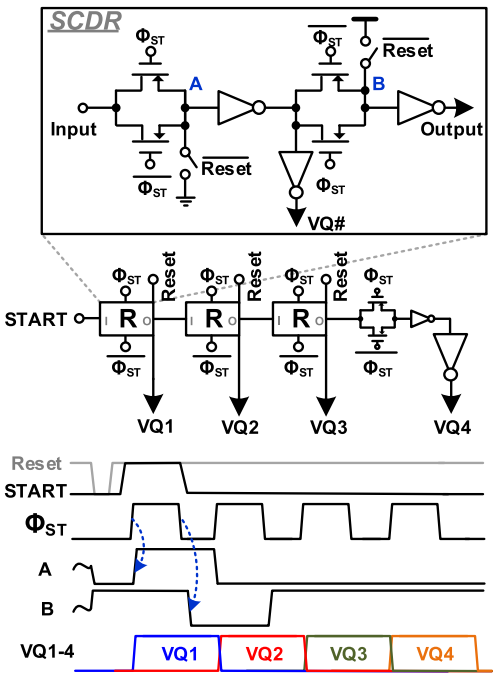

Fig. 10. (a) Circuit schematic of the dynamic shift register and (b) its timing diagram.

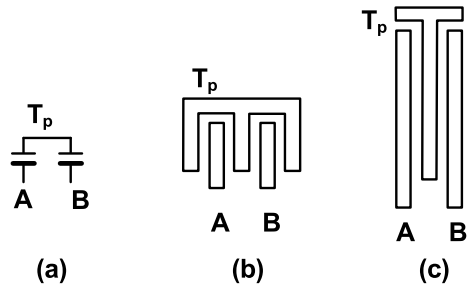

Fig. 11. (a) Schematic example. (b) Corresponding layout in a conventional fringe structure. (c) Modified structure.

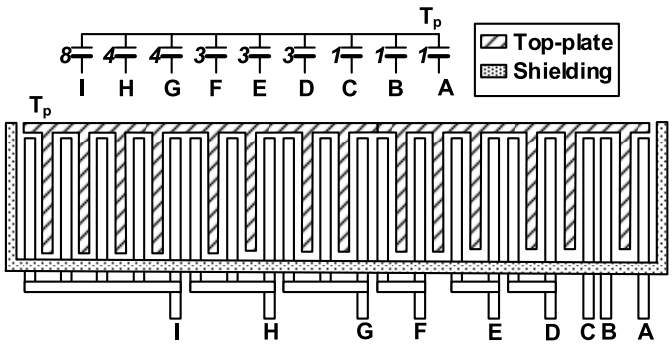

Fig. 12. Layout of the adopted DAC structure (partially).

to V_{dd}, the 1st SCDR passes the START signal and charges the node A to V_{dd}. Later when Φ_{ST} changes from V_{dd} to G_{nd}, node A holds V_{dd} and node B discharges to G_{nd}. This operation is similar to a master–slave D-FF but now the power is full dynamic. The registered data are stored in the parasitic capacitance in nodes A and B, thus requiring a high-speed periodical refreshment similar as the DRAM to prevent the charge leakage. This is well fit to our design as the SA loop is at a very high speed. In the next rising edge of Φ_{ST}, the 2nd SCDR captures the output of the 1st SCDR and the VQ_1 changes from V_{dd} to G_{nd} once the START signal goes low. Such operation propagates to the 3nd SCR and the 4th semi-SCR which eventually performs an SR function. The reset and START signals come from a shrunk version of the sampling signal and the Φ_{ST} signal is from the self-time loop.

B. Unit Capacitance and DAC Structure

The DAC is a key building block of the SAR ADC as it affects the accuracy, speed, and power. Especially in the multi-bit SAR ADC, there is more than one DAC as well as multiple feedback controls from different comparators. In general, the DAC layout should be dense with a consistent unit capacitor structure to obtain high speed and good matching. The conventional fringe DAC structure [20] achieves a compact area as it allows the top plate of the unit capacitor to be shared with each other. However, such structure results in a wide layout thus leading to a large bottom plate parasitic resistance and capacitance. Worth noting that the delay caused by the routing is exponentially related to its length (L) ($\text{delay}_{\text{rout}} \propto L^2$), implying that long L can greatly degrade the speed of the SA loop. Other structure based on the Wovmen [8] relaxes this constraint with a penalty of worse mismatching since it also adopts the vertical coupling capacitance. Moreover, both the conventional fringe and Wovmen structures lead to a larger top-plate parasitic than the bottom plate, which is undesirable in top-plate sampling as it affects the full swing of the ADC. In this design, we modify the fringe structure to mitigate the long layout issue, keep the utilization of the fringing field only in the lateral and simultaneously reduce the top-plate parasitic. Fig. 11(a) shows the schematic example and (b) illustrates the corresponding layout with a conventional fringe structure. It can be inferred that this structure requires a total of five fingers even with a shared top-plate (T_p). Fig. 11(c) depicts the modified structure. The top plate is still shared between two unit capacitors but unfolded to a single finger. Comparing with a conventional structure, the number of fingers has shrunk to 3 which simultaneously reduces the top-plate parasitic capacitance by ~30% under the same amount of unit capacitance. Fig. 12 demonstrates part of the total DAC layout structure in this design. Each unit capacitor shares its top plate with others and the top plate is well protected by a bottom plate or shielding to prevent any undesired coupling. On the other hand, as the spacing between the metals for different plates is designed to permit a minimum DRC allowance, the inconsistent fringing capacitance in different unit leads to a mismatch in the DAC. Fig. 13 shows the mismatch error $\Delta C/C\%$ for all the capacitors shown in Fig. 12 under different extraction corners (nominal, $C_{\max}$, and $C_{\min}$). It can be observed that the worst matching is from capacitor B-C as their bottom plate finger meets more next adjacent top plate when comparing it with others, thus leading to a larger capacitance. With maximum systematical mismatch error and random mismatch error (~0.1% estimated based on a similar

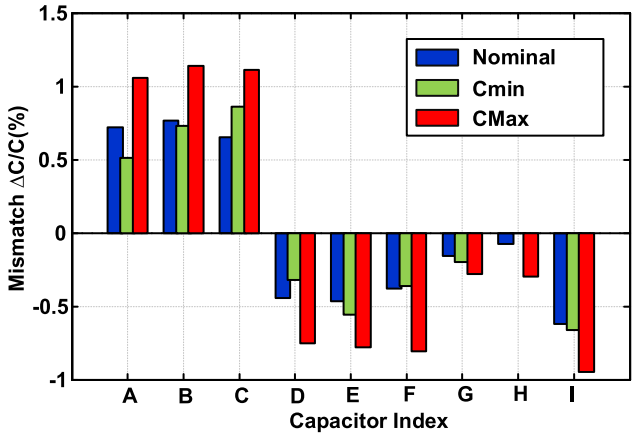

Fig. 13. Systematical capacitance mismatch in different extraction corners.

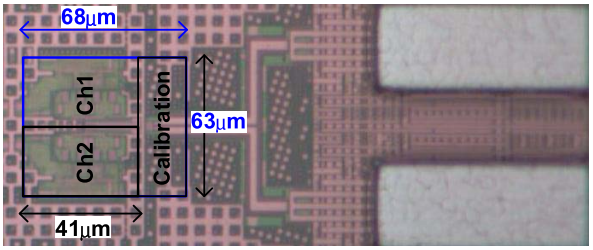

Fig. 14. Chip microphotograph.

structure provided by the foundry), the total mismatch is ∼2%, which corresponding to ∼3 dB SNDR degradation in this design. The DNL pattern obtained in the measurement is mainly caused by this systematical mismatch which can be identified in multiple samples. Layout techniques like common centroid or inter-digital can improve this issue with a penalty on the DAC settling speed.

VII. Measurement Results

The ADC realized in a 28-nm 1P9M CMOS process has its microphotograph shown in Fig. 14. The active area is 0.043 mm^2 including the on-chip background offset calibration. The input capacitance is around 64 fF including parasitics but without considering the input routing, PAD, and ESD devices. Fig. 15 illustrates five measured samples and their SNDR under a wide range of temperature, supply, and common-mode voltage variations with low-frequency input. The chip with worst performance is #3 while it is still able to keep an SNDR above 35 dB from −40 to 125 °C. When running at around 2 GS/s, the SNDR of the chip #3 stays above 38 dB in a ±10% supply and common-mode voltage variations. We use the chip (#4) with mean performance to report the results. Fig. 16(a) illustrates the output spectrum of chip #4 sampled at 2.4 GS/s with a Nyquist input. The clock skew spur and 3rd harmonic are well below 50 dB thanks to the adopted common-clock bootstrapped technique [6]. Other large spurs are due to the systematical DAC mismatch as discussed in Section VI-B. The SNDR and SFDR are 40.05 and 54.34 dB, respectively. Fig. 16(b) depicts the SNDR and SFDR across low frequency and to frequency higher than Nyquist at 2.4 GS/s. The SNDR remains quite flat until around 1.2-GHz input. The SFDR is mainly limited by the 3rd

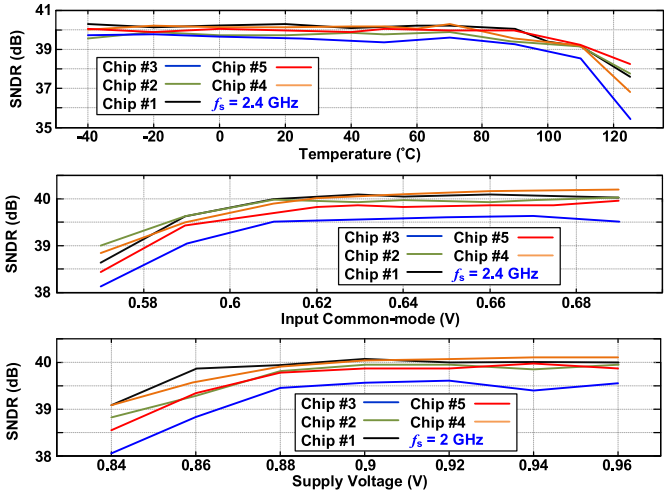

Fig. 15. Measured SNDR with low-frequency (∼10 MHz) input under temperature, input common mode, and supply voltage variation of five samples.

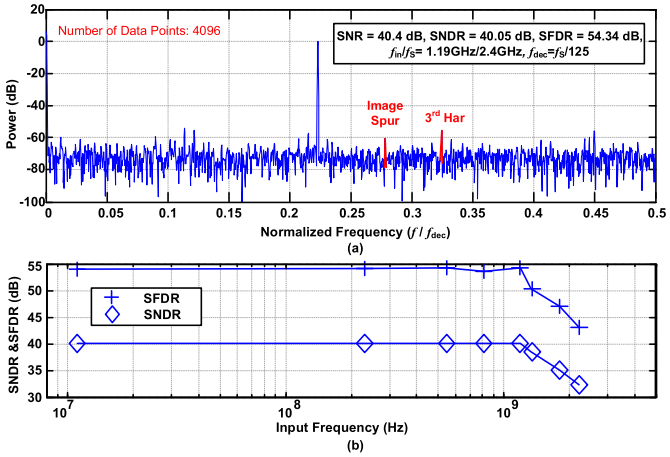

Fig. 16. Output spectrum with near Nyquist input (output decimated by 125×). (b) Measured SNDR and SFDR across input frequencies.

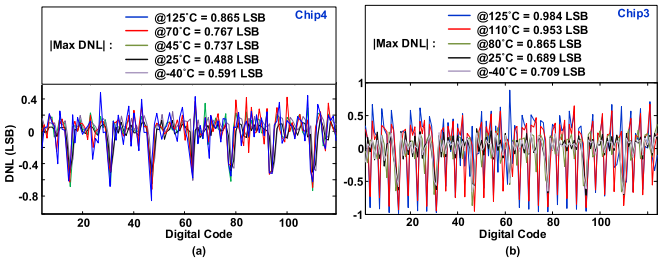

Fig. 17. Measured DNL under various temperature in (a) Chip #4 and (b) Chip #3.

harmonic above 1.19 GHz. The time-interleaved spur [image spur indicated in Fig. 16(a)] is well below 54 dB. We suspect that is due to the insufficient margin left for the sampling time and equipment's issues (such as splitter, filter, and signal generator). Fig. 17(a) and (b) shows the measured DNL of chips #4 and #3 in several temperature points, respectively. Further, there is a DNL pattern due the DAC mismatch within the LSB array in the split DAC. The maximum DNL and INL are 0.737 and 0.639 LSB in chip #4 and 0.854 and 0.722 LSB in chip #3, respectively, in various temperatures.

TABLE I
COMPARISON WITH STATE-OF-THE-ART DESIGNS

Publication	[2] ISSCC'14	[5] JSSC'15	[3] ISSCC'13	[21] VLSI'16	This work
Architecture	Folding Flash	2b/cycle SAR	SAR	4xTI SAR*	2xTI 1-2b SAR
Technology	40nm	45nm	32nmSOI	16nm	28nm
Supply (V)	1.1	1.25	1.0	0.95	0.9
Resolution	7b	7b	8b	10b	7b
f_S (GS/s)	2.2	1.0	1.2	1.6	2.4
SNDR@Nyq(dB)	37.4	40.8	39.3	50.3	40.05
Input Cap. (F)	300f	600f	128f	N/A	64f
Power (mW)	27.4	7.2	3.06	8.2	5.0
FoM@Nyq. (fJ/conv.-step)	205.7	80	34	19.23	25.3
DNL/INL (LSB)	0.6/0.6	0.4/0.5	0.79/0.91	0.62/0.81	0.49/0.57
Area (mm^2)	0.052	0.016	0.0015	0.023	0.0043
Offset Cal.	No need	Foreground	Background	Background	Background

*Need timing-skew calibration (offchip)

The total power consumption is 5 mW at a single 0.9-V supply with offset calibration. The analog power, including the comparators and the sampling bootstrapped circuits, takes 40%, the SA logic circuits consume around 29%, the DAC switching occupies 4%, the clock generator, buffers, and calibration circuit consume 21% and 6%, respectively (estimated from the simulation result). The calculated Walden FoM at the Nyquist input is 25.3 fJ/conversion step. Table I summarizes and compares this work with the state-of-the-art ADCs, achieving a good energy efficiency with the necessary calibration on chip.

VIII. CONCLUSION

A 7-b 2.4-GS/s two-way interleaved 1-then-2 b/cycle SAR ADC has been presented. The PVT sensitivity of the conventional multi-bit SAR ADC has been improved with the proposed architecture and techniques. With a PRS and 1-then-2 b/cycle, all the pre-charging is removed which saves both speed and power consumption. A low overhead background offset calibration technique is introduced which is well embedded in the proposed architecture. With an improved fringe DAC structure and dynamic circuit, measurement results show the effectiveness of the proposed design. It draws only 5-mW power from a 0.9-V supply at a conversion rate of 2.4 GHz with a Walden FoM of 25.3 fJ/conversion step.

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