A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver

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***Abstract*— This paper describes a four-element multiple-input multiple-output (MIMO) transmitter (TX) system that features an analog spatial de-interleaver to simplify the baseband-input complexity and increase the spatial matching of the sub-TXs. The MIMO diversity gain and power-combining gain are jointly exploited to relax the output power of the four power amplifiers and eliminate their output matching networks, leading to a compact implementation of the entire TX system. The MIMO effectiveness is improved by introducing an radio-frequency to baseband dc feedback technique that enhances the matching among the sub-TXs against process variation. In the verification, the TX system is co-designed with a compact antenna array-on-PCB that generates a null zone in the propagation pattern, and the electric-field polarization angle, to achieve diversity propagation. All techniques together improve the signal-to-noise ratio or data rate by generating multiple data streams according to the signal power arriving at the receiver over different fading channels. The four-element TX chip fabricated in 65-nm CMOS occupies a die area of 1.44 mm^2. It covers an RF range of 0.7–2.5 GHz, and shows an equivalent isotropically radiated power of 23.9 dBm. When transmitting a 20-MHz 64-QAM orthogonal frequency division multiplexing signal at 2.3 GHz, the average system efficiency is 61% and error-vector magnitude is −26 dB.**

***Index Terms*— Antenna array, beamforming, CMOS, diversity gain, error-vector magnitude (EVM), fading channel, mobile, multiple-input multiple-output (MIMO), MIMO decoder, matching network (MN), pulse-shaping filter (PSF), power amplifier (PA), transmitter (TX), signal-to-noise ratio (SNR), wideband.**

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I. Introduction

MULTIPLE-INPUT multiple-output (MIMO) technology [1] has been widely utilized in cellular base-stations and Wi-Fi routers to enhance the link capacity and reliability via multipath propagation [2]. Recently, the focus on MIMO has been shifted to mobile terminals, aiming to improve the sensitivity and flexibility of the receiver in a small form factor: e.g., using the spatial blocker rejection to improve the signal-to-noise ratio (SNR), support the space-division multiple access (SDMA), or enable the multiple spatial data streaming [3]–[5]. Still, there are other potentials of MIMO have not been explored for mobile radios, especially on the transmitter (TX) that dominates the system power.

Beamforming [6] is a multi-antenna technique capable to support SDMA and enhance the output power (P_{out}), but is incapable to generate multiple spatial data streams if the phase shifting is obtained either on the RF or the local-oscillator (LO) paths. Although existing multi-phase LO generation techniques can cover a wide range of transmission angles, the high angular resolution still involves complicated circuits [6]. Alternatively, parallel baseband (BB) streams can have more flexibility to improve the angular resolution, and support various MIMO encoding schemes to further increase the signal quality or data rate of the communication. To be described in this paper, with a set of reconfigurable BB signals, the MIMO theory [7] can be realized in different approaches to aid the signal-quality enhancement or channel-capacity maximization.

MIMO implementation for mobile devices has to balance the hardware complexity, power consumption and form factor. Comparing with a single-element TX, a MIMO TX involves multiple TXs operating in parallel, and a set of reconfigurable BB signals to support space-time block code (STBC) [8] and singular value decomposition MIMO [9]. The form factor can be lowered by the full integration of all TX elements and power amplifiers (PAs) [10], [11]. Yet, the output bandwidth (BW), area and power efficiencies are highly affected by the presence of the output matching network (MN), which is essential for each PA to deliver a P_{out} of over 20 dBm in low-voltage CMOS technologies. Last but not the least, when multiple PAs are operated alongside, the heat dissipation

and EMI radiation become more severe, impacting the power efficiency and signal integrity. For the BB implementation, parallel BB streams significantly increase the complexity of the input interface and impact the form factor of the system [12], [13]. Although the single-bit TX in [12] can handle multiple data streams via polar PWM modulation, the linearity is degraded, thereby entailing I/Q-domain distortion calibration. The PWM modulation also calls for a power-hungry high-speed digital interface (24.5 GHz for 5-GHz operation [12]). A more straight-forward technique could be the data interleaving. It can reduce the BB complexity and number of digital-to-analog converters (DACs) [14], but at the cost of a higher sampling rate for the DACs that increases with the number of TX elements.

This paper describes a compact 4-element MIMO TX system with integrated 4-element PAs combining a number of system- and circuit-level techniques to address the above concerns. Unlike [12], here the multi-mode MIMO spatial de-interleaver linearly modulates the digital BB signals to each TX element via only one pair of I/Q-DACs, avoiding the need of linearity calibration. To ensure the effectiveness of the MIMO algorithms [15], an RF-to-BB DC feedback circuit technique has been proposed to enhance the spatial matching among the TX elements, avoiding any inter-channel gain calibration, and the loss of dynamic range to re-balance the output power. To deliver a higher equivalent isotropically radiated power (EIRP), a compact inverter-based self-biased 4-element PA is proposed. The analog BB circuitry is based on an analog spatial de-interleaver. It features a switched-capacitor (SC) interpolator to function as a mixed-signal pulse-shaping filter (PSF), which can benefit from a single channel of interleaved input data to simplify the hardware and reduce signal mismatches. Comparatively, the power consumption and die area of the proposed MIMO TX chip are smaller than those of a single-element TX chip [16], [17] for a similar communication quality. Finally, to demonstrate the feasibility of 4×1 beamforming and 4×4 MIMO that can enhance the signal strength or data rate, the MIMO TX system is co-designed with a MIMO antenna array-on-PCB for field tests over a practical channel.

Section II describes the system architecture and key MIMO theory of the proposed multi-mode-MIMO TX. Section III details the design of the key RF and BB circuitries. Section IV covers both the chip-level and system-level measurement results. Finally, the conclusions are drawn in Section V.

II. System Architecture and Key MIMO Theory

A. MIMO TX System

The proposed 4-element MIMO TX system (Fig. 1) features a software-defined MIMO precoder, followed by a single pair of I/Q-DAC that compositely generate all BB signals for all TX elements in single data stream via the proposed analog spatial de-interleaver. The TX chip integrates 4 direct conversion sub-transmitters (sub-TX_{1-4}), and a 4-element PA (PA_{1-4}); each can have a relaxed output power of 14-dBm P_{out}. An antenna board with 4 commercial antennas was also designed to measure the TX performance in a practical multi-path channel fading environment. Unlike

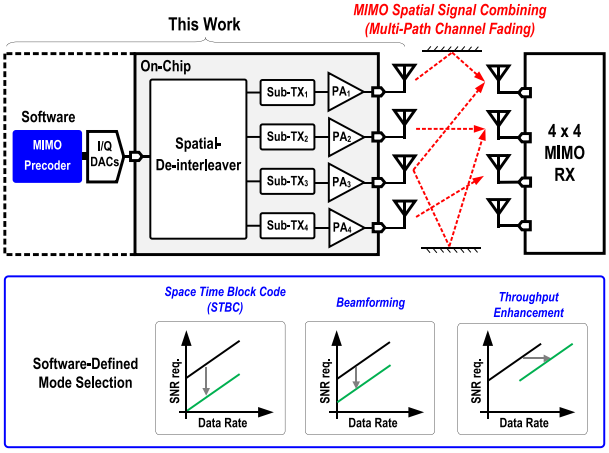

Fig. 1. Proposed 4-element multi-mode-MIMO TX system. The MIMO precoder is implemented in software for reconfigurability. The wideband MIMO TX chip integrates an analog spatial de-Interleaver, 4 sub-TXs, and 4 power-relaxed PAs that can directly interface with the antennas (i.e., no output matching networks).

the beamforming TX in [6], the proposed TX can utilize the singular value decomposition to optimize the channel capacity by allocating the transmission power to more data streams, while supporting TX diversity under the beamforming or STBC technique. The MIMO precoder supports different SNR scenarios by using the *STBC*, *beamforming*, *throughput enhancement or mixed* modes. Note that in the throughput-enhancement mode, the diversity gain and power-combining gain are not available.

The proposed MIMO TX system has 3 key features: 1) an analog spatial de-interleaver reduces the complexity of the BB input interface. Specifically, only one pair of I/Q-DACs is adequate for MIMO, similar to single-input single-output (SISO)-design. Unlike the idea introduced in [14], our spatial de-interleaver does not increase the required sampling frequency of the I/Q-DACs, while offering multi-element up-sampling, and pulse-shaping-filtering in the analog domain. 2) For the 4 spatially-matched sub-TX_{1-4}, each features an RF-to-BB DC feedback technique to reduce the possible gain mismatch among the sub-TX_{1-4} against process variation. 3) Inverter-based 4-element PAs that utilize the spatial power-combining gain and diversity gain available from the MIMO algorithm to eliminate the MN, enabling a compact die area, a wider RF bandwidth and a higher EIRP efficiency. Another DC feedback technique is also introduced to the cascode device of each PA, which enhances the robustness of its gain and linearity against process variation.

B. Beamforming/STBC MIMO Precoder

The MIMO precoder can deal with different SNR scenarios. When the SNR is low, the precoder is configured to support 4×4 MIMO + STBC, improving the equivalent SNR. The transmitted signal can be encoded by the following 3/4 code rate matrix [8],

$$C = \begin{bmatrix} c_1 & c_2 & c_3 & 0 \\ -c_2^* & c_1^* & 0 & c_3 \\ -c_3^* & 0 & c_1^* & c_2 \\ 0 & -c_3^* & c_2^* & c_1 \end{bmatrix}, \quad (1)$$

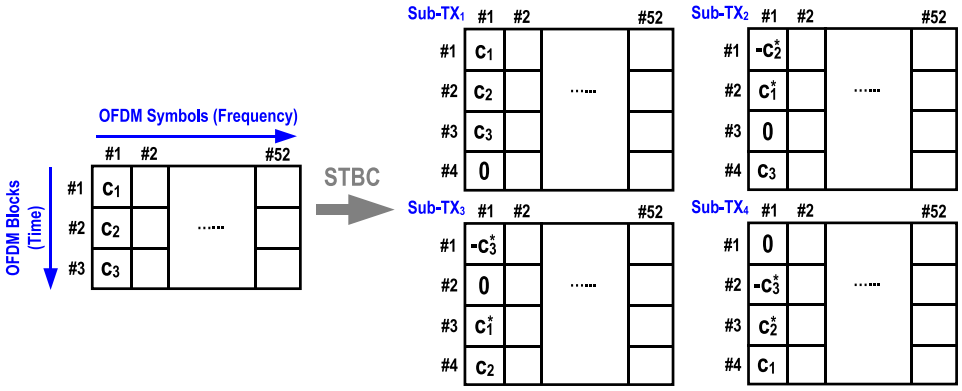

Fig. 2. Principle of the STBC mapping for the 802.11n signal.

where (.)* is the complex conjugate operation. Fig. 2 depicts the arrangement of the symbols c_1 to c_3. We assume a slow fading channel to ensure that the coded signal is orthogonal, which implies the channel coefficients can be kept constant for 4 orthogonal frequency division multiplexing (OFDM) blocks. At the receiver end, the STBC code can be decoded as,

$$\begin{cases} y_{p,1} = h^*_{p,1} r_{p,1} + h_{p,2} r^*_{p,2} + h_{p,3} r^*_{p,3} + h^*_{p,4} r_{p,4} \\ y_{p,2} = h^*_{p,2} r_{p,1} - h_{p,1} r^*_{p,2} - h^*_{p,4} r_{p,3} + h_{p,3} r^*_{p,4} \\ y_{p,3} = h^*_{p,3} r_{p,1} + h^*_{p,4} r_{p,2} - h_{p,1} r^*_{p,3} - h_{p,2} r^*_{p,4} \end{cases}, \quad (2)$$

where $y_{p,k}$ is the decoded STBC signal of c_k of the n^{th} receiver; $h_{p,k}$ is the gain from the k^{th} TX to the p^{th} receiver; and $r_{p,k}$ is the received signal of the k^{th} block of the STBC in the p^{th} receiver. The SNR of the STBC coded signal can be derived as,

$$SNR_{STBC} = \frac{\left(\sum_{p=1}^{4}\sum_{k=1}^{4}|h_{p,k}|^2\right)^2 \times \sum_{m=1}^{3}|c_m|^2}{\sum_{p=1}^{4}\sum_{\substack{k=1 \\ k+r\neq 5}}^{4}\sum_{r=1}^{4}|h_{p,k}n_{p,r}|^2}, \quad (3)$$

where $n_{p,r}$ is the received noise at the r^{th} block of the p^{th} receiver. The calculated SNR improvement brought by the STBC is 7.3 dB.

STBC is no longer appropriate if the SNR is low and the channel is fast fading in a multi-path environment. Thus, the precoder can be configured to transmit only one beam-forming signal. Theoretically, a 4×1 beamforming system can improve the equivalent SNR by 6 dB. The demodulation in the receiver is similar to that of a SISO system.

Finally, when the SNR is high, the MIMO encoder can be reconfigured to deliver multiple data streams. With the knowledge of the MIMO channel, the singular value decomposition of the channel is given by,

$$H(j\omega_m) = U(j\omega_m)\sum(j\omega_m)V^H(j\omega_m), \quad (4)$$

where $(.)^H$ is the Hermitian operator; $H(j\omega_m)$ is the MIMO channel matrix; $U(j\omega_m)$ and $V(j\omega_m)$ are the orthogonal matrices; $\sum(j\omega_m)$ is a diagonal matrix with $\sigma_{m,k}$ on the diagonal with descending order, and $\sigma_{m,k}$ are the singular values of $H(j\omega_m)$. The transmitted signal is precoded as

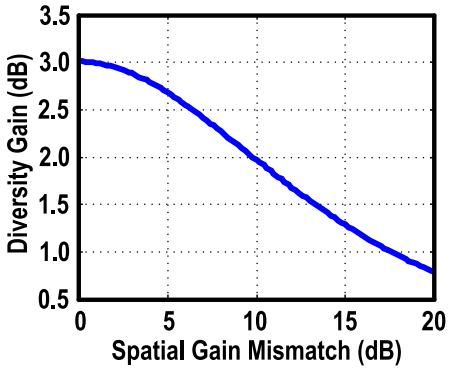

Fig. 3. Simulated diversity gain against the spatial gain mismatch of two sub-TXs under a non-fading channel.

$x_p(j\omega_m) = V(j\omega_m)x(j\omega_m)$, where $x(j\omega_m)$ is the original data stream vector. The received signal can be decoded as $y(j\omega_m) = U(j\omega_m)R(j\omega_m)$, where $R(j\omega_m)$ is the receive signal vector. In this coding scheme, different modulation styles can be flexibly adopted to support different decoupled channels with respect to the corresponding singular value $\sigma_{m,k}$, thereby maximizing the system's throughput. Note that there is no diversity gain and power-combining gain in this mode.

Mainly the spatial gain mismatch among the sub-TXs will affect the diversity gain extracted from the propagation channel [18]. The diversity gain with respect to the spatial gain mismatch of two sub-TXs in non-fading channels are simulated in Fig. 3 as an example, where the ratio of their transmitted power is swept under a fixed total output power. The diversity gain drops by 0.5 dB for a spatial gain mismatch of 6 dB, but will be larger if under a fading channel.

C. MIMO BB-Signal Generation With Simplified Hardware

A typical approach to generate the BB I/Q signals in a single-element TX is to upsample the modulated signal in the digital domain [19], followed by analog filtering to suppress the upsampling replicas. Extending this approach to a MIMO TX will increase substantially the numbers of BB input ports and I/Q-DACs, increasing the likelihood of channel mismatch between elements and layout complexity. Although applying the interleaving technique in the mixed-signal domain [14] can reduced the required number of I/Q-DACs and I/O pins, the

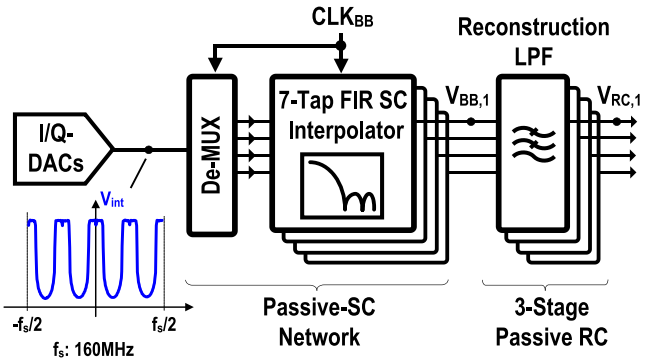

Fig. 4. Block schematic of the proposed analog spatial de-interleaver to reduce the number of BB ports and I/Q-DACs. The BB data is spectrally squeezed into a pair of I/Q-DACs enhancing the BW efficiency.

DAC's sampling rate f_{DAC} has to be raised accordingly,

$$f_{DAC} = N_{MIMO} N_{up} f_{BB}, \tag{5}$$

where N_{MIMO} is the number of elements for the MIMO TX; N_{up} is the upsampling factor of the BB signal in the digital domain, and f_{BB} is the sampling rate of the modulated signal.

In this work, the upsampling and pulse-shaping functions are partially shifted to the analog domain to relax f_{DAC}. Obviously, if performing the complete pulse shaping in the analog domain with a SC network, the order of the required finite impulse response (FIR) filter will be too high. To balance the filtering effort, the BB signals are 2×-upsampled in the digital domain before interleaving as $v_{int}[n]$ that can be generated by just a pair of I/Q-DACs. Accordingly, N_{up} in (5) can be halved, so as f_{DAC}. The signal is then de-interleaved and interpolated on-chip so that the up-sampling replicas can be handled by a 6th-order FIR filter. The DAC replicas are handled by a passive-*RC* filter. The implementation is based on an analog spatial de-interleaver (Fig. 4). For 20-MHz-BW 802.11n WLAN signals, they can be spectrally squeezed into a pair of 160-MHz I/Q-DACs to enhance the BW efficiency. Also, by upsampling the modulated signal in the digital domain, the PSF can be applied for both 802.11n (8.125 MHz) and LTE (9 MHz) signals without changing the filter coefficients. If no upsampling is applied in the digital domain, the required rejection for the 802.11n/LTE PSF is 20.78/30 dB at 11.875/21.72 MHz. To share the PSF for both standards, the 802.11n/LTE signals here are upsampled by $2\times/1.25\times$, in order that they provide a rejection of 40/36 dB at 31.875/29.4 MHz.

The 4-channel signals are interleaved at the MIMO precoder. The z-transform of the interleaved signal $v_{int}[n]$ can be derived as,

$$V_{int}(z) = X_1\left(z^4\right) + z^{-1}X_2\left(z^4\right) + z^{-2}X_3\left(z^4\right) + z^{-3}X_4\left(z^4\right), \tag{6}$$

where $X_k(z)$ is the Z-transform of the signal of the kth channel.

The PSF is realized by a 40-MHz de-multiplexer (de-MUX) followed by a 160-MHz 7-tap FIR SC interpolator. The latter has 3 transmission zeros at 30.7, 42.7 and 64.1 MHz, to effectively reject the upsampling replicas, such that the spectral mask of 802.11n can be met after simple 3-stage passive-RC reconstruction filtering (Fig. 5).

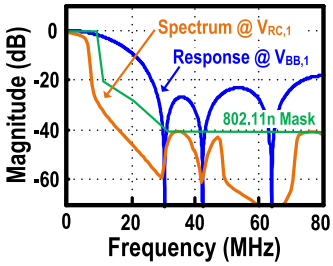

Fig. 5. Filtering profile of the PSF to meet the 802.11n spectral mask.

D. MIMO Diversity Gain Enabling the Use of Low-Power PAs Without Output MNs

To achieve a P_{out} of 23 dBm for WLAN applications [Fig. 6(a)], a MN is normally entailed for impedance transformation, differential-to-single-ended conversion and power combination [20]. Unlike the millimeter-wave TX [13], the MN for sub-10 GHz radios should require bulky inductor(s), and will limit the power efficiency (70.8% in [10]) and output BW, while increasing the die area ($350 \times 350\ \mu m^2$ each [10]). In fact, a number of practical problems arise due to the high-swing signal at the output node of the MN. Firstly, due to finite on-chip isolation (e.g., via the substrate and power rails), the LO can be easily frequency-pulled by the PA + MNs. Secondly, hot-carrier injection (HCI) and transconductance degradation emerge over time due to concentrated heat dissipation. Finally, there is significant EMI radiation critical to the user's health concern, raising the production cost due to the required absorption-rate tests [21].

Inspiring by those facts, we exploit here the 7.3-dB (6-dB) diversity gain offered by the STBC or beamforming technique to increase the EIRP of the PA, reducing the actual power radiation of the TX. This *virtual gain*, explored in [22], enhances the signal strength of the radio, but the concerns raised above in terms of chip area, heat dissipation and EMI radiation remain unsolved. On the contrary, the diversity gain offers an alternative for mobile radios to reduce the radiation power and simplify the hardware. In this work [Fig. 6(b)], we utilize the diversity gain to relax P_{out} of each element by 6 dB, while providing the same signal quality when comparing it to the typical SISO communication. The main levy of MIMO is the additional antennas for combining the transmitted power in the air. In other words, a MN with a 4:1 transform ratio is naturally built, relaxing the required single element P_{out} of each PA by 12 dB (i.e., only 11 dBm). It implies the reduction of the output swing of each PA from 9 to 2.25 V, easily obtained in standard CMOS without any MN, as detailed next.

As mentioned, 4-element beamforming can generate a 6-dB diversity gain for EIRP (i.e. $4\times P_{out}$) without actual power radiation, while the power consumption (P_{DC}) for such TX remains the same, the power efficiency (η) of each PA element is equivalently increased by 4x,

$$\eta_{EIRP} = \frac{P_{out} \times 4}{P_{DC}} = \eta_{SISO} \times 4 \tag{7}$$

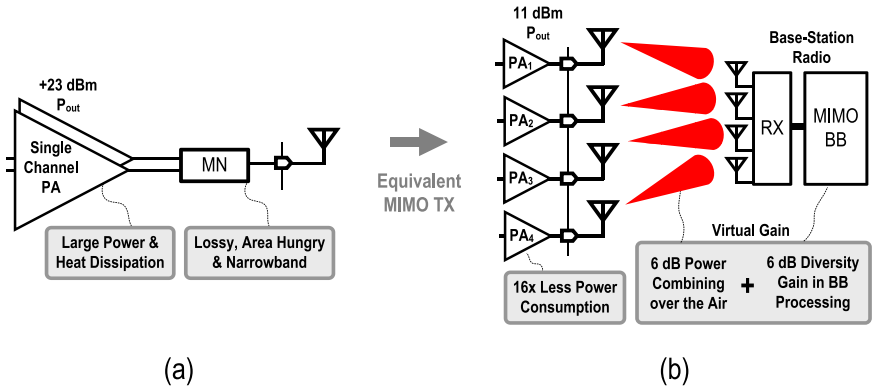

Fig. 6. (a) Typical single-element TX requires a high-power PA of 23 dBm to fit the WLAN applications. (b) For a 4-element MIMO TX having an antenna array, it can benefit from the virtual gain to relax the required Pout of each PA (e.g., 11 dBm in this 4-element TX). The small Pout essentially reduces the heat dissipation and EMI radiation on chip, while avoiding the need of output MNs that are lossy, area-hungry and narrowband.

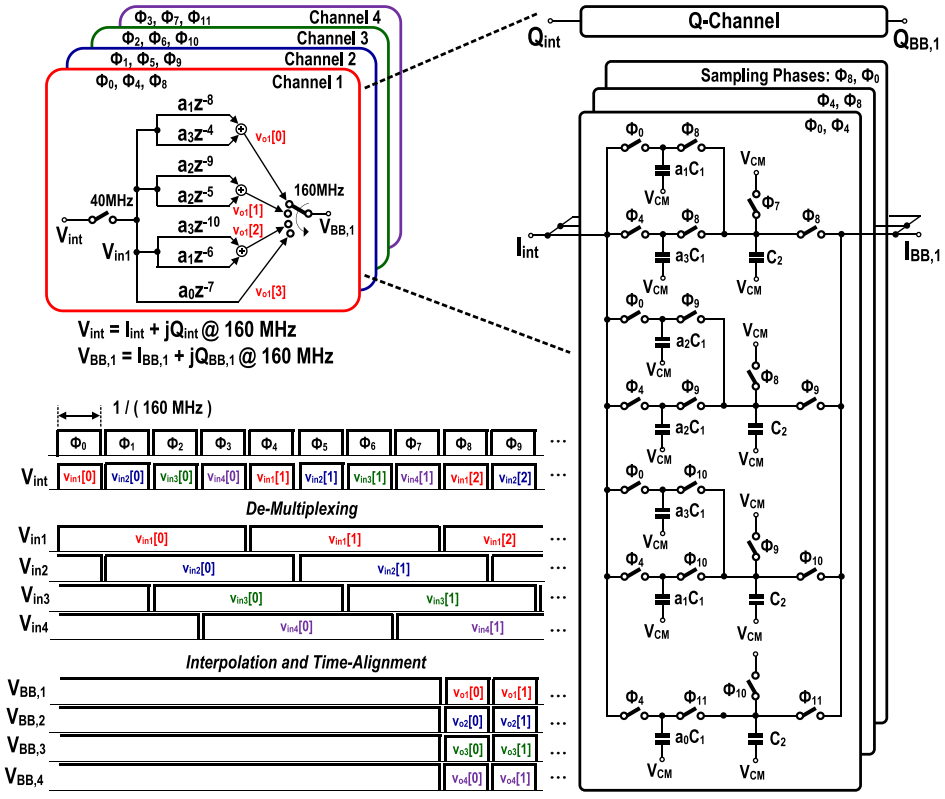

Fig. 7. The analog spatial de-interleaver implemented as a De-MUX plus a 7-tap FIR SC interpolator.

where η_{EIRP} refers to the EIRP power efficiency of the TX with the diversity gain from MIMO [13], and η_{SISO} denotes the power efficiency of the SISO TX without the diversity gain. Thus, a $\eta_{\mathrm{EIRP}} > 100\%$ is possible for MIMO systems. Also, with much lower on-chip power dissipation, the concerns of device reliability, heat dissipation and EMI radiation are relaxed simultaneously. Yet, expanding the number of TX elements will require more antennas and baseband streams, and impact the overall system form factor. An excessive number of TX elements can also cause narrow radiation beam and degrade the communication quality [13]. The trade-off between system form factor, EIRP P_{out} and power efficiency has to be well considered. Note that the enhancements of EIRP and EIRP efficiency are unavailable in the throughput-enhancement mode.

III. Circuit Implementation

A. Analog Spatial De-Interleaver

The analog spatial de-interleaver is based on a SC interpolator (Fig. 7) driven by a 13.33-MHz clock with 12 non-overlapping phases. The DAC's output signal is de-interleaved and sampled in 1 phase, then being hold for 3 phases. The signal is upsampled by 4× and filtered by a 7-tap interpolator, so that the filtered signal is a weighted sum of 2 consecutive samples. For channel 4, $v_{in4}[1]$ is sampled at Φ_7 and thus the filtered signal corresponding to $v_{in4}[0]$ and $v_{in4}[1]$ can

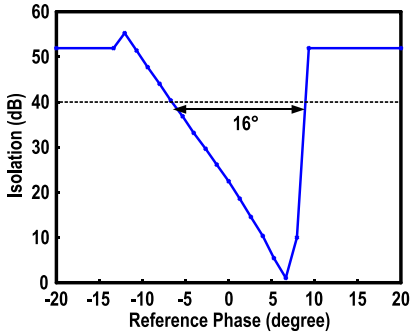

Fig. 8. Simulated signal isolation between different TX sub-channels.

be outputted from Φ_8 to Φ_{11}. In order to perform signal alignment for each channel, the signals of channels 1 to 3 have additional delays; this explains the need for a 12-phase clock (instead of 8) for the proposed 7-tap SC interpolator. The sampling switches are transmission gates driven by complementary clocks, where the PMOS and NMOS have the same aspect ratio (4/0.06 μm) to cancel the clock feedthrough. The simulated on-resistance of the switch is <550 Ω. The largest sampling capacitance of the SC interpolator is 196 fF, such that the RC time constant of the SC sampling is 119 ps under a 50-Ω source impedance.

To guarantee that the DAC's output signal is de-interleaved correctly, the DAC signal and the BB clock reference signal should be synchronized. The sampling switches of the SC interpolator should be opened before the DAC output signal changes its value to minimize the crosstalk among the BB signals. The simulated channel isolation with respect to the phase of the BB reference signal (Fig. 8) is <40 dB within 16° at an 80-MHz reference signal. It implies that the previous sample is attenuated by 40 dB with respect to the current sample in 556 ps. If the N^{th} sample voltage is settled as,

$$v_{sam}(t) = e^{-\frac{t-NT}{\tau}} v_{sam}((N-1)T) + \left(1 - e^{-\frac{t-NT}{\tau}}\right) v_{sam}(NT), \quad (8)$$

where T is the sampling period of the clock, and τ is the time constant of the sampling switch, then, the required time for $v_{sam}(t)$ to settle with a 40-dB isolation is 4.62τ (i.e., 550 ps).

The BB sampling clock is generated by a frequency divider. The reference signal has the same frequency (160 MHz) as the DAC sampling frequency to ease the synchronization. The reference signal is firstly converted to a differential pulse via a differential inverter buffer, and passed to a 6-stage D flip-flop-based frequency divider to generate a 12-phase clock. Finally, a non-overlap pulse generator converts the divider outputs into 12-phase differential non-overlap pulses for driving the transmission-gate switches, as shown in Fig. 7. The total power consumption is $\sim 400\mu$W.

Since we design the SC interpolator with a linear phase, the only contribution to the in-band group delay variation of the analog spatial de-interleaver derives from the passive-RC reconstruction low-pass filter (LPF). The simulated group delay variation of the reconstruction LPF is 3.09 ns, which is negligibly small when comparing with the guard interval of the IEEE 802.11n (400/800 ns).

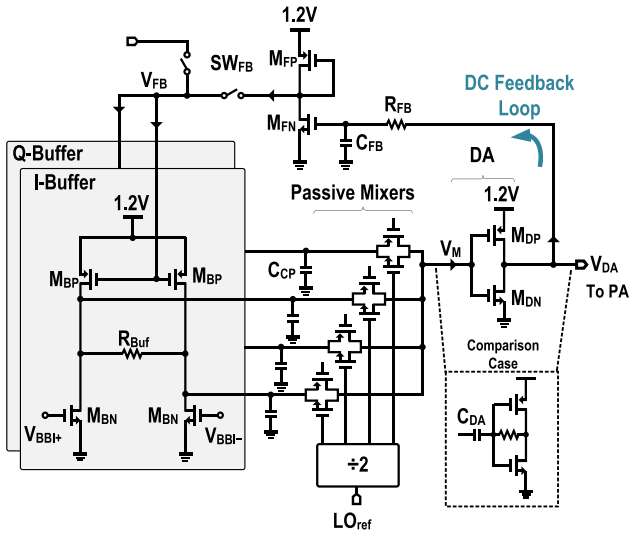

Fig. 9. Each sub-TX features a pair of I/Q-buffers followed by a set of quadrature passive mixers before driving to the DA. The 4-phase LO has a 25% duty cycle to prevent I/Q crosstalk. An RF-to-BB DC feedback loop is applied to enhance the spatial matching against process variation.

B. Spatially-Matched Sub-TXs

For each sub-TX (Fig. 9), the BB I/Q signals from the analog spatial de-interleaver are buffered separately with a differentially connected resistance (R_{Buf}) of 2.5 kΩ to reduce the gain of the buffer, lowering the counter intermodulation (CIM) products. The simulated gain of the buffer is 3.3 dB. In order to suppress the CIM products caused by the passive mixers, the buffered BB signals are directly up-converted to RF by a set of quadrature passive mixers using transmission gates. The 25%-duty-cycle 4-phase LO is generated by a typical div-by-2 circuit using D flip-flops. There are 4 coupling capacitances (C_{CP}) of 1.25 pF added before the passive mixers to provide an AC path for the high-frequency currents. The simulated insertion loss of the passive mixer is 5 dB when loaded by a driver amplifier (DA) that has a 1.1-pF input capacitance. The DA is designed to provide a 13-dB gain while driving a gate capacitance of 2 pF from the PA, while keeping an output BW up to 2.5 GHz.

The output bias level of the inverter-based DA is extracted by a DC feedback path, and fed back to the BB I/Q-buffers to avoid the gain loss against process corners. A diode-loaded stage (M_{FN} and M_{FP}) with a 2-dB gain is added to ensure the feedback loop is negative. The bypass switches (SW_{FB}) are for performance comparison during the measurements.

From simulations, the DC voltages of V_{DA} and V_M are 635.0 and 626.9 mV at the slow-fast (SF) corner, and the sub-TX has a gain of 11.2 dB with the proposed DC feedback technique, which is 0.1 dB smaller than the typical gain value. In comparison, a constant-biased BB buffer followed by a self-biased DA with a 2-pF AC-coupling capacitor (C_{DA}) has the bias voltages of 221.6 and 758.0 mV, and has a gain of 5.2 dB at the SF corner (typical gain is 6.3 dB). Thus, the DC feedback technique effectively reduces the gain drop of the sub-TX when comparing with that using an AC-coupling capacitor that introduces ~5 dB gain drop due to the extra parasitic capacitance from the DA. Further, a large C_{CP} can

help avoiding this gain drop, but consumes large area since a total of 16 C_{CP} will be necessary in this MIMO design. The 4 sub-TXs and 8 BB buffers are placed alongside in the layout, and the separation between sub-TX_1 to sub-TX_4 is ~1.2 mm, implying possible gradient effects. Here, the DC feedback technique allows each TX to be self-biased, showing less gain variation against PVT as confirmed by simulations. As a result, better gain matching among the sub-TXs is expected.

To analytically investigate the robustness of the TX system to process variation, the sensitivity of the drain voltage to process variation of the proposed PA can be estimated via the sensitivity function,

$$S = [1 + GH]^{-1}, \tag{9}$$

where G is the forward gain and H is the feedback gain of the feedback loop. Using small signal analysis, we can obtain the sensitivity function (S_{DA}) of V_{DA},

It is noteworthy that the process variation directly impacts the voltage V_{DA}, and thus the sensitivity to process variation can be estimated using S_{DA}. From (10), as shown at the bottom of this page, S_{DA} is reduced when the loop gain drops. Thus, in the proposed DC feedback loop, a large loop gain can reduce the sensitivity of the overall DC bias to process variation. Yet, the stability should not be compromised. Our DC feedback loop has a simulated phase margin of 93°; it accounts the 1-MHz-BW of the LPF ($R_{FB}C_{FB}$) as the dominant pole, which is far from the second pole at 500 MHz. Such a LPF also reduces the unwanted feedback signals from RF to BB, where the rejection at 0.7 GHz (i.e. the lowest LO frequency targeted in this work) is simulated to be 66 dB. The simulated double mixing spurs at 2LO + BB is < -70 dBc. The DC bias of V_{FB} will not contribute to the LO feedthrough, as it appears as a common-mode voltage for the differential I/Q-buffers.

C. Inductor-Less Wideband PA With Self-Biasing to Enhance Robustness

To enhance the power and area efficiencies, and reduce the RF output ports (Fig. 10), we utilize a single-ended inductor-less wideband PA for each TX element. Its self-biased cascode architecture reduces the switching power loss due to the Miller effect, while allowing 3-V operation with standard 1.2-V transistors. Each TX element can deliver a simulated P_{out} of 14.1 dBm and can cover a BW of 0.7 to 2.5 GHz. The latter is limited by the parasitic of C_{AC}, and the drain and pad capacitance at the output node.

The cascode device features a feedback bias resistor (R_{SB}) from the output node (V_{out}) to improve the PA insensitivity to process variation. This self-bias technique improves the gain variation significantly against strong NMOS-to-PMOS process mismatch (i.e., FS and SF corners). Fig. 11 plots the simulated gain with respect to the input power at the typical and SF corners. With and without R_{SB}, the gain variation is 0.1

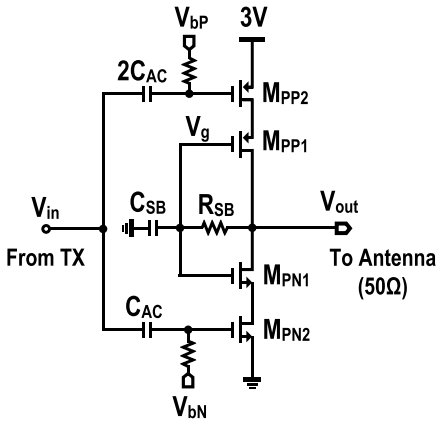

Fig. 10. Proposed inductor-less wideband PA with cascode transistors for high- voltage operation. Self-biasing using $R_{SB}C_{SB}$ improves its robustness against process variation.

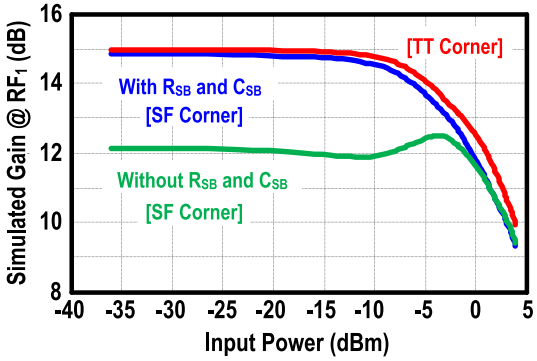

Fig. 11. Simulated gain of the wideband PA at the TT and SF corners with and without R_{SB} and C_{SB}.

and 3 dB lower than the typical case, respectively. Also, the PA will generate, without the R_{SB}, additional non-linearity distortion when the input power reaches −10 dBm (Fig. 11). Monte-Carlo simulations of process variation are also performed to compare the PA performance with and without the self-bias technique. Out of 100 runs, the standard deviation of the PA gain is reduced by 66% from 1.68 to 0.75 dB.

The capacitor C_{SB} is added to suppress the AC component at the cascode gate node V_g. Plus, the AC magnitude at V_g is mainly dominated by the capacitor divider formed by the gate-drain capacitances of M_{P1}, M_{N1} and C_{FB}, rather than the lowpass corner (88 MHz) introduced by $R_{SB}C_{SB}$. Hence, the phase of the AC signal at V_g is in-phase with the drain voltage. By increasing C_{SB}, the in-phase AC magnitude at V_g is reduced, hence increasing the gain of the PA. A large AC magnitude at V_g improves the linearity of the PA as the over-drive voltages of M_{PN1} and M_{PP1} are reduced. Fig. 12 plots the simulated gain and linearity with respect to C_{SB}. In this design, we choose a capacitance of 1 pF to have a balance performance of 15-dB gain and 13.7-dBm −3-dB gain-compression point.

$$S_{DA} = \frac{1}{1 + g_{m,BP}(r_{o,BP}//r_{o,BP})(g_{m,DP} + g_{m,DN})(r_{o,DP}//r_{o,DN})(\frac{g_{m,FN}}{g_{m,FP}})}. \tag{10}$$

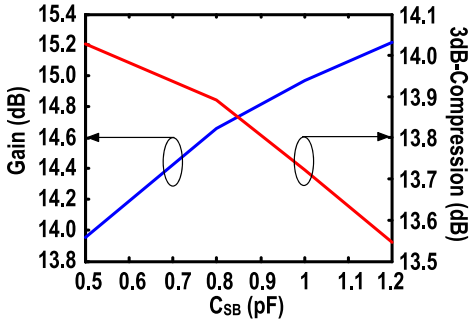

Fig. 12. Simulated gain and -3 dB gain-compression point of the proposed PA at different C_{SB} capacitance.

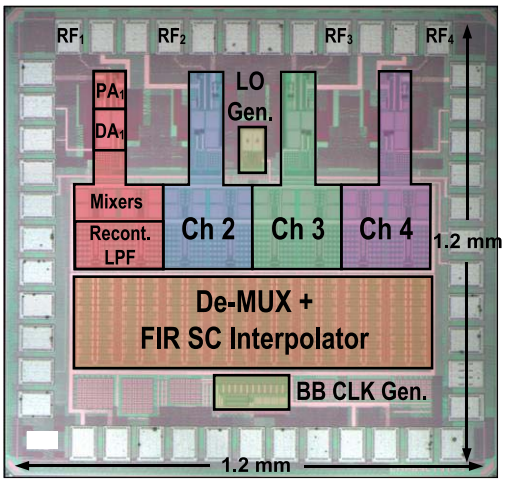

Fig. 13. Fabricated MIMO TX chip in 65-nm CMOS.

The gate biases of M_{PP2} and M_{PN2} can be customized from Class-A to Class-C modes to trade-off the gain with the drain efficiency (DE). In our design, both M_{P2} and M_{N2} are biased as Class-B PA (V_{bN} and $V_{bP} = V_{th}$) to achieve a 15-dB gain, while delivering a 13.7-dBm P_{out} with a 7.3-mA DC current (i.e. DE = 50%) at a −1.3-dBm input power. The size of $M_{PP1,2}$ is 624/0.06 μm and $M_{PN1,2}$ is 250/0.06 μm. Considering the possible mismatch between the gate biases of M_{P2} and M_{N2}, the proposed feedback technique can also balance the DC of V_{out} through M_{PP1} and M_{PN1}. From simulation, a 50-mV offset between M_{PP2} and M_{PN2} only degrades the PA gain by 0.5 dB.

IV. Experimental Results

The 4-element MIMO TX chip fabricated in standard 65-nm CMOS occupies 1.44 mm^2 (Fig. 13). The experimental results are organized as continuous wave (CW) measurement, modulated signals measurement and 4 × 4 MIMO diversity gain measurement. The BB signals are generated from a pair of off-the-shelf DACs (TI DAC5652) with a 10-bit resolution and a 160-MHz sampling rate. The digital signals and clocks are generated and synchronized from the Agilent 16902B Pattern Generator. The output signals are measured by Keysight 9030A PXA Signal Analyzer with ∼3.9-dB power compensation accounting for the loss of the PCB and connectors. To measure the power difference between the TX elements,

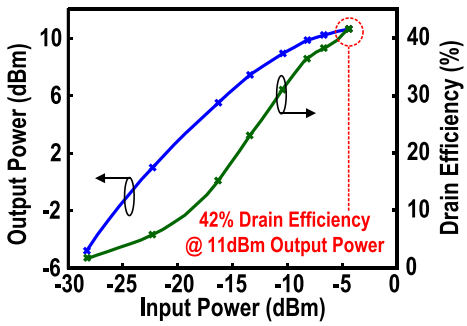

Fig. 14. Measured Pout and DE of the PA for each element.

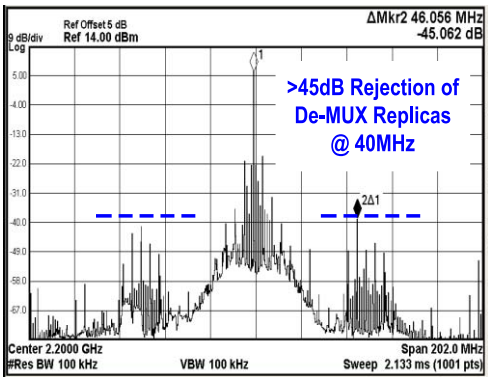

Fig. 15. Measured replicas generated by the De-MUX in the output spectrum.

we utilize the 4-port Agilent DSO91304A Oscilloscope, which features an identical connector setup for each port.

A. CW Measurement

The back-off DE and single-element P_{out} are measured against the BB input power (Fig. 14). At a -5-dBm BB input power, a peak P_{out} (i.e. −3-dB gain compression point) of 10.7 dBm is achieved, corresponding to a DE of 42% for the PA of each element. The DE is still >15% at a 6-dB back-off, owing to the Class-B mode of each PA. However, minor distortion can be observed at low input power. With the proposed de-MUX, the upsampling replicas are rejected by >45 dB (Fig. 15). The gain mismatch (between elements 1 and 4) is reduced from 1.25 to 0.17 dB when the DC feedback technique is enabled.

The BB-to-RF signal gain and peak system efficiency are measured against frequency (Fig. 16). From 0.7 to 2.5 GHz, the system efficiency is >20% and the gain variation is < ±1 dB. The system efficiency at 2.3 GHz can be calculated as 27.6% after accounting the 4-element composite P_{out}.

B. Modulation-Signal Measurement

We employ an 802.11n 20-MHz 64-QAM OFDM signal to evaluate the BB and RF linearity. It is essential to apply the same signals to each element as crosstalk through the air and PCB cannot be completely avoided. The output of each elements is down-converted and sampled by the PXA Signal Analyzer and demodulated in MATLAB, with other elements terminated by the matched input ports of the Oscilloscope. Each TX element shows a −30-dBc first adjacent

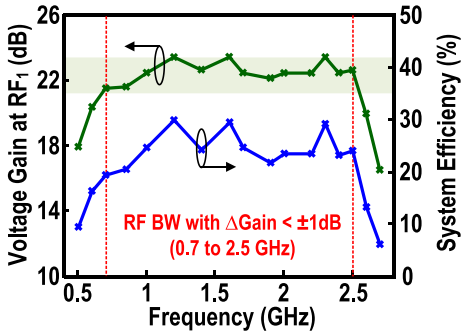

Fig. 16. Measured voltage gain and system efficiency over a wide range of RF.

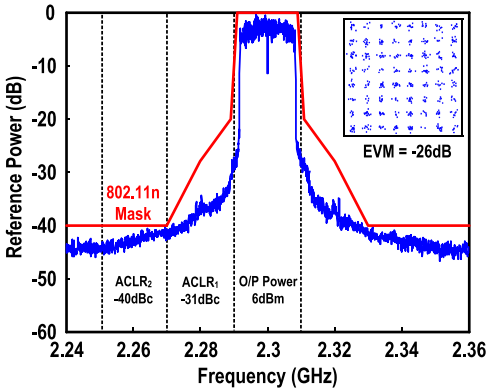

Fig. 17. Measured spectrum mask and EVM for an 802.11n 20-MHz 64-QAM OFDM signal.

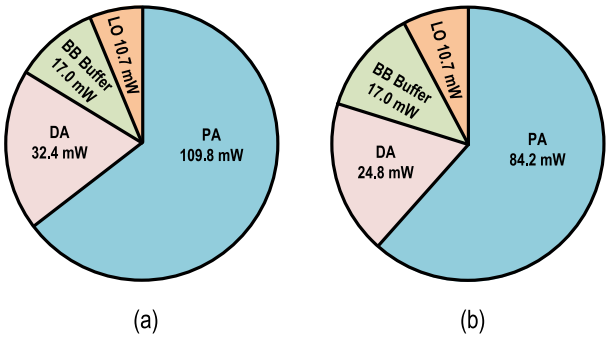

Fig. 18. Power breakdown of the MIMO TX at 2.3 GHz, with a 10.6-dBm output power as (a) Psat and (b) Pave.

channel leakage ratio ($ACLR_1$), a −40-dBc $ACLR_2$ and a −26-dB error vector magnitude (EVM) at a 6-dBm average power (P_{ave}) (Fig. 17). The result includes digital predistortion for better $ACLR_{1,2}$ and EVM.

The power breakdown at peak P_{out} and reported P_{ave} at 2.3 GHz is shown in Fig. 18. An average EIRP system power efficiency (EIRP η_{ave}) can be calculated as 11.6%. The power consumption of the LO increases from 4.0 to 11.3 mW from 0.5 to 2.5 GHz, while the power consumption of other circuitries remains relatively constant.

C. MIMO Diversity Gain Measurement

A 2.3-GHz 4-element MIMO antenna array is developed to verify the diversity gain [Fig. 19(a)]. By using 4 commercial chip antennas from Johanson 2450AT18A100 the PCB is reasonably small (6.5 cm ×3.8 cm) to fit in a mobile terminal

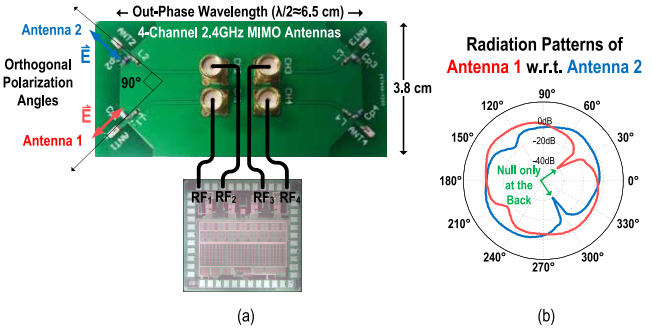

Fig. 19. (a) Antenna array-on-PCB using 4 SMD chip antennas. (b) Propagation pattern of the chip Antenna 1 with respect to Antenna 2.

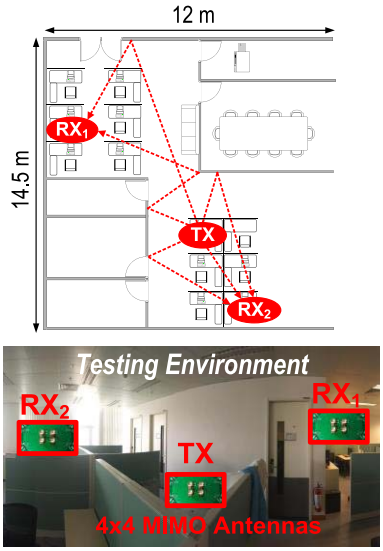

Fig. 20. MIMO diversity gain validation in a practical environment.

such as a tablet. $S_{11} < -15$ dB is achieved at 2.3 GHz at each antenna SMA input port. To achieve the diversity gain, the propagation diversity for each element is crucial. A typical beamforming TX [6] requires the antennas to be placed at a uniform distance, typically half-wavelength ($\lambda/2$), to utilize the wavelength diversity. Yet, in a multi-element MIMO system, the null zone in the propagation pattern and the electric-field polarization angle can also be utilized for diversity propagation [Fig. 19(a)]. The chip antenna is polarized linearly, and has a propagation pattern as shown in Fig. 19(b) [23]. The propagation pattern is mostly isotropic, but has null zones at the vertical polarization angle. This idea applied here reduces the PCB dimension by 2x when comparing with a typical beamforming TX.

Line-of-sight communication tests have been extensively studied [7]. Differently here, the field test is based on a multipath channel fading environment (Fig. 20). Two RX sites (i.e. RX_1 and RX_2) are measured separately to investigate the SDMA performance under 4 × 4 MIMO. The OFDM signals are applied to the TX with the antenna array-on-PCB. The RX is emulated by the PXA Signal Analyzer for channel modeling assuming noise independence. With the measured channel models of RX_1 and RX_2 (Fig. 21), the diversity in each path can be clearly observed. The BF and STBC algorithms

TABLE I
CHIP SUMMARY AND BENCHMARK WITH THE STATE-OF-THE-ART

	This Work	ISSCC 2016 [2]	ISSCC 2015 [16] [1]	TCAS-I 2017 [12]
Technology	65nm CMOS	45nm CMOS	65nm CMOS	28nm CMOS
Targeted Applications	Mobile TX	Base-Station TX	Mobile PA	Base-Station TX
Supply Voltage (V)	1.2 / 3	1.1 / 1.7 / 2.5 / 2.7 (SoC)	1.8 / 3.3	12 / 5 / 3.3 (FPGA)
System Architecture	**4-element Spatial De-interleaved MIMO TX**	2 x 2 MIMO	SISO	8-element FPGA MIMO TX
External Matching Parts	**No**	Yes (4 inductors, 3 capacitors, 1 transformer per channel)	No	No
Active Area (mm^2)	**0.76**	9 (only TX and CLK gen.)	0.9	N/A
Composite P_{sat} (dBm)	**10.6 + 6**	13.2 + 3	22.4	-6.0 + 9
Channel Gain Mismatch (dB)	**0.17**	N/A	N/A	N/A
No. of I/Q-DACs Required	**1**	4	1	0
Output BW (GHz)	0.7 to 2.5 (±1dB gain error)	0.4 to 4 (claimed LO coverage)	2 to 6 (±0.8dB gain error)	0.05 to 6
Test under 20MHz 64-QAM OFDM Signals				
Measured at RF (GHz)	2.3	2.6	2.3	5.24
Power Consumption at P_{ave} (P_{sat}) (mW)	137 (170)	500	215 [2] (611)	8388 [4]
EVM (dB)	-26	-46 [3]	-28	N/A
MIMO EIRP Performance				
EIRP P_{ave} (dBm)	**19.2 (=6 + 6 + 7.2)**	6 (=0 + 3 + 3)	13	7 (=-11 + 9 + 9)
EIRP System Efficiency (%)	**61.0**	0.8	9.3	0.06

1 : TX excluded, only PA and DA
2 : Estimated from the reported P_{DC} @ P_{sat} by PAE of a typical Class-AB PA
3 : Linearity target for basestation
4 : P_{DC} extracted from FPGA datasheet [24] (includes output interface only)

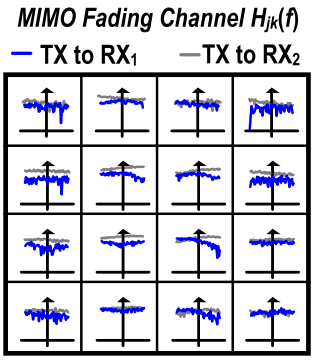

Fig. 21. Measured channel models of RX_1 (Blue) and RX_2 (Grey).

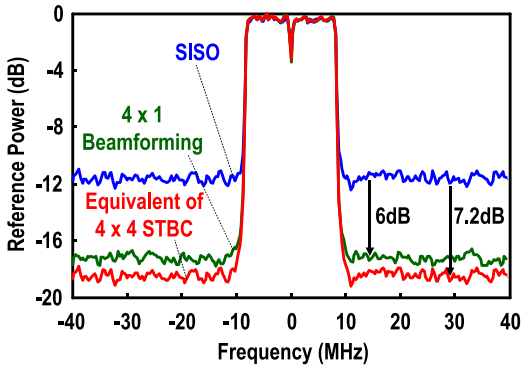

Fig. 22. Signal quality with and without MIMO diversity gain in a practical environment.

are applied to the measured channels, with a diversity gain of 6 and 7.2 dB extracted, respectively (Fig. 22). Moreover, when the TX communicates with the only RX_1, the signal detected by RX_2 can be rejected by 31 dB when applying the beamforming signal (i.e., SDMA is enabled).

D. TX Performance Improvement via MIMO

The equivalent P_{out} of the 4-element MIMO TX is directly boosted by the diversity gain, resulting in an EIRP P_{out} of 23.9 dBm (i.e. 10.7 + 6 + 7.2 dBm) by using the STBC algorithm. Since P_{out} is increased without consuming actual DC power, the peak system efficiency is boosted from 27.6% to 144.4%, which is not possible for a typical SISO TX. The average system efficiency is enhanced from 11.6% to 61.0%. The output noise floor is measured to be −153.8 dBc/Hz at a 10.7-dBm output power. Based on the diversity gain provided by the MIMO techniques, the measured noise floor of the beamforming and STBC modes are −159.8 and −161 dBc/Hz, respectively.

It is possible to enhance the data rate by transmitting 3-parallel data streams simultaneously [Fig. 23(a)] if the SNR

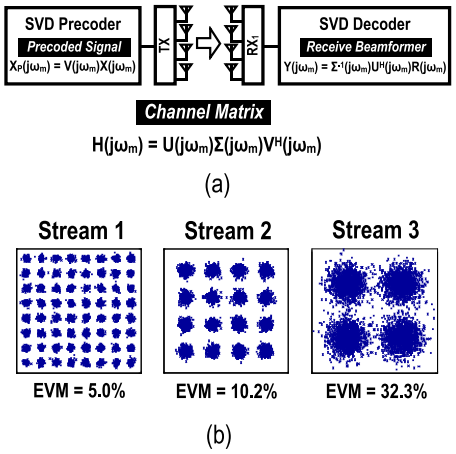

Fig. 23. Multiple data streams with MIMO in a practical environment.

is 4.8 dB higher than the SISO test case (Fig. 22). According to the singular values of each element, 64-QAM, 16-QAM and quadrature phase shift keying (QPSK) signals can be separately adopted for the 3 elements. The measured EVMs for the 3 streams are 5.0%, 10.2% and 32.3%, respectively, which represent a similar signal quality [Fig. 23(b)]. Note that by increasing the data rate of the MIMO radio, the diversity gain reduces. Neither the diversity gain nor power-combining gain is available in the maximum-throughput mode.

E. Comparison With the State-of-the-Art

Unlike the base-station MIMO TX [2] that targets better link capacity and reliability (Table I), this work exploits the virtual gain offered by the MIMO techniques to eliminate the need of high-power PAs and their associated output MNs, enhancing the output BW and equivalent MIMO system efficiency 6x better than the existing SISO TX [16]. Comparing to [12], this work with integrated PAs delivers a higher EIRP. Moreover, the BB data is also modulated linearly without calibration.

V. Conclusions

This work has revealed that MIMO techniques can aid the realization of a TX system with enhanced BW, area and power efficiencies. A novel analog spatial de-interleaver is proposed to reduce the baseband complexity of the MIMO system. It not only reduces linearly the required BB inputs without increasing the BW of their digital interface, but also eases the matching of the BB signals. At the system level, the virtual gain (power- combining gain + diversity gain) generated by MIMO offers 3 key advantages: the relaxed output power of each element of the PA, reduced P_{DC} of each PA element, and nullifies the MN. They together lead to a wider output BW, and better area and power efficiencies. For MIMO effectiveness, all sub-TX and PA elements feature a DC feedback technique to enhance their spatial matching against process variation. The TX chip, validated both at circuit level and in field tests using a practical channel, confirmed its capability of enhancing the signal strength or data rate using the MIMO techniques. This work has the potential of reshaping the future of power-efficient WLAN chips in portable devices (e.g., tablet), which can accommodate an array of GHz-range MIMO antennas.

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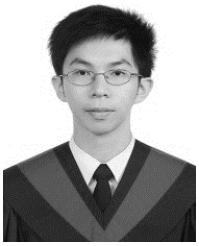

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Dr. Martins was Founding Chairman of both the IEEE Macau Section (2003–2005) and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS) / Communications (COM) (2005–2008) [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS - APCCAS'2008, and was the Vice President for Region 10 (Asia, Australia, and the Pacific) of IEEE CASS (2009–2011). Since then, he was the Vice President (World) Regional Activities and Membership of the IEEE CASS (2012–2013), and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: Express Briefs (2010–2013), nominated Best Associate Editor of T-CAS II from 2012 to 2013. He was also a member of the IEEE CASS Fellow Evaluation Committee (2013 and 2014), and the CAS Society representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS) - Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference - ASP-DAC'2016. He was a Nominations Committee Member (2016) and is currently the Chair of the IEEE Fellow Evaluation Committee (class of 2018), both of the IEEE CASS. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese Academician living in Asia.