A 1-V 10b 40MS/s Pipelined ADC with Low-Voltage Circuit Techniques in 0.18μm CMOS

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***Abstract*— This paper presents a 1-V 10b 40MS/s Pipelined ADC with an effective resolution bandwidth up to 66MHz. Two low-voltage circuit techniques are employed: 1) *feedback current biasing* - which ensures the accuracy of the current source biasing over the process variations without the use of cascode structure in low-voltage environment; 2) low-voltage current-mode sub-ADCs - which allows current-mirror sharing between the low-voltage comparators thus implying a reduction in static power consumption. The proposed ADC was implemented in 0.18μm 1P6M CMOS technology. Chip measurement results show that the DNL and INL are within 0.9 and 1.1 LSB, respectively. The ADC maintains the SNDR over 54.5dB and 51.5dB for input frequencies of 9.1MHz and 66MHz, respectively. The active die area is 2.2mm^2 and the ADC consumes 40mW at 1-V supply.**

***Index Terms*— Pipelined ADC, Low-voltage, Current-mode comparator.**

I. INTRODUCTION

The downscaling of the modern deep submicron CMOS processes continues to create challenges to low-voltage analog circuit designs. The supply voltage is dropping down due to the thinner gate-oxide in advanced CMOS processes. In addition, battery-operated devices often require a lower supply voltage to work. This imposes an operation under the nominal supply voltage at a specific technology node, e.g. 1V at 0.18μm CMOS, for lower cost [1]-[5]. Both cases create stringent requirements in analog and mixed-signal IC designs due to the low supply voltage headroom which demand special low-voltage circuit techniques to overcome those obstacles [1]-[8].

This paper presents an implementation of a 1-V 10b 40MS/s pipelined ADC in 0.18μm 1P6M CMOS with MiM-capacitor option. The proposed ADC is implemented in 1.5b/stage (as shown in Fig. 1) with reset-opamp techniques [3],[5] to avoid using floating switches. Two low-voltage circuit techniques are proposed in the design, namely, *feedback current biasing,* used in the opamps to achieve accurate current biasing independent of process variations without the use of cascode and long-channel devices; and *low-voltage current-mode sub-ADCs* that combine static current mirrors used in the sub-ADC stages to reduce the static power consumption. Moreover, additional and diversified low-voltage techniques will also be used [6]-[8] in the design to avoid the use of

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floating switches. The whole ADC is implemented in 1-V without clock boosting, bootstrapped switches, special low-threshold devices, and in particular any digital calibration.

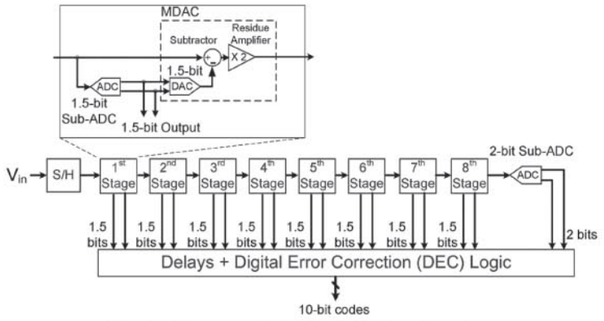

Fig. 1. The overall pipelined ADC architecture.

II. Feedback Current Biasing

Fig. 2 shows the current-mirror opamp that is used in the Sample-and-Hold (S/H) and the Multiplying Digital-to-Analog Converters (MDACs) in the ADC. The NMOS differential pair M1A and M1B has larger tranconductance than their PMOS counterpart, and the differential currents from the drains of the pair are routed to the NMOS current mirrors M3A – M3D. This ensures that the second pole associated with these mirrors is at higher frequency than the PMOS mirrors that are used in traditional current mirror opamps (for description of the opamp's functionality please refer to [8]). For correct operation the bias current of M3A is provided by currents' subtraction between M2A and M1A. The bias current of M1A is provided by the tail current source M0, which can have larger channel length to achieve accurate current matching over process variations (because it is not in the signal path). However, the channel length of M2A can't be too large, since the drain junction capacitance of M2A is in the main signal path and the phase margin will be degraded by this parasitic capacitance. This capacitance can be comparable to the gate capacitance of M3A since M2A is a PMOS transistor with large current handling capability. On the other hand, using a smaller channel length in M2A will imply large current spread over process corners due to the channel length modulation effect from the variation of the gate-source voltage V_{gs} in M3A. Since now the current in M3A would be the subtraction of M2A from M1A it will impose a very large current variation in M3A. This could drive either M3A into cutoff and M1A into triode, or M2A into triode region over the process corners. To overcome this difficulty a feedback biasing circuit is used, as proposed and shown also in Fig. 2. The biasing circuit will simulate the operating point of the main opamps, i.e. MxZ, MxY are the corresponding scaled down versions of Mx, MxA-MxD in main opamp (e.g. M3Z is a scaled-down version of M3A to M3D). The feedback loop composed by M3Z, M6Y, M6Z, M2Y and M2Z ensures identical drain voltages in M2Z and M2A. Since their drain voltages are identical, the current matching between them is accurate over process variations even with small transistor lengths. Choosing larger channel lengths for M0Z and M0 also allows accurate matching between them. Now, since the currents through M2Z and M0Z are identical, this technique guarantees closely tracked currents between M2A and M1A, then minimizing M3A's current variation.

The purpose of the current mirror pair M6Y, Z is to ensure that the feedback loop is negative. A large NMOS capacitor MC1 is added in the drain of M2Z to stabilize the feedback loop. The simulated results show that with +/- 80mV drain voltage variation in M2A over process corners, the current in M3A is within +/- 2% with only L = 0.25μm in M2A. Finally, the transistor pair formed by M4A and M4B doesn't require completely in the saturation region (more details in [8]), which allows the maximization of the output signal swing under 1-V supply voltage.

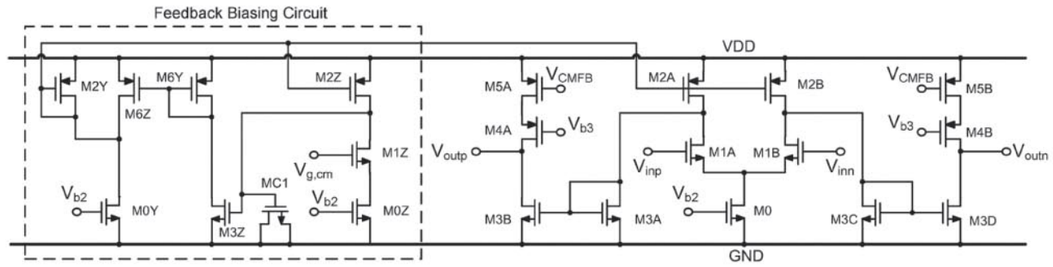

Fig. 2. The low-voltage current mirror opamp with the feedback current biasing techniques.

III. Low-Voltage Current-Mode Sub-ADC

The 1.5b sub-ADC contains two comparators while the final 2b sub-ADC contains three. Conventional voltage-mode differential pair architectures are not possible to be used in low-voltage designs due to limited voltage swing and input common-mode range. Also, switched-capacitor comparators cannot be utilized due to the floating switches problems. A current-mode comparator [9] will be adopted in this design due to its capability in low-voltage operation and adjustable threshold. The current-mode comparator also exhibits very low kick-back noise from the latch since it is shielded in two steps by the current-mirror and the input resistors. However, due to the current-mode operation the comparator will draw static power in the current mirror, and in order to reduce it a low-voltage current-mode sub-ADC architecture is proposed, as shown in fig. 3 in 1.5b version, to share the static current mirror in the sub-ADC. The current mirror voltages V_{binp}, V_{binn} are generated from the input signal V_{inp} and V_{inn}, and V_{brefp}, V_{brefn} are generated from the supply rails in order to produce reference voltages for the comparators. These mirror nodes can be shared among two comparators as shown in Fig. 3, since they have identical thresholds with different polarities (+/- 0.25 V_{ref} comparator thresholds as required in 1.5b stages). The zero-crossing points of the two comparators are defined as follows:

$$V_{inp} - V_{inn} = \pm\tfrac{1}{8}V_{DD} = \pm\tfrac{1}{4}V_{ref} \qquad (1)$$

The offset of the comparators are far below the specifications due to the large offset tolerance of the 1.5b/stage pipelined ADC architecture with Digital Error Correction (DEC). Finally, the 2b sub-ADC exhibits a similar technique with different current mirror ratios for different threshold voltages. In terms of power each 1.5b sub-ADC consumes 250μW whereas the whole 2b sub-ADC draws 500μW.

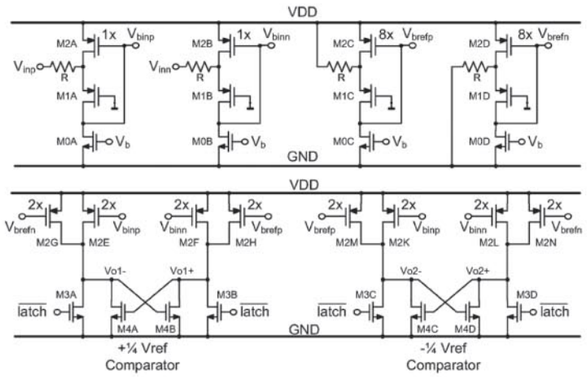

Fig. 3. The low-voltage current-mode 1.5b sub-ADC architecture.

IV. Circuit Implementation

The proposed reset-opamp ADC has been implemented with a traditional 1.5b/stage pipelined ADC architecture, with a front-end S/H, 8 MDACs, 8 1.5b sub-ADC stages and a final 2b sub-ADC, as illustrated before in Fig. 1. The full-scale differential input range is $1V_{p\text{-}p}$ and all reference voltages are generated on-chip from the supply rails by the capacitive charge redistribution [3]. The supply rails are heavily decoupled by on-chip PMOS capacitors to obtain stable reference voltages and low inductive supply noise.

To cope with several issues emerging from a low-voltage design in the absence of floating switches, various other advanced low-voltage circuit techniques are further utilized. For low-voltage operation of the opamp, the virtual-ground Common-Mode (CM) voltage is set at 0.75V while the opamp output CM voltage is set at 0.5V. To handle the low-voltage Common-Mode Feedback (CMFB) a Virtual Ground Common-Mode Feedback (VG-CMFB) technique [6] has been utilized. Besides that, the front-end interface with the continuous-time input signal is implemented by a Cross-Coupled input S/H [7]. Finally since the DC gain of the single-stage current-mirror opamp is not enough for 10b operation, a Low-Voltage Finite Gain Compensation (LV-FGC) technique [8] is employed also.

V. Experimental Results

The prototype ADC has been fabricated in a standard 1.8-V 0.18μm 1P6M CMOS process with MiM capacitor (V_{thn}/V_{thp} = 0.63 / -0.65V typical). The chip microphotograph is shown in Fig. 4 with an active die area of $2.2mm^2$. The 10b digital data are captured by a logic analyzer and transferred to a computer for data analysis. Fig. 5 presented the printed-circuit board and the measurement setup.

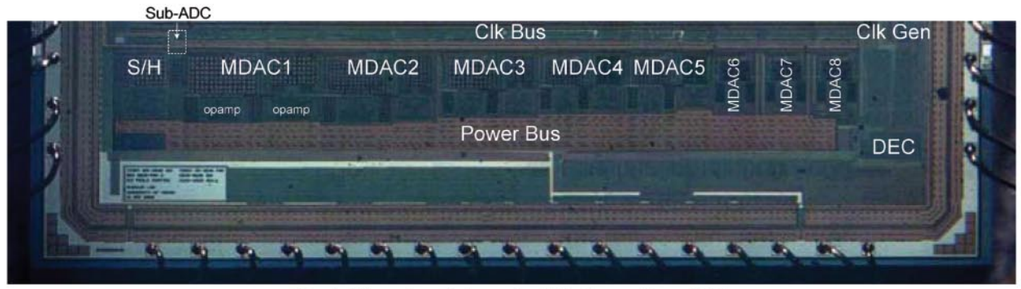

Fig. 4. The microphotograph of the low-voltage ADC.

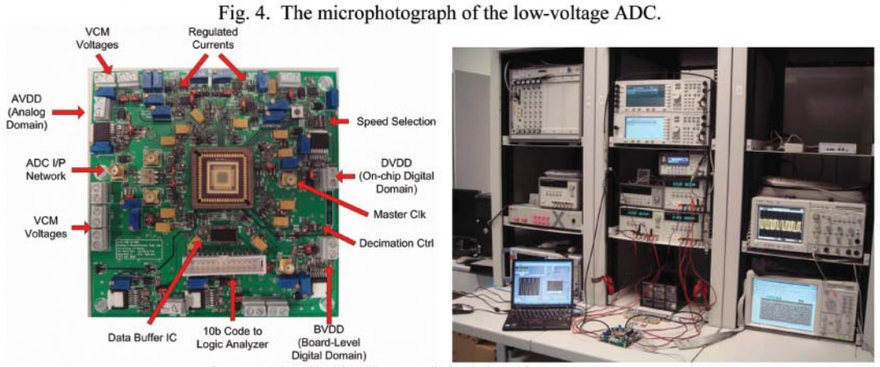

Fig. 5. Printed-Circuit Board design and Measurement Setup.

The static performances of the ADC are measured using the traditional sine-wave histogram method. The measured Differential

Nonlinearity (DNL) and Integral Nonlinearity (INL) of the ADC are +0.5 / -0.9 LSB and +1.1/-1 LSB, respectively and are represented in Fig. 6.

The dynamic performances of the ADC are also measured by evaluating the spectrum of the captured data. Fig. 7 shows an FFT spectrum of the ADC with f_{in} = 9.1MHz, amplitude of A_{in} = -0.1 dBFs input signal with SNDR = 54.5 dB, THD = -70 dB and SFDR = 74 dBc, respectively. The ADC consumes 40mW from 1-V supply, and the performance is summarized in Table 1.

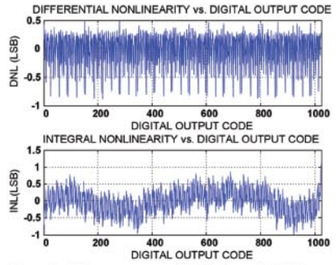

Fig. 6. The measured DNL and INL.

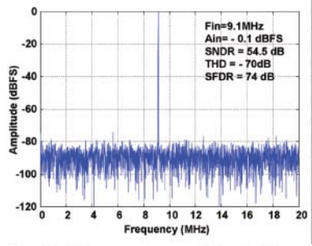

Fig. 7. The spectrum of the ADC.

Technology	0.18μm 1P6M CMOS with MiM
Resolution	10b
Supply Voltage	1V
Full-Scale Input Range	1Vp-p differential
Sampling Rate	40 MS/s
ADC Active Area	2.2 mm^2
ADC Core Power	40 mW
DNL	+0.5 / -0.9 LSB
INL	+1.1 / -1 LSB
SNDR @ fin = 9.1MHz	54.5 dB
ENOB @ fin = 9.1MHz	8.8
SFDR @ fin = 9.1MHz	74 dB
THD @ fin = 9.1MHz	- 70 dB
Effective Resolution Bandwidth	66MHz

TABLE I Performance Summary

VI. Conclusions

This paper presents an implementation of a 1-V 10b 40MS/s pipelined ADC fabricated in 0.18μm CMOS with MiM option. Two circuit techniques are employed in the design to cope with low-voltage analog design requirements. The first technique, namely the feedback current biasing, is employed in all opamps in the ADC to suppress the process variations in the current matching of short-channel MOSFET. Second the low-voltage current mode sub-ADC architecture is proposed to share the static current mirrors among all comparators in a sub-ADC to reduce the static power consumption. The measured DNL and INL are within 0.9 and 1.1 LSB respectively. The ADC achieved a peak SNDR of 54.5 dB with an effective resolution bandwidth as large as 66MHz, while consuming only 40 mW under the very low supply voltage (1-V), with an active die area of $2.2mm^2$.

Acknowledgment

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Author Biography

Sai-Weng Sin (S'98 – M'06) received the B.Sc., M.Sc. and Ph.D. degrees (all with the highest honors) in Electrical and Electronics Engineering from University of Macau, Macao SAR, China, in 2001, 2003 and 2008 respectively. He is currently working in the field of low-voltage, high-speed monolithic analog-to-digital converter designs.

Dr. Sin is currently an Post-Doctoral Research Fellow in the Faculty of Science and Technology, University of Macau, and is also coordinating the Data Conversion Research Line in Analog and Mixed-Signal VLSI Laboratory, University of Macau. His research interests include low-voltage, high-speed analog integrated circuit designs, high-performance data converters, as well as in the timing-jitter analysis and low-jitter clock generator designs for high-performance, high-speed mixed-signal systems. He has published over 20 technical journals and conference papers in the field of interests.

Dr. Sin received the Financial Support Award for Student Paper Contest in 2005 International Symposium on Circuits and Systems (ISCAS) held in Kobe, Japan, the Paper with Certificate of Merit for the 2006 RIUPEEEC Conference, as well as Award of Dean Honor List, Faculty of Science and Technology, University of Macau, in 1999-2000 and 2000-2001 respectively and the Excellent Scholarship of CEM (Companhia de Electricidade de Macau) for the outstanding academic achievement in 2000-2001 (organized by University of Macau). He also received the Post-Graduate Studentships of University of Macau during 2001-2003 (for M.Sc.) and 2004-2007 (for Ph.D.)..

Seng-Pan U (S'94–M'00–SM'05) received the B.Sc. degree in electronics engineering from Jinan University, Guangzhou, China, in 1991. He received the M.Sc. degree in Electrical and Electronics Engineering (EEE) from University of Macau (UM), Macao SAR, China in 1997 and the joint Ph.D. degree in EEE from the UM and the Instituto Superior Técnico, Universidade Técnica de Lisboa (IST/UTL), Lisbon, Portugal in 2002.

Dr. U has been with Dept. of EEE, Faculty of Science and Technology (FST), UM since 1994, where he is currently Associate Professor and leading the Analog & Mixed-Signal VLSI research laboratory. During 1999-2001, he was also on leave to the Integrated CAS Group, Center of Microsystems, IST/UTL, as a Visiting Researcher.

In 2001, Dr. U co-founded the Chipidea Microelectronics (Macau), Ltd., devoted in advanced analog and mixed-signal Semiconductor IP (SIP) product development, and was Engineering Director for leading the data conversion and system solution divisions. Since 2003 he has been the Vice-President (IP Operations Asia Pacific) and General Manager of the company.

Dr. U has published about 70 scientific journal and conference papers. He was also a co-author of *Design of Very High-Frequency Multirate Switched-Capacitor Circuits – Extending the Boundaries of CMOS Analog Front-End Filtering* (Springer, 2005). His research interests are CMOS analog and mixed-Signal integrated circuits, high-performance data-converters, integrated Analog Front-Ends for communication & consumer electronics.

Dr. U received the Excellent Young Scholar Award 2001 (First Prize) and The Most Favorite Teacher Award 2002 and 2003 for the Dept. of EEE, as well as The FST Teaching Awards 2004 from the UM. He also received The Young Researcher Award 2002 from Macau International Institute. In 2005, he was the recipient of the National Lecture Fellowship awarded from K.C.Wong Education Foundation. Dr. U is also the advisor for various international student paper award recipients, e.g. "Silver Leaf Certificate" of The 2005 IEEE Ph.D. Research in Micro-Electronics & Electronics (PRIME), 2nd Place of Conceptual Category of IEEE DAC/ISSCC Student Design Contest 2005, 2nd Prize of IEEE MWSCAS 2004 Student Paper Contest, Outstanding Student Paper Award of ASICON 2003.

Rui P. Martins (M'88 - SM'99 – F'08) received the Bachelor (5-years), the Masters, and the Ph.D. degrees and the *Habilitation* for Full-Professor in electrical engineering and computers from the Electrical Engineering and Computers Department, Instituto Superior Técnico (IST), Technical University of Lisbon (TUL), Lisbon, Portugal, in 1980, 1985, 1992 and 2001, respectively.

He has been with the Electrical Engineering and Computers Department of IST/TUL, since October 1980. Since 1992, he has also been with the Electrical and Electronics Engineering Department, Faculty of Science and Technology (FST), University of Macau (UM), Macao SAR, China, on leave from IST, where he is a Full-Professor since 1998. In FST he was the Dean of the Faculty from 1994 to 1997 and presently he is the Vice-Rector (Research) of University of Macau, post that he holds since 1997. He has co-authored 2 books, 1 book chapter, 2 US Patents (1 submitted and 1 pending), close to 30 scientific journal papers and more than 100 refereed conference papers in the areas of microelectronics, electrical and electronics engineering, and engineering education. His research interests include multirate signal processing, analog and mixed-signal integrated circuit design, as well as microwave filtering.

Dr. Rui Martins is an IEEE Fellow, was the Founding Chairman of the IEEE Macau Section from 2003 to 2005, and he is the Chairman of the IEEE Macau Joint-Chapter on CAS/COM since its creation in August 2005. He was the recipient of 2 government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001.