A 2-μW 45-nV/$\sqrt{\text{Hz}}$ Readout Front End With Multiple-Chopping Active-High-Pass Ripple Reduction Loop and Pseudofeedback DC Servo Loop

Jiangchao Wu, *Member, IEEE*, Man-Kay Law, *Member, IEEE*,
Pui-In Mak, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*—This brief presents an ultra-low-power low-noise chopped capacitively coupled instrumentation amplifier (CCIA) that is suitable for neural recording applications. An active high-pass filter is embedded in the ripple reduction loop (RRL) to suppress the residual noise and relax the capacitor size. Multiple chopping is employed to further reduce the residual output ripple due to the RRL offsets. A dc servo loop (DSL) using a 14-nA pseudofeedback amplifier is proposed to achieve a subhertz high-pass corner while using only a 15-pF on-chip capacitor. The complete CCIA is implemented in a standard 0.18-μm CMOS process. It occupies an area of 0.23 mm^2 (including the DSL) and consumes 1.7 μA from a 1.25-V supply, achieving a noise efficiency factor of 2.9 that compares favorably with the state of the art.**

***Index Terms*—Capacitively coupled instrumentation amplifier (CCIA), dc servo loop (DSL), multiple chopping, neural recording front end, pseudofeedback amplifier, ripple reduction loop (RRL).**

I. Introduction

RECENTLY, neural activity monitoring is becoming popular in human health care applications for early disease detection, including epilepsy, depression, Parkinson's disease, essential tremor, and many more. Neural signals can be classified into local field potential (LFP) or spike potential (SP), with an amplitude of 5 mV from 0.1 Hz to 200 Hz or 500 μV from 200 Hz to 10 kHz, respectively [1]. These challenging recording fidelity requirements impose stringent power, noise, and area trade-offs in neural acquisition front-end designs.

Chopper modulation is an established technique to reduce the offset and $1/f$ noise and has been widely used in recent low-noise neural acquisition front-end implementations. A side effect, however, is the generation of significant output ripple due to the up-modulated offset and $1/f$ noise. A direct way to solve this problem is to add a low-pass filter at the output of the chopper amplifier [2], but the low cutoff frequency requirement (in kilohertz) makes this solution unattractive in many applications. In [3] and [4], correlated double sampling or a synchronous switched-capacitor notch filter is used to achieve spur-free amplification with low power consumption, respectively. However, they both suffer from increased input-referred noise (IRN) due to the folding back of the broad-band noise. Even though the ac-coupled continuous-time ripple reduction loop (RRL) in [5] can reduce the output ripple with no noise folding effect, it still suffers from the residual output ripple introduced by the RRL offsets. As a result, a RRL filtering capacitor as large as 80 pF is required for ripple suppression. In [6] and [7], a switched-capacitor filter is employed to suppress the ripple, but the IRN is again sacrificed as a result of noise aliasing.

Due to the large input electrode offset, a dc servo loop (DSL) is generally employed in neural amplifiers to avoid saturating the amplifier output. One way to obtain the subhertz high-pass corner without using excessively large passive components is to use pseudoresistors implemented with MOSFETs [8], but at the expense of limited linearity under different biasing conditions. In [6], a very large time constant switched-capacitor integrator is presented to achieve a high-pass corner of 0.5 Hz by using only a small capacitor while preserving good linearity. Nevertheless, the large current consumption of 300 nA (~17% of the total power consumption) and the increased IRN due to noise folding ultimately limit the noise efficiency factor (NEF) of the neural acquisition front end.

This brief proposes a fully integrated low-noise chopper-stabilized capacitively coupled instrumentation amplifier (CCIA) with optimized power and area for neural recording applications. By using the proposed multiple-chopping active-high-pass RRL, reduced residual output ripple by using a smaller RRL filtering capacitor can be achieved without suffering from the noise folding effect. A continuous-time DSL employing a 14-nA pseudofeedback amplifier to achieve a subhertz high-pass corner by using only a 15-pF on-chip capacitor is also introduced. Unlike [8] that requires a large loading capacitor to reduce the DSL-induced IRN, the DSL output is fed back to the internal node of the main amplifier that can simultaneously reduce the IRN and the loading capacitor requirement. The neural acquisition front end achieves a NEF of 2.9 and compares favorably with the state of the art.

II. Proposed Neural Recording Front End

In this brief, the chopper-stabilized CCIA topology is chosen based on its superior performance in terms of power-noise efficiency and common-mode rejection ratio (CMRR).

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J. Wu and P.-I. Mak are with State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China.

M.-K. Law is with State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: mklaw@umac.mo).

R.-P. Martins is with State-Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China, and also with Instituto Superior Técnico /Universidade de Lisboa, Portugal, Lisboa, Portugal.

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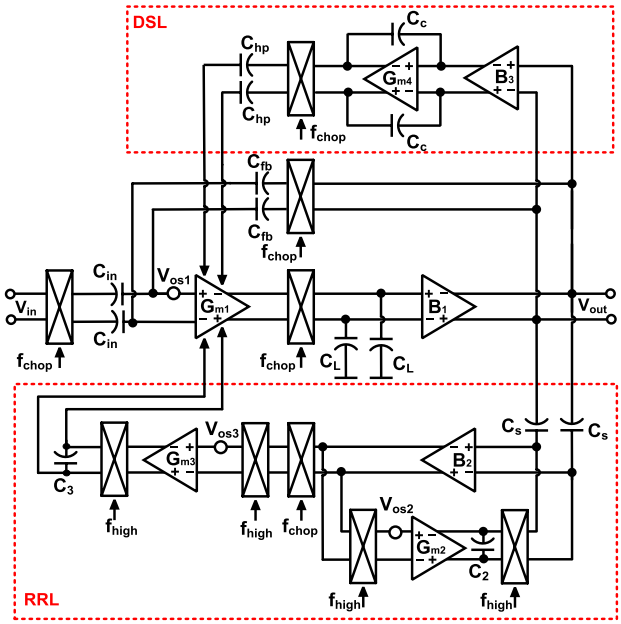


Fig. 1. Proposed chopper-stabilized CCIA topology.

Fig. 1 presents the proposed neural recording front end. A single-stage folded-cascode amplifier (G_{m1}) with internal chopping is utilized to achieve low power consumption without loading the amplifier output. The RRL employs an active high-pass filter composed of a gain stage G_{m2} and a buffer B_2 to further reduce the residual noise from the output, and relax the value of C_3. The RRL output is fed back to the main amplifier internally instead of to the main amplifier output to increase the RRL loop gain. Reusing the current of G_{m1} can reduce the overall power consumption while avoiding additional poles that can degrade the system stability. Multiple chopping is proposed to modulate the RRL offsets to high frequency and to effectively suppress the output ripple. An ultra-low bandwidth pseudofeedback buffer B_3 is inserted before G_{m4} to achieve a subhertz high-pass corner with reduced loading capacitance while dissipating only nanowatt power. The DSL output is connected to the internal node of G_{m1} to reduce the IRN.

Fig. 2 shows the circuit implementation of the folded-cascode main amplifier. With an input-referred offset $V_{\rm OS1}$ (as shown in Fig. 1), the output ripple can be expressed as

$$V_{\rm out,ripple} = g_{m0,1}V_{\rm OS1} \times \frac{1}{2\pi f_{\rm chop}C_p} \times \frac{g_{m4,5}R_{\rm out}}{1+j2\pi f_{\rm chop}C_L R_{\rm out}} \approx V_{\rm OS1} \times \frac{g_{m0,1}g_{m4,5}}{C_pC_L} \times \frac{1}{(2\pi f_{\rm chop})^2} \quad (1)$$

where g_{mi} is the transconductance of M_i, $f_{\rm chop}$ is the chopping frequency, C_p is the parasitic capacitance at the source of $M_{4,5}$, $R_{\rm out}$ is the equivalent output impedance, and C_L is the loading capacitor. For a given bias current, the output ripple can be reduced by increasing C_p (using a large $M_{4,5}$) or C_L. In this brief, C_L is designed to achieve the required signal bandwidth, while a current ratio of 1:12 between the output and input branch is chosen to reduce the IRN.

A. RRL

As shown in Fig. 1, the proposed RRL senses the ac current at $V_{\rm out}$ through C_s. As the input of $B_{1,2}$ can be viewed as

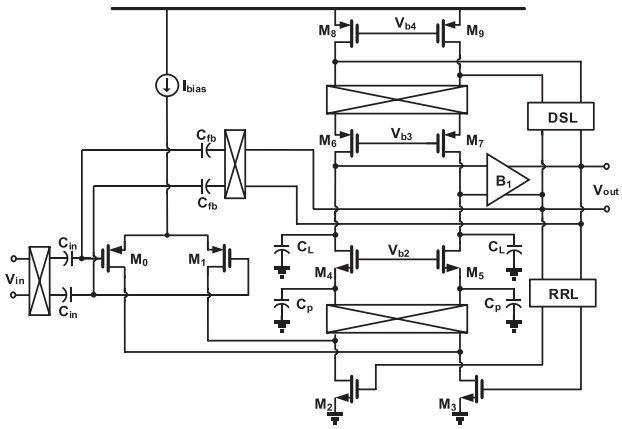


Fig. 2. Circuit implementation of the folded-cascode main amplifier.

virtual grounds at $f_{\rm chop}$, the corresponding current gain can be expressed as C_s/C_L. The generated ac ripple at the input of B_2 passes through the active high-pass filter, which suppresses the residual noise (i.e., the neural signal band) from $V_{\rm out}$, and is then demodulated by $f_{\rm chop}$ back to dc. The signal is then up-modulated by $f_{\rm high}$ and amplified by G_{m3}, followed by demodulation, and is fed back to the gate of $M_{2,3}$ for current reuse, as illustrated in Fig. 2. Assuming that the choppers in G_{m2} and G_{m3} are disabled, the corresponding loop gain of the proposed RRL ($T_{{\rm RRL},p}$) can be derived as

$$T_{{\rm RRL},p} \approx \frac{G_{m3}R_{\rm out,3}}{1+sR_{\rm out,3}C_3} \times \frac{1+(j2\pi f_{\rm chop}-s)R_{\rm out,2}C_2}{G_{m2}R_{\rm out,2}} \times g_{m2,3}R_{\rm out,1} \times \frac{C_s}{C_L} \quad (2)$$

where $R_{{\rm out},i}$ and C_i are the corresponding equivalent output impedance and loading capacitance of G_{mi} in Fig. 1, respectively. Note that C_2 (parasitic capacitance) can be small. Without the active high-pass filter, the corresponding RRL loop gain ($T_{\rm RRL,c}$) can be approximated as

$$T_{\rm RRL,c} \approx \frac{G_{m3}R_{\rm out,3}}{1+sR_{\rm out,3}C_3} \times g_{m2,3}R_{\rm out,1} \times \frac{C_s}{C_L}. \quad (3)$$

The unity-gain frequency of G_{m2} ($f_{0,Gm2}$) should be high enough to pass the ac ripple at $f_{\rm chop}$. Assuming that $f_{0,Gm2} = f_{\rm chop}$, the unity-gain frequencies of the RRL without and with the active high-pass filter can be deduced from (2) and (3) as

$$f_{0,{\rm RRL},c} \approx g_{m2,3}R_{\rm out,1} \times \frac{C_s}{C_L} \times \frac{G_{m3}}{C_3} \times \frac{1}{j2\pi} \quad (4)$$

$$f_{0,{\rm RRL},p} \approx \frac{f_{\rm chop} \times f_{0,{\rm RRL},c}}{f_{\rm chop}+f_{0,{\rm RRL},c}}. \quad (5)$$

Furthermore, the RRL unity-gain frequency should be $\leq f_{\rm chop}/2$ to avoid affecting the main amplifier response. With $f_{0,{\rm RRL},p} = f_{0,{\rm RRL},c}$, we can theoretically reduce C_3 by approximately two times. The corresponding output ripple can be evaluated by dividing (1) with the RRL loop gain at dc

$$V_{\rm out,ripple} \approx V_{\rm OS1} \times \frac{1}{G_{m3}R_{\rm out,3}C_pC_s} \times \frac{g_{m0,1}g_{m4,5}}{g_{m2,3}R_{\rm out,1}} \times \frac{1}{(2\pi f_{\rm chop})^2}. \quad (6)$$

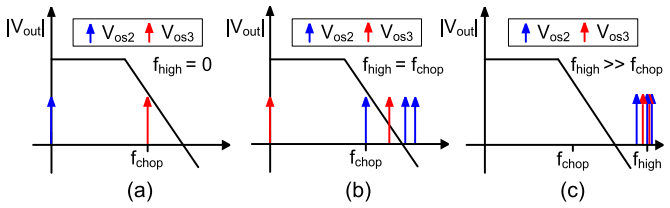


Fig. 3. Illustrative diagram of the RRL offset-induced residual output ripple when (a) $f_{\rm high} = 0$, (b) $f_{\rm high} = f_{\rm chop}$, and (c) $f_{\rm high} \gg f_{\rm chop}$.

As shown in (6), $V_{\rm out,ripple}$ is independent of C_L. A reduced $V_{\rm out,ripple}$ can be achieved by increasing either C_s or $f_{\rm chop}$. However, this can either increase the chip area or increase the leakage, residual ripple, and offset. Increasing G_{m3} or $g_{m2,3}$ can also reduce the ripple at the expense of increased IRN. In this brief, we set G_{m3} to 0.7 μS to reduce $V_{\rm out,ripple}$, and the increased RRL noise is compensated by using a C_3 of 15 pF.

Traditionally, the RRL offsets are suppressed by $T_{\rm RRL}$ and cannot be reduced by chopping. Even though these noise sources can sometimes be tolerated, it can lead to residual output ripple that can degrade the accuracy. Fig. 3 shows the residual output ripple induced by $V_{\rm OS2}$ and $V_{\rm OS3}$ (as shown in Fig. 1). The offset of B_2 is suppressed by the loop gain of the active high-pass filter and contributes to negligible output ripple. Conventionally, $f_{\rm high}$ is set to zero. $V_{\rm OS2}$ is modulated twice and leads to an increased offset and second-order harmonics, while $V_{\rm OS3}$ generates the first-order residual. When $f_{\rm high} = f_{\rm chop}$, $V_{\rm OS2}$ contributes to the odd-order ripple, and $V_{\rm OS3}$ causes the offset and second-order ripple.

To reduce such residual ripple without introducing noise aliasing as in [6], we propose to use multiple chopping to chop $V_{\rm OS2}$ and $V_{\rm OS3}$ by using a high chopping frequency $f_{\rm high}$. By pushing the RRL offsets to a high frequency, their induced residual output ripple can be sufficiently suppressed. Considering the case when $f_{\rm high} \gg f_{\rm chop}$, $V_{\rm OS2}$ is modulated to $f_{\rm chop}$ at the input of G_{m3}, with additional high frequency images at $(2f_{\rm high} - f_{\rm chop})$ and $(2f_{\rm high} + f_{\rm chop})$, which can be readily suppressed by C_3. For the remaining offsets $V_{\rm OS3}$ at dc and $V_{\rm OS2}$ at $f_{\rm chop}$, they are then up-modulated by $f_{\rm high}$, and the high-order harmonics at $(f_{\rm high} - 2f_{\rm chop})$, $(f_{\rm high} - f_{\rm chop})$, $f_{\rm high}$, $(f_{\rm high} + f_{\rm chop})$, and $(f_{\rm high} + 2f_{\rm chop})$ can be further filtered by C_3 and C_L as illustrated in Fig. 3(c). Assuming that the main amplifier has a single dominant pole, the residual output ripple suppression ratio can be approximated as $f_{\rm high}/f_{\rm chop}$. Even though the residual output ripple generated by the RRL can be largely reduced by having $f_{\rm high} \gg f_{\rm chop}$, this can increase the leakage and reduce $T_{\rm RRL}$, limiting the resultant output ripple suppression level. Based on the simulation results, the optimal ratio between $f_{\rm high}$ and $f_{\rm chop}$ is 4, which is further verified by measurement results in Section III.

B. DSL

In order to reduce the loading capacitor in the DSL amplifier due to the small unity-gain frequency requirement, the DSL feedback node is connected to an internal node (source of $M_{6,7}$) instead of to the input of the main amplifier. The high-pass corner frequency $(f_{\rm hp})$ can be defined as

$$f_{\rm hp} = \frac{C_{\rm hp}}{C_{\rm fb}} \times \frac{g_{m6,7}}{g_{m0,1}} \times f_{0,\rm DSL}. \tag{7}$$

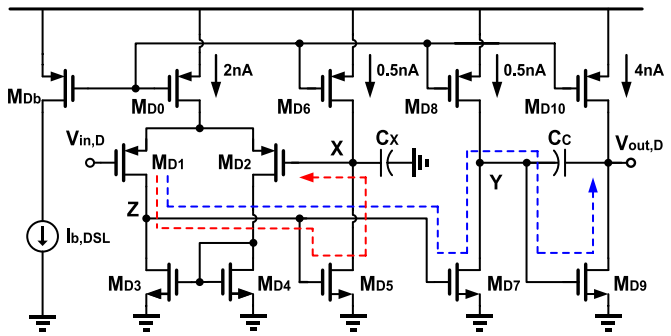


Fig. 4. Simplified circuit implementation of the pseudofeedback amplifier.

As indicated in (7), the required $f_{0,\rm DSL}$ can be reduced by $g_{m0,1}/g_{m6,7}$ when compared to the conventional topology with the same $f_{\rm hp}$, resulting in a corresponding reduction in the DSL amplifier loading capacitor. Moreover, the IRN introduced by the DSL can also be reduced by $g_{m0,1}/g_{m6,7}$. This relaxes the loading capacitor requirement and will be discussed in Section II-C. Fig. 4 shows the simplified circuit implementation of the pseudofeedback amplifier employed in the DSL that can further reduce the loading capacitor (C_C) requirement (the actual implementation is pseudodifferential). It consists of an ultralow bandwidth buffer (M_{D0-6}), a pseudobuffer branch (M_{D7-8}), and an amplification stage G_{m4} (M_{D9-10}). The feedback path directly connects node X to the input. $M_{D5,7}$ and $M_{D6,8}$ are identical, thus maintaining the unity-gain property at node Y. The signal at node Y is further amplified by G_{m4}. The 3-dB bandwidth can be expressed as

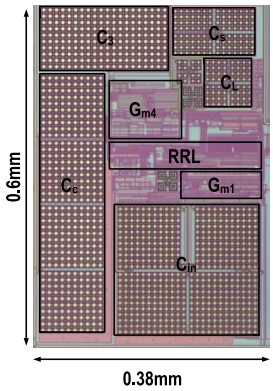
$$f_{3\,\rm dB} = \frac{1}{2\pi \times C_C \times R_{{\rm out},Y} \times g_{m,D9} \times R_{{\rm out},D}} \tag{8}$$

where $R_{{\rm out},Y}$ is the output impedance at node Y, $g_{m,D9}$ is the transconductance of M_{D9}, $R_{{\rm out},D}$ is the output impedance at $V_{{\rm out},D}$, and C_C is the compensation/loading capacitor. The corresponding unity-gain frequency can be approximated as

$$f_{0,\rm DSL} = \frac{1}{4\pi \times C_C \times R_{{\rm out},Y}}. \tag{9}$$

The transistor output impedance can be up to teraohms using a nanoampere-level bias current, which is utilized to generate the ultralow $f_{0,\rm DSL}$ with a reduced C_C. In this brief, only a C_C of 15 pF is required to achieve the 0.5-Hz high-pass corner. The mismatch-induced offsets by $M_{D5,7}$ and $M_{D6,8}$ are suppressed by the large DSL loop gain. As the DSL only consumes a total current of 14 nA, $f_{\rm hp}$ is expected to vary due to process variation. Simulation results from 1000 Monte Carlo runs show that $f_{\rm hp}$ can vary by $\pm$0.5 Hz. The designed $f_{\rm hp}$ can be restored by calibrating $I_{\rm b,DSL}$ within a range from 7 to 210 nA, which can be implemented using on-chip trimming networks during wafer testing. In addition, $f_{\rm hp}$ remains constant from 30 °C up to 100 °C, covering the range for typical human health care applications.

For stability considerations, the feedforward and feedback paths are considered separately. The feedforward path contains three poles, with $\omega_{p,Y} = 1/(C_C \times g_{mD,9} \times R_{{\rm out},D} \times R_{{\rm out},Y})$, $\omega_{p,\rm out} = 1/(C_C \times R_{{\rm out},D})$, and $\omega_{p,Z} = 1/(C_Z \times R_Z)$. In this design, $\omega_{p,Z}$ is pushed to high frequency by minimizing the corresponding parasitic capacitance C_Z. With



Device	Size (μm)	g_m/I_d	Device	Value (μS)
$M_{0/1}$	18/0.5	25.3	G_{m1}	14.5
$M_{2/3}$	1/19.2	6.2	G_{m2}	0.7
$M_{4/5}$	1.2/10	19	G_{m3}	0.7
$M_{6/7}$	2/6	18.7	G_{m4}	0.025
$M_{8/9}$	2/30	11.4		
Device	**Size (μm)**	**g_m/I_d**	**Device**	**Value (pF)**
$M_{D1/2}$	4/0.3	27	C_{in}	12
$M_{D3/4}$	3/50	21	C_{fb}	0.24
$M_{D5/7}$	0.5/6	27	C_L	1.5
$M_{D6/8}$	0.25/24	20	C_{hp}	0.2
M_{D9}	0.5/6	24	C_s	2
M_{D10}	2/24	20	C_X/C_C	2.1/15

Fig. 5. Chip photograph and the key component parameters.

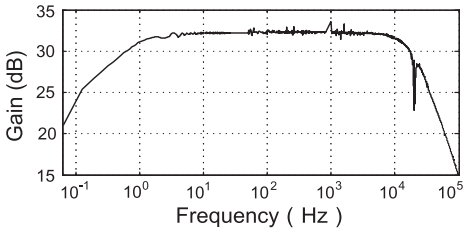


Fig. 6. Measured frequency response of the complete CCIA.

C_C equal to 15 pF, the term $g_{m,D9} \times R_{\text{out},D}$ is designed to be large (∼60 dB) in order to have $\omega_{p,Y} \ll \omega_{p,\text{out}} \ll \omega_{p,Z}$ to ensure system stability. The feedback path contains two poles at nodes X and Z, and a compensation capacitor C_X is inserted to ensure $\omega_{p,X} \ll \omega_{p,Z}$. On the other hand, the bandwidth of the main amplifier should be $\ll \omega_{p,X}, \omega_{p,Z}$ to prevent the created notch from entering the signal band.

C. Noise Analysis

The IRN of the main amplifier $\overline{V_{\text{in,op}}^2}$ is originated in the main amplifier, RRL, and DSL and can be expressed as

$$\overline{V_{\text{in,op}}^2} \approx \frac{4kT\gamma}{g_{m0}} + 4kT\gamma\left(\frac{g_{m2,3}}{g_{m0,1}^2} + \frac{g_{m8,9}}{g_{m0,1}^2}\right) + \overline{V_{n,\text{RRL}}^2} \times \left(\frac{g_{m2,3}}{g_{m0,1}}\right)^2 + \overline{V_{n,\text{DSL}}^2} \times \left(\frac{1}{sC_{\text{hp}}}\right)^2 \times \left(\frac{g_{m6,7}}{g_{m0,1}}\right)^2 \quad (10)$$

where γ is the thermal noise coefficient, g_{mi} represents the transconductance of the transistor M_i, and $\overline{V_{n,\text{RRL}}^2}$ and $\overline{V_{n,\text{DSL}}^2}$ are the noise generated by the RRL and DSL, respectively. Furthermore, $\overline{V_{n,\text{RRL}}^2}$ is mainly contributed by the noise of G_{m3} and can be reduced by $g_{m0,1}/g_{m2,3}$. The noise from B_2 is suppressed by the loop gain of the active high-pass filter, while the noise from G_{m2} is reduced by C_3. Apart from the dominant pole produced by C_C in G_{m4}, $\overline{V_{n,\text{DSL}}^2}$ is also reduced by $g_{m0,1}/g_{m6,7}$. Subsequently, a large loading capacitor is not required for $\overline{V_{n,\text{DSL}}^2}$ suppression. Plus, $M_{0,1}$ operates in the weak inversion region with a g_m/I_d of 25.3.

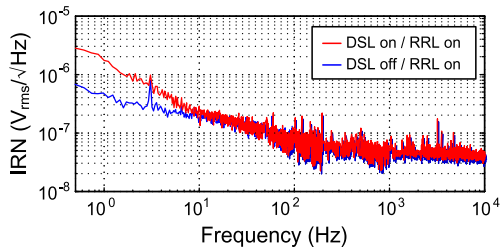


Fig. 7. Measured IRN of the CCIA with RRL on and DSL on/off.

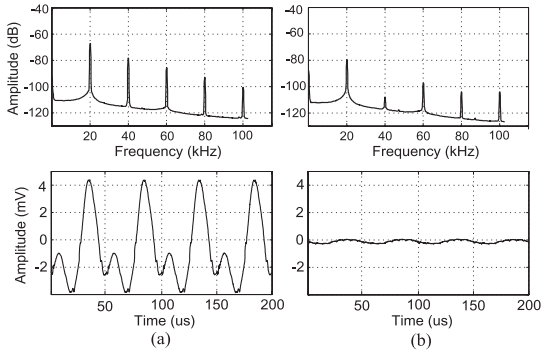


Fig. 8. Measured output spectrum and transient waveform of the CCIA with (a) $f_{\text{chop}} = 20$ kHz, $f_{\text{high}} = 20$ kHz; and (b) $f_{\text{chop}} = 20$ kHz, $f_{\text{high}} = 80$ kHz.

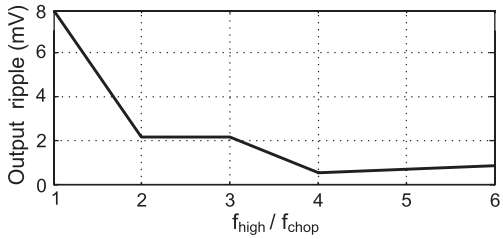


Fig. 9. Measured output peak-to-peak ripple with different $f_{\text{high}}/f_{\text{chop}}$ ratios.

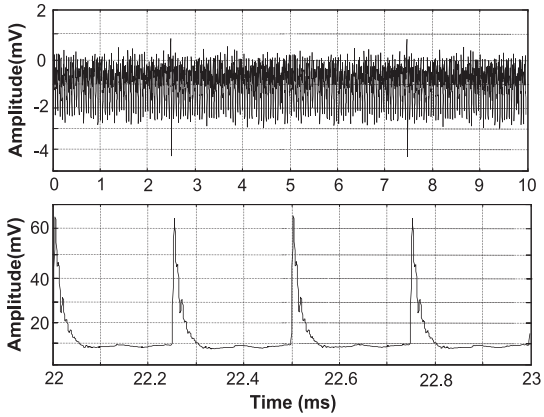


Fig. 10. Measured output waveforms from generated LFP and SP inputs.

III. Measurement Results

The complete neural acquisition front end was implemented in a standard 0.18-μm CMOS technology. The gain is designed to be approximately 34 dB with a chopping frequency of 20 kHz. With C_L equal to 1.5 pF, the complete front end consumes 1.7 μA from a 1.25-V supply, with 1.35 μA, 0.18 μA,

TABLE I
PERFORMANCE COMPARISON WITH THE STATE OF THE ART

	JSSC'09 [5]	JSSC'11 [6]	TBCAS'11 [9]	JSSC'12 [10]	JSSC'12 [11]	JSSC'13 [8]	This work
Technology(μm)	0.7	0.065	0.18	0.35	0.065	0.18	0.18
Supply (V)	5	1	1.8	3.3	0.5	1.8	1.25
Current (μA)	230	1.8	11	22.4	10	1.38	1.7
Bandwidth (kHz)	--	0.1	1	10	10	1	10
CMRR (dB)	120	134	82	110	75	--	85
Area (mm^2)	4.8	0.2	--	0.15	0.013	--	0.23
IRN (nV/$\sqrt{\text{Hz}}$)	15	60#	40	32.9	48	91	45
NEF*	8.8	3.3#	12.3	4.5	5.99	5.12	**2.9**
$V_{out,ripple}$ (mV)	0.07	0.3	2	--	--	--	0.37
C_{DSL} (pF)	--	15	--	--	--	510	**15**
C_{RRL} + C_L (pF)	164	33	--	--	--	--	**18**

* $NEF = V_{ni,rms}\sqrt{\frac{2I_{total}}{4kT\times\pi\times BW\times V_T}}$ # Excluding the DSL

and 14 nA (simulation) from the main amplifier, RRL, and DSL, respectively. Buffers are inserted at the output node to avoid additional loadings due to bond wires and printed circuit board (PCB) traces during measurement. Fig. 5 shows the chip photograph and the key component parameters. The active area is 0.23 mm^2.

Fig. 6 shows the measured frequency response, with a dc gain of 32 dB and a 3-dB bandwidth from 0.5 Hz to 10 kHz. The measured f_{hp} from three samples (without calibrating $I_{b,\text{DSL}}$) are 0.5, 0.7, and 0.8 Hz, respectively. Fig. 7 shows the measured IRN without and with the DSL, respectively. It can be observed that the DSL mainly contributes to the low frequency noise, and the corresponding integrated noise with DSL on from 0.5 Hz to 10 kHz is 5.7 μV_{rms}, leading to a NEF of 2.9. Without the effect of noise folding, the measured thermal noise density is approximately $45\ \text{nV}/\sqrt{\text{Hz}}$. Fig. 8 shows the measured output spectrum and transient waveform with $f_{\text{chop}} = 20$ kHz, and $f_{\text{high}} = 20$ and 80 kHz, respectively. With increased f_{high}, the first- and second-order harmonics values at the output are reduced as expected. The output ripple is reduced from 8 to 0.37 mV_{pp}, demonstrating the effectiveness of the proposed multiple chopping technique. Fig. 9 shows the measured output ripple with respect to different $f_{\text{high}}/f_{\text{chop}}$, where the lowest output ripple is achieved with $f_{\text{high}}/f_{\text{chop}} = 4$. With higher ratios, T_{RRL} decreases, and the ripple gradually increases. The measured input impedance of the amplifier is 1.8 MΩ, which is large enough to prevent signal degradation with a commercial TiN microelectrode (typically ranging between 30 and 400 kΩ). Fig. 10 shows the measured output waveforms using generated LFP and SP inputs. For signal emulation, the digital raw data are first amplified by 40 dB using field-programmable gate array (FPGA) and fed to a 12-b digital-to-analog converter to generate an amplified emulated analog output. The signal is then attenuated back to the original signal level for testing purpose. The measured maximum input offset tolerance of the proposed amplifier is 5 mV due to the limited output swing of the implemented common-mode feedback circuit and the DSL internal feedback. Table I compares the proposed CCIA with the state of the art. Our work achieves the smallest RRL + main amplifier $(C_{\text{RRL}} + C_L)$ and DSL (C_{DSL}) filtering/loading capacitance while preserving low IRN. The reduced power consumption by the RRL current reuse and the DSL pseudofeedback amplifier with internal feedback leads to a NEF of 2.9 that is competitive with the state of the art.

IV. CONCLUSION

This brief presents a chopper-stabilized CCIA implemented in a standard 0.18-μm CMOS technology optimized for neural recording applications. The proposed multiple-chopping active-high-pass RRL achieves a smaller RRL filtering capacitor and reduced residual output ripple without suffering from the noise folding effect. The proposed pseudofeedback amplifier-based DSL consumes only 14 nA to achieve a subhertz high-pass corner using only a 15-pF capacitor. The achieved NEF of 2.9 compares favorably with the state of the art.

REFERENCES

[1] R. Harrison, "The design of integrated circuits to observe brain activity," *Proc. IEEE*, vol. 96, no. 7, pp. 1203–1216, Jul. 2008.
[2] Q. Huang and C. Menolfi, "A 200 nV offset 6.5 nV/$\sqrt{\text{Hz}}$ noise PDF 5.6 kHz chopper instrumentation amplifier in 1 μm digital CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2001, pp. 362–363.
[3] M. Belloni, E. Bonizzoni, A. Fornasari, and F. Maloberti, "A micro-power chopper-CDS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2521–2529, Dec. 2010.
[4] R. Burt and J. A. Zhang, "Micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2729–2736, Dec. 2006.
[5] R. Wu, K. A. A. Makinwa, and J. H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an ac-coupled ripple-reduction loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3232–3243, Dec. 2009.
[6] Q. Fan, F. Sebastiano, H. Huijsing, and K. A. A. Makinwa, "A 1.8 μW 60 nV/$\sqrt{\text{Hz}}$ capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.
[7] Y. Kusuda, "Auto correction feedback for ripple suppression in a chopper amplifier," *IEEE J. Solid-State Circuits*, vol 45, no. 8, pp. 1436–1445, Aug. 2010.
[8] J. Yoo *et al.*, "An 8-channel scalable EEG acquisition SoC with patient-specific seizure classification and recording processor," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 214–228, Jan. 2013.
[9] J. Xu *et al.*, "A 160 μW 8-channel active electrode system for EEG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 555–567, Dec. 2011.
[10] J. Guo *et al.*, "32.9 nV/$\sqrt{\text{Hz}}$ –60.6 dB THD dual-band micro-electrode array signal acquisition IC," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1209–1220, May 2012.
[11] R. Muller, S. Gambini, and J. M. Rabaey, "A 0.013 mm^2, 5 μW, dc coupled neural signal acquisition IC with 0.5 V supply," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 232–243, Jan. 2012.