A Comparative Study of 8-Phase Feedforward-Coupling Ring VCOs

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***Abstract*—This brief studies comparatively the different 8-phase feedforward-coupling (FC) ring voltage-controlled oscillators in terms of their oscillation modes, oscillation frequency, and phase noise. Among the 3 feasible topologies, the one with sub-feedback loops containing 2 direct-path inverters + 1 feedforward-path inverter (i.e., 2D + 1F) can achieve a better phase noise than the common 4D + 1F topology at the same frequency and power budget. It is also shown that the bimodal oscillation problem of the 2D + 1F topology can be eliminated by inserting an auxiliary FC path. Prototyped in 65-nm CMOS, the proposed 2D + 1F topology at 3.1 GHz shows a phase noise of −95.1 dBc/Hz at a 1-MHz offset, corresponding to a 159.9-dBc/Hz figure-of-merit that is 4.2 dB higher than the common 4D + 1F topology.**

***Index Terms*—8-phase ring voltage-controlled oscillators (RVCO), CMOS, feedforward coupling (FC), phase noise, bimodal oscillation, clock generation, LO generation.**

I. Introduction

TAKING the speed benefit of nanoscale CMOS technologies, GHz-range radio-frequency (RF) generation can be based on the ring voltage-controlled oscillators (RVCOs) for its wide tuning range, inherent multi-phase outputs, and compactness in die size. Recent efforts at the system level have demonstrated the potential of the RVCO to replace the bulky LC-VCO [1] even for GHz-range wireless radios [2], [3]. The inherent multiple-phase (e.g., 4/8/16-phase) outputs of a RVCO can be utilized to support harmonic-rejection mixers [4] widely used in modern wideband RF transceivers. This brief studies 8-phase RVCOs with different feedforward-coupling (FC) styles. Although some FC topologies have been reported in [5] and [6], the systematic analysis and comparison of all the possible topologies are still missing. Thus we analytically describe and compare their non-zero oscillation modes, current-ratio requirement between the main-path and FC-path inverters, oscillation frequency, phase noise and figure-of-merit (FoM). To eliminate the tedious differential equations, we propose a 1st-order linear oscillatory model for the FC-RVCO as introduced in [7], to generalize the analysis.

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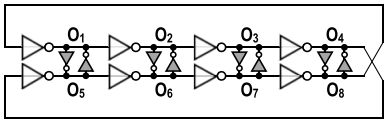

Fig. 1. Conventional 8-phase RVCO with cross-coupled latches.

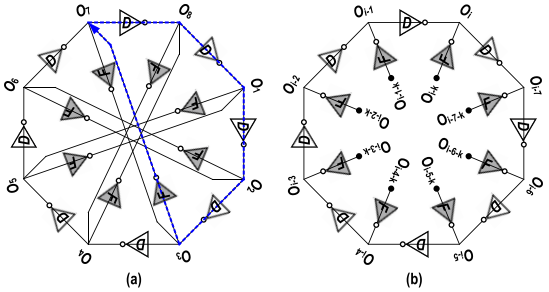

Fig. 2. (a) The rearranged schematic of the conventional 8-phase RVCO made up by Direct-path inverters (**D**) and Feedforward-path inverters (**F**). (b) General structure of an 8-phase FC-RVCO. The input of each **F** can be associated with the output of different **D**.

II. General Model of the 8-Phase FC-RVCOs

A. Conventional 8-Phase FC-RVCO

A typical RVCO with an even number of delay elements (e.g., inverters) cannot generate a non-zero frequency. Extra current paths are entailed to change the oscillation mode, such that the self-gain of certain modes can be greater than that of the zero-frequency mode. The conventional solution [5] adds a latch to each pair of differential outputs as Fig. 1 shows. On the other hand, we can rearrange the schematic by representing the inverter-based delay-cell with the direct-path inverters labeled with **D**, and the latch with the FC-path inverters labeled with **F**, as Fig. 2(a) illustrates. To be presented next, such a topology is only one of the feasible cases, and there are other topologies not yet explored. For this reason, we are interested in comparing the merits of different FC-RVCO topologies in terms of the 4 key performance metrics: oscillation modes, oscillation frequency, phase noise and phase error. To facilitate the analysis, we will introduce next the general model of an 8-phase FC-RVCO.

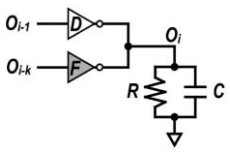

Fig. 3. 1st-order model of one delay cell of an 8-phase FC-RVCO [4].

B. Feasible 8-Phase FC-RVCO Topologies

Generally the input of each feedforward inverter as Fig. 2(a) exhibits can be connected to any output of the direct-path inverter ring, resulting in the general topology of Fig. 2(b). According to the 1st-order equivalent circuit of Fig. 3, the transfer function of the combined single-stage is expressed as,

$$V_{\mathrm{O,i}} = -\frac{G_{\mathrm{m,D}}R}{1+j\omega RC}V_{\mathrm{O,i-1}} - \frac{G_{\mathrm{m,F}}R}{1+j\omega RC}V_{\mathrm{O,i-k}} \tag{1}$$

where $V_{\mathrm{O,i}}$, $V_{\mathrm{O,i-1}}$ and $V_{\mathrm{O,i-k}}$ represent the output voltages at nodes i, $i-1$ and $i-k$ ($k \in [1, 7]$), respectively; $G_{\mathrm{m,D}}$ and $G_{\mathrm{m,F}}$ are the equivalent transconductance of the inverters **D** and **F**, respectively; R and C are the equivalent output resistance and loading capacitance at the node $\mathrm{O_i}$, respectively. Assuming that the current ratio between the inverters **D** and **F** is r, we have $G_{\mathrm{m,F}} = rG_{\mathrm{m,D}}$. Since $V_{\mathrm{O,i-1}} = V_{\mathrm{O,i-k}}e^{j(k-1)\theta}$ where θ is the phase shift between $V_{\mathrm{O,i-1}}$ and $V_{\mathrm{O,i}}$, the transfer function $H(\omega) = V_{\mathrm{O,i}}/V_{\mathrm{O,i-1}}$ can be given by,

$$H(j\omega) = -\frac{G_{\mathrm{m,D}}R}{1+r}\cdot\frac{X+jY}{1+j\omega RC} \tag{2}$$

where $X = 1 + r\cos(1-k)\theta$, $Y = r\sin(1-k)\theta$ and θ can be obtained as,

$$\theta = \pi + \beta - \varphi \tag{3}$$

Here β is the phase of $(X + jY)$, and φ is the phase of $(1 + j\omega RC)$. On the other hand, since the total phase shift of the loop must be $2m \times \pi (m \in \mathbb{Z}_+)$ to satisfy the phase condition of the Barkhausen Criterion, all the possible values of θ for an 8-Phase FC-RVCO can be expressed as,

$$\theta = \frac{2m\times\pi}{8}, m \in [1, 7] \tag{4}$$

where each m represents one of the seven potential oscillation modes named Mode-m. Only the modes that also satisfy the gain condition of the Barkhausen Criterion can guarantee the oscillation of the FC-RVCO. To fulfill the gain condition, $|H(j\omega)|$ must satisfy,

$$|H(j\omega)| = \left|\frac{G_{\mathrm{m,D}}R}{1+r}\cdot(\cos\theta + r\cos k\theta)\right| \geq 1 \tag{5}$$

According to (4) and (5), the phase and gain conditions for an 8-phase FC-RVCO (Fig. 2) can be met simultaneously at a non-zero frequency only for the three topologies with $k = 2, 4, 6$. According to the inverter numbers within each sub-feedback loop, we named these 3 topologies as **4D + 1F** ($k = 4$) [Fig. 2(a)], **2D + 1F** ($k = 6$) [Fig. 4(a)], **6D + 1F** ($k = 2$) [Fig. 4(b)].

According to (4), only the odd modes (m is odd number) can generate 8 unique phases. In the even modes (m is even number), $V_{\mathrm{O,i}}$ and $V_{\mathrm{O,i-4}}$ become in phase since $4\theta = \pi \times m$ and the 8 outputs only have 4 unique phases. Thus, the even modes should be prevented for the applications requiring 8-phase outputs.

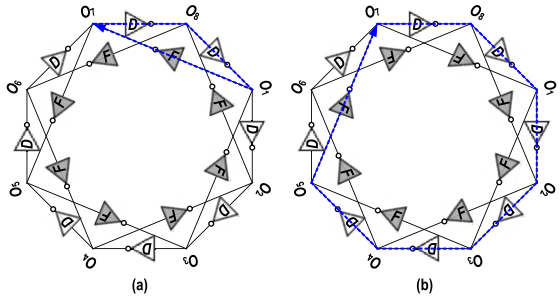

Fig. 4. The other two feasible 8-phase FC-RVCOs generalized from Fig. 2 under k = 2 and 6. They are named as (a) FC-RVCO$_{k=6}$ (**2D + 1F**) and (b) FC-RVCO$_{k=2}$ (**6D + 1F**).

III. Design and Analysis of 8-Phase FC-RVCOs

A. Current Ratio Between D and F

The ratio of transistor sizes between **D** and **F** can be mapped as their current ratio $1 : r$, which needs to be properly selected for robust startup. According to (4) and (5), we can plot $|H(j\omega)|$ as a function of r for the 7 modes as illustrated in Fig. 5(a)-(c). Also φ can be obtained according to (3) and (4) as shown in Fig. 5(d)-(f). Since $\varphi = \arctan(\omega RC)$, it must be within the range of $0 < \varphi < \pi/2$ for non-zero frequency oscillation modes. Particularly, Mode-4 corresponds to a stable steady state without oscillation, since φ is always zero ($\omega = 0$). For all the 3 topologies, Mode-4 has the largest gain for a small r, which suggests the FC-RVCO cannot oscillate if the FC path is too weak. For the conventional **4D + 1F** topology [Fig. 5(a) and (d)], Mode-3 can always meet the phase requirement when its gain becomes larger than that of Mode-4 when $r > 0.15$. Since φ decreases when r goes up, using a larger size of **F** reduces the oscillation frequency. Thus, one should choose a small r to raise the oscillation frequency. According to the simulation, $r = 0.5$ can secure a reliable oscillation at different process corners. Since Mode-3 is the only oscillation mode at $r = 0.5$, the conventional **4D + 1F** topology is free of the even-mode oscillation problem.

Yet, for both **2D + 1F** and **6D + 1F** topologies, Mode-2 can also satisfy the Barkhausen Criterion when $r > 0.125$. When the gain of Mode-2 is close to that of Mode-3, the FC-RVCO may oscillate in Mode-2, depending on the initial voltage of each node. We verified this bimodal oscillation phenomena by simulations. The **2D + 1F** and **6D + 1F** topologies will oscillate in Mode-2 if the initial value of $V_{\mathrm{O,i}}$ is close to that of $V_{\mathrm{O,i-4}}$, while in Mode-3 if there is a big difference between the initial values of $V_{\mathrm{O,i}}$ and $V_{\mathrm{O,i-4}}$. For applications requiring 8-phase outputs, we have to find a way to secure the FC-RVCO only working in Mode-3, as presented later.

B. Oscillation Frequencies

Fig. 6 compares the simulated oscillation frequencies of the 3 topologies that employ the same transistor size for inverters **D** and **F**. All of them operate in Mode-3. Due to the different phase relationships between the inputs of inverters **D** and **F**, the FC path of the **2D + 1F** topology helps reducing the charging/discharging time of the loading capacitor while the FC paths in both the **4D + 1F** and **6D + 1F** prolong the charging/discharging time. Thus the **2D + 1F** topology achieves the highest oscillation frequency. Also a larger r increases the frequency of the **2D + 1F** topology while decreases the frequencies of **4D + 1F** and **6D + 1F** topologies. Particularly

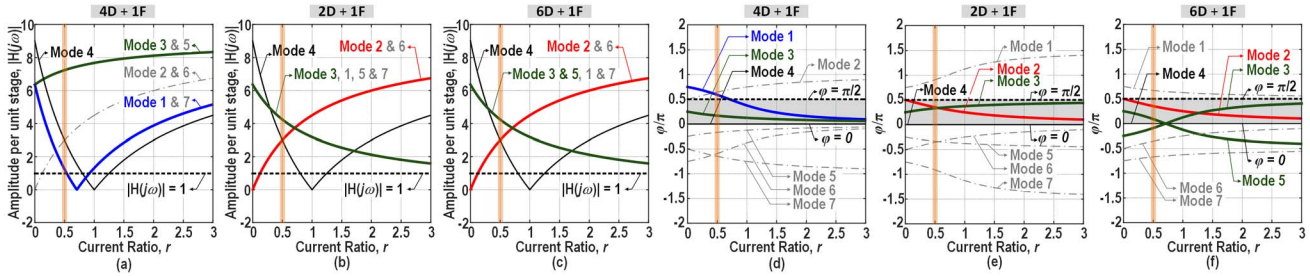

Fig. 5. Calculated amplitude per unit stage of the FC-RVCO with a DC gain $G_{m,D}R = 9$ for topologies (a) **4D + 1F**, (b) **2D + 1F**, and (c) **6D + 1F**. Calculated normalized φ for topologies (d) **4D + 1F**, (e) **2D + 1F**, and (f) **6D + 1F**. The dash lines represent modes that cannot satisfy the phase condition.

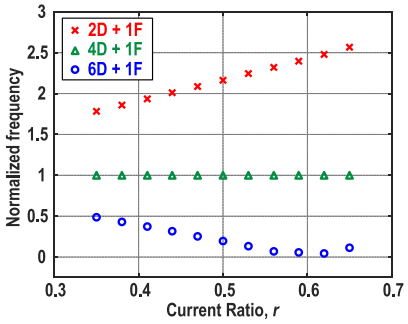

Fig. 6. Simulated oscillation frequency of different topologies normalized to the frequency of topology **4D + 1F** (The same transistor sizes for **D** and **F** in the three topologies).

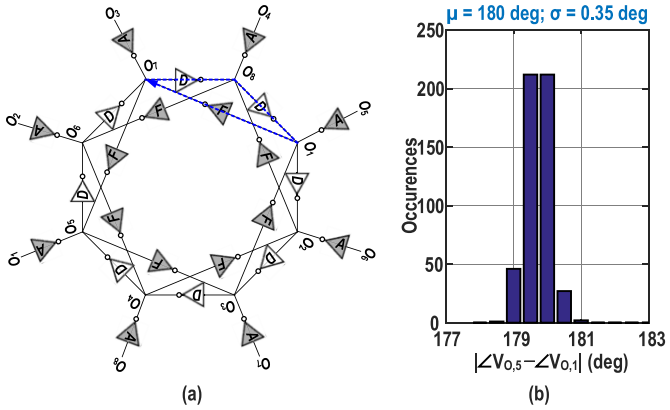

Fig. 7. (a) Proposed 8-phase FC-RVCO using an auxiliary FC-path **A** to avoid even-mode oscillation and (b) the phase differences between $V_{O,5}$ and $V_{O,1}$ from the Monte-Carlo simulations (500-runs).

for $r = 0.5$, the oscillation frequency of **2D + 1F** topology is ∼2.1× higher than that of the **4D + 1F** topology. Since the power consumption increases by ∼1.7× and the phase noise degrades by ∼4.5 dB, the figure-of-merit (FoM) of the **2D + 1F** topology is slightly degraded by ∼0.7 dB.

The speed advantage of **2D + 1F** topology can be exploited to improve the phase noise and FoM. If we raise the transistor channel length in the **2D + 1F** topology, the loading capacitor will increase while the equivalent output resistance decreases. Thus, we can reduce the oscillation frequency of the **2D + 1F** topology to be the same as that of the **4D + 1F** topology. On the other hand, the power dissipation of a RVCO comes from the switching power due to the charging and discharging of the loading capacitance, and the short-circuit power due to the direct current path from the supply to the ground. Although the larger loading capacitor of the **2D + 1F** topology increases its switching power, the reduced transistor size in-turn helps decreasing the short-circuit power. By properly choosing the transistor size, it is possible to keep both the oscillation frequency and power dissipation of the **2D + 1F** and the **4D + 1F** topologies as the same.

C. Prevention of Even-Mode Oscillation

To prevent the oscillation in Mode-2 for the **2D + 1F** topology, the proposed design utilizes an auxiliary FC path **A** from $V_{O,i-4}$ to $V_{O,i}$ to force their voltages out-of-phase [Fig. 7(a)]. For $r = 0.5$, the Monte-Carlo simulation confirms that very small transistor sizes of $(W/L)_A > 0.06(W/L)_D$ are adequate to ensure a $\sim 180^o$ phase difference between $V_{O,5}$ and $V_{O,1}$ in presence of the process variation and device mismatch [Fig. 7(b)] which avoids the FC-RVCO from entering into Mode-2 even when the initial voltage of $V_{O,i}$ and $V_{O,i-4}$ are exactly the same. Table-I lists the transistor sizes of the **2D + 1F** and the **4D + 1F** topologies used in our design, which can achieve the same oscillation frequencies with the same power consumption. Although [6] has reported a fast 8-phase RVCO with a similar topology as the original **2D + 1F** topology from Fig. 4, it did not include a complete analysis of all potential modes and compare the phase noise of all the feasible topologies.

D. Phase Noise

The phase noise of the FC-RVCO can be evaluated by employing the linear time-variant model [8], [9]. According to [10], the phase noise of an oscillator can be written as,

$$\mathcal{L}(\Delta\ \omega) = 10\log_{10}\left[\frac{\sum_i N_{L,i}}{2q_{max}^2(\Delta\ \omega)^2}\right] \tag{6}$$

where $\Delta\omega$ is the offset frequency, q_{max} is the maximum charge displacement across the capacitor at each output node, and $N_{L,i}$ is the effective current noise power produced by the i^{th} MOS device given by:

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(\phi)\overline{i_{n,i}^2(\phi)}d\phi \tag{7}$$

where $\Gamma_i(\phi)$ is the impulse sensitivity function (ISF) that characterizes the device noise to phase conversion properties of the i^{th} MOS device and $\overline{i_{n,i}^2(\phi)}$ is the cyclostationary thermal noise power density of the i^{th} noise source. Since the $\overline{i_{n,i}^2(\phi)}$ of a MOS transistor mainly depends on the transconductance

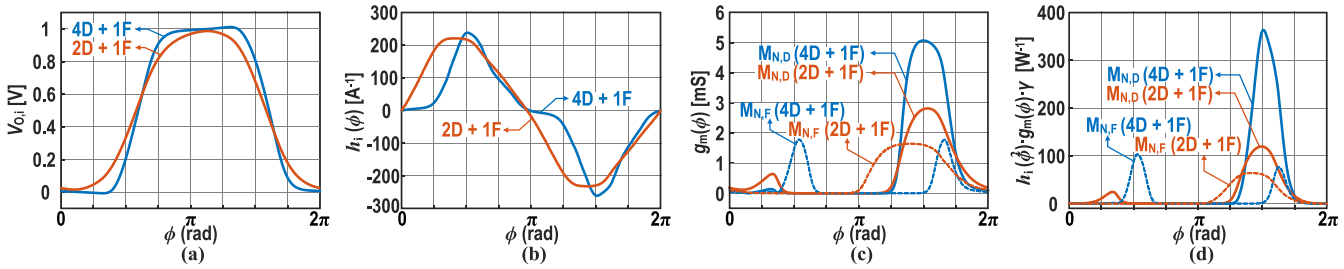

Fig. 8. Simulated (a) output waveform, (b) non-normalized ISF waveform, (c) g_m of NMOS transistors and (d) $h_i^2(\phi)g_m(\phi)\gamma$ of NMOS transistors.

TABLE I
COMPARISON OF TRANSISTOR SIZES, CHANNEL NOISE FACTOR γ AND PHASE NOISE CONTRIBUTIONS FROM g_m AND g_{DS}

		4D + 1F				2D + 1F			
		W / L	γ	$N_{h,gm}$*	$N_{h,gds}$#	W / L	γ	$N_{h,gm}$*	$N_{h,gds}$#
D	$M_{P,D}$	13µm / 65nm	1.23	46.9	15.8	10.4µm / 140nm	0.81	17.7	13.2
	$M_{N,D}$	5µm / 65nm	1.16	46.9	16.6	4µm / 140nm	0.79	20.1	14.0
F	$M_{P,F}$	6.5µm / 65nm	1.25	12.5	15.7	6.5µm / 180nm	0.73	12.5	4.2
	$M_{N,F}$	2.5µm / 65nm	1.16	13.0	14.5	2.5µm / 180nm	0.72	13.3	4.4
A	$M_{P,A}$	N/A	N/A	N/A	N/A	0.4µm / 60nm	1.20	1.2	1.5
	$M_{N,A}$	N/A	N/A	N/A	N/A	0.2µm / 60nm	1.13	1.5	2.2
Sum		N/A	N/A	119.3	62.6	N/A	N/A	66.3	39.5

*$N_{h,gm} = \left[\int_0^{2\pi} h_i^2(\phi) g_m(\phi)\, \gamma d\phi\right]/(2\pi)$; #$N_{h,gds} = \left[\int_0^{2\pi} h_i^2(\phi) g_{ds}(\phi)\, d\phi\right]/(2\pi)$

g_m in the saturation region, and the channel conductance g_{ds} in the triode region, we can evaluate the noise contributions from g_m and g_{DS} separately [11].

Fig. 8(a) and (b) plot the output voltage waveforms and the non-normalized ISFs $h_i(\phi) = \Gamma_i(\phi)/(2\pi f_0 q_{max})$ for both **4D + 1F** and **2D + 1F** topologies at $f_0 = 3.33$ GHz. Here the $h_i(\phi)$ already includes the information of q_{max} to calculate the phase noise as required by (6). Fig. 8(c) plots the g_m of the NMOS transistors. In the **4D + 1F** topology, $M_{N,D}$ has the largest peak value of g_m which dominates the phase noise contribution as Fig. 8(d) presents. In the proposed **2D + 1F** topology, the peak value of the g_m and, consequently, its contribution to the phase noise is significantly reduced due to the smaller transistor size. Besides, the use of long-channel transistors also helps reducing the channel noise factor γ as Table I presents, which further reduces the noise contribution from g_m. Table I summarizes the noise contributions from g_m and g_{ds} of each transistor. The large channel length used in the **2D + 1F** topology also helps to reduce the g_{ds} and thus its noise contribution. The phase noise contribution from PMOS transistors is significantly reduced for the **2D + 1F** topology similar to that of the NMOS transistors. It is also verified that the noise contributions from transistors in the auxiliary path are negligibly small due to their tiny transistor sizes. Using the effective current noise power obtained from Table I, we can estimate that the **2D + 1F** topology can achieve a ~2.4 dB lower phase noise in the $1/f^2$ region compared with the **4D + 1F** topology.

The larger transistor gate area in the **2D + 1F** topology (Table I) also reduces the transistor flicker noise power density which aids suppressing the $1/f^3$ phase noise. The simulation shows that the **2D + 1F** topology can achieve a 4.1 dB phase noise improvement at a 1-MHz offset, of which the additional 1.7 dB improvement comes from the reduced 1/f noise upconversion. The performance of the proposed **2D + 1F** topology in presence of process variation and device mismatch is studied by Monte-Carlo simulations as shown in Fig. 9.

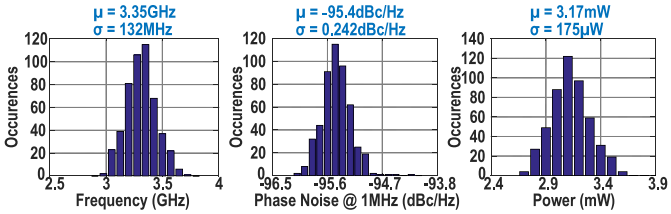

Fig. 9. Frequency, phase noise and power consumption of the **2D + 1F** topology from the Monte-Carlo simulations (500-runs).

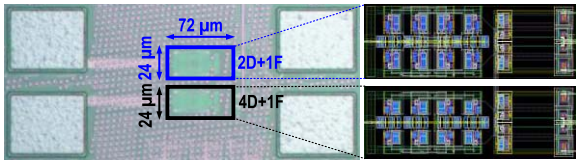

Fig. 10. Chip micrograph of the conventional and proposed FC-RVCOs.

E. Phase Error

Device mismatch can induce phase error between the outputs of the FC-RVCO, which can also be assessed statistically via the Monte-Carlo simulations. Thanks to the transistors with larger gate area, the standard deviation of the worst-case phase error of **2D + 1F** topology is reduced by 1.7× at $r = 0.5$.

IV. EXPERIMENTAL RESULTS

Both the FC-RVCOs **2D + 1F** and **4D + 1F** were fabricated in 65-nm CMOS for comparison (Fig. 10) and operated in Mode-3 (Fig. 5) with their transistor sizes listed in Table I. The frequency tuning is based on 3-bit ($B_3B_2B_1$)

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work		TCAS-I'11 [12]	TCAS-II'13 [13]	TCAS-I'13 [14]
Technique	8-Phase FC-RVCO (**2D + 1F**: Proposed)	8-Phase FC-RVCO (**4D + 1F**: Conventional)	8-Phase RVCO with Dual-Delay Paths	8-Phase RVCO with Channel Thermal Noise Reduction	8-Phase RVCO with CML Buffers
Frequency Range (GHz)	2.68 to 3.56 (28.2%)	2.73 to 3.77 (32.0%)	1.77 to 1.92 (8.13%)	0.486 to 1.012 (70.2%)	2.2 to 2.7 (20.4%)
Power (mW) @ V_{DD}	3.23 @ 1V	3.43 @ 1V	13 @ 1.8V	10 @ 1V	10.1 @ 1.8V
Carrier Frequency (GHz)	3.11	3.11	1.86	0.645	2.5
PN @ 1/10 MHz (dBc/Hz)	−95.1 / −120.0	−91.2 / −115.9	−102 / −123.4	−110.8 / −133.8	-92.83 / N/A
FOM*@ 1/10 MHz (dBc/Hz)	**159.9 / 164.7**	155.7 / 160.4	156.3 / 157.7	157.0 / 160.0	150.7 / N/A
Core Area (mm^2)	0.0017	0.0017	0.0024	0.0225	N/A
CMOS Technology	65 nm	65 nm	0.18 μm	65 nm	0.18 μm

* $\text{FoM} = -\text{PN} + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(P_{\text{DC}}/1\text{mW})$

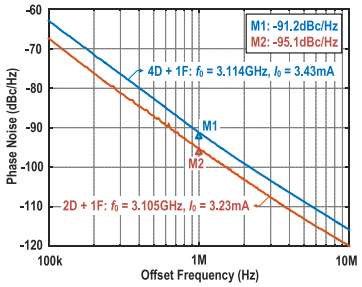

Fig. 11. Measured phase noise versus offset frequency.

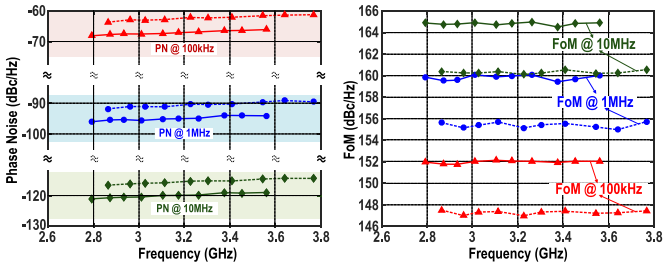

Fig. 12. Measured (a) phase noise and (b) FoM versus oscillation frequency at different frequency offsets (Solid line: **2D + 1F**; Dash line: **4D + 1F**).

digitally-controlled binary-sized varactor bank placed at the output nodes. Both designs feature the same die area of 0.0017 mm^2.

We measured the phase noise with the Keysight E5052B Signal Analyzer as Fig. 11 shows. At a 1-V supply, the phase noise at 1 MHz offset frequency of the **2D + 1F** topology is 3.9 dB better than that of the **4D + 1F** topology, which is consistent with the prediction from the analysis and simulation. The measured output power at 3.1 GHz is −11.7 dBm (−11.8 dBm) for **4D + 1F** (**2D + 1F**) topology. Fig. 12(a) shows the measured phase noise of both FC-RVCOs across the frequency tuning range. Fig. 12(b) compares the measured FoMs for the two topologies. The **2D + 1F** topology shows a consistent ∼4 dB better FoM at 1-MHz offset over the whole tuning range. The measured VCO gain varies from 80 to 197.1 MHz/V (68.5 to 167 MHz) for the **4D + 1F** (**2D + 1F**) topology when $B_3B_2 = 01$. Table II exhibits the performance summary together with two recently reported multi-phase RVCOs for comparison. This brief shows a consistently improved FoM over a wide range of frequency offsets.

V. CONCLUSION

This brief presented the design and comparison of 8-phase RVCOs with different FC paths. The three feasible topologies: **2D + 1F**, **4D + 1F** and **6D + 1F**, are studied and compared analytically. The analysis shows that the **2D + 1F** topology can achieve the highest oscillation frequency that can be exploited to improve the phase noise by employing small-size long- channel transistors. By adding an auxiliary FC path, the proposed **2D + 1F** topology can also avoid the even-mode oscillation and always offer the 8-phase outputs. Prototyped in 65-nm CMOS, the proposed **2D + 1F** topology consistently shows ∼4 dB better FoM than the common **4D + 1F** topology over a wide range of frequency offsets.

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