Algebraic Series-Parallel-Based Switched-Capacitor DC–DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density

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***Abstract*— This article presents an algebraic series–parallel (ASP) topology for fully integrated switched-capacitor (SC) dc–dc boost converters with flexible fractional voltage conversion ratios (VCRs). By elaborating the output voltage (V_{OUT}) expression into a specific algebraic form, the proposed ASP can achieve improvements on both the charge sharing and bottom-plate-parasitic losses while maintaining the high topology and fractional VCR flexibility of conventional two-dimensional series–parallel (2DSP) converters. The proposed method consists of a generic ASP topology framework with systematic parameter determination for a precise converter implementation, and can theoretically surpass the power-conversion efficiency (PCE) of 2DSP converters. Fabricated in 65-nm bulk CMOS, we designed a fully integrated ASP-based SC rational boost converter by cascading with the Dickson topology, with a total of seven rational VCRs to boost an input voltage of 0.25–1 V to a 1-V output. Delivering a maximum loading power of 20.4 mW, the chip prototype achieves a peak efficiency of 80% at a power density of 22.7 mW/mm^2.**

***Index Terms*— Algebraic, boost converter, charge sharing loss, dc–dc, parasitic loss, power density, rational, series–parallel (SP), switched-capacitor (SC), voltage conversion ratio (VCR).**

I. Introduction

THE emerging narrowband Internet-of-Things (NB-IoT) market requires low-power systems, which can be directly powered by wireless energy-harvesting (EH) devices to achieve high system portability. Typically, the generated voltage from a thermoelectric generator and/or a single solar cell can be low, in the order of 0.2–0.5 V. Due to the limited voltage generated by EH devices, a boost dc–dc converter to step up the harvested voltage according to the system requirement becomes necessary. Being the interface between the EH front end and the system load, the dc–dc converter should feature high power-conversion efficiency (PCE), good ambient energy adaptation, and small form factor [1], [2]. In contrast to the inductor-based converter, the switched-capacitor (SC) approach exhibits advantages of full integration in bulk CMOS with competitive efficiency and power delivery capability [3]–[9]. Yet, the conventional SC converters generally suffer from voltage conversion ratio (VCR) inflexibility due to the rigid SC network. Consequently, a highly efficient SC converter preferably with rational-boost VCR reconfigurability is necessary for wide-range EH source/load adaptation.

To generate fine-grained step-down VCRs, several state-of-the-art solutions have successfully achieved optimal charge sharing losses [10]–[12]. However, the widely adopted topology-cascaded structure, which involves an integer and a fractional part [13]–[16], still suffers from suboptimal losses to realize flexible rational-boost VCRs in wide-range on-chip voltage multiplication scenarios. The integer part can be accomplished by using a well-established integer topology, such as the Dickson type for optimal losses [17], [18], while the series–parallel (SP) topology is one of the most well-known choices for the fractional ratio (m/n) realization. For flexible m/n generation, we can employ an m-row-by-n-column power-cell matrix to construct the SP power stage [19]–[23], denoted here by the two-dimensional series–parallel (2DSP) topology. Together with the integer part, e.g., Dickson, the 2DSP-based method is capable of high rational-boost VCR generation, and some of the flying capacitors (C_{fly}) can be reconfigured to generate either the integer or fractional part [13], [24] for full capacitor utilization to reduce the charge sharing loss, represented by the equivalent output impedance R_{SSL} in [25].

This article first revisits the fundamentals of the 2DSP topology for fractional VCR generation. Although the 2DSP can achieve high VCR flexibility through an $m \times n$ capacitor matrix, we can theoretically demonstrate that it in fact suffers from suboptimal R_{SSL} due to the use of extra C_{fly}. Exception only holds for $m = 1$, but a $1 \times n$ cell matrix will significantly

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sacrifice the VCR flexibility. In addition, the 2DSP also exhibits large bottom-plate voltage swing, i.e., $|\Delta V_{\mathrm{CB}}|$, which can increase the parasitic loss. All these limitations ultimately degrade the overall achievable PCE of the 2DSP-based method for on-chip SC dc–dc converter implementations for wide-range rational-boost VCR generation. By exploiting the basic power-cell operations of the 2DSP, we propose an algebraic series–parallel (ASP) topology based on the specific algebraic elaboration of the V_{OUT} expression. We tackle the 2DSP issues in two aspects: 1) resolving the suboptimal R_{SSL} and 2) reducing the bottom-plate parasitic loss (or simply the parasitic loss) through minimizing the corresponding capacitor voltage swing. The proposed ASP-based topology can theoretically achieve improved conduction loss and parasitic loss than the 2DSP one, while retaining the fractional VCR generation flexibility. By systematically assigning the operating voltages of the power cells in the proposed framework, arbitrary rational-boost VCRs using the ASP-based method (Dickson + ASP) can be achieved without using extra C_{fly}. The $|\Delta V_{\mathrm{CB}}|$ in each cell is also analytically bounded to reduce the parasitic loss.

We organize this article as follows. Section II gives a brief rational-boost VCR generation analysis using the conventional 2DSP-based topology. Section III introduces the proposed ASP-based topology with analysis and comparison. Section IV details the implementation of a boost converter using the proposed ASP-based method. Section V shows the experimental results with discussions. Finally, we draw the conclusion in Section VI.

II. Boost VCR Generation by 2DSP-Based Topology

We define a particular rational-boost VCR by an integer part together with a fractional part as follows:

$$\mathrm{VCR} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = K + \frac{m}{n} \tag{1}$$

where $K, m, n \in N^+$ with $m \leq n$ and m, n are relatively prime. The VCR expression in (1) can also be written as n: $(Kn + m)$. As discussed in [25], for a generic SC dc–dc topology under the area-constrained condition, R_{SSL} with optimized capacitance assignment and the corresponding C_i determination are expressed as follows:

$$R_{\mathrm{SSL}} = \frac{1}{C_{\mathrm{TOT}} f_S} \left(\sum_{i=1}^{N} |a_{c,i}| \right)^2 \tag{2a}$$

$$C_i = \frac{|a_{c,i}| C_{\mathrm{TOT}}}{\sum_{k \in C_{\mathrm{fly}}} |a_{c,k}|} \tag{2b}$$

where $a_i = Q_{\mathrm{Ci}}/Q_{\mathrm{OUT}}$ is the charge multiplier of the ith capacitor C_i, which is defined as the capacitor charge flow Q_{Ci} normalized to the output charge Q_{OUT}, N is the total number of power cells, f_S is the power-stage switching frequency, and C_{TOT} is the total flying capacitance. Summarizing from the existing cases, the optimal R_{SSL} for generating the boost VCR expressed in (1) is

$$R_{\mathrm{SSL,opt}} = \frac{1}{C_{\mathrm{TOT}} f_S} \left(\frac{Kn + m - 1}{n} \right)^2 \tag{3}$$

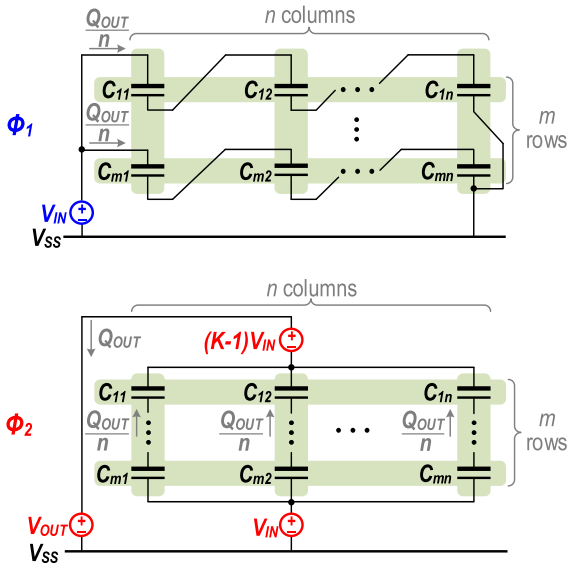

Fig. 1. Generalized two-phase operation model for the 2DSP-based topology for generating a VCR of n: $(Kn + m)$. The symbolic voltage $(K - 1)$ V_{IN} can be realized by an integer topology.

which is applicable to all the traditional SC boost topologies and the recently proposed ones, e.g., [10]–[12]. Note that (3) involves the loss from both the integer and fractional parts. For the rest of this article, we assume that the generation of the integer part (K) adopts the Dickson topology for optimal losses. The fractional ratio (m/n) generation using the 2DSP topology is detailed as follows.

A. Conventional 2DSP-Based Topology

Fig. 1 shows the two-phase operation for implementing the VCR in (1) using the 2DSP-based topology, where the symbolic voltage $(K - 1)V_{\mathrm{IN}}$ is generated by the integer part. The $m \times n$ capacitor array serves to produce the fractional part (m/n), and the flexible selection of m and n ensures high fractional VCR possibilities. Assuming the integer part exhibits optimal R_{SSL}, the corresponding R_{SSL} expression for a general 2DSP-based topology under balanced C_{fly} charge flow, i.e., $|a_{c,\,i}| = 1/n$, is

$$R_{\mathrm{SSL,2DSP}} = \frac{\left(\sum_{i=1}^{N_{C\_2DSP}} |a_{c,i}| + \sum_{k=1}^{N_{C\_int}} |a_{c,k}| \right)^2}{C_{\mathrm{TOT}} f_S} = \frac{(m + K - 1)^2}{C_{\mathrm{TOT}} f_S} \tag{4}$$

where $N_{C\_2\mathrm{DSP}}$ and N_{C_int} are the total number of "unit" power cells in the 2DSP and the integer parts, respectively. The detailed derivation of (4) is provided in the Appendix. We can qualitatively compare the $R_{\mathrm{SSL,2DSP}}$ in (4) with the $R_{\mathrm{SSL,opt}}$ in (3) through the following equation:

$$\sum_{i=1}^{N} |a_{c,i}|_{(\mathrm{2DSP})} - \sum_{i=1}^{N} |a_{c,i}|_{(\mathrm{opt})} = m + K - 1 - \frac{Kn + m - 1}{n} = \frac{1}{n}(mn - n - m + 1). \tag{5}$$

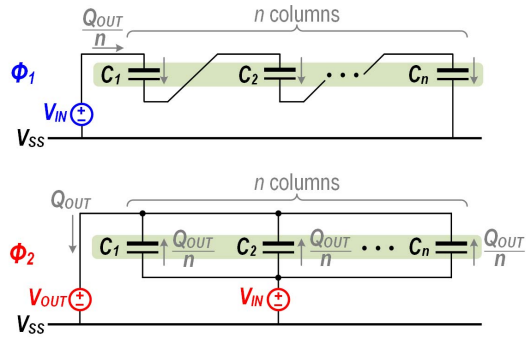

Fig. 2. Special case of 2DSP with $K = 1$ and $m = 1$.

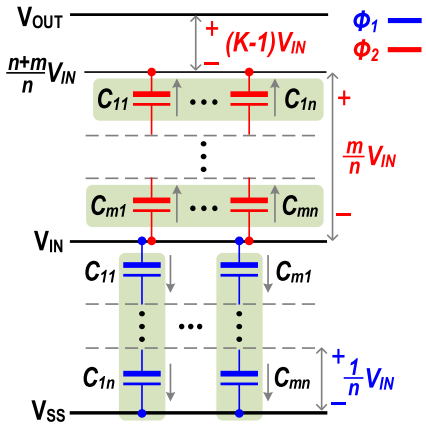

Fig. 3. Internal-level generation for a 2DSP-based topology with VCR $= n$: $(Kn + m)$.

Since m/n is defined as a proper fraction with $n \neq 1$, the only possible solution to equate $R_{SSL,2DSP}$ with $R_{SSL,opt}$, i.e., make (5) equal to 0, is $m = 1$. That means the 2DSP-based topology mostly achieves suboptimal R_{SSL}, except when using a $1 \times n$ array (as shown in Fig. 2, which is a special case of 2DSP) to implement a VCR of $(K + 1/n)$. Depending on n, such a special case can only realize a limited set of fractional ratios between (0, 1/2), which can significantly limit its application for flexible rational VCR generation. Similarly, since $|a_{c,i}| = 1/n$, we can equivalently consider that there are $(mn - m - n + 1)$ excessive number of SC cells employed in a 2DSP-based topology when compared with the optimal case. Accordingly, those cells generate excessive charge-sharing losses, resulting in suboptimal R_{SSL}.

B. Algebraic VCR Elaboration of 2DSP-Based Topology

To resolve the sub-optimal R_{SSL} issue in a 2DSP while maintaining the VCR flexibility, we first investigate its fundamental two-phase operations, as shown in Fig. 3. In Fig. 3, the integer part generation is represented by the voltage $(K - 1)V_{IN}$ for simplicity. The realization of the VCR in (1) by the 2DSP-based topology can be algebraically elaborated as

$$\text{(2DSP-based)} \quad V_{OUT} = V_{IN} + \left(m \times \frac{V_{IN}}{n}\right) + (K-1)V_{IN} \tag{6}$$

where the second and third terms are generated by the 2DSP cell matrix and the integer stage, respectively. The output voltage V_{OUT} is eventually achieved by stacking both parts over V_{IN}.

As shown in Fig. 3, the $m \times n$ cell matrix is charged by V_{IN} for voltage division in Φ_1, and the voltage on each capacitor is $V_{Ci} = (1/n)V_{IN}$. The capacitor array is reconfigured into an $n \times m$ matrix to generate the fractional part m/n in Φ_2, and is stacked over V_{IN} to generate a rational-boost VCR of n: $(n + m)$. One limitation of the 2DSP is that the fractional part reconfigurability is highly dependent on m and n, resulting in an excessive number of capacitors, which will lead to a suboptimal R_{SSL}.

Apart from that, the limited capacitor voltage of $(1/n)V_{IN}$ also results in higher bottom-plate switching voltage $|\Delta V_{CB}|$, which contributes to a significant parasitic loss. The above intuition comes from inspecting the integer Dickson and SP topologies. Specifically, both topologies can generate the same integer-boost VCR with the same number of "unit" power cells. However, $|\Delta V_{CB}|$ in the SP one linearly increases stage by stage, while the sustained voltage on each cell is fixed at V_{IN}. This phenomenon is directly opposite to the Dickson one. Hence, we can intuitively consider that, for a particular integer VCR, the limited capacitor voltage, e.g., in the SP topology, can result in higher bottom-plate switching voltages. The same mechanism is also applicable to the fractional VCR generation by the Dickson and SP topologies, and can be used to explain the intrinsic parasitic-loss phenomenon in the 2DSP.

To resolve the suboptimal R_{SSL} and increased parasitic-loss limitations in the conventional 2DSP, we propose the algebraic SP (ASP) topology, which can theoretically achieve optimal R_{SSL} and improved parasitic loss as follows.

III. Proposed ASP-Based Topology

A. ASP Concept

Fig. 4 shows the two-phase ASP-based implementation for realizing the VCR in (1), featuring identical charge flow through each cell. The corresponding algebraic V_{OUT} expression is given by

$$\begin{aligned}\text{(ASP-based)} \quad V_{OUT} = {} & K V_{IN} + (n - m - 1)(K - 1)V_{IN} \\ & + mK V_{IN} + (n-1)(V_{IN} - V_{OUT}). \end{aligned} \tag{7}$$

As observed in (7), it is constructed by the summation of different terms, including $(n-m-1)$ times of $(K-1)V_{IN}$, m times of KV_{IN}, and $(n-1)$ times of $(V_{IN} - V_{OUT})$. The introduced $(V_{IN} - V_{OUT})$ term enables flexible m/n generation without V_{IN} dividing operation as in 2DSP. The corresponding two-phase operation is shown in Fig. 4. As observed, we charge C_{xi}, C_{yi}, and C_{zi} to $(K-1)V_{IN}$, KV_{IN}, and $(V_{IN} - V_{OUT})$ in parallel during Φ_1, which correspond to the second, third, and fourth terms in (7), respectively. During Φ_2, all the $(2n-2)$ cells are connected in series between KV_{IN} and V_{OUT}, featuring the SP operating principle. The increased capacitor voltage helps lower the $|\Delta V_{CB}|$ and hence the parasitic loss. Note that both the required numbers of ASP cells (C_x, C_y, and C_z) and their specific connections in Φ_2 are highly dependent on the

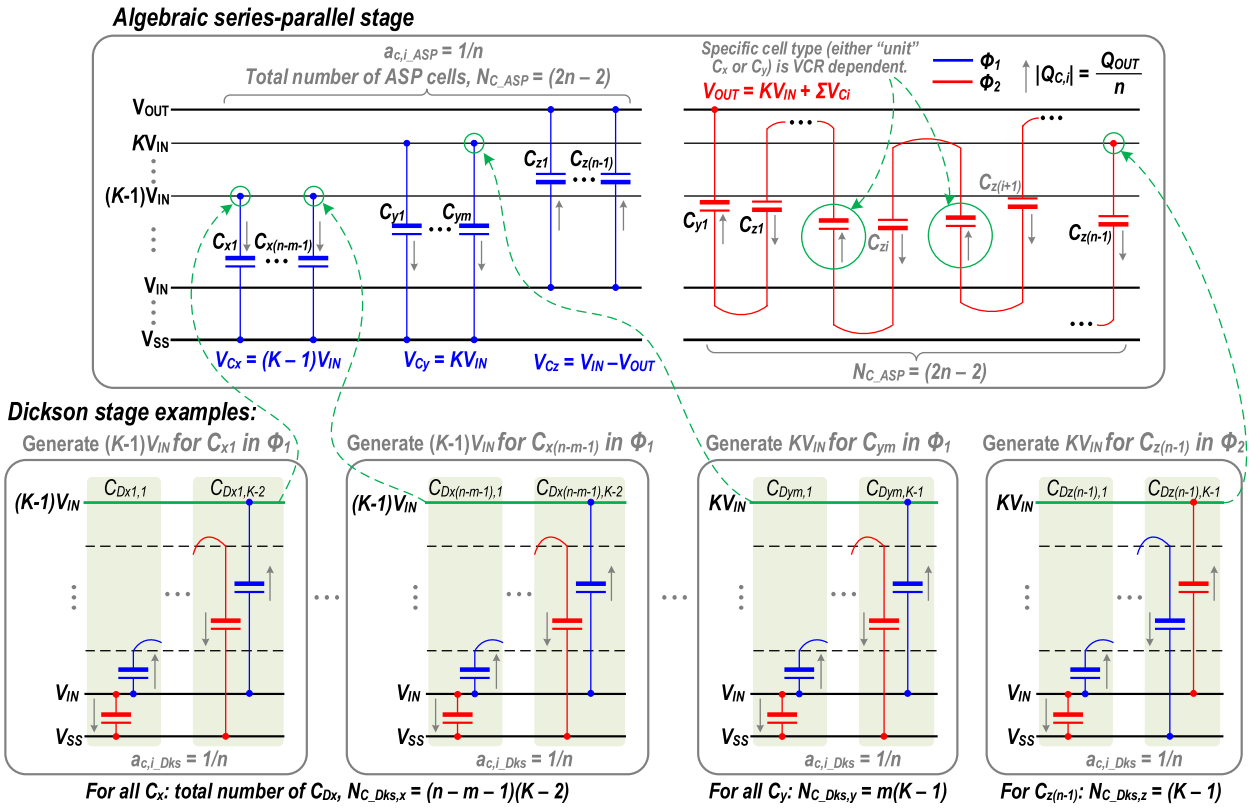

Fig. 4. Power-cell operation states for the proposed ASP-based topology generation method with the integer-level generation by the Dickson topology. Blue (red): capacitor operating status in Φ_1 (Φ_2).

targeted VCR. The parameterized topology generation details will be introduced in Sections III-B and III-C.

The required integer voltage multiplications of $KV_{\rm IN}$ and $(K-1)V_{\rm IN}$ can be generated by using the Dickson topology for optimal intrinsic losses. The Dickson stages as shown in Fig. 4 operate in parallel to one another. Note that the conventional SP topology can achieve a comparable $R_{\rm SSL}$ and a higher $M_{\rm SSL}$ defined as $V_{\rm OUT}^2/(R_{\rm SSL} f_S E_{\rm TOT})$, where $E_{\rm TOT}$ denotes the total stored energy in the flying capacitors according to [25]. Consequently, SP is preferred in applications where the flying capacitors are frequently discharged or exhibit a limited voltage rating. However, it comes with the tradeoff of a much higher parasitic loss than that of the Dickson topology. In this article, with the on-chip capacitors capable of sustaining the designed voltage levels, we mainly consider the steady-state operation and use $R_{\rm SSL}$ as the performance metric for fair comparisons.

To achieve optimal $R_{\rm SSL}$, all the capacitors in the Dickson topology should be of the same size. We consider each capacitor in the Dickson stage transferring the same "unit" charge amount, i.e., $|(1/n)Q_{\rm OUT}|$, as shown by the arrow sign in Fig. 4 (top right). The ASP stage includes a total of $(n-m-1)$ cells for C_x, indicating that a total charge amount of $[(n-m-1)/n]Q_{\rm OUT}$ should be delivered from $(K-1)V_{\rm IN}$ during Φ_1. This corresponds to a total of $N_{C\_{\rm Dks},x} = (n-m-1)(K-2)$ "unit" capacitors in the corresponding Dickson stage. Similarly, $N_{C\_{\rm Dks},y} = m(K-1)$ is necessary to carry the charge flow for C_y from $KV_{\rm IN}$. During Φ_2, it requires $N_{C\_{\rm Dks},z} = (K-1)$ for the Dickson stage to realize $KV_{\rm IN}$. In summary, the generation of both $KV_{\rm IN}$ and $(K-1)V_{\rm IN}$

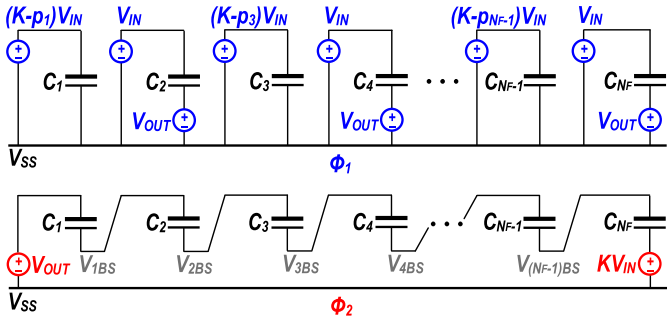

Fig. 5. Two-phase operation of the proposed ASP-based topology framework.

using the Dickson stage in both operating phases requires a total number of $N_{C\_\rm Dks} = (Kn-2n+m+1)$ "unit" power cells. As the Dickson topology also exhibits uniform charge flow with modular power cells, together with the ASP part ($N_{C\_\rm ASP} = 2n-2$), the total number of "unit" cells to implement a VCR of n: $(Kn+m)$ with the ASP-based framework is $(Kn+m-1)$. Since each "unit" cell delivers a uniform charge amount of $(1/n)Q_{\rm OUT}$, the proposed ASP-based topology can theoretically achieve the optimal $R_{\rm SSL}$ according to (3).

B. ASP Topology Framework

Based on the concept illustrated in Fig. 4, Fig. 5 shows a generic two-phase model for the proposed ASP-based topology framework, which requires a total number of $N_F = 2n-2$, where $N_F = N_{C\_ASP}$, cells for generating the fractional part, i.e., m/n, of VCR $= n{:}(Kn+m)$. From (7), there

are $(n-1)$ cells connected to $(V_{\rm IN}-V_{\rm OUT})$, and the other $(n-m-1)$ and m cells are charged to $(K-1)V_{\rm IN}$ and $KV_{\rm IN}$, respectively. As shown in Fig. 5, the odd cells are with $(K-p)V_{\rm IN}$ and the even cells are with $(V_{\rm IN}-V_{\rm OUT})$. This arrangement is crucial to ensure pair-wise subtraction mode operation [24], [26] for reduced $|\Delta V_{\rm CB}|$ (and hence the parasitic loss). To determine whether a particular odd cell should be connected to $(K-1)V_{\rm IN}$ or $KV_{\rm IN}$, we introduce the configuration factor p, which can be programmed to either 0 or 1 to generate $(K-p_i)V_{\rm IN}$, with i denoting the cell index. Note that the defined p is not applicable for even cells. According to (7), the summation of all p_i should be equal to $(n-m-1)$. For the framework shown in Fig. 5, the steady-state voltage balancing equation is

$$\begin{aligned}&(K-p_1)V_{\rm IN}+(V_{\rm IN}-V_{\rm OUT})+(K-p_3)V_{\rm IN}+(V_{\rm IN}-V_{\rm OUT})\\&\quad+\ldots+(K-p_{N_F-1})V_{\rm IN}+(V_{\rm IN}-V_{\rm OUT})\\&\quad=V_{\rm OUT}-KV_{\rm IN}.\end{aligned}\tag{8}$$

By reorganizing (8), we can derive the VCR expression as follows:

$$\mathrm{VCR_{ASP}}=K+\frac{N_F-2\sum_{k=1}^{N_F/2}p_{2k-1}}{N_F+2}.\tag{9}$$

By substituting $\Sigma p_i=n-m-1$ and $N_F=2n-2$ into (9), we can have the same VCR expression as (1). From (9), we can observe that the selection of p is not unique, i.e., there exists more than one set of p that can achieve the same VCR with optimal $R_{\rm SSL}$. Yet, it may introduce suboptimal parasitic loss, which can be significant for on-chip implementation. Section III-C details a systematic p selection strategy to ensure parasitic-loss reduction.

C. Determination of Configuration Factor p_i

From Fig. 5, the determination of the configuration factor p_i is only necessary when i is odd. However, the bottom-plate switching voltage $|\Delta V_{\rm CBi}|$ is well defined for i being both odd and even. Consequently, we have to consider every cell to evaluate the stage-by-stage parasitic loss. As all the even stages are fixed to $(V_{\rm OUT}-V_{\rm IN})$, a particular choice for p_i when i is odd can influence $|\Delta V_{\rm CB}|$ for both the ith and $(i+1)$th stages. From Fig. 5, we first obtain the general expression for the bottom-plate voltage $V_{\rm iBS}$ in Φ_2 for a particular stage i, which is dependent on both the current and prior stages and can be written as follows:

$$V_{\rm iBS}=\begin{cases}\left(\dfrac{i+1}{2}\right)V_{\rm OUT}-\left[\dfrac{i+1}{2}(1+K)-1-\displaystyle\sum_{k=1}^{\frac{(i+1)}{2}}p_{2k-1}\right]V_{\rm IN}\\(i\text{ is odd})\\\left(\dfrac{i}{2}+1\right)V_{\rm OUT}-\left[\dfrac{i}{2}(1+K)-\displaystyle\sum_{k=1}^{\frac{i}{2}}p_{2k-1}\right]V_{\rm IN}\\(i\text{ is even}).\end{cases}\tag{10}$$

Accordingly, we can get the general expression of $|\Delta V_{\rm CBi}|$ as follows:

$$|\Delta V_{\rm CBi}|=\begin{cases}|\left(\dfrac{i+1}{2}\right)\left(\dfrac{m}{n}-1\right)+1+\displaystyle\sum_{k=1}^{\frac{(i+1)}{2}}p_{2k-1}|V_{\rm IN},\\(i\text{ is odd})\\|\dfrac{i}{2}\left(\dfrac{m}{n}-1\right)+\displaystyle\sum_{k=1}^{\frac{i}{2}}p_{2k-1}|V_{\rm IN},\\(i\text{ is even})\end{cases}\tag{11}$$

which can be further expressed iteratively as follows:

$$|\Delta V_{\rm CBi}|=\begin{cases}|\Delta V_{CB(i-1)}+\left(\dfrac{m}{n}+p_i\right)V_{\rm IN}|, & (i\text{ is odd})\\|\Delta V_{CB(i-1)}-V_{\rm IN}|, & (i\text{ is even}).\end{cases}\tag{12}$$

From (12), $|\Delta V_{\rm CBi}|$ depends on the ith cell configuration and $|\Delta V_{\rm CB(i-1)}|$. Consequently, we can systematically select p_i to minimize $|\Delta V_{\rm CBi}|$. Note that $\Delta V_{\rm CB0}=0$ is a predefined condition. Based on (12), we can observe that, when $i=1$, $|\Delta V_{\rm CB1}|$ is smaller by selecting $p_1=0$, resulting in $|\Delta V_{\rm CB1}|=(m/n)V_{\rm IN}$. This choice also enables $|\Delta V_{\rm CB2}|$ to be bounded by $V_{\rm IN}$. Similarly, $|\Delta V_{\rm CB3}|=[2(m/n)+p_3-1]V_{\rm IN}$, which can also be bounded by $V_{\rm IN}$ through properly selecting p_3 according to the required m/n. We can then systematically deduce p_i for each stage by iteratively performing the steps involved. This configuration ensures per-stage $|\Delta V_{\rm CB}|$ optimization, and we should always select p_i such that

$$|\Delta V_{\rm CBi}|<V_{\rm IN}\tag{13}$$

This also forms the basis for p_i selection to achieve parasitic-loss reduction in this article. By enforcing the constrained condition in (13) into the expressions in (11), we have

$$-2<\left(\frac{i+1}{2}\right)\left(\frac{m}{n}-1\right)+\sum_{k=1}^{(i+1)/2}p_{2k-1}<0,\quad(i\text{ is odd})\tag{14}$$

$$-1<\frac{i}{2}\left(\frac{m}{n}-1\right)+\sum_{k=1}^{\frac{i}{2}}p_{2k-1}<1,\quad(i\text{ is even}).\tag{15}$$

We can further rewrite (14) and (15) to define the possible range for p_i as follows:

$$\begin{aligned}&\left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{\frac{i}{2}}p_{2k-1}-2\\&\quad<p_i<\left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{i/2}p_{2k-1},\ (i\text{ is odd})\end{aligned}\tag{16}$$

$$\begin{aligned}&\frac{i}{2}\left(1-\frac{m}{n}\right)-\sum_{k=1}^{\frac{(i-1)}{2}}p_{2k-1}-1\\&\quad<p_{i-1}<\frac{i}{2}\left(1-\frac{m}{n}\right)-\sum_{k=1}^{\frac{(i-1)}{2}}p_{2k-1}+1,\ (i\text{ is even})\end{aligned}\tag{17}$$

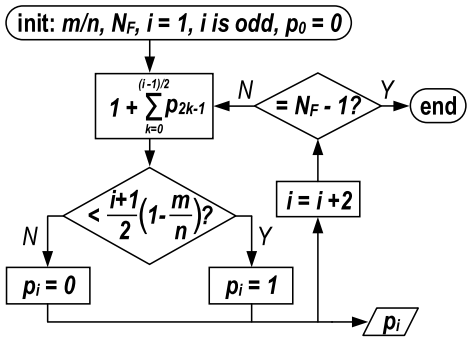

Fig. 6. Flowchart of the factor p_i determination process for the ASP topology for fractional m/n generation.

Here, as p_i selection is only necessary when i is odd, we replace the index i by $(i+1)$ in (17) to obtain

$$\left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{\frac{i}{2}} p_{2k-1}-1 < p_i < \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{\frac{i}{2}} p_{2k-1}+1,\ (i \text{ is odd}). \quad (18)$$

Note that, for a particular p_i, it should satisfy both (16) and (18) simultaneously. To ensure that $|\Delta V_{\mathrm{CBi}}|$ in each cell is well bounded, we can combine both inequalities to achieve the unified upper/lower bounds for p_i, defined as follows:

$$\left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{(i-1)/2} p_{2k-1}-1 < p_i < \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=1}^{(i-1)/2} p_{2k-1},\ (i \text{ is odd}). \quad (19)$$

We can then use (19) to systematically determine p_i to obtain a unique power-cell arrangement with parasitic-loss reduction. As an example, when $i = 1$, we have $p_1 = 0$. This is consistent with our previous observation. Note in (19) that the difference between the upper and lower boundaries is always 1. In general, we should have $p_i = 1$ if the lower bound is > 0, which is equivalent to selecting $p_i = 1$ if the upper bound is > 1) and vice versa. Thus, we can further summarize the p_i selection criteria as follows:

$$p_i = \begin{cases} 1, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=0}^{(i-1)/2} p_{2k-1} > 1 \\ 0, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right)-\sum_{k=0}^{(i-1)/2} p_{2k-1} < 1 \end{cases} (i \text{ is odd}). \quad (20)$$

From (20), it can be observed that the result of p_i is dependent on m/n and the configuration of all the previous stages. Fig. 6 shows the corresponding flowchart for p_i determination.

Fig. 7 shows the graphical summary of p_i selection for different cells under different m/n, enabling direct p_i searching. With a given fractional ratio m/n, the required number

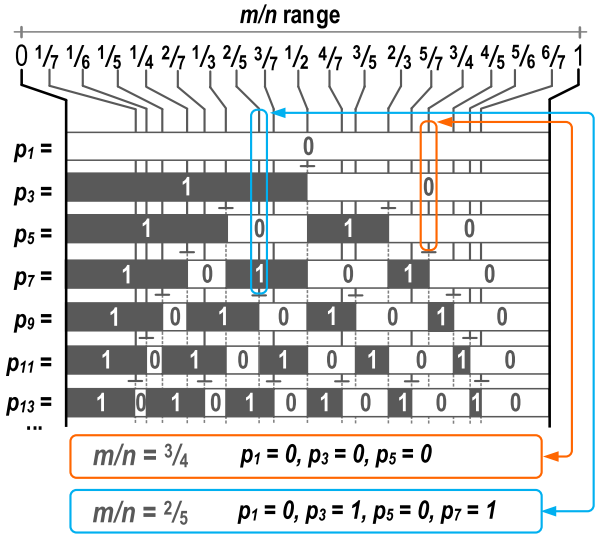

Fig. 7. Graphic summary for fast searching of p_i with specific m/n.

of cells $N_F = 2n-2$ for the ASP topology also indicates the required number of p_i. By locating the vertical lines with a given m/n in Fig. 7, the corresponding set of p_i can be obtained, as demonstrated by the examples of 3/4 and 2/5. It can be observed that the summation of p_i under a particular m/n is always equal to $(n-m-1)$, which matches to the V_{OUT} elaboration in (7). The contents shown in Fig. 7 can be further extended according to the VCR resolution requirement. Note that the ASP power-cell ordering, as shown in Fig. 5, can ensure that $|\Delta V_{\mathrm{CB}}|$ can be well bounded below V_{IN} for a reduced parasitic loss through the proposed p_i selection for a specific m/n.

D. Loss Analysis and Comparison

As discussed in Section III-A, the proposed ASP-based topology can achieve the optimal charge sharing loss. Here, we analyze the parasitic loss. In theory, the definition of parasitic-loss power is

$$P_{\mathrm{ls,BP}} = \sum_{i=1}^{N} \beta C_i |\Delta V_{\mathrm{CBi}}|^2 f_S \quad (21)$$

where C_i is defined in (2b) and β is the ratio between the parasitic capacitance and C_{fly}. The quadratic relationship between $P_{\mathrm{ls,BP}}$ and $|\Delta V_{\mathrm{CBi}}|$ in (21) indicates that the restriction of $|\Delta V_{\mathrm{CBi}}|$ is essential for effective parasitic-loss reduction. For easy comparison, based on (21), we define two other forms of $P_{\mathrm{ls,BP}}$ by introducing the normalized $|\Delta V_{\mathrm{CBi}}|$ with V_{IN} (λ_{CBi}) and V_{OUT} (κ_{CBi}) as follows:

$$P_{\mathrm{ls,BP}} = \beta C_{\mathrm{TOT}} f_S V_{\mathrm{IN}}^2 \sum_{i\in C_{\mathrm{fly}}} \left(\frac{a_i \lambda_{\mathrm{CBi}}^2}{a_{\mathrm{TOT}}}\right) \quad (22a)$$

$$= \beta C_{\mathrm{TOT}} f_S V_{\mathrm{OUT}}^2 \sum_{i\in C_{\mathrm{fly}}} \left(\frac{a_i \kappa_{\mathrm{CBi}}^2}{a_{\mathrm{TOT}}}\right) \quad (22b)$$

$$\lambda_{\mathrm{CBi}} = \frac{|\Delta V_{\mathrm{CBi}}|}{V_{\mathrm{IN}}} \text{ and } \kappa_{\mathrm{CBi}} = \frac{|\Delta V_{\mathrm{CBi}}|}{V_{\mathrm{OUT}}}. \quad (23)$$

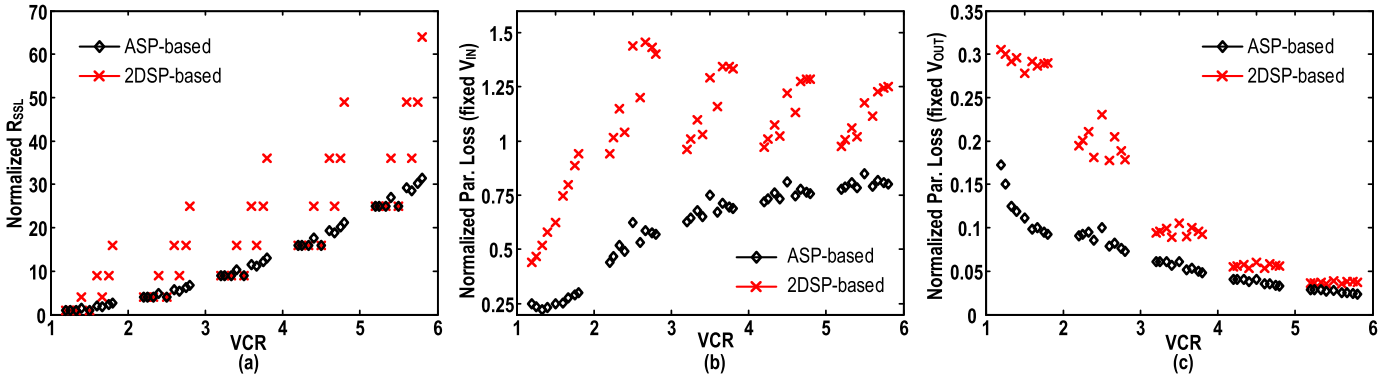

Fig. 8. Theoretical comparison between the proposed ASP-based and conventional 2DSP-based topologies with fractional VCR from 1:1 to 1:6 on (a) R_{SSL} (normalized to $C_{TOT}f_S$), (b) parasitic loss (normalized to $\beta C_{TOT}f_S V_{IN}$) under fixed V_{IN}, and (c) parasitic loss (normalized to the same $\beta C_{TOT}f_S V_{OUT}$) under fixed V_{OUT}.

As both (22a) and (22b) are topology dependent, they can facilitate the loss comparison between different topologies under the same specification of V_{IN} or V_{OUT}.

For fair comparisons, we select the Dickson stage to implement the integer voltages for both the proposed ASP-based and conventional 2DSP-based topologies in generating the rational-boost VCR of (1). Under the same total-capacitance constraint, Fig. 8(a) shows the R_{SSL} comparison between the proposed ASP-based and 2DSP-based topologies with the same set of rational VCRs between $\times 1$ and $\times 6$, where $m/n = \{1/5,\ 1/4,\ 1/3,\ 2/5,\ 1/2,\ 3/5,\ 2/3,\ 3/4,\ 4/5\}$. Note that the loss contributions from the Dickson stages have been included for fair comparisons. For the integer-gain generation, although only one integer level is required in the 2DSP-based topology, the corresponding required number of "unit" power cells is typically more than that of the ASP-based one. Hence, it results in a higher R_{SSL} with the same capacitor area. The difference in the number of "unit" capacitors can be calculated by

$$N_{C\_Dks,2DSP} - N_{C\_Dks,ASP} = (K-1)n - (Kn - 2n + m + 1) = n - (m+1). \quad (24)$$

Note that (24) is equal to or greater than 0, since m/n is a proper fraction. The R_{SSL} expression used to estimate the corresponding loss in the 2DSP-based topology for the comparison shown in Fig. 8(a) is derived in the Appendix, which also provides the corresponding derivations for the 2DSP-based parasitic loss. From Fig. 8(a), the ASP-based topology achieves an evident R_{SSL} reduction in contrast to the 2DSP-based one, except for the cases under $m = 1$, i.e., a special case of 2DSP that is essentially the conventional SP converter. With $m = 1$, both implementations give the same R_{SSL}.

Fig. 8(b) and (c) shows the parasitic-loss comparison between the topologies generated by the ASP-based and 2DSP-based methods. The integer and fractional parts in both the topologies contribute to the power loss. Evaluated by (22a) and (22b), it can be observed that the proposed ASP-based technique can effectively reduce the parasitic loss for all the generated VCRs when compared with the 2DSP-based ones. In Fig. 8(c), the loss difference between the two topologies becomes smaller as the VCR increases, which is mainly due to the quadratically scaled parasitic loss at higher VCRs, i.e., V_{IN} decreases.

E. Voltage Rating Versus Input Range

In terms of the capacitor's voltage rating, according to Fig. 4, the highest capacitor-sustained voltage in the ASP-based topology is KV_{IN} when generating a VCR $= K + m/n$. Consequently, the C_{fly} voltage rating can result in the constraint $KV_{IN,max,ASP} \le V_{rate,Cap}$, where $V_{IN,max,ASP}$ is the maximum tolerated input voltage level by the ASP-based converter and $V_{rate,Cap}$ is the capacitor-rated voltage. Accordingly, the practical maximum input voltage range of an ASP-based topology is dependent on the integer gain K together with the capacitor's characteristics.

Considering the overstress on the power switches, we should consider the maximum blocked voltage $V_{SW,blk}$ across a switch under two conditions: 1) VCR > 2 and 2) VCR ≤ 2. When VCR > 2, the maximum $V_{SW,blk}$ in an ASP-based topology is $(V_{OUT} - V_{IN})$. Consequently, $(V_{OUT} - V_{IN}) \le V_{rate,SW}$, where $V_{rate,SW}$ is the rated voltage of the power switch. By introducing the VCR expression in the above inequality, we have $(K - 1 + m/n)V_{IN} \le V_{rate,SW}$. Considering VCR ≤ 2, the maximum $V_{SW,blk}$ equals V_{IN}. Accordingly, we have $V_{IN} \le V_{rate,SW}$. In summary, the sustained input voltage range of the proposed ASP-based topology is dependent on the VCR and the rated voltage of the switch.

F. Design Examples

To apply the proposed ASP-based topology framework, we first need to determine the parameter N_F according to a given m/n. We can then obtain the required set p_i according to the selection process in Fig. 6, or through the graphical direct searching method in Fig. 7. The final step is to substitute the set p_i back into the framework to generate concrete topology implementation.

Fig. 9 shows the configurations for the proposed ASP-based topology for different fractional m/n ratios. Each cell group denotes the topology configuration for different VCRs, with V_{iBS} connected to KV_{IN} in Φ_2 when $i = N_F$. Fig. 10 shows the

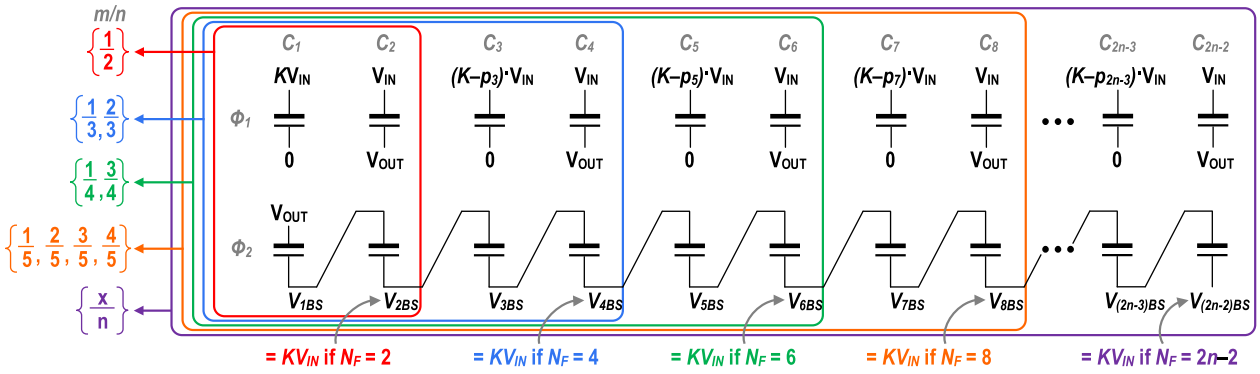

Fig. 9. Configuration examples of the proposed ASP topology for different m/n possibilities.

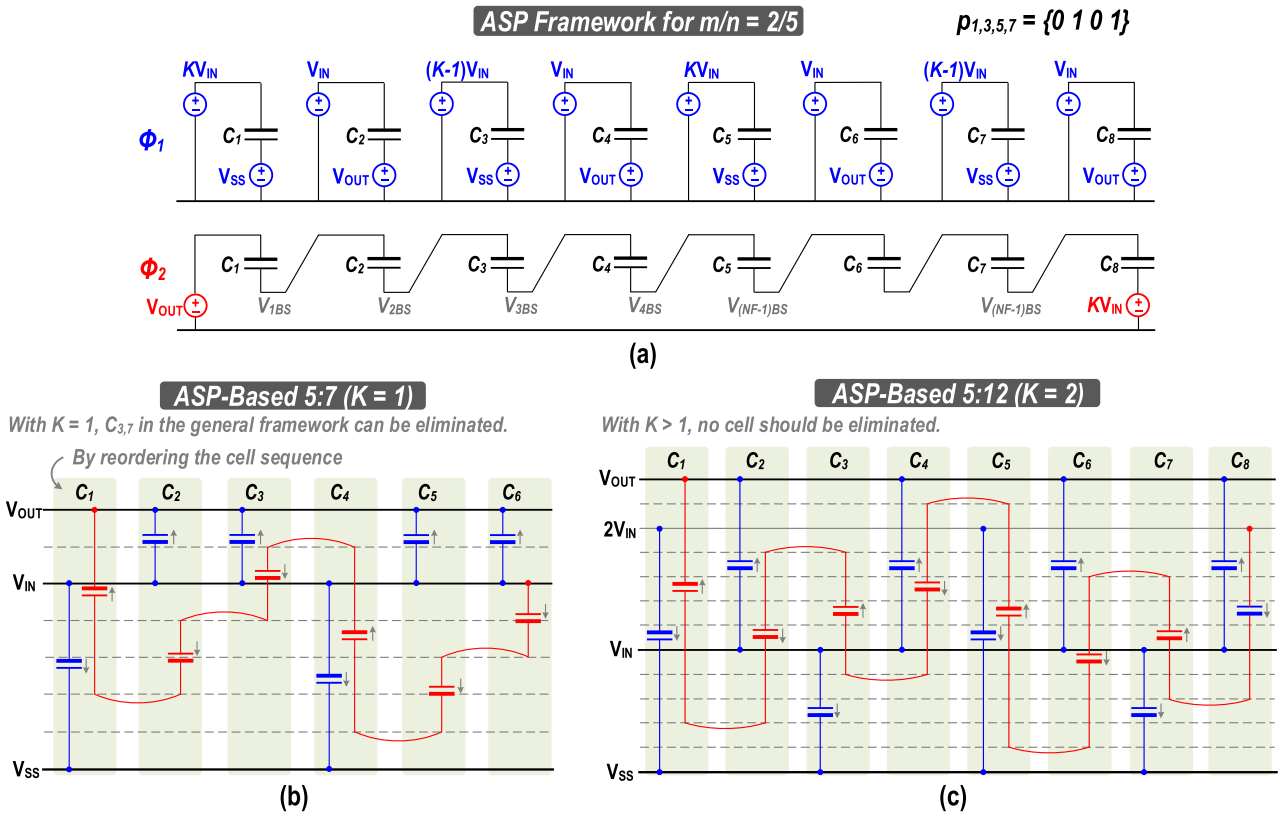

Fig. 10. Examples of (a) ASP framework for the defined $m/n = 2/5$ and arbitrary $K \geq 1$, (b) specific ASP-based operation for VCR = 5:7 ($K = 1$), and (c) VCR = 5:12 ($K = 2$).

dual-phase examples for the rational-boost VCRs of 5:7 and 5:12 using the proposed ASP-based topology.

Moreover, when $K = 1$, some of the capacitor voltages of $(K - p_i)V_{\mathrm{IN}}$ may become 0. In that case, those cells will have no effect in the voltage pumping, and can be removed from the topology generation, e.g., the case for 5:7 shown in Fig. 10. As shown in Fig. 10, although the 5:7 and 5:12 cases have the same fractional part of 2/5, different number of cells are employed in the two cases.

IV. Converter Design

A. System Overview

We implemented the proposed ASP-based topology in a fully integrated SC boost converter with seven rational VCRs to support a wide input-voltage range. Each C_{fly} can be reconfigured to generate either the integer or fractional part to achieve full capacitance utilization for reduced R_{SSL}. Fig. 11 shows the overview of the implemented converter. The SC power stage operates in dual-branch interleaving with 180° phase difference. Each branch consists of four power cells (C_{1-4}) with the top-plate and bottom-plate terminals selected among V_{IN}, V_{OUT}, and V_{SS} for implementing different VCR configurations. Four-phase non-overlapping (NOV) clock signals are generated by using an external master clock to reduce the reversion loss. We adopted an adaptive boot-strapping (ABS) technique based on [12] for robust power switch on/off operation over a wide voltage-dynamic range. We control all the seven VCRs by topology configuration logics through a 3-bit external binary code (D_{VIN}).

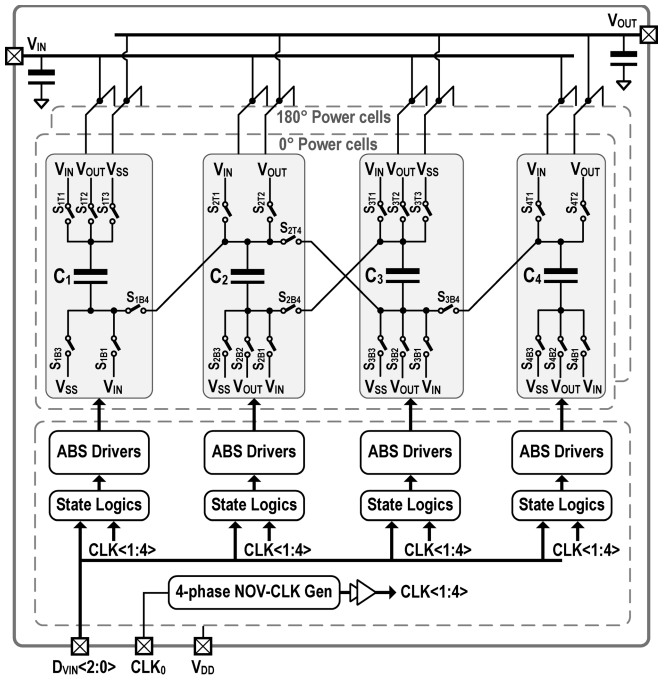

Fig. 11. System overview of the implemented SC boost converter.

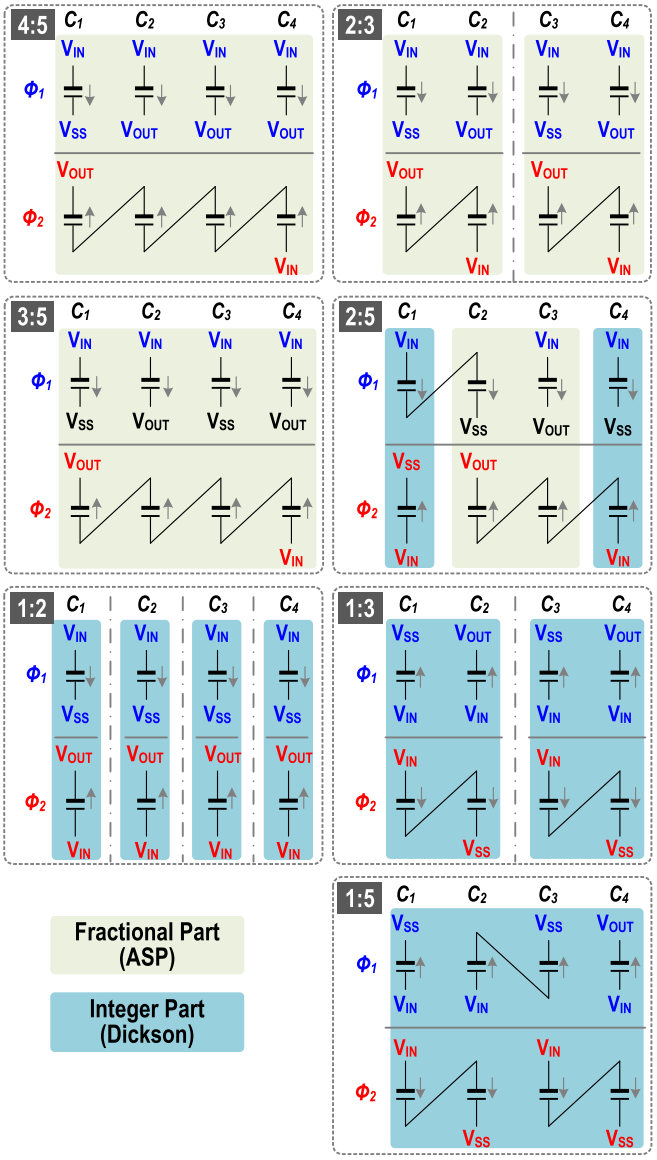

Fig. 12. Annotation and summary of the power-stage operating modes under all the seven targeted VCRs from ×1.25 to ×5.

B. VCR Reconfiguration

The SC boost converter covers a VCR range from ×1.25 to ×5, containing {4:5, 2:3, 3:5, 1:2, 2:5, 1:3, 1:5}. Due to the uniform cell charge-flow property, the corresponding total required numbers of cells are {4, 2, 4, 1, 4, 2, 4}, meaning that all the seven VCR cases can be fully partitioned by using C_{1-4}. Fig. 12 shows the power-cell operations and partitioning for all the implemented VCRs, with C_{1-4} configured to serve as either the Dickson or ASP power cell in different modes. We determine the generations of rational VCRs of 4:5, 2:3, 3:5, and 2:5 based on the proposed ASP topology. A typical voltage doubler implements the 1:2 ratio, and the conventional Dickson topology generates the VCRs of 1:3 and 1:5 for reduced parasitic loss. C_{1-4} are identical as they have the same charge flow under all the seven implemented VCRs, which cover all the VCR possibilities with four C_{fly}.

C. Power-Switch Implementation and Driving

We implement all the switches connected to V_{OUT} with PMOS transistors to facilitate the gate driver design, while using NMOS transistors for all the other switches for better conductance. With reference to [28], we employed the dynamic body biasing technique to the switches, as indicated in Fig. 13, to improve the switch on-/off-resistance ratio. To apply the body biasing technique, a deep N-well is necessary to isolate the substrate of the NMOS switch. Fig. 13(a) shows the power-cell implementation of C_1, together with its corresponding switch control logics. As S_{1T2}, S_{1T3}, and S_{1B3} are simply connected to either V_{OUT} or V_{SS}, they can be driven by simple clock buffers. For the switches connecting to V_{IN} or the adjacent power cell, i.e., S_{1T1}, S_{1B1}, and S_{1B4}, as their drain–source terminal potentials are highly dynamic according to V_{IN}, their gate driving signals are generated by using the ABS drivers to ensure proper switch on/off operations. As shown in Fig. 13(b), the ABS driver in off-phase dual-branch architecture (modified from [12] with simplified control) is capable of accommodating the reference terminal to the lower potential side. Functional blocks $RCT_{0/180}$ sense the lower potential side across a particular switch in order to adaptively select the reference terminal and generate the proper switch-off signal. CP_1 and CP_2 are for the driver internal control and the switch-on control, respectively. The VCR can be reconfigured by using the 3-bit digital code $D_{\text{VIN}<2:0>}$. Fig. 13(c) shows the implementation of the four-phase NOV clock generator using NOR gates and inverter-based delay lines, controlled by the external master clock CLK_0. In this article, we employed the dual-branch architecture as the power stage. In addition to the normal two-phase NOV clock signals A_2 and B_2, two additional NOV signals, i.e., A_1 and

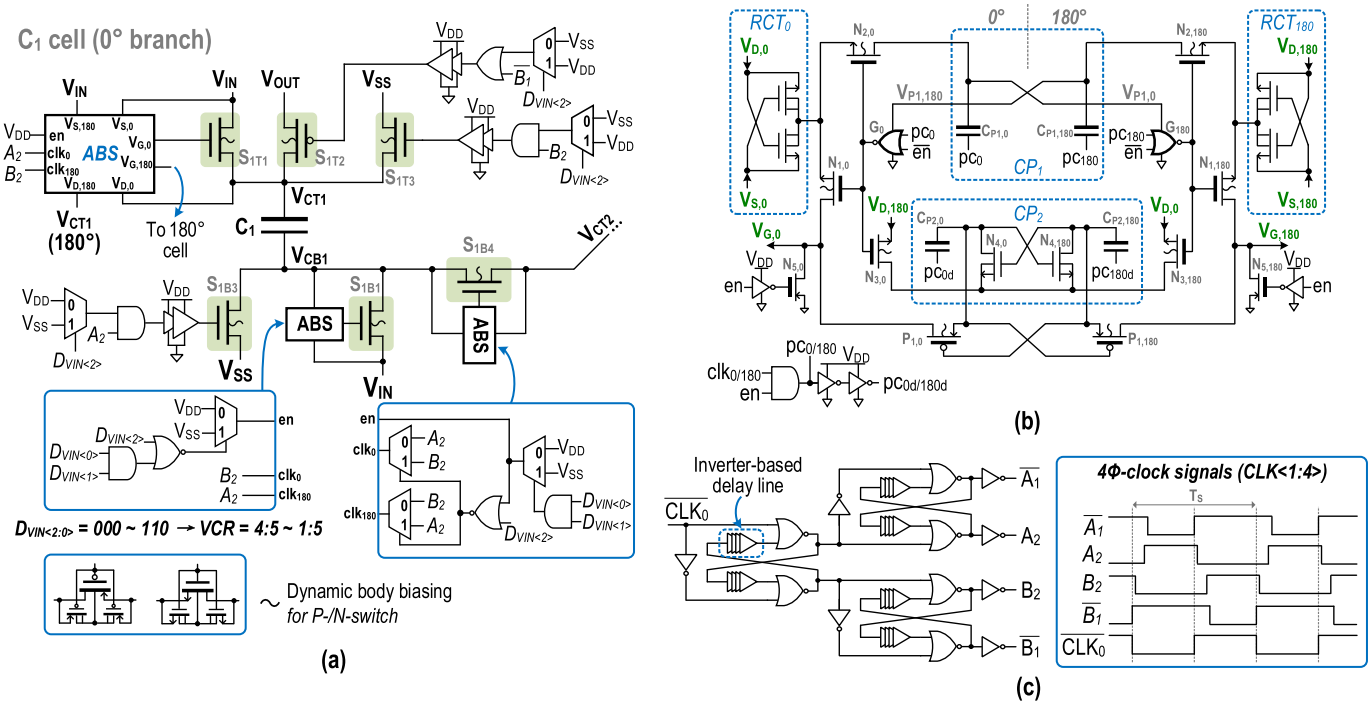

Fig. 13. Implementation details of (a) power cell C_1 with switch controls, (b) ABS driver circuitry, and (c) four-phase NOV clock generator. All the logic cells are powered by an externally supplied V_{DD}.

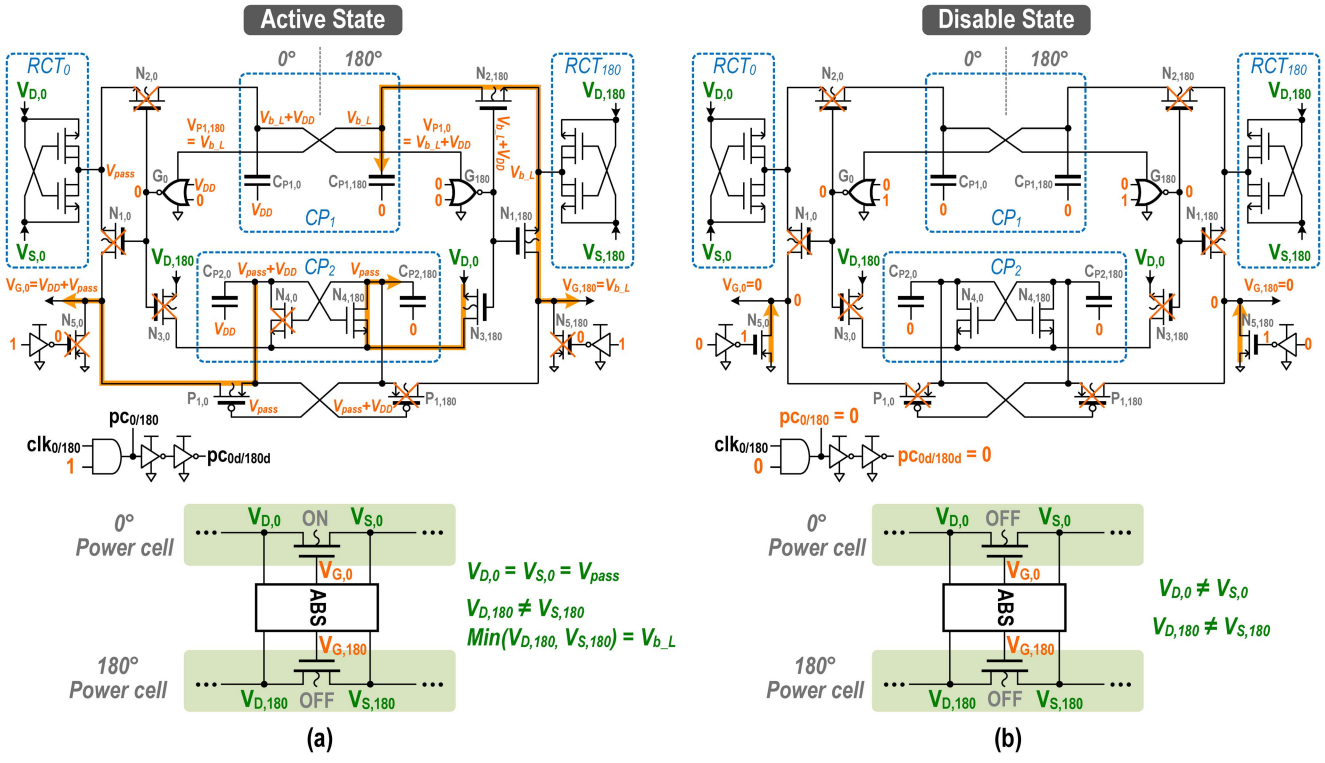

Fig. 14. Operation example of the ABS driver in (a) active state and (b) disable state.

B_1, are implemented to prevent the short-circuit and reversion losses according to [27]. Note that the clock phases $A_{1,2}$ and $B_{1,2}$ are for power switch control and should be distinguished from the power-stage operation phases $\Phi_{1,2}$. In addition, as VCR changes, the power-cell control phases are reassigned to adapt to different topology configurations.

The operation of the ABS circuit includes two states: 1) the active state and 2) the disable state. Fig. 14(a) shows the

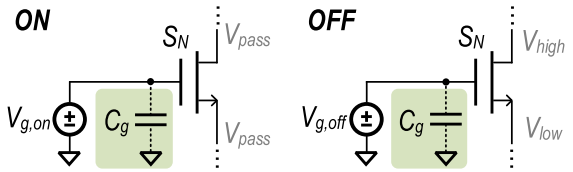

Fig. 15. Power-switch gate parasitic capacitance model.

ABS active state, with $en = 1$, $pc_0 = V_{\rm DD}$, and $pc_{180} = 0$. Consequently, the switches in the 0° power cell are turned on, and the ones in the 180° power cell are turned off. The CP_1 block generates the voltages $V_{\rm P1,0} = V_{b\_L} + V_{\rm DD}$ and $V_{\rm P1,180} = V_{b\_L}$ to supply to the NOR gates G_{180} and G_0, respectively. As observed, V_{b_L} is equal to the lower potential between $V_{D,180}$ and $V_{S,180}$ sensed by RCT_{180}. The switch $N_{2,180}$ is turned on by the output of G_{180}, which also turns on $N_{1,180}$ to pass the switch-off signal to $V_{G,180}$. In addition, the output of G_{180} also controls $N_{3,180}$, which connects $V_{D,0}$ to the CP_2 block (here $V_{D,0} = V_{\rm pass}$) to charge $C_{\rm P2,180}$. In the 0° power-cell side, the output of G_0 is 0, turning off $N_{1,0}$, $N_{2,0}$, and $N_{3,0}$. Consequently, RCT_0 is disconnected from the other parts of the driver circuit. The driving signal $V_{G,0}$ is generated from the CP_2 block by $C_{\rm P2,0}$. The cross-coupled switches $P_{1,0/180}$ connect $C_{\rm P2,0/180}$ and the driver outputs $V_{\rm G,0/180}$. The control signals are complementarily generated in the next clock cycle. The disable switches $N_{5,0/180}$ are always off throughout the active state.

In the disable state, as shown in Fig. 14(b), the switches in both the 0°/180° power cells are turned off. To achieve that, $N_{5,0/180}$ switches are turned on by setting $en = 0$. Accordingly, the outputs of $G_{0/180}$ are set as "low." Together with $pc_{0/180} = 0$, all the switches inside the ABS driver are disabled. In this state, there is no switching activity in the driver circuit.

D. Switching-Loss Discussion

Considering only the NMOS-based power-switch implementation for simplicity, the corresponding on/off behavior can be modeled as shown in Fig. 15, where C_g models the gate parasitic capacitance. We further define the switch-on/-off gate voltages as $V_{g,\rm on}$ and $V_{g,\rm off}$. From Fig. 15, the N-switch (S_N) passes the voltage $V_{\rm pass}$ in the turn-on state (assuming negligible turn-on resistance $R_{\rm on}$) and isolates the channel terminal voltages $V_{\rm high}$ and $V_{\rm low}$ ($V_{\rm high} > V_{\rm low}$) in the turn-off state, respectively. The corresponding loss power induced by driving the gate capacitance, i.e., $P_{\rm ls,GD}$, can be expressed by

$$P_{\rm ls,GD} = f_S \sum_{i \in SW} C_{g,i} \Delta V_{g,i}^2 \tag{25}$$

$$\Delta V_{g,i} = |V_{g,i,\rm on} - V_{g,i,\rm off}|. \tag{26}$$

The capacitance of C_g depends on the switch size, which is determined by the required turn-on resistance $R_{\rm on}$. Based on the optimization method in [25], $R_{\rm on}$ of an arbitrary power switch in a topology can be determined by

$$R_{{\rm on},i} = \frac{1}{G_{{\rm SW},i}} = \left(\frac{a_{{\rm SW},i} G_{\rm TOT}}{\sum_{k \in {\rm SW}} a_{{\rm SW},k}} \right)^{-1} \tag{27}$$

TABLE I
SUMMARY OF POWER-SWITCH SELECTION

DC Switches		Floating Switches	
Terminal Condition	Switch Type	Terminal Condition	Switch Type
$V_{pass}=V_{lowest}$	NMOS	$(V_{high}-V_{pass})>(V_{pass}-V_{low})$	NMOS
$V_{pass}=V_{highest}$	PMOS	$(V_{high}-V_{pass})<(V_{pass}-V_{low})$	PMOS

where $G_{{\rm SW},i}$ is the conductance of the ith switch, $G_{\rm TOT}$ represents the total switch conductance within a constrained chip area, and $a_{{\rm SW},i}$ denotes the switch charge multiplier, which is defined as $Q_{{\rm SW},i}/Q_{\rm OUT}$. Since C_g is proportional to the switch area that is inversely proportional to $R_{\rm on}$, we can define a process-dependent coefficient $K_{\rm SW}$ to correlate C_g and $R_{\rm on}$ as follows:

$$C_{g,i} = \frac{K_{\rm SW}}{R_{{\rm on},i}} \tag{28}$$

where $K_{\rm SW}$ can be obtained through simulation. In the above analysis, the parameters $a_{{\rm SW},i}$ and $\Delta V_{g,i}$ are topology dependent, and can be used to compare the switching-loss performance between different topologies under the same VCR and design constraints.

Referring to the power-cell implementation shown in Fig. 13, we classify the power switches into two operating types by observing their drain–source terminal connections, as listed in Table I. The first type is with one of the terminals connected to either the system highest or lowest dc potential, i.e., either $V_{\rm OUT}$ or $V_{\rm SS}$ for boost conversion, within the power stage, denoted as the dc switch. The second type is with both terminals connected to internal floating voltage levels within $V_{\rm OUT}$ and $V_{\rm SS}$, e.g., the switches connected to $V_{\rm IN}$ or between two adjacent power cells, denoted as the floating switch. To reduce the switch gate-driving voltage, either NMOS or PMOS can be selected based on its terminal conditions, as summarized in Table I. Furthermore, as $V_{\rm pass}$ for a certain internal node in a power stage can vary under different VCRs according to Table I, complementary p-n switches may be required to attain the optimal switch driving loss. However, this inevitably increases the switch area and the switch control complexity. Therefore, as discussed in Section IV-C, all the switches are implemented by using NMOS to enhance the power density, except for those connected to $V_{\rm OUT}$.

For a dc switch to achieve the maximum conductance, the corresponding ΔV_g is generally chosen as the rated voltage $V_{\rm rate,SW}$ of the power switch, resulting in

$$\Delta V_{g,\rm dc} = |V_{\rm rate,SW}|. \tag{29}$$

In contrast, ΔV_g for an NMOS-based floating switch with maximum conductance can be expressed as follows:

$$\Delta V_{g,\rm float\_N} = |V_{\rm pass} + V_{\rm rate,SW} - V_{\rm low}(\Phi_{\rm off})|. \tag{30}$$

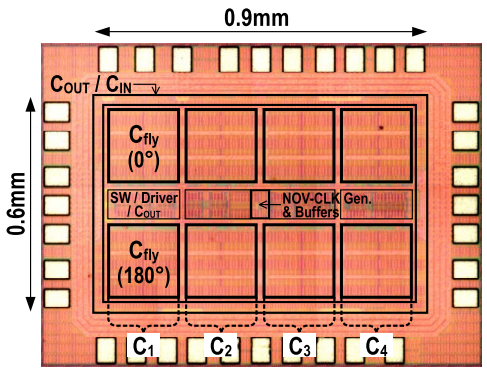

Fig. 16. Annotated die micrograph of the converter prototype.

Similarly, for a PMOS-based floating switch

$$\Delta V_{g,\text{float\_P}} = |V_{\text{pass}} - V_{\text{rate,SW}} - V_{\text{high}}(\Phi_{\text{off}})|. \quad (31)$$

Referring to Fig. 12, the corresponding vector $a_{\text{SW},i}$ can be interpreted by the charge multiplier $a_{c,i}$. The corresponding $\Delta V_{g,i}$ can be determined by using (29)–(31). In this article, we set $\Delta V_{g,\text{dc}}$ to be V_{DD}, which equals V_{OUT}. Due to the uniform charge-flow characteristic, all the power switches have identical charge multiplier among the power cells.

V. Chip Implementation and Measurement

We implemented the designed SC boost converter with seven rational VCRs in a 65-nm bulk CMOS process. The total flying capacitance is ∼3 nF. All the C_{fly} are implemented by parallel-connected metal–insulator–metal (MIM) and MOS capacitors, which are stacked vertically to reduce the spatial area. The total-capacitance density is ∼15 fF/μm^2, with 2 and 13 fF/μm^2 from MIM and MOS capacitors, respectively. It can boost a V_{IN} between 0.25 and 1 V to a V_{OUT} of 1 V. We employed low-voltage power switches to improve the switch on-resistance (R_{on}) and reduce the switching loss, while using MIM capacitors in the ABS drivers. All the logic cells in the ABS drivers are powered by an external V_{DD} source, which consumes significantly less power when compared with the targeted P_{OUT}. The on-chip filtering capacitance contains 1 nF at V_{OUT} and 0.3 nF at V_{IN}. Fig. 16 shows the annotated die micrograph, with the power switches, drivers, NOV clock generators, and buffers placed between the dual-branch power cells. The chip occupies an active area of 0.54 mm^2. This work mainly focuses on demonstrating the VCR flexibility and SC power-stage efficiency when compared with the conventional 2DSP. In the implemented chip prototype, we externally adjust the frequency of the master clock CLK_0 to realize pulse–frequency modulation (PFM) for load-regulation control. A 3-bit digital control is applied to achieve VCR reconfiguration. An on-chip close-loop load regulation can be accomplished by using the PFM approaches as in [14], [23], [29], and [30], together with a resistive ladder-based input voltage detector [9], [13]. To resolve the start-up issue at low V_{IN}, on-chip charge-pump techniques can be adopted as in [31]–[33].

Fig. 17 shows the performance comparison between the proposed ASP (both simulated and measured) and conventional 2DSP (simulated) topologies for the implemented fractional VCRs of {4:5, 2:3, 3:5, 2:5}. In the simulation, both topologies occupy the same chip area with the bottom-plate parasitic loss set to 8% of the nominal capacitance to model the parasitic effect of integrated MOS capacitors. For the loss-power contribution in the modeled ASP cases, statistically around 38%–44% is from the conduction loss, 54%–60% is from the parasitic loss, and less than 4% is from the switch driving loss. From Fig. 17, all the fractional VCRs generated by using ASP evidently show improved PCE than the 2DSP counterpart. Fig. 17 also exhibits the measurement results of the ASP implemented in a 65-nm bulk CMOS process. It can

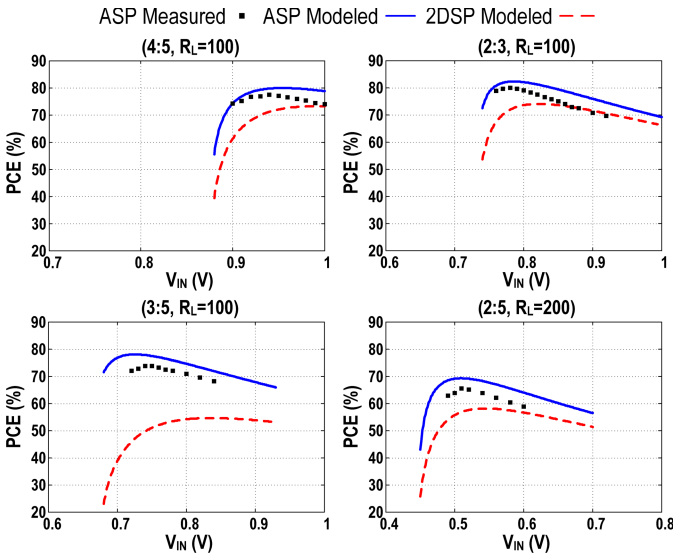

Fig. 17. Measured and simulated PCE for the fractional VCR implementations using the proposed ASP-based topology, and the simulated PCE of the conventional 2DSP-based one ($V_{\text{OUT}} = 1$ V).

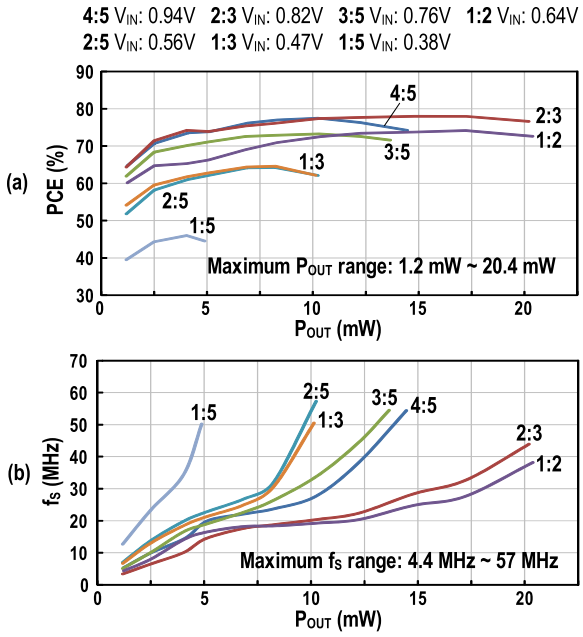

Fig. 18. Measured output power range under fixed V_{OUT} of 1 V (dc) for all the seven VCRs versus (a) PCE and (b) switching frequency f_S.

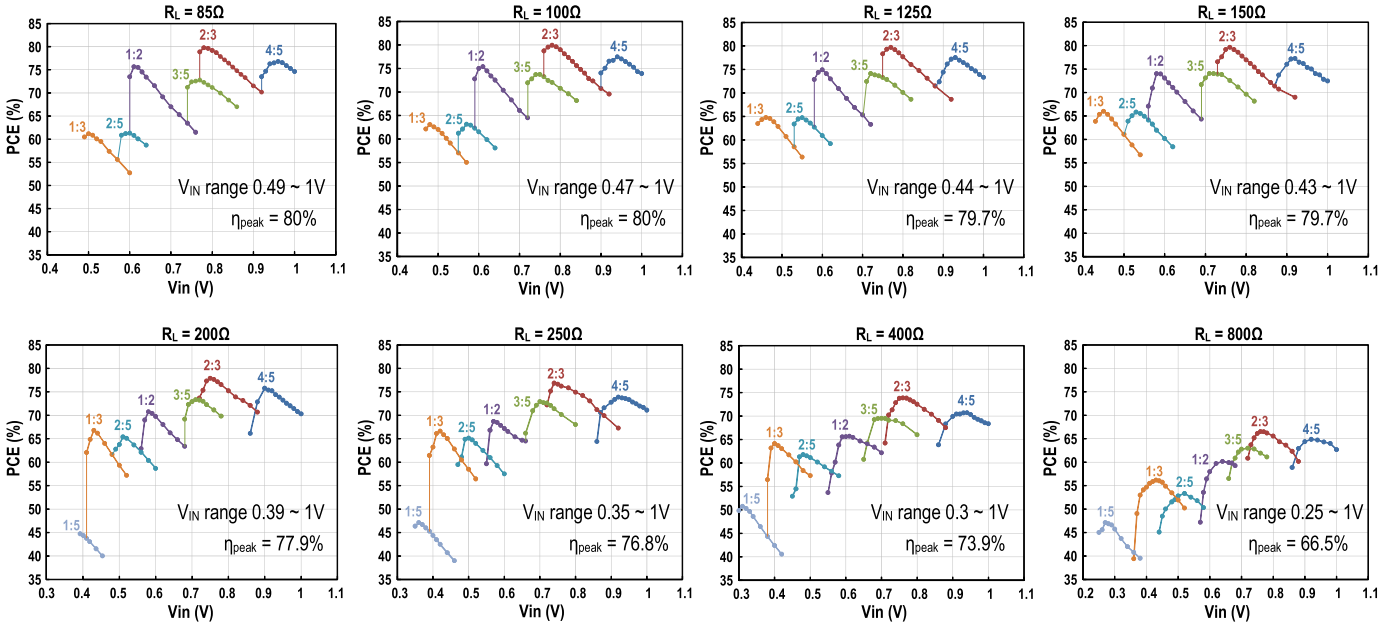

Fig. 19. Measured PCE over the targeted V_{IN} range under different resistive loads when generating a V_{OUT} of 1 V.

be observed that the simulated ASP performance is consistent with the measured results.

Fig. 18 depicts the measured output power range versus the PCE and the switching frequency f_S for each implemented topology with a fixed $V_{\mathrm{OUT}} = 1$ V and variable R_L. The output power range is from 1.2 to 20.4 mW, with the highest power delivered at VCR = 1:2. Fig. 18(b) shows the relationship between f_S and the delivered output power P_{OUT} for each VCR under a specific V_{IN} and V_{OUT}. Note that due to the specific V_{IN} selection, the results in the plot do not include the overall peak PCE point for the converter. The general trend of increased switching frequency under a higher VCR at the same P_{OUT} can be clearly observed. The curves for each VCR shown in Fig. 18(b) is measured under a fixed V_{IN} and V_{OUT} (>1 V), with P_{OUT} varied through modulating the resistive load R_L. Specifically, we first increase P_{OUT} by reducing R_L and then increase f_S to obtain $V_{\mathrm{OUT}} > 1$ V. When the converter is operating in the deep fast switching limit (FSL) region, a change in the smallest R_L step during the measurement can no longer ensure $V_{\mathrm{OUT}} > 1$ V through increasing f_S, indicating the maximum deliverable P_{OUT} for a particular VCR.

Fig. 19 plots the measured PCE using a variable resistive load R_L using an electric load (KIKUSUI PLZ164WL) over the targeted V_{IN} range with $V_{\mathrm{OUT}} = 1$ V. The loading range is from 85 to 800 Ω, except for VCR = 1:5 with R_L limited to 200 Ω due to the higher R_{SSL}. The measured peak PCE (η_{peak}) is ∼80% with R_L between 85 and 100 Ω at VCR = 2:3. From Fig. 8(c), the ASP-based 2:3 shows a lower parasitic loss than the case for 4:5, which is, in turn, lower than the 1:2 one. Consequently, the achieved PCE for 1:2, 4:5, and 2:3 progressively increases, as plotted in Fig. 19. For the 3:5 case, although its parasitic loss is slightly less than that of 2:3, the increased R_{SSL} as observed in Fig. 8(a) eventually limits the achievable PCE, as shown in Fig. 19. Fig. 20 displays the measured converter switching frequency over the targeted V_{IN} range under different loading conditions. It can be observed that the converter operating frequency is proportional to the loading level as expected. Fig. 21 presents the measured steady-state output waveforms for the 4:5 and 2:3 scenarios with $R_L = 85$ Ω. The V_{OUT} ripples are 76 and 84 mV for the two VCRs, respectively, without external filtering capacitors.

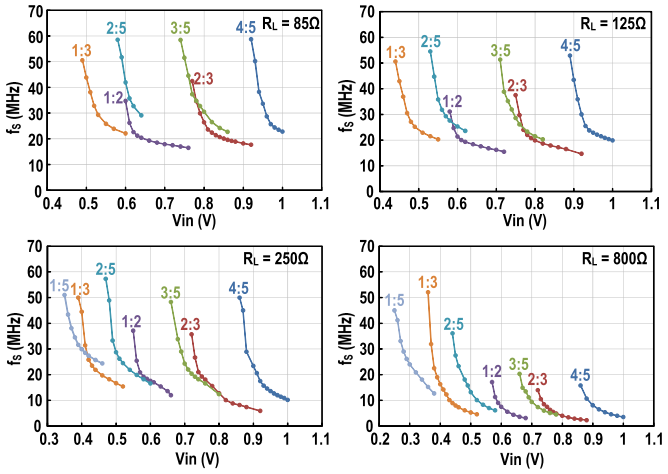

Fig. 20. Measured converter-switching frequency over the targeted V_{IN} range under different resistive loads with $V_{\mathrm{OUT}} = 1$ V.

Table II lists the performance comparison of the proposed converter topology with the state of the art. The design presented in [15] is based on the SP topology. It adopts high-density-MIM (HD-MIM) capacitors as C_{fly}, which feature low bottom-plate parasitic capacitance. As the proposed ASP-based converter exhibits lower R_{SSL} and parasitic losses, it can achieve a comparable η_{peak} as [15], but with ∼1300 times power-density improvement by employing MIM+MOS as C_{fly}. In contrast to the customized design using the fully depleted silicon-on-insulator (FD-SOI) process in

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	JSSC'16 [15]	JSSC'15 [24]	JSSC'15 [30]	TVLSI'15 [13]	JSSC'17 [16]	JSSC'18 [34]	ISSCC'16 [35]	CICC'15 [36]
Technology	**65nm CMOS**	180nm CMOS	28nm FD-SOI	180nm CMOS	0.35μm CMOS	180nm CMOS	65nm CMOS	0.35μm HVCMOS	65nm CMOS
Conversion type	**Boost**	Boost	Boost	Boost	Boost	Boost	Buck-Boost	Buck-Boost	Buck-Boost
Topology type	**ASP-based (ASP+Dickson)**	SP-based (transposed SP)	Customized	Customized	SP-based (transposed SP)	Moving-sum (Dickson+SP)	AVFI	Binary Recursive	SP
VCR type	**Rational**	Rational	Rational	Integer	Rational	Integer	Rational	Rational	Rational
Number of VCR	**7**	14	3	2	4	*22	13 (boost)	9 (boost)	3 (boost)
VCR range	**1.25 ~ 5**	1.33 ~ 8	1.5 ~ 2.5	4 ~ 6	2 ~ 4 (boost)	10 ~ 31	1.1 ~ 7 (boost)	1.14 ~ 4 (boost)	1.5 ~ 3 (boost)
Integrated C_{fly}	**MOS + MIM**	HD-MIM	MOS + MOM	MOS + MIM	Off-chip	N/R	MOS + MIM	MIM	N/R
V_{IN} Range [V]	**0.25 ~ 1**	0.45 ~ 3	1	1	1.4 ~ 3	0.25 ~ 0.65	0.26 ~ 1.3 (boost)	2 ~ 6 (boost)	0.5 ~ 1 (boost)
V_{OUT} [V]	**1**	3.3	1.2 ~ 2.4	3 ~ 6	4.8	4	1.2	5	1
I_{OUT_MAX} [mA]	**20.1**	0.015	1	0.24	10	*0.001	21.7 (boost)	1.4 (boost)	0.0033 (boost)
η_{peak} [%]	**#80**	81	#88	58	82	60	83.2 (boost)	70.9 (boost)	70.4 (boost)
P-density @η_{peak} [mW/mm^2]	**#22.7**	*0.0174	#4.9	*2.4	N/A	*~0.0001	10.8 (boost)	*0.15 (boost)	*0.0069 (boost)
Fully integrated	**Yes**	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes

*Estimated from the corresponding literature #Regulation control executed externally

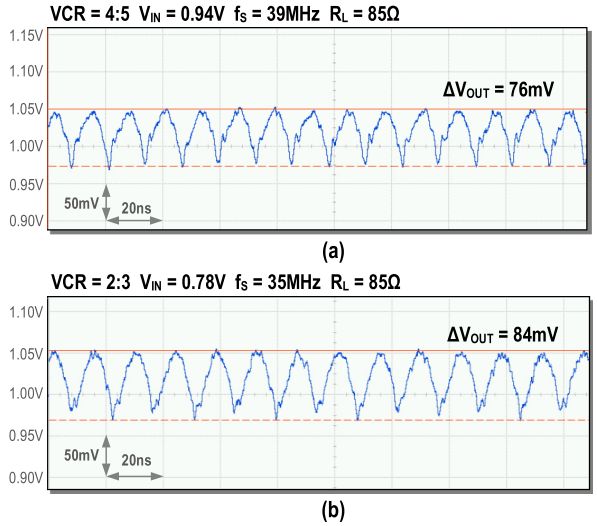

Fig. 21. Measured steady-state V_{OUT} ripple with $R_L = 85\ \Omega$ at (a) 4:5 and (b) 2:3.

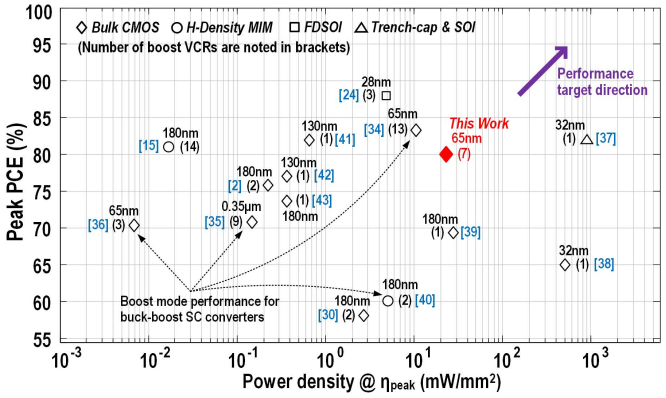

Fig. 22. Performance benchmarking with state-of-the-art fully integrated SC boost converters.

[24], which achieves a higher peak PCE, this work attains a >4.6 times higher power density in bulk CMOS with finer-grained VCRs. The proposed converter also demonstrates higher peak efficiency and power density than the ones in [30], [35], and [36] in boost-conversion modes. When compared with the boost mode in [34], the achieved power density is 2.1 times higher through reducing the power stage control redundancy. Fig. 22 benchmarks this work with the other fully integrated SC boost converters, in both bulk CMOS and special processes. It can be observed that this work exhibits a higher power density while achieving a high number of VCRs when compared with the existing designs in bulk CMOS.

VI. CONCLUSION

This article presents an ASP-based topology design technique, which can systematically realize an arbitrary rational-boost VCR with improved efficiency and power density for fully integrated SC dc–dc converters. The proposed methodology can effectively obtain both optimal R_{SSL} and reduced bottom-plate-switching voltage, while maintaining the VCR flexibility as in the conventional 2DSP-based converters. We fabricated a fully integrated SC boost topology with seven rational VCRs in a standard 65-nm bulk CMOS process. The chip prototype attains a measured peak PCE of 80% under a power density of 22.7 mW/mm^2. It exhibits an improved PCE versus power density when compared with the state-of-the-art fully integrated SC boost converters with multiple VCRs in bulk CMOS.

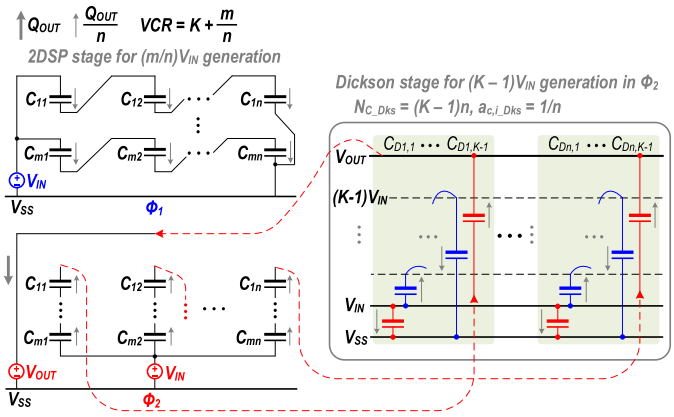

Fig. 23. Two-phase operation of a 2DSP-based topology with the integer-stage implementation using the Dickson converter.

APPENDIX

We first derive the R_{SSL} general form for the 2DSP-based topology. The total number of "unit" power cells used in the 2DSP-based topology is the sum of the "unit" cells for the fractional (N_{C_2DSP}) and integer (N_{C_int}) parts. Note that each cell has an identical charge multiplier. Based on the definition given in (2a) and the 2DSP-based topology model shown in Fig. 23, we can obtain

$$|a_{c,i}|_{2DSP} = \frac{1}{n}, |a_{c,i}|_{int} = \frac{1}{n} \tag{A1}$$

$$N_{C\_2DSP} = mn, N_{C\_int} = (K-1)n \tag{A2}$$

$$R_{SSL,2DSP} = \frac{\left[\sum_{i=1}^{mn+(K-1)n} \left(\frac{1}{n}\right)\right]^2}{C_{TOT} f_S} = \frac{(m+K-1)^2}{C_{TOT} f_S}. \tag{A3}$$

Note that (A3) is exactly the same as (4).

For the bottom-plate parasitic loss in the 2DSP-based topology, by employing (A1) and (A2), the loss-power expression in (22) and (23) can be rewritten as follows:

$$P_{ls,BP\_2DSP} = \frac{\beta C_{TOT} f_S V_{IN}^2}{n(m+K-1)} \sum_{i \in C_{fly}} \lambda_{CBi}^2. \tag{A4}$$

We further derive $\lambda_{CB,i}$ for each capacitor in both the 2DSP and Dickson parts. From Fig. 23, $V_{CB,i}/V_{IN}$ for each cell in both phases can be expressed as follows:

$$\frac{V_{CB}}{V_{IN}}(\Phi_1) = \begin{bmatrix} \frac{n-1}{n} & \cdots & \frac{1}{n} & 0 \\ \vdots & \ddots & \vdots & \vdots \\ \frac{n-1}{n} & \cdots & \frac{1}{n} & 0 \\ \frac{n-1}{n} & \cdots & \frac{1}{n} & 0 \end{bmatrix}_{m \times n}$$

$$\frac{V_{CB}}{V_{IN}}(\Phi_2) = \begin{bmatrix} 1+\frac{m-1}{n} & \cdots & 1+\frac{m-1}{n} & 1+\frac{m-1}{n} \\ \vdots & \ddots & \vdots & \vdots \\ 1+\frac{1}{n} & \cdots & 1+\frac{1}{n} & 1+\frac{1}{n} \\ 1 & \cdots & 1 & 1 \end{bmatrix}_{m \times n}. \tag{A5}$$

The elements in (A5) are arranged according to the capacitor position shown in Fig. 23. With (A5), we can determine λ_{CB} accordingly as follows:

$$\lambda_{CB} = \left| \frac{V_{CB}}{V_{IN}}(\Phi_2) - \frac{V_{CB}}{V_{IN}}(\Phi_1) \right| = \begin{bmatrix} 1-\frac{n-m}{n} & \cdots & 1-\frac{2-m}{n} & 1-\frac{1-m}{n} \\ \vdots & \ddots & \vdots & \vdots \\ 1-\frac{n-2}{n} & \cdots & 1 & 1-\frac{n-(n+1)}{n} \\ 1-\frac{n-1}{n} & \cdots & 1-\frac{1}{n} & 1 \end{bmatrix}. \tag{A6}$$

By substituting each element in the matrix in (A6) into (A4), we can have the parasitic loss power for the 2DSP-based topology according to a specific set of VCRs, V_{IN}, C_{TOT}, and f_S.

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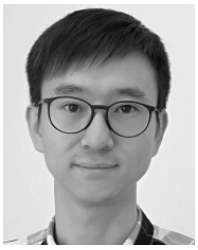

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Rui P. Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, Ph.D. degrees, and the Habilitation degree for full professor in electrical engineering and computers from the Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), University of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

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Dr. Martins was a Vice Rector (Research) from 2008 to 2018, and will be a Vice Rector (Global Affairs) from 2018 to 2023. He was the Founding Chair of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of the IEEE CAS Society (CASS)], the General Chair of the IEEE Asia–Pacific Conference on CAS (APCCAS) in 2008, the Vice President (VP) Region 10 (Asia, Australia, and Pacific) from 2009 to 2011, and the VP of the World Regional Activities and Membership of IEEE CASS from 2012 to 2013. He was also a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, 2018 (Chair), and 2019, the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014, and the IEEE CASS Nominations Committee from 2016 to 2017. He was also the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC) in 2016. In July 2010, he was unanimously elected as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia. He was also the VP and President of the Association of Portuguese Speaking Universities (AULP) from 2005 to 2014 and from 2014 to 2017, respectively. He was a recipient of the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016 and two Macao Government decorations: the Medal of Professional Merit (Portuguese) in 1999 and the Honorary Title of Value (Chinese) in 2001. He was an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013. He was a Nominated Best Associate Editor from 2012 to 2013.