A 2.4-GHz Mid-Field CMOS Wireless Power Receiver Achieving 46% Maximum PCE and 163-mW Output Power

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***Abstract*—This brief presents a 2.4-GHz power receiver using CMOS technology for the next-generation sub-Watt-level mid-field wireless charging. The power receiver mainly consists of an on-board matching network and an integrated two-stage differential cross-connected (CC) rectifier. When designing the CC rectifier, we use a special routing consideration for the on-chip load capacitor C_L for reducing the effect of the routing parasitic inductance. By separating the input power source ground and the rectifier ground on the PCB, we designed the differential rectifier directly connected to the single-ended matching network and the power source without using a balun, which significantly reduces the design complexity. Also, the microstrip line (ML) manufactured on the Rogers 4003 substrate is co-designed with the bonding wire for a precise matching. We use the 1.8-V I/O devices in a 28-nm bulk CMOS for the rectifier. Measurement results show that the power receiver, including the matching network and the rectifier, achieves a 46% peak power conversion efficiency (PCE) at 163-mW dc output power.**

***Index Terms*—Mid-field wireless power transfer, power at a distance, power receiver, CMOS, differential cross-connected rectifier.**

I. Introduction

WIRELESS power transfer through both near-field and far-field operations have been widely studied in the past decade. For the near-field case, it transfers power through the magnetic field based on inductive coupling coils. Its power transmission level ranges from micro-watt to kilo-watt, for a wide range of applications including medical implants, mobile phones, smart watches, and electric vehicles. However, the transmission distance is quite limited, and is related to the coil sizes. On the contrary, for the far-field case, it transfers power through electromagnetic waves through an antenna. The distance can reach several meters, but the received power is very low (usually in the microwatt level). Far-field energy harvesting is often used in passive RFID and Internet-of-Things (IoT) applications. To compromise between the transmission distance and the received power, a couple of companies came up with the mid-field operation in office environments [1]–[3], as shown in Fig. 1(a). The power transmitter can be installed under the display monitor, and it sends power to the nearby electronic devices. Fig. 1(b) shows

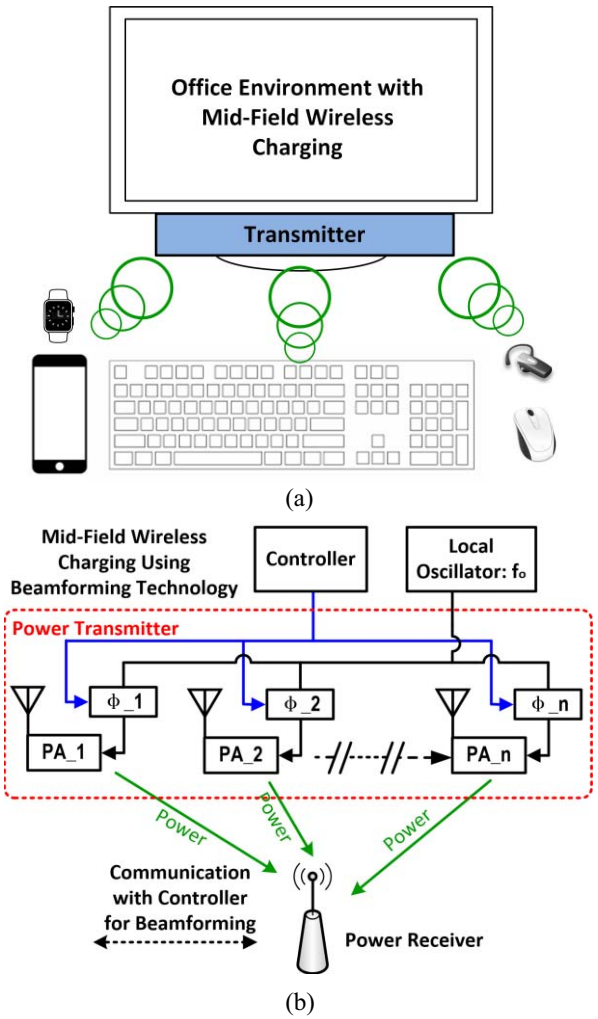

Fig. 1. (a) Application scenario of mid-field wireless charging, and (b) block diagram of the wireless power transfer system with beamforming technology.

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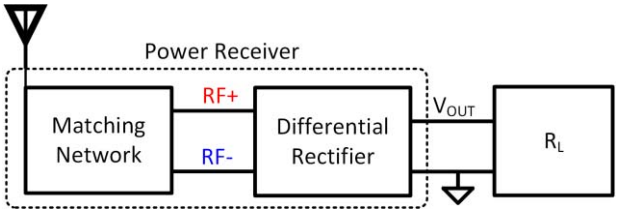

Fig. 2. Block diagram of power receiver.

the block diagram of the mid-field wireless power charging system. The system mainly consists of a wireless power transmitter, a power receiver and a controller. In the transmitter, PAs drive the phase-array antennas with separate phase control blocks. For the power receiver to harvest more power in this environment, beamforming technology can be applied [4]. In the beamforming process, the controller will firstly communicate with the receiver, and then sends the phase delay information to each phase control blocks according to the communication result. With the phase shift among input signals of the PAs of the antenna array, the electromagnetic waves radiated from antennas will positively superimpose on the receiving antenna. Then, the transmitted power can be significantly increased in this way and the received power can reach milliwatt levels, allowing to charge devices like earphone, mouse, keyboard, smart watch, and even the mobile phone, with a the transmission distance that can reach as long as 1 meter. Therefore, we designed a 2.4-GHz Wi-Fi band power receiver in the sub-Watt level for this mid-field application.

We organized the remainder of this brief as follows. In Section II, we introduce the design considerations and the main contributions of this brief, which include, an optimized layout of the C_L of the rectifier to suppress the output ripple, a one-branch impedance matching network without balun for the differential rectifier by separating the power source and the rectifier grounds, and the modeling of the bonding wire which is co-designed as part of the matching network to obtain a more precise matching especially in the high input power case. In Section III, experimental results are shown and discussed, followed by the conclusions in Section IV.

II. Power Receiver Design

A. CMOS Rectifier Design

Fig. 2 shows the block diagram of the power receiver. This brief mainly focuses on the rectifier and the matching network designs. Basically, there are two choices for the CMOS rectifier topology: the diode-connected and the cross-connected (CC) [5], [6]. For the CC topology, the power transistors are switched on/off by the RF input voltages, for their on-resistances to be relatively small with the same transistor sizes. In general, the CC topology has a better performance in terms of the peak efficiency when compared with other passive topologies [6]. Therefore, we choose the CC topology in this design.

To boost the output voltage, we use a two-stage CC rectifier as presented in Fig. 3(a). The NMOS transistors are designed in deep N-wells, for the second stage to work in the same

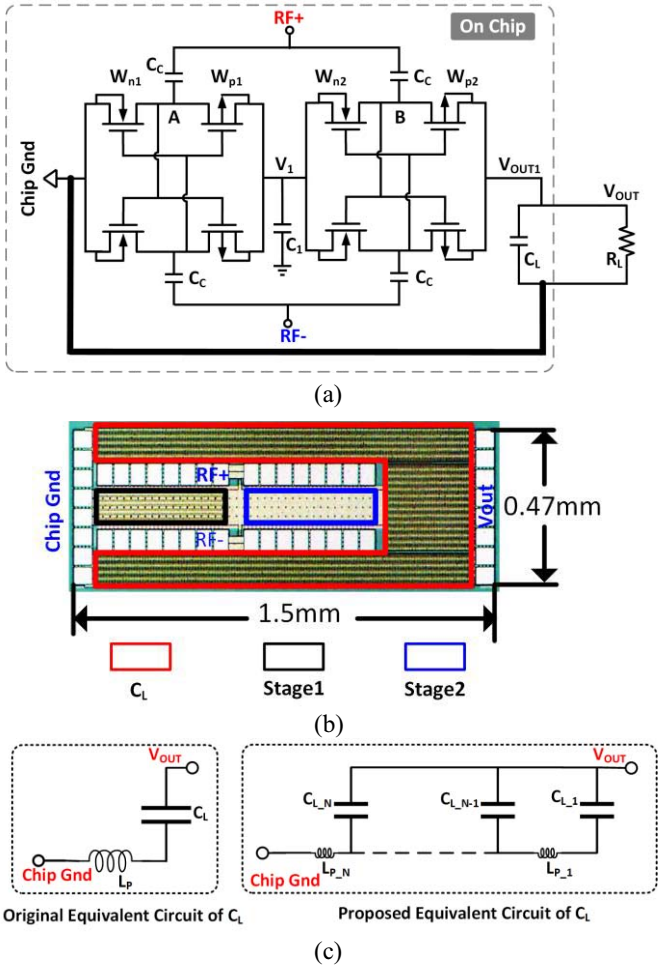

Fig. 3. (a) Schematic of the two-stage rectifier; (b) chip micrograph of the rectifier; and (c) equivalent circuits of the traditional C_L layout (left) and the proposed circuit (right).

AC status but with different DC potentials as the first stage. Because the inputs of these two stages are AC coupled, with the two stages stacked for a higher DC output voltage. To handle sufficiently high voltages for battery charging, both PMOS and NMOS transistors use 1.8-V I/O devices.

B. On-Chip Load Capacitor

The bold ground line in Fig. 3(a) represents a parasitic inductor from the C_L bottom plate to the chip ground. The length of the ground routing metal is the same as the length of the rectifier layout, which is about 1 mm in our case and leads to a considerably large parasitic inductance. This parasitic inductance will degrade the filtering function of C_L, and induce large output voltage ripple. Traditionally, with C_L placed near V_{OUT}, its equivalent circuit is shown on the left of Fig. 3(c). In this design, we paved part of C_L along both sides of RF+ and RF− to the chip ground pads, as shown in Fig. 3(b). Therefore, in the equivalent circuit of our C_L, the large parasitic inductance is divided into many small pieces, as shown on the right side of Fig. 3(c), which can also be understood as a capacitive transmission line. In this way, the proposed layout of C_L will favorably have a better filtering effect than the traditional one. Post-layout simulation have

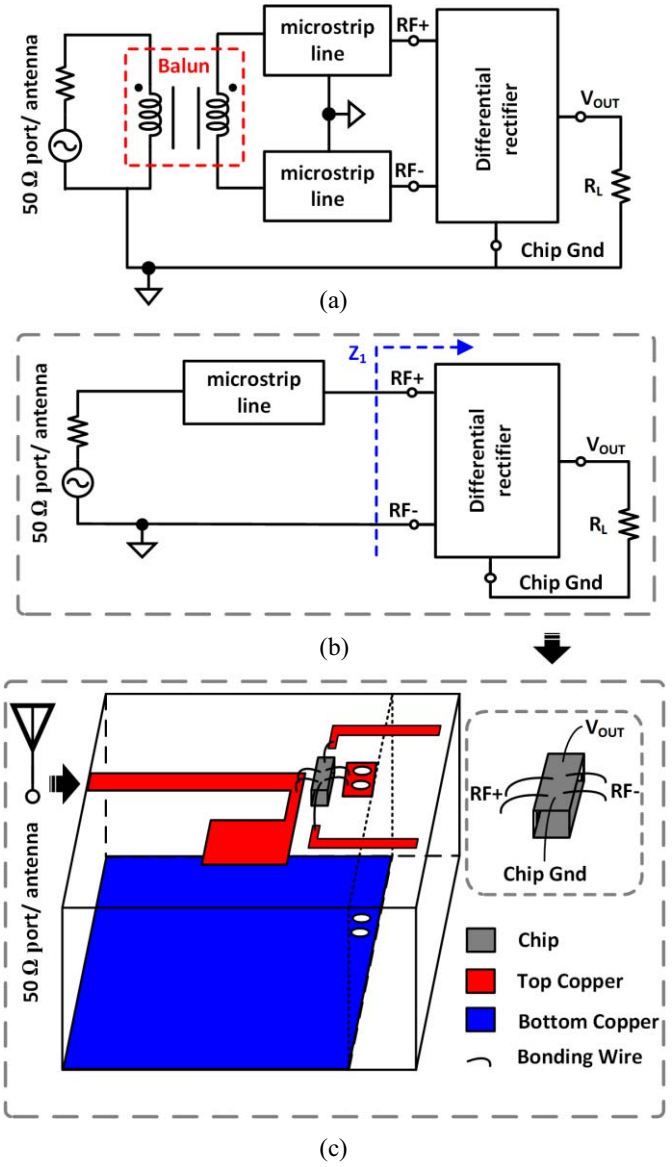

Fig. 4. (a) Traditional and (b) the proposed matching method for differential rectifier; (c) 3D view of the matching network and the chip on PCB.

been used to verify this method. Assuming the L_P is 10pH, and C_L is 3nF, according to the simulation results, the output ripple will be about 160mV. When we manually divide both L_P and C_L into 20 pieces to emulate our proposed method, the ouput ripple is significantly reduced to 15mV. The chip area of the rectifier, including C_L and pads, is 1.5×0.47 mm^2, as given in Fig. 3(b).

C. Single-Ended Source to Differential Rectifier

As mentioned above, the differential CC rectifier topology is used in this brief for higher PCE. However, many commercial antennas and the power source equipment are single-ended. A typical way to convert a single-ended source into a differential source is to use a balun [7]–[9]. Obviously, we need a differential matching network after the balun, as presented in Fig. 4(a). But, the balun itself will bring certain voltage and

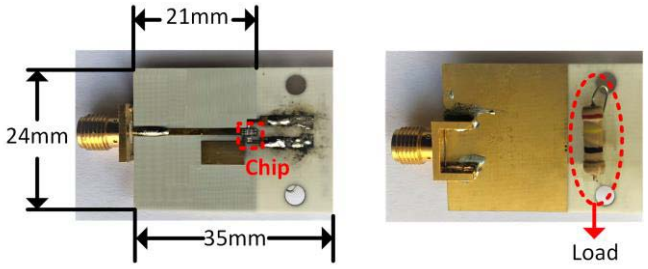

Fig. 5. Details of the PCB and the chip: (left) top view of the PCB with the chip, (right) bottom view of the PCB with the load.

phase unbalances between two input ports. Also, if we implement it on PCB, it would occupy a large board area and also degrades the system efficiency. In the design, we eliminate the balun and use only a single-ended matching network by separating the grounds of the power source and the rectifier, as shown in Fig. 4(b). Fig. 4(c) shows the detailed implementation. We connect the antenna signal line to the microstrip line on the PCB top plate, and then connect it to RF+ of the rectifier. Further, we connect the antenna ground to the PCB bottom plate which is strongly coupled to the PCB top plate, forming the matching network, which then connects to RF− through the conduction holes. The chip substrate, which is also the rectifier ground, is separated from RF− (the source ground). Therefore, the differential rectifier can directly connect to the single-ended antenna or power source without using a balun.

D. Co-Designed Matching Network

In the far-field/mid-field wireless charging scenarios, the power will be harvested through a RF antenna with certain output source impedance. For the maximum output extraction, the load impedance (rectifier input impedance) should match the source impedance. To achieve this, one possibility is to co-design a specific antenna that directly matches the rectifier input impedance, while another way is to design a matching network to transform the rectifier input impedance to match the antenna impedance. The first approach can reduce the number of components, and also increases the system PCE. But the designed antenna will not be compatible with other communication systems, for example if we reuse the 2.4-GHz WiFi antenna. Therefore, we choose the second solution which can work with generic antennas.

For the matching network design, a fully integrated solution with an on-chip inductor can reduce the size of the solution, but its PCE suffers from the low-Q on-chip inductor. Also, we can design the matching network on a PCB with discrete passive components. However, the discrete passive components also have the low-Q problem and an inaccurate value, and also the parasitics on board will affect the matching accuracy, degrading the PCE. On the other hand, the matching network using a microstrip line on the PCB provides a one-step solution and better efficiencies [7], [10]. Fig. 5 shows the front and back views of the matching network in this brief. To further decrease the power loss, we designed the microstrip line on a Rogers RO4003 substrate which has a low loss tangent parameter. We chose a thickness of 0.508 mm for the PCB substrate.

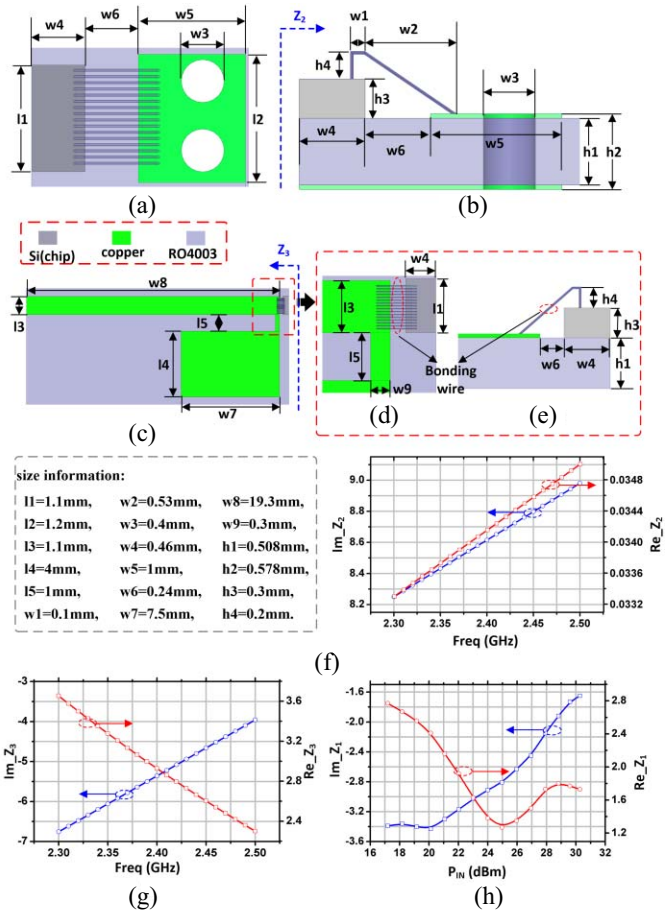

Fig. 6. (a) Top view and (b) side view of the bonding wire and conduction holes (RF− side); (c) matching network with bonding wire; (d) top view and (e) side view of bonding wire (RF+ side); (f) simulated impedance of Z_2, (g) simulated impedance of Z_3; and (h) simulated Z_1.

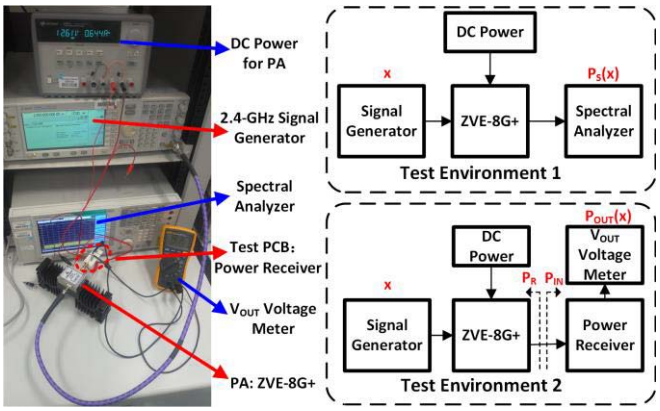

Fig. 7. Measurement setup environment.

In this design, the effect of the bonding wire should also be carefully considered. Fig. 6(a) and (b) show the models of bonding wires and conduction holes. According to the simulation results exhibited in Fig. 6(g), the impedance of bonding wire and conduction holes is 0.038+j8.61 (Z_2) at 2.4 GHz. While the post-layout simulation of the rectifier shows that the designed rectifier has an input impedance of 1.92−j3.1 (Z_1) when P_{IN} is 22dbm, as shown Fig. 6(h). Then, the bonding wire impedance is comparable to the rectifier input

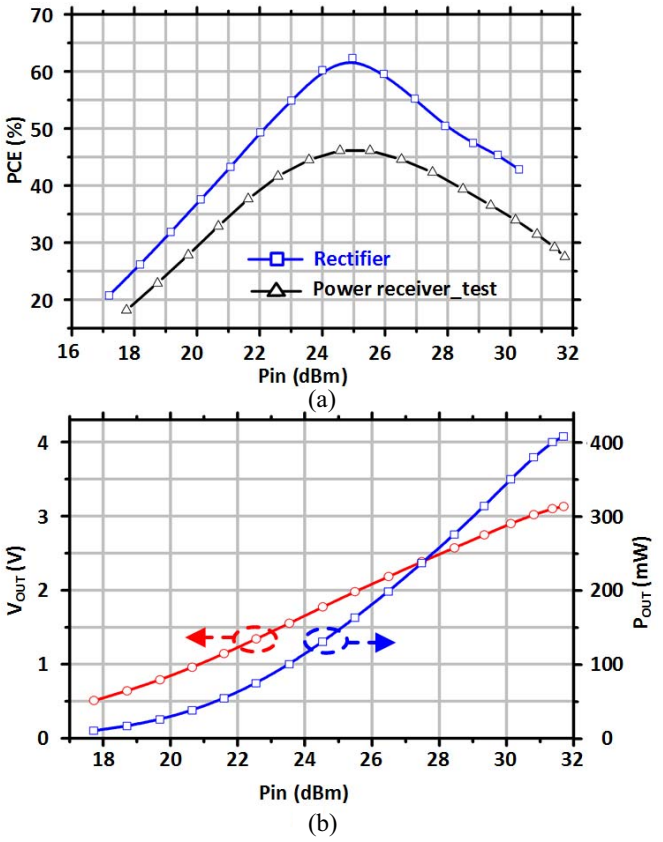

Fig. 8. Measurement results of the power receiver: (a) PCE of power receiver (measured), and PCE of rectifier (matching network de-embedded), (b) output voltage and output power versus input power.

impedance, which means the bonding wire should be considered in the network. Then the microstrip line is co-designed with the bonding wire to make the output impedance Z_3 nearly conjugate with $Z_1 + Z_2$. The detailed model of the co-designed matching network is shown in Fig. 6(c), (d), and (e). Simulation results of the output impedance Z_3 (when the input is connected to a 50-Ω port) is plotted in Fig. 6(g).

E. Parasitic Analysis

For the current PCB design, there are parasitics mismatch among RF+, RF−, chip GND, and V_{OUT}. Electromagnetic (EM) simulation for these couplings has been done to investigate their effects on the PCE. According to the EM simulation results, the parasitic capacitances are 200 fF between RF+ and chip GND, 318 fF between RF− and chip GND, 180 fF between RF+ and V_{OUT}, 324 fF between RF− and V_{OUT}, respectively, which correspond to a couple hundreds of Ohms at 2.4 GHz. In this application, those impedance values are much larger than the rectifier input impedance Z_1. Simulation results show that parasitic mismatches only affect Z_1 by less than 3%, and the PCE by less than 1%. Also, the coupled ripples from RF+/RF− to V_{OUT} are well suppressed by the on-chip C_L.

III. Measurements

To measure the sub-Watt level power receiver, a power amplifier (PA) ZVE-8G+ which has a 50-Ω output impedance at 2.4 GHz is employed as the power source. Fig. 7 shows

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

	[5]	[7]	[9]	[11]	[12]	[13]	[14]	[15]	**This work**
Frequency (GHz)	2	0.868	0.915	0.868	2.4	0.9	2.4	0.9	**2.4**
Technology (nm)	CMOS 65	CMOS 130	CMOS 130	CMOS 90	CMOS 130	CMOS 65	CMOS 180	CMOS 180	**CMOS 28**
No. of Stages	1	1	3	5	1	5	3	3,4 and 7	**2**
Input Matching	Not Included	Included	Included	**	Included	Not Include	Not Included	Not Included	**Included**
$\eta_{RF\text{-}DC}$ (Peak) @ Pin	58% @ -10dBm*	50% @ -2.5dBm	29.3 @ 0.2dBm	40% @ -17dBm	30% @ 10dBm	36.5% @ -10dBm	47% @ 8.9dBm	42.3% @ 3dBm	**46% @ 25.5dBm**
Max P_{OUT} (mW)	0.19*	0.71*	0.48*	0.024*	13.2*	0.05	5*	0.846*	**408**

* Estimate from graph; ** co-design with antenna;

the measurement setup. In the test setup 1, the PA output power, $P_S(x)$, is measured by a spectrum analyzer, where x is the PA input power from the signal generator. Assuming the PA's output impedance and the spectrum analyzer's input impedance are both 50 Ω, and therefore are well matched, the measured PA output power $P_S(x)$ is the maximum available power ($P_S = P_R + P_{IN}$) for the rectifier under test in the setup 2. Then, the rectifier DC output power $P_{OUT}(x)$ is measured with test setup 2. Therefore, the receiver PCE can be obtained from $\eta_R = P_{OUT}(x)/P_S(x)$, with the considerations of the impedance mismatch factor (reflected power P_R), conduction loss of the matching network, and the power loss of the rectifier.

Fig. 8 plots the measured output voltage, output power, and PCE of the receiver varying with $P_S(x)$. The R_L is 24 Ω. The designed power receiver can achieve a maximum PCE of 46% with 163-mW DC output power and 1.85-V output voltage. The maximum output DC power is 408 mW with 27.8% PCE and 3.1-V output voltage. Fig. 8(a) also plots the PCE of the rectifier after de-embedding both the insertion loss (0.54dB of the matching network through EM simulation) and the mismatch factor between Z_1 and $Z_2 + Z_3$, which shows the maximum PCE of the rectifier can reach 62.3%.

Table I presents the comparison with other state-of-the-art CMOS works, where the proposed power receiver (including the matching network) attains a good PCE and the highest DC output power.

IV. CONCLUSION

This brief presented a power receiver for the sub-Watt power level mid-field wireless charging scenario. The designed power receiver consists of a microstrip-line based matching network and a two-stage CMOS differential CC rectifier. An on-chip capacitive routing path has been used for reducing the parasitic routing inductors at high frequency. Single-ended source connecting to differential rectifier is realized by separating the source ground and the rectifier ground. Therefore, the balun is eliminated in the system, and the total efficiency increases. Model of the bonding wire is built and co-designed to get a precise matching. Consequently, a maximum PCE of 46% for the power receiver is measured with 163-mW DC output power, while the maximum DC output power can reach up to 408 mW.

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