A 5.35-mW 10-MHz Single-Opamp Third-Order CT ΔΣ Modulator With CTC Amplifier and Adaptive Latch DAC Driver in 65-nm CMOS

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***Abstract*— This paper reports a continuous-time (CT) third-order delta-sigma modulator that features a single amplifier biquad (SAB) and a passive integrator to simplify the circuit to just one power hungry operation amplifier (opamp). Such setup not only relaxes the gain and bandwidth requirement of the opamp design but also enhances the overall modulator stability which enables a power-efficient loop filter implementation. We used an SAR architecture in the quantizer with an advanced feedback technique to alleviate its speed penalty. By incorporating the proposed CT complementary (CTC) opamp and an adaptive latch scheme in the DAC driver, the modulator attains a signal bandwidth of 10 MHz with 79.6-dB signal-to-noise and distortion ratio (SNDR) while only consuming 5.35 mW from 1.2- and 1.8-V power supplies. The prototype has a dynamic range of 84.5 dB and a Schreier FoM of 177.2 dB with an active area of 0.033 mm^2.**

***Index Terms*— Analog-to-digital conversion (ADC), continuous-time (CT) delta-sigma modulator, DAC driver, passive integrator, single amplifier biquad (SAB).**

I. Introduction

RECENT years witnessed considerable research efforts being imposed to the continuous-time (CT) delta-sigma (ΔΣ) modulator as it has inherent benefits in anti-alias filtering [1] and power efficiency when compared with its discrete-time (DT) counterpart. On the other hand, driven by the applications, such as wireless communications and very-high-bit-rate digital subscriber line (VDSL), the required dynamic range and bandwidth have been pushed close to their limits while it is still necessary to maintain low power consumption. Under a certain technology and signal-to-noise and distortion ratio (SNDR), the maximum sampling rate has restrictions which basically determine the achievable design's bandwidth. In order to improve the dynamic range (DR) performance, a multi-bit quantization and high-order loop filter (LF) can be adopted. However, the former solution imposes a quantizer (QTZ) and a digital power consumption while the latter calls for more power hungry operation amplifiers (opamps).

The opamp in the wideband CT ΔΣ modulator is often power hungry due to the stringent requirements. While the finite gain and gain bandwidth (GBW) of the opamp lead to a non-ideal noise transfer function (NTF), which reduces the stability and the amount of the inband quantization noise attenuation of the modulator, such issue becomes more serious with multiple stages in series in high-order designs. In order to reduce the number of opamps used in the LF, we can adopt either analog [2] or digital [3] noise-coupling (NC) techniques which are suitable for a modulator with SAR analog-to-digital conversion (ADC) as the multi-bit QTZ. But, simultaneously, the SAR QTZ limits the maximum speed of the modulator. Similarly, an additional feedback time slot needs to be allocated to the 2nd stage NC SAR ADC in the digital NC approach [3]. In addition, its 2nd stage quantization results will be wasted when compared with the cascaded CT ΔΣ modulator. Alternatively, noise-shaping QTZs, such as the voltage-controlled oscillator (VCO) QTZ [4]–[6], can reach extra order without opamps. However, when the VCO is adopted, its linearity limits the output swing of the LF or an additional calibration circuit is required for the VCO tuning gain. Besides, the noise-shaped integrating QTZ (NSIQ) [7], [8], and the incorporation of both the VCO and the NSIQ [9] can also achieve additional order(s). But the bandwidth of the modulator is limited by the speed of the NSIQ which also calls for extra active components.

This paper presents a third-order CT ΔΣ modulator that only utilizes one opamp in the LF [10]. A single amplifier biquad (SAB) integrator jointly with a passive integrator in the LF not only can relax the opamp design but also facilitate the excess-loop-delay (ELD) compensation without the active adder. We also propose several low-power circuit techniques, including the continuous-time complementary (CTC) opamp, the adaptive latch in the DAC driver, and an SAR QTZ with advanced feedback to further improve the overall power efficiency. Implemented in 65-nm CMOS, the prototype decibel SNDR in a 10-MHz signal bandwidth, consuming only 5.35 mW with 0.033 mm^2 of active core area.

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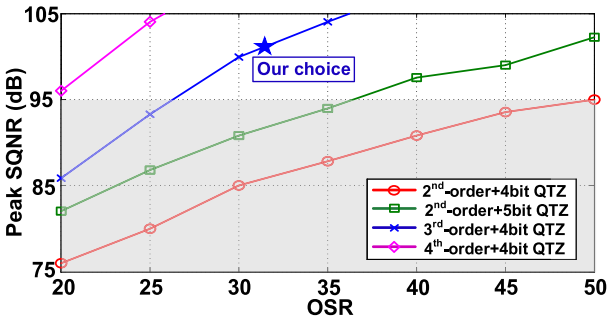

Fig. 1. Peak SQNR versus OSR for different CT $\Delta\Sigma$ modulators.

The remainder of this paper is organized as follows. Section II discusses the architecture considerations with behavior evaluations. Section III describes in detail the integrators and modulators. Section IV analyses the opamp's requirements and the modulator's stability. Section V introduces other low-power design techniques and their respective implementations in detail. Section VI provides the measurement results, and Section VII concludes this paper.

II. Architecture Selection With Behavior Evaluation

For the target applications, the required DR is around 85 dB with a bandwidth of ~10 MHz. In order to provide sufficient design margins for device noise and PVT variations, 95-dB signal-to-quantization-noise ratio (SQNR) is set as our goal in the behavioral evaluation. Fig. 1 indicates the relationship among oversampling rate (OSR), peak SQNR, LF order, and QTZ resolution with 4-dB maximum NTF out-of-band gain. It can be found that four topologies can meet the target specifications under various OSRs: 1) 2nd-order LF + 4-bit QTZ; 2) 2nd-order LF + 5-bit QTZ; 3) 3rd-order LF + 4-bit QTZ; and 4) 4th-order LF + 4-bit QTZ. The choice among these four cases involves different tradeoffs in terms of LF stability, QTZ's speed, opamp bandwidth, as well as the overall power consumption. A high LF order and out-of-band gain (case 4) can increase the inband quantization noise attenuation of the modulator, but with lower LF stability. Simultaneously, the high LF order also increases the number of power hungry amplifiers in the integrators. On the other hand, with higher bit resolution in the QTZ (case 2), the choice of the QTZ architecture is limited. While energy efficiency architecture, such as the SAR, may not be fast enough, the power hungry flash ADC requires additional calibration to handle the offset among the comparators. More bit quantization also leads to higher digital power which is critical in a wideband design with high sampling rate. Finally, case 1 with a high OSR, requires the QTZ to run at higher conversion rate and opamps with larger bandwidth to stabilize the modulator. This is quite undesirable especially in wideband designs. Based on the above, we select the third-order LF, 4-bit QTZ, and 32 OSR as it can enable a reasonable choice of LF implementation with the SAR as the QTZ.

Fig. 2 shows the selected 3rd-order CT-$\Delta\Sigma$ modulator architecture. In this design, we choose the cascade of integrators in

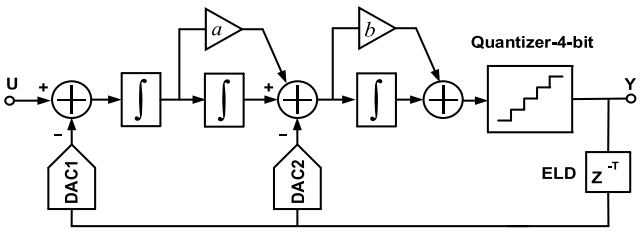

Fig. 2. General structure of the 3rd-order CIFF-FB CT $\Delta\Sigma$ modulator.

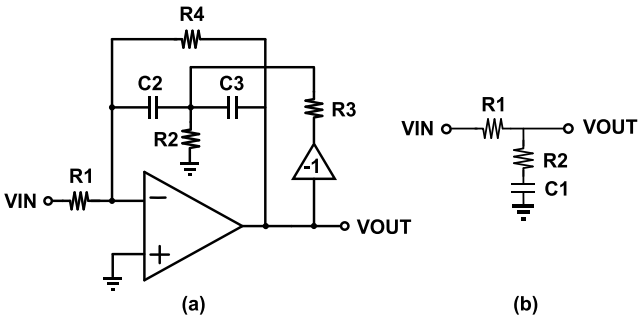

Fig. 3. (a) SAB integrator. (b) Passive integrator.

feedforward-feedback (CIFF-FB) rather than feedback (CIFB) or feedforward (CIFF) structures, which trades the signal TF (STF) peaking [11] with noise suppression of the succeeding integrators [12]. Besides, the CIFB structure requires N DACs in the Nth-order modulator for feedback, thus leading to a large power consumption from the DACs and their driver circuits. Such power can be significant in wideband designs with a high sampling rate and multi-bit QTZ.

It can be easily recognized that the integrators dominate the overall power consumption of the proposed modulator due to the implementation of the LF. The opamps of the 1st stage and summing stage are the most power-hungry amplifiers in the LF. Next, we will focus on the design of the low-power integrators to further improve the energy efficiency of the adopted architecture.

III. Integrator and Modulator Designs

A. Conventional SAB and Passive Integrator

The SAB allows a single opamp to achieve an LF order higher than 1 in the modulator which has been widely adopted in CT $\Delta\Sigma$ modulators [13]–[17]. Fig. 3(a) shows the conventional implementation of the SAB integrator that uses a combination of active and passive circuits to achieve a 2nd-order filtering with a single amplifier. It also helps to reduce the delay introduced by the integrator, thus assuring modulator's stability [14]. However, the complex RC network not only increases design difficulty but also the sensitivity of the SAB TF coefficients under process and mismatch variations. Furthermore, no analysis can be found in the literature that discusses the opamp design constraints when comparing it with the conventional approach. In Section III-C, we will conduct such comparison based on the MATLAB behavioral model results, focusing on its bandwidth and gain specifications.

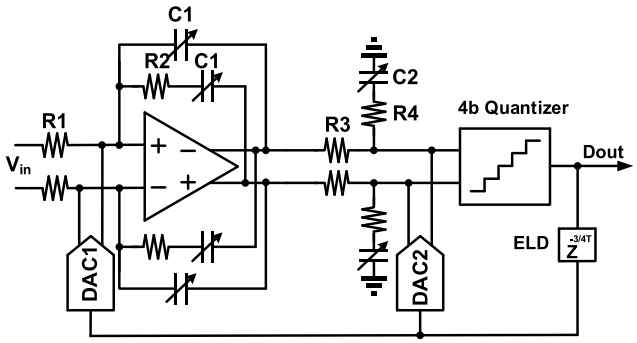

Fig. 4. Block diagram of the proposed 3rd-order ΔΣ ADC.

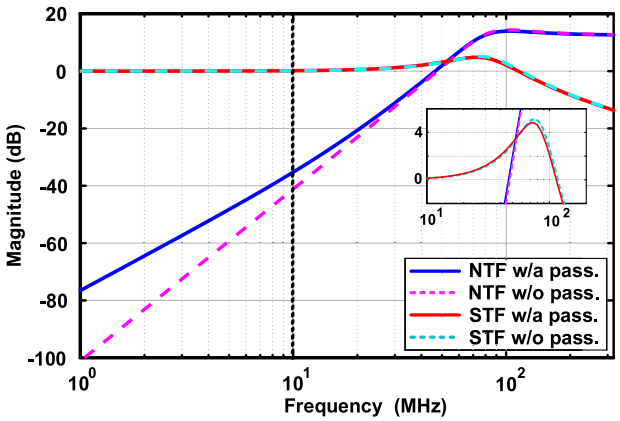

Fig. 5. STF and NTF magnitude response for 3rd-order LF, and 2nd-order LF + passive integrator.

Besides SAB, the passive filter can also enhance the LF order with a small power overhead [18], [19]. As Fig. 3(b) shows, higher order can be obtained with passive components, including resistors and a capacitor; however, such passive integrator exhibits a drawback because its TF is non-ideal which affects the inband quantization noise attenuation. We will analyze its design impact in Section III-C.

B. Proposed Modulator

The SAB jointly with the passive integrator replace the power-hungry 1st–3rd integrators from the architecture in Fig. 2. We implement the first and second integrators, as well as the first feedforward path, with an improved version of the SAB integrator. Further, the passive integrator substitutes the last integrator and the second feedforward path. Such combination enables a 3rd-order LF implementation with one opamp, thus significantly reducing the power consumed by the integrators. The passive integrator also allows ELD compensation without any active adder. Fig. 4 shows the circuit schematic of the proposed modulator with the other parts in the block format. We use non-return-to zero (NRZ) current-steering DACs (DAC1/DAC2) to alleviate the impact of the clock jitter and improve the power supply rejection ratio (PSRR). The value of the input resistor ($R1$) is determined by the noise requirement of the modulator, which simultaneously decides the conducted current of the DAC1 and capacitor loads ($C1$), implying that the value of $R1$ induces a tradeoff between the noise budget and power of the DAC and opamp. In the modulator, we choose $R1 = 1$ kΩ to balance such tradeoff with the target SNR specifications for low power. In [16], a feedback resistor is introduced to improve the SQNR by optimizing the zero in the NTF, but its induced non-shapeable thermal noise indeed yields a diminishing return on the overall SNR. The proposed SAB integrator removes the feedback resistor in the RC biquad which alleviates a non-shapeable noise source thus improving the overall SNDR of the modulator.

DAC1 and DAC2 are the main feedback and the ELD compensation DAC, respectively. We adopt an SAR architecture in the 4-bit QTZ due to its outstanding energy efficiency and no offset issue with only one comparator, which is critical in our design as the passive integrator attenuates the input swing of the QTZ to about 0.5 V_{pp}. The ELD is introduced by the QTZ and feedback path, which is caused by the sampling of the SAR QTZ and the latching operation of the main DAC. The proposed modulator also shows a strong stability even with a high out-of-band gain which benefits from the SAB together with the passive integrator, as it is detailed next.

C. Passive Integrator and ELD Compensation

Even though the passive integrator can supply extra noise shaping with little power overhead, it imposes that the TF of the LF is non-ideal as shown by the follow TF of the proposed modulator

$$H(s) = \left(\frac{\frac{1}{R_1 C_1} s + \frac{1}{R_1 R_2 C_1^2}}{s^2} + k_{\mathrm{DAC2}} \right) \times \frac{\frac{R_4}{R_3 + R_4} s + k_3}{s + k_3},$$
$$k_3 = \frac{1}{C_2 (R_3 + R_4)} \tag{1}$$

where k_{DAC2} is the feedback coefficient of DAC2. Based on (1), Fig. 5 shows the STF and NTF of the modulator with and without the passive integrator. The STF peak results from the CIFF-FB architecture, which has the feedforward path in the LF. When compared with the STF of the ideal 3rd-order modulator, the STF peak drops from 5.1 to 4.8 dB because the non-ideal effect of the passive integrator. A zero of the NTF is pushed away from DC to the left plane on the S-domain with the location of the zero determined by $k3$. It worsens the inband quantization noise attenuation of the modulator. But the influence is not significant when the bandwidth of the modulator is small. Fig. 6 shows the peak SQNR of the 2nd-order LF, 3rd-order LF, and 2nd-order LF + passive integrator modulator under various out-of-band gains. If compared with the ideal 3rd-order LF, the SQNR of the passive integrator drops from 107 to 101 dB. Such influence is negligible since our target is around 82 dB. On the other hand, the passive integrator combined with the 2nd-order LF enables an improvement of ∼10 dB in the SQNR with a small power overhead.

In the proposed modulator the passive integrator is also used as a passive adder to achieve ELD compensation. The feedback current of DAC2 is added at the output of the LF where its swing is small because of the passive integrator's attenuation.

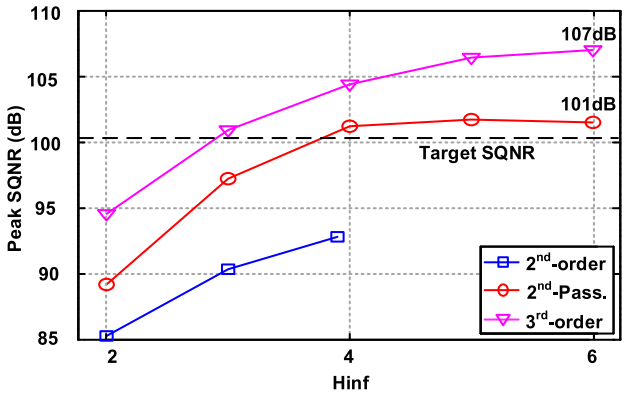

Fig. 6. Peak SQNR versus the out-of-band gain with 2nd-order LF, 3rd-order LF, and 2nd-order LF + Passive integrator.

Then, the TF of ELD compensation path can be expressed as

$$H_{\mathrm{ELD}}(s) = k_{\mathrm{DAC2}} \cdot \frac{\frac{R_4}{R_3+R_4}s + \frac{1}{C_2(R_3+R_4)}}{s + \frac{1}{C_2(R_3+R_4)}} \tag{2}$$

where k_{DAC2} is the feedback coefficient dependent on the feedback current of the current-steering DAC2 (applicable due to the small DAC2 output voltage swing and the high impedance of the current-steering DAC). In the conventional architecture, the modulator requires active components to achieve the ELD compensation [20]. Since such component has a finite bandwidth, it limits the feedback speed and raises the possibility of modulator's instability. When compared with the active structure, the passive adder proposed in this design inherently has a large bandwidth without much power overhead.

D. Noise and Distortion Considerations

In order to reach an SNDR ~82 dB, an 85-dB SNR is set as our target where 3-dB margin is reserved for the biasing circuits, off-chip clock jitter and residual DAC mismatch error. The noise contributed by $R2$–$R4$ and DAC2 is ignorable due to the high gain of the first integrator in the signal band. In this design, the noise induced by the clock jitter is greatly relaxed by the proposed DAC driver, low jitter clock receiver [21], and NRZ DAC. In CT SDMs, the clock jitter adds a random phase modulation to the feedback signal during data latching in the main DAC. Such jitter whitens the quantization noise, thus deteriorating the overall modulator resolution without experienced any noise shaping. In the RZ DAC, the amount of induced noise from the jitter is dependent on the feedback data. While it only depends on the difference between two sequential data in the NRZ DAC, its jitter sensitive is greatly reduced [1]. On the other hand, the noise from the DAC1 and the 1st opamp are very criterial since they do not experience any noise-shaped effect. When compared with the resistor DAC [12], the current-steering DAC has a better PSSR but it suffers from a large current noise density [22]. In order to suppress its noise, we use a 1.8-V power supply to improve the overdrive voltage of the current mirror. In this design, the unit current of DAC1 is 40 μA that leads to a ~90-dB SNR.

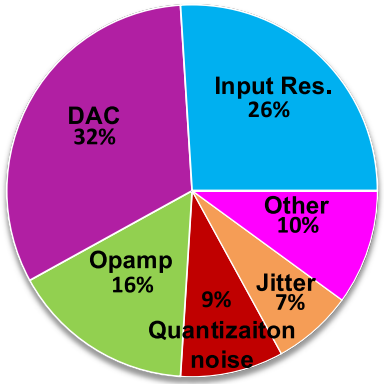

Fig. 7. Noise breakdown.

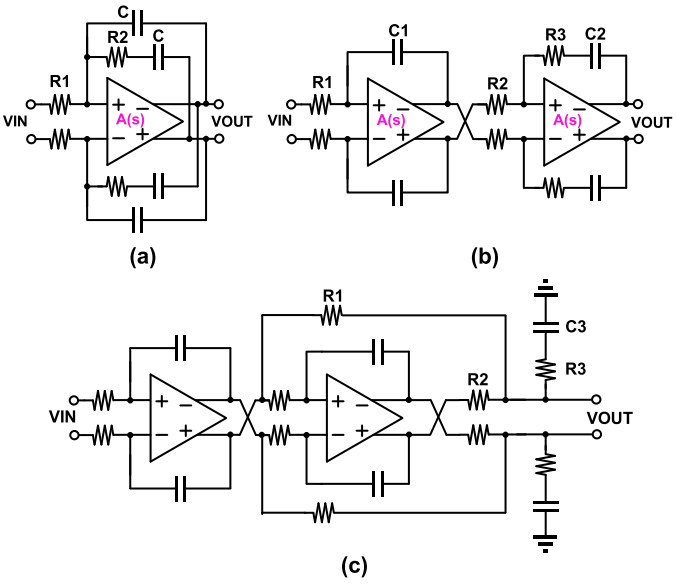

Fig. 8. (a) SAB integrator. (b) Conventional integrator. (c) Feedforward architecture with passive integrator.

The noise contribution from the 1st opamp can be reduced by enhancing the g_m of the input pair. The distortion caused by the opmap's nonlinearity can be suppressed by increasing the DC gain. In typical condition, the spurious-free dynamic range (SFDR) of our design is better than 100 dB, and its effect on SNDR is therefore negligible when considering its noise contribution. Fig. 7 gives the overall noise breakdown of the modulator. We obtain such result based on simulations without process and mismatch effect and the achieved SNR is ~85 dB that matches well with our target and the measurement result. The major sources are the main DAC and input resistor ($R1$). The input resistance ($R1 = 1$ kΩ) determined the load of the integrator, which is a tradeoff between the noise and power.

IV. Opamp Requirements and Modulator Stability

In this section, we develop an analysis to compare the opamp design requirements between the conventional and the proposed integrator. The comparison is based on the gain and bandwidth as well as the corresponding modulator stability.

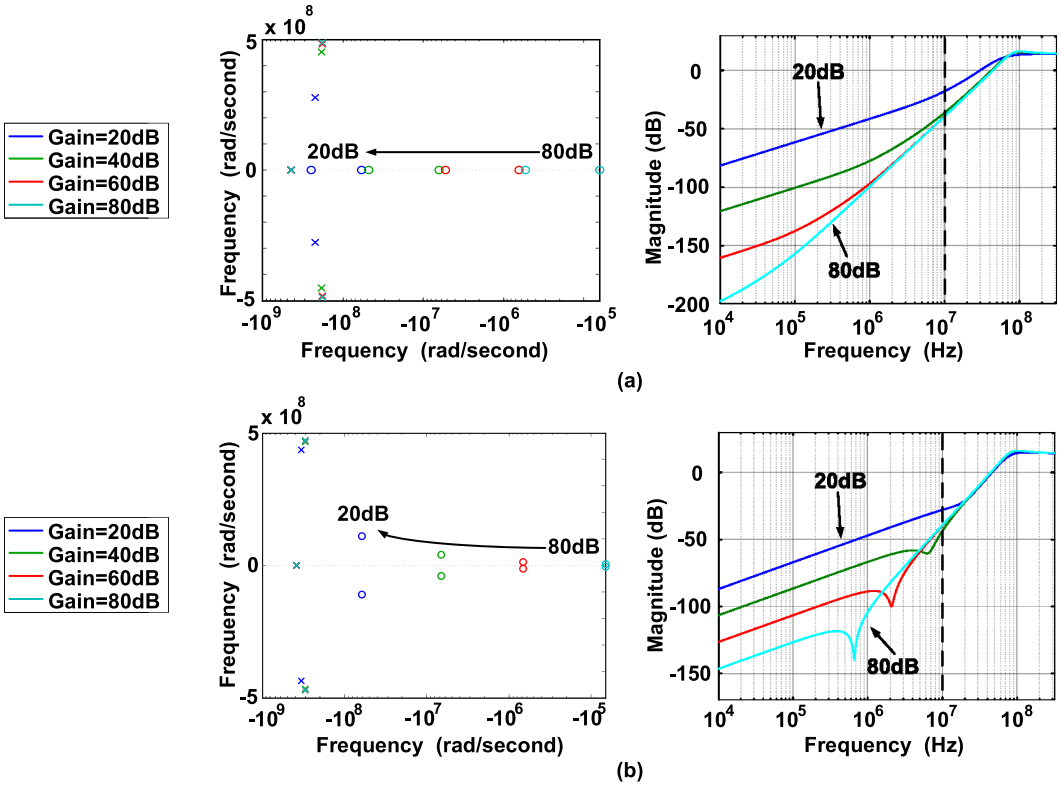

Fig. 9. Pole/zero map and NTF of (a) conventional integrator. (b) SAB integrator with finite opamp gain.

Fig. 8(a) and (b) illustrates the circuit structures of the SAB and the conventional integrators, respectively. Both the gain and bandwidth requirements comparison are based on these setups while no optimized zero is manipulated. Comparing the gain can be straight forward; however, to compare the bandwidth and the stability may be arguable as there is only one opamp in the proposed integrator. Fig. 8(c) shows a conventional feedforward architecture with passive integrator, where the 2nd opamp delay can be eliminated. Nevertheless, as the last integrator is passive and since we use the feedforward architecture, the TF of the LF will be affected which can be recognized by the following expression:

$$H(s) \propto \frac{\frac{R_1R_3}{k}s + \frac{R_1}{C_4k}}{s + \frac{R_1+R_2}{C_4k}}, \quad k = R_1R_2 + R_1R_3 + R_2R_3. \tag{3}$$

As discussed in Section III-C, the constant term of the denominator determines the non-ideal effect introduced by the passive integrator. If we compare it with the second term from (1), under the same attenuation factor (equal numerator), the zero location of the NTF is about two times farther away from DC than the proposed architecture, which worsens the inband quantization noise attenuation due to the passive integrator. Therefore, we consider the circuit of Fig. 8(b) when comparing with the conventional approach rather than the feedforward architecture.

To avoid losing the generality, we model the opamp as a single-pole amplifier and replace the following passive integrator by an ideal integrator. The transfer function (TF) of the single pole amplifier can be expressed as

$$A(s) = \frac{A_{\mathrm{DC}}}{\frac{s}{\omega} + 1}, \quad \mathrm{GBW} = \frac{A_{\mathrm{DC}}\omega}{2\pi} \tag{4}$$

where A_{DC} and ω are the open-loop gain and the dominant pole of the amplifier. We use this TF to model the opamp in Fig. 8(a) and (b). Based on the behavioral simulation results, we can obtain the impact of the opamp with finite unity gain bandwidth (UGBW) and gain in both integrators.

A. OPAMP Gain Requirement Analysis

Fig. 9(a) and (b) shows the pole/zero map and the NTF of the conventional and the SAB integrators with the finite opamp gain, respectively. In the conventional integrator, the finite gain pushes the zero away from the origin to the left-half plane which worsens the inband attenuation of the modulator [23]. Moreover, the NTF only experiences a little deviation when the gain is above the 60 dB. In the SAB integrator, as Fig. 9(a) illustrates, the zeros are also pushed away from DC whose location can be expressed by the following TF of the SAB integrator:

$$H_{\mathrm{SAB}}(s) = \frac{A}{A+1} \frac{\frac{1}{CR_1}s + \frac{1}{C^2R_1R_2}}{s^2 + \left(\frac{2}{CR_2(1+A)} + \frac{1}{CR_1(1+A)}\right)s + \frac{1}{C^2R_1R_2(1+A)}}. \tag{5}$$

Based on (4), Fig. 9(b) shows the NTF and the pole/zero map of the modulator with finite opamp gain. Different from manipulating the optimized zero in the conventional approach

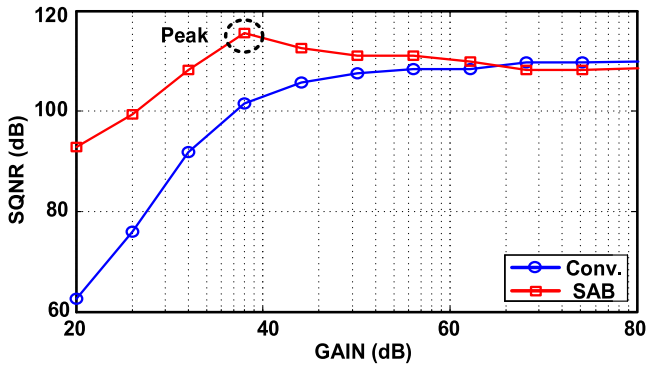

Fig. 10. Peak SQNR versus the gain of the amplifier with SAB and conventional integrator.

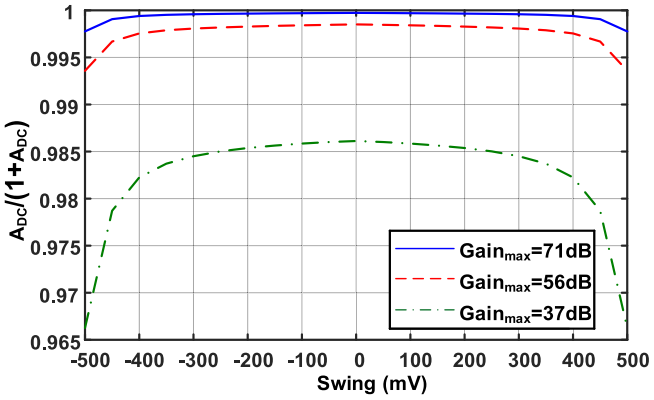

Fig. 11. The close-loop gains of the opamps with various output swings.

which requires an additional feedback resistor, these two complex zeros exist inherently in the SAB structure and are caused by the finite opamp gain. Such two inherent zeros can optimize the inband quantization noise attenuation in the modulator when the low-gain opamp is used. Fig. 10 illustrates the SQNR improvement of the SAB integrator with various gain values. The model results indicate that the peak improvement is at ∼40-dB opamp gain where the modulator also achieves the best SQNR with the SAB integrator. It is worth noting that if an optimized zero is placed with an additional feedback resistor, a similar peak SQNR can be obtained in the conventional integrator, but it induces area and noise overhead.

Nevertheless, when facing an implementation, the opamp design considerations also involve linearity. As the low-gain opamp fails to provide enough suppression on its nonlinearity, it limits the performance of the modulator through the odd-order harmonics. Fig. 11 depicts the gains of three opamps across various output swings obtained from simulations. We design these opamps with the same architecture and a similar GBW but with different open-loop gains. It is worth referring that the nonlinearity due to the gain variation can be suppressed by the open-loop gain of the amplifier, which is proportional to $A_{\mathrm{DC}}/(1 + A_{\mathrm{DC}})$. Table I shows the SFDR and SNDR of the modulator when we use these opamps. For low-gain scenarios, the SFDR determined by the HD3 limits the SNDR of the modulator.

TABLE I
SFDR AND SNDR FOR OPAMP GAIN LINEARITY

Gain(dB)	SFDR(dB)	SNDR(dB)
71	103.7	99
56	89.1	88.7
37	62.9	62.7

B. OPAMP Gain Bandwidth Product Requirement Analysis

We setup a similar comparison for the UGBW requirement of the opamp. Unlike the conventional integrator, the finite UGBW in the SAB integrator not only introduces a gain error and an additional pole, but also moves the poles from the origin to the left-half plane. The TF of the SAB integrator under the influence of the finite GBW can be written as

$$H_{\mathrm{SAB}}(s) = \frac{\frac{1}{CR_1}s + \frac{1}{C^2R_1R_2}}{s^2 + \frac{s}{GBW}\left(s^2 + \left(\frac{2}{CR_2} + \frac{1}{CR_1}\right)s + \frac{1}{C^2R_1R_2}\right)}. \quad (6)$$

Based on (5), Fig. 12(a) and (b) shows the pole/zero map and the NTF of the modulator, respectively, to analyze the influence of the finite GBW of the opamp. The decrease of the GBW pushes the location of the zero away from DC and places the poles at lower frequency which worsens the inband attenuation of the modulator. Moreover, the NTF only experiences a little deviation when the GBW is above 1.5 f_S, implying that the improvement of the inband attenuation is almost saturated. Based on the model from (3), when the GBW increases from 0.5 to 1.5 f_S, the SQNR improves by 13 dB. In addition, when the GBW is larger than 1.5 f_S, the improvements stay around only 2–3 dB. Such tradeoff between the GBW and SQNR is also similar to the conventional integrator [23] which indicates that the SAB integrator does not induce extra burden on the 1st opamp.

C. Modulator Stability Analysis

The stability of the modulator and ELD compensation are critical concerns for a high-speed modulator. To have a fair comparison between the SAB and the conventional integrator, we study the SQNR versus the opamp bandwidth with different delays for ELD compensation. As the modeling results of Fig. 13 show, if ELD is ∼0.8 Ts, the ELD compensation encounters difficulty to stabilize the modulator in the conventional integrator with <2.1 f_S opamp bandwidth. However, after ELD compensation, the modulator with the SAB integrator stays robust even when the opamp bandwidth is only ∼1 f_S. Intuitively, the reason why the SAB integrator shows a stronger stability is because there is only one amplifier in the integrator; therefore, it experiences less phase shift with higher feedback speed [14]. To obtain the target SQNR of 99 dB and compensate the 0.75 Ts ELD introduced by the SAR QTZ, we designed the opamp bandwidth as 1.5 f_S.

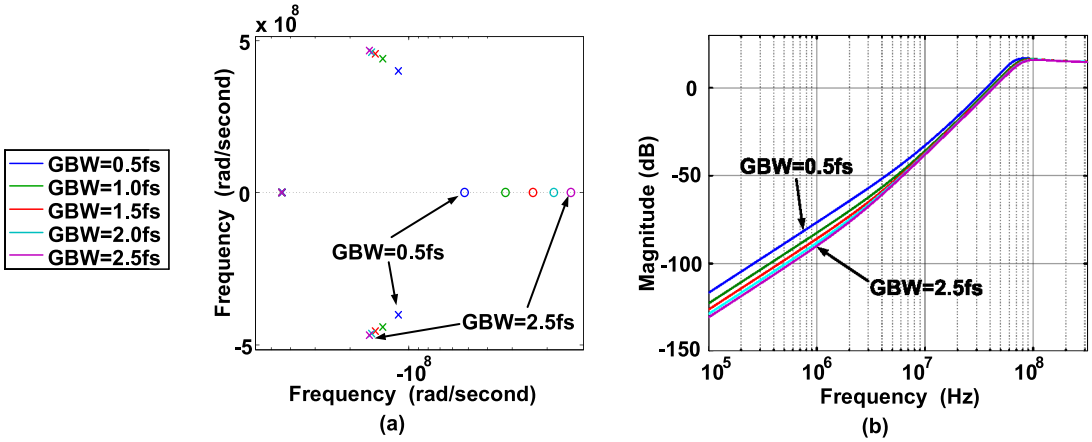

Fig. 12. Pole/zero map and NTF of SAB integrator with finite opamp bandwidth.

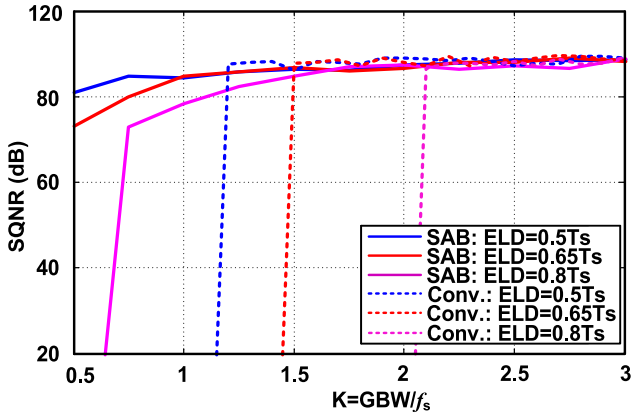

Fig. 13. Peak SQNR versus the bandwidth of the amplifier with different delays for ELD compensation in the SAB and the conventional integrator.

V. Low-Power Techniques and Circuit Implementation

Besides the architecture and the integrator optimization, we also present here some circuit techniques to further improve the energy efficiency of the modulator. In this section, we first discuss the proposed CTC opamp followed by the design of the QTZ and the DAC driver.

A. Proposed CTC Opamp and Design Considerations

From our analysis in Section IV, it can be recognized that the proposed LF does not induce extra burden in the opamp design when comparing it with the conventional approach. While reducing the number of opamps to 1 in the 3rd-order LF, the opamp becomes more critical for both the modulator performance and the power efficiency. In previous works of CT ΔΣ modulator design, the two-stage topology with feedforward path and Miller compensation techniques [15], [24] is widely adopted due to its outstanding power efficiency in a wideband design. Here, we utilize this setup as a base while applying the current-reused concept to improve both the gain and bandwidth of the amplifier. Fig. 14 shows the circuit schematic of the proposed CTC amplifier utilized in the SAB integrator. The current-reused concept was first demonstrated in [25] where the complementary switched-capacitor technique presented doubles the g_m of the 1st stage based on a DT operation. However, such technique is not applicable for the opamp in the CT LF. If M4a, b are supported by a DC biasing resistor ($R_{\rm DC}$) that replaces the CTC bias circuit in Fig. 14, the TF of the amplifier will be affected which can be recognized by the following expression:

$$\frac{V_{\rm out}}{V_{\rm in}} \propto \frac{2R_{\rm DC}+\frac{1}{sC_2}}{R_{\rm DC}+\frac{1}{sC_2}}. \tag{7}$$

A pole–zero doublet is introduced by the extra feedforward path, leading to a 6-dB loss before the zero location. The location of the pole ($-1/R_{\rm DC}C_2$) is about 2x larger than the zero ($-1/2R_{\rm DC}C_2$). In the proposed amplifier, we introduce a CTC biasing circuit which provides a feedforward path from the inputs to the push–pull pair (M4a and M4b). This helps to place the zero close to the pole for cancelling the effect of the pole–zero doublet and avoiding gain loss. We designed the power of the CTC bias circuit to be around 1/10 of the 1st stage of the amplifier such that its influence in terms of bandwidth can be negligible. Moreover, when we use larger capacitance in $C2$, the equivalent g_m of the first stage is almost twofold closer to the conventional structure but it adds additional load to the inputs. Here, $C2$ is 400 fF to balance the equivalent g_m enhancement in the first stage, the area and the extra load to the inputs.

When comparing with the conventional topology, post-layout simulation results show that the CTC structure can double the g_m of the 1st stage. Fig. 15 shows the simulated Bodeplot of both the conventional (with feedforward and Miller compensation techniques) [15], [24] and the proposed (with additional feedforward path using CTC biasing circuit) opamps. Under the same power consumption and load, the proposed amplifier has an additional 6-dB open-loop gain while the GBW extends from 629 to 827 MHz, which is limited by the non-dominant poles at high frequency and the finite value of the feedforward capacitor $C2$. The proposed topology also leads to about 10° phase margin reduction which is not significant in our design as we adopt the SAB integrator.

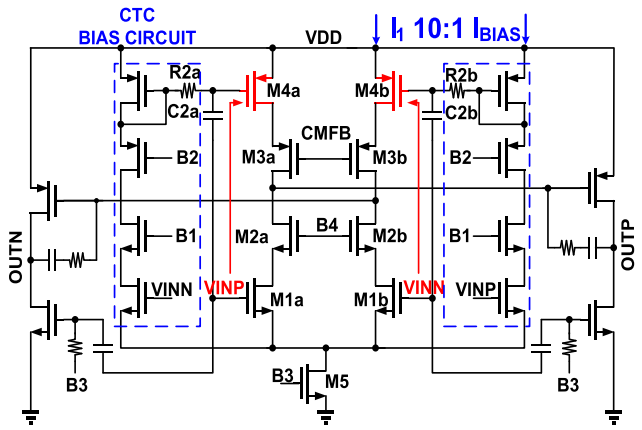

Fig. 14. Two-stage CTC feedforward amplifier.

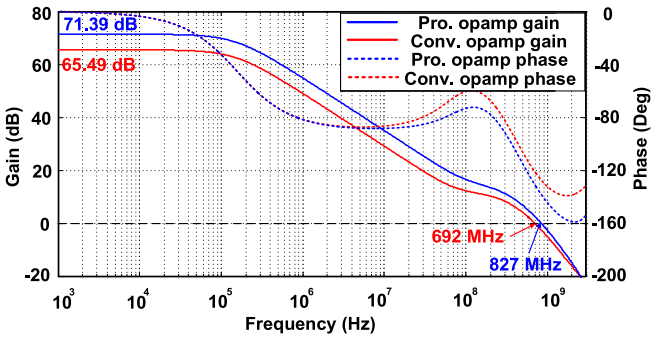

Fig. 15. Open-loop gains of the proposed and conventional opamps.

Consequently, the amplifier only consumes 1.6 mW at 1.2 V and achieves a 72-dB DC gain with a 1.5 f_S GBW.

B. DAC Driver and Feedback Timing

The feedback control of the DAC and its noise contribution has a significant impact on the bandwidth and noise performance of the modulator, respectively. Besides, the error from the DAC driver mismatch and jitter directly affect the SNDR of the modulator without noise shaping, which can dominate the overall performance as the sampling frequency is as high as 640 MHz. In order to alleviate the supply noise, we adopt a current-steering topology in the DAC. We present an advanced feedback technique, as well, which allows a fast DAC feedback speed with SAR QTZ. We also use an adaptive latch DAC driver that reduces the number of devices in the circuit feedback propagation path thus leading to a low jitter and mismatch error with low power.

Fig. 16 exhibits the DAC feedback timing and driver circuit. To avoid the inter-symbol interference (ISI) in the feedback DACs, the QTZ's outputs need to be decoded from the binary to the thermometer. However, the decoder delay can significantly prolong the feedback time that limits the overall speed of the modulator. Instead, we feedback the outputs of the SAR QTZ in a segment based where we decode the first 3 MSBs' decisions D⟨1 : 3⟩ in advance and the LSB feedback without decoding logic. Since the SAR QTZ decides bit by bit from the MSB, it permits the first few

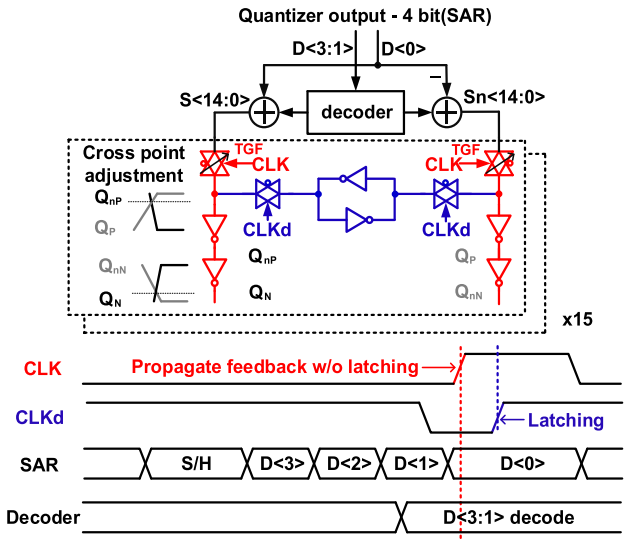

Fig. 16. Adaptive latch in the DAC driver and feedback timing.

MSBs to be decoded in advance which removes the extra timing overhead from the decoder. While the feedback of the LSB can be fast without any decoding, the decoded MSBs' decisions are ready in advance, thus enabling a fast feedback operation.

Unlike other DAC drivers [15], [26], the proposed adaptive latch driver allows the logic to propagate without involving the latch operation. During the critical signal propagation (CLKd = 0), the latch is disconnected from the feedback path and the CLK signal enables the propagation after the LSB decision from the QTZ is ready. The latch circuit resumes at CLKd = 1 after the feedback is at a steady state. The critical path of the logic propagation only consists of three gates, and it is free of the latch load. Simulations indicate that the root-mean-square (rms) jitter from the DAC driver is only ∼23.5 fs which is negligible in the overall DAC circuit, and the power of the unit cell is ∼10.64 μW when running at 640 MHz.

The DAC control signals (Q_{nP}– Q_P and Q_{nN}–Q_N) have a high and low cross-point, respectively, which are adjusted through the sizing ratio of PMOS and NMOS in the transmission gate (TGF). Those cross-points are optimized separately to avoid the switches to open simultaneously which induces the DAC dynamic error. Fortunately, when the multi-bit NRZ DAC is used and directly driven by the thermometer output of the QTZ, the total nonlinear error due to the dynamic error is first order noise shaped because it is proportional to $|D(n) - D(n-1|$.

C. ASAR-Based Quantizer

As the output swing of the LF is attenuated by the passive integrator in our design, we did not consider the Flash QTZ due to the comparator offset issue. Instead, the SAR architecture inherently avoids such problem due to the single comparator structure. To achieve a high-speed operation, an asynchronous clocking scheme is utilized with the monotonic switching procedure [27]. The dynamic offset issue is resolved due to the small input swing of the QTZ. We use the

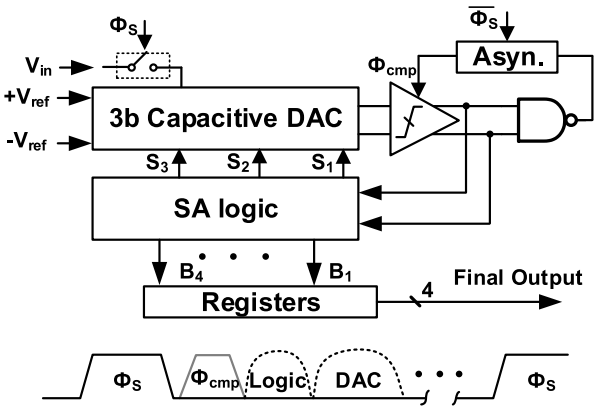

Fig. 17. Block diagram of 6-bit ASAR-based QTZ.

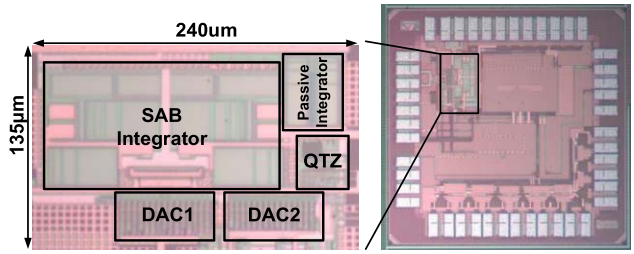

Fig. 18. Die photograph.

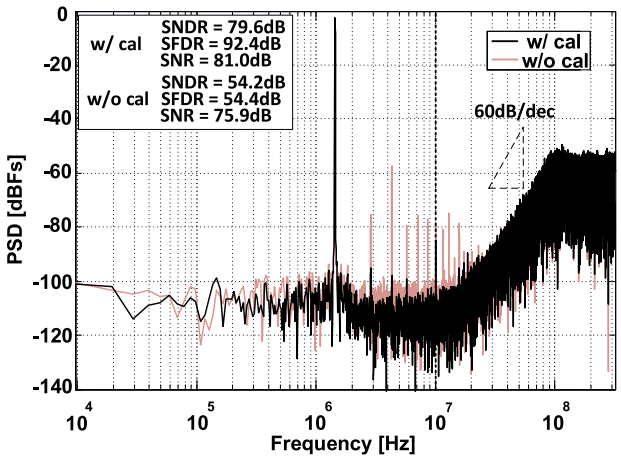

Fig. 19. Measured single-tone FFT spectrum.

dynamic control logic and custom-designed unit capacitor to further improve the power efficiency. Fig. 17 shows the block and timing diagrams of our 4-b SAR QTZ which consists of a transmission gate sampler, SAR logic, asynchronous loop control, 3-b capacitive DAC array, comparator, and register. During (Φ_S), the input (V_{in}) is first sampled with the top-plate sampling scheme. Then, the first comparison clock (Φ_{cmp}) is triggered by the falling edge of Φ_S and the SA logic controls the DAC to perform the successive approximation operation based on the comparator's decision. The following three comparisons are sequentially trigged by the previous outputs of the comparator through the asynchronous loop

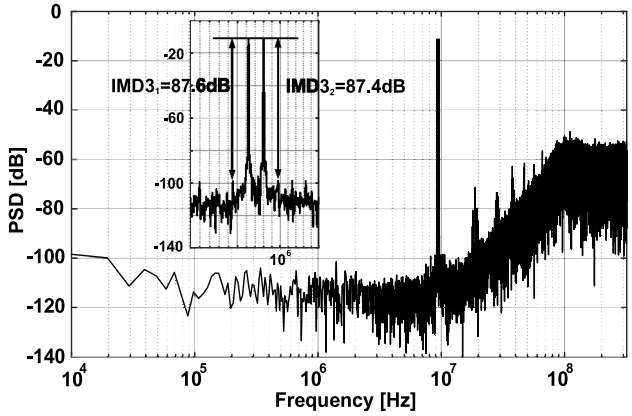

Fig. 20. Measured two-tone FFT spectrum.

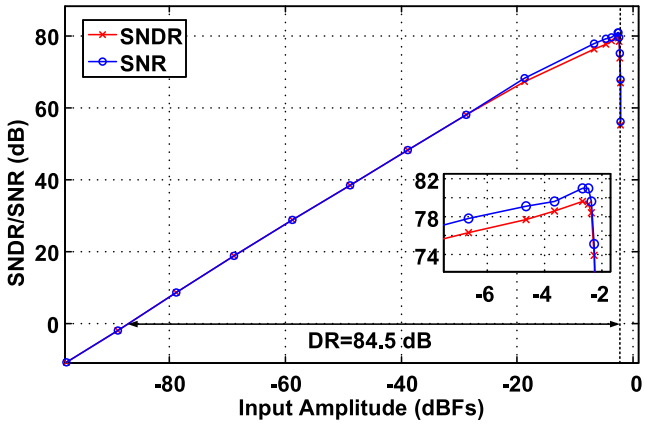

Fig. 21. SNDR and SNR versus input amplitude.

control. In total, four comparisons give 4 bits and finally the comparator's decisions are latched by the registers.

VI. Measurement Results

The CT ΔΣ modulator fabricated in 65-nm CMOS has an active area of 0.033 mm^2 as Fig. 18 illustrates. We obtained the measurement results under a 1.2-V power supply except for the DAC1 which is with a 1.8-V supply to improve its thermal noise performance. The modulator is running at 640 MHz with a signal bandwidth of 10 MHz. The OSR is 32. Fig. 19 shows the output spectrum of the modulator for a single-tone signal with −3.1 dBFS at a frequency of ∼2.05 MHz. The achieved SNDR and SNR are 79.6 and 81 dB, respectively, after the DAC mismatch calibration [28]. The SFDR is 92.4 dB, and the out-of-band harmonics are not suppressed by the calibration leading to relatively large spurs. The 60 dB/decade spectral slope validates the 3rd-order noise shaping by using the SAB and the passive integrator.

Fig. 20 presents the two-tone intermodulation distortion (IMD) measurement results. The input amplitude is −11.25 dBFS at ∼9.25 and 9.6 MHz, and we demonstrate an IMD_3 of 87.4 and 87.6 dB, respectively. Fig. 21 shows the SNR and SNDR versus the input amplitude at a 1.4-MHz input frequency, indicating that the proposed design obtains

TABLE II
SUMMARY OF PERFORMANCE AND BENCHMARK WITH STATE OF THE ART

	JSSC[3] I.Jong 2017	JSSC[7] T.Kim 2016	JSSC[9] T.Kim 2017	ISSCC[18] B.N 2016	ISSCC[29] Y.Shu 2013	VLSI[30] G.Wei 2015	JSSC[31] S.Zeller 2014	This work
Area (mm^2)	0.1	0.08	0.17	0.027	0.08	0.066	0.04	0.033
Technology (nm)	28	130	130	65	28	28	65	65
Supply Voltage (V)	1.1/1.2	1.2	1.2	1.0	1.2/1.5	0.9/1.8	1.1	1.2/1.8
Fs (MHz)	320	640	640	1000	640	432	650	640
Bandwidth (MHz)	10	10	15	10	18	5	10	10
Power (mW)	4.2	7.19	11.4	1.57	3.9	3.16	1.8	5.35
Peak SNDR (dB)	74.4	75.3	80.4	72.2	73.6	80.5	68.9	79.6
DR (dB)	80.8	78.5	82.9	77	78.1	83.9	71.2	84.5
FOMSch/SNDR (dB)	168.1	166.7	171.6	170.2	170.2	172.5	168.6	172.3
FOMSch/DR (dB)	174.5	169.9	174.1	172.0	174.7	175.9	166.0	177.2
FoMWa (fJ/conv.step)	49.0	75.9	44.1	23.6	27.7	36.5	41.4	36.5
Calibration	No	No	No	No	Yes	Yes	No	Yes

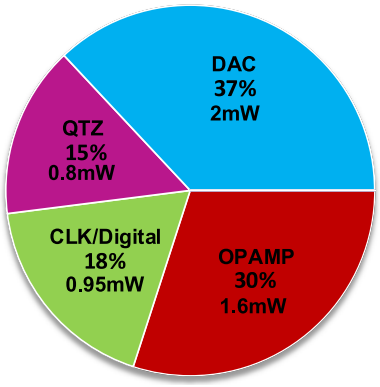

Fig. 22. Power breakdown.

a DR of 84.5 dB. Fig. 22 shows the power breakdown of the modulator. The total power consumption of the modulator is 5.35 mW, including 4.4 and 0.95 mW from the analog and digital circuits, respectively. The analog part comprises the opamp, DAC and QTZ, and the digital part includes the clock generator the digital buffer, and the control logic. The power consumption of the opamp is 1.6 mW which is only 30% of the total. Table II gives the performance summary and compares this paper with state-of-the-art CT $\Delta\Sigma$ designs under similar BW and SNDR. The prototype attains a peak SNDR of 79.6 dB and a DR of 84.5 dB, resulting in the highest Schreier FoM of 172.3 dB (SNDR) or 177.2 dB (DR), and the best Walden FoM of 36.5 fJ/conversion step.

VII. CONCLUSION

This paper presented a 3rd-order CT $\Delta\Sigma$ modulator by combining an SAB and a passive integrator. It facilitates a small area and power-efficient modulator architecture with single amplifier. The SAB realizes a 2nd-order TF with an RC network which provides 40 dB/decade slopes with little power overhead and strong stability for the non-ideal effect of the opamp. The passive integrator implements 20 dB/decade slopes with the negligible non-ideal effects and enables ELD compensation without the active adder. Moreover, in order to improve the power efficiency of the amplifier and address the jitter and switch driver mismatch in the DAC drivers, we proposed a CTC amplifier and an adaptive latch DAC driver circuit, respectively. These techniques implemented in a CT $\Delta\Sigma$ modulator achieve an SNDR of 79.6 dB and a Schreier FoM of 172.3 dB with 10-MHz signal bandwidth.

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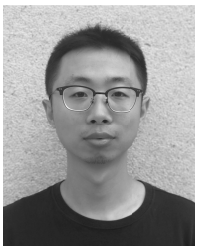

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Rui Paulo Martins (M'88–SM'99–F'08) was born in 1957. He received the bachelor's, master's, the Ph.D. degrees, and the Habilitation degree for Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering, IST, since 1980. He is currently with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macau, China, where he has been a Chair Professor since 2013. He was the Dean of the Faculty, FST, from 1994 to 1997, and he has been a Vice Rector with the University of Macau since 1997. From 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed (in 2013), as a Vice Rector (Research) until 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 45 theses, Ph.D. (24), and Masters (21). He has co-authored seven books, 11 book chapters, 442 papers, in scientific journals (141) and in conference proceedings (301), and other 64 academic works, in a total of 554 publications. He holds 30 patents, USA (28) and Taiwan (2). He was a Co-Founder of Synopsys, Macau, from 2001 to 2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in 2011 to the State Key Laboratory of China (the 1st in Engineering in Macau), being its Founding Director.

Dr. Martins was a Founding Chairman of both IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 (2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was a General Chair of the 2008 IEEE Asia-Pacific Conference on CAS—APCCAS'2008, and was a Vice President of Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. Since then, he was a Vice President (World) of the Regional Activities and Membership of IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated Best Associate Editor of T-CAS II from 2012 to 2013. In addition, he has been a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019, and the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016 and received the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016. He was a Nominations Committee Member of the IEEE CASS in 2016, and he was the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration) in 1999 and the Honorary Title of Value from Macao SAR Government (Chinese Administration) in 2001. In 2010 was elected, unanimously, as Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia.