Design and Experimental Verification of a Power Effective Flash-SAR Subranging ADC

U-Fat Chio, *Student Member, IEEE*, He-Gong Wei, *Student Member, IEEE*, Yan Zhu, *Student Member, IEEE*, Sai-Weng Sin, *Member, IEEE*, Seng-Pan U, *Senior Member, IEEE*, R. P. Martins, *Fellow, IEEE*, and Franco Maloberti, *Fellow, IEEE*

***Abstract*—This brief presents the architectural concept of an optimal subranging ADC, obtained with the cascade of a Flash and a SAR, which is also explored through its practical design and experimental confirmation. The solution doubles the optimal speed of operation of the SAR ADCs at the relative low power cost of a low-resolution Flash. The digital correction method and a capacitor-based DAC ensure nondemanding requirements for the Flash. The effectiveness of the architecture is verified in a 90-nm CMOS chip whose active core area is 0.64 mm^2. The ADC obtains a peak SNDR of 51.8 dB and SFDR of 63.4 dB at 90 MS/s consuming 13.5 mW from a 0.9-V supply. Measured DNL and INL are 0.87 LSB and 1.55 LSB, respectively.**

***Index Terms*—Analog-to-digital converter (ADC), digital error correction (DEC), Flash ADC, SAR ADC, subranging ADC.**

I. Introduction

THE FAST shrinking of CMOS process technologies increases silicon capacity, diminishes supply voltage, allows higher complexity, boosts operating speed, and reduces power. However, low voltage challenges high-performance analog interfaces, especially analog-to-digital converters (ADCs).

This brief addresses the requisite of architectures that demand moderate resolution and high sampling rate ADCs [1]–[3]. Examples are handheld equipments for wireless like WIFI (IEEE 802.11) and WIMAX (IEEE 802.16) or cellular communication systems like WCDMA, CDMA2000, and TD-SCDMA. Since portable terminals demand long battery-operating times, the optimal ADC must be power efficient in terms of low supply voltage. SAR ADCs, mainly used for low-speed applications [4], execute quite efficiently the quantization at low supply voltage. Plus, technology evolution enables the speed enhancement because comparators are faster and digital logics complete the SAR algorithm quicker. Therefore, it is possible to obtain medium-resolution converters at high speed with very high power efficiency.

Manuscript received July 28, 2009; revised December 5, 2009 and February 25, 2010; accepted April 1, 2010. Date of publication June 28, 2010; date of current version August 13, 2010. This work was supported by Research Grants from University of Macau and Macao Science and Technology Development Fund (FDCT). This paper was recommended by Associate Editor J. Li.

U-F. Chio, H.-G. Wei, Y. Zhu, S.-W. Sin, and S.-P. U are with the Analog and Mixed-Signal VLSI Laboratory, Faculty of Science and Technology, University of Macau, Macao, China (e-mail: alpha.ufc@ieee.org).

R. P. Martins is with the Analog and Mixed-Signal VLSI Laboratory, Faculty of Science and Technology, University of Macau, Macao, China, and also with the Instituto Superior Técnico, TU of Lisbon, 1049-001 Lisboa, Portugal (e-mail: rmartins@umac.mo).

F. Maloberti is with the Department of Electronics, University of Pavia, 27100 Pavia, Italy (e-mail: franco.maloberti@unipv.it).

Digital Object Identifier 10.1109/TCSII.2010.2050937

The optimum speed of SAR converters is controlled by the single-bit time conversion that for a given technology and resolution, achieves maximum power effectiveness. For example, the 90-nm CMOS technology permits the design of 9-bit SAR with 50 MHz conversion speed [5]. Above that limit, it would be necessary to use more ingenious circuit schemes.

The Flash converter is normally viewed as a power hungry solution because it requires a number of comparators that increase exponentially with the number of bits. However, the power consumed by comparators is only large at very high speed and high resolution. For medium resolution (e.g., 5-bit), the power requested is relatively low if the speed is not very high; consequently, preamplifiers do not need a large gain.

This brief verifies on silicon with experimental results a power effective subranging ADC architecture that uses a 5-bit Flash as the first stage and a 5-bit SAR as the second stage. Digital error correction (DEC) brings the resolution to 9-bit. The brief is organized as follows. Section II introduces the principles for a wise architectural choice leading to high speed and medium-to-high resolution. Thereafter, the proposed architecture of a Flash-SAR subranging ADC (hereafter abbreviated as FL-SA ADC) is presented. Section III describes the 90-nm CMOS circuit implementation. Section IV reports the experimental results. The conclusions are drawn in Section V.

II. Choice of Architecture

A/D conversion is obtained with many algorithms. For obtaining power effectiveness, what often matters is not inventing new methods but finding the best use of known algorithms and achieving the optimum for the foreseen technology and the given specifications. High speed and medium-to-high resolution normally call for pipeline, two-step, or subranging schemes. The basic building blocks are the track-and-hold, the comparator, and the op-amp.

With medium resolution, the input track-and-hold is a source follower with passive sampling. Clock feedthrough is minimized with dummy elements and body effect is cancelled out by connecting the source and substrate. The power depends on the capacitive load that, in turn, is proportional to the number, N, of comparators served by the T&H. Since g_m/C_L is the relevant parameter, the power increases with the square of N.

The power of the comparator depends on the resolution. For several tens of mV, just a latch makes the comparator. For resolutions from ten to few tens of mV, however, it is necessary to use a simple preamplifier before the latch. With resolutions below 10 mV, on the other hand, the preamp gain must be relatively large with the need of auto-zero or calibration techniques to keep the offset below the resolution [6].

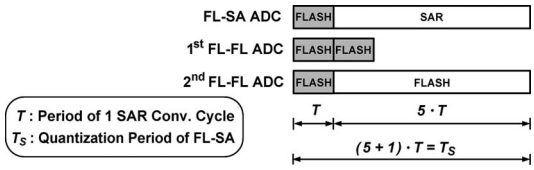

Fig. 1. Timing definition of the proposed FL-SA and FL-FL ADCs.

In general, the power consumption of an op-amp is high, equivalent to the amount drawn by several comparators (about 10 or even more), which is traded for the fast settling and high accuracy of the residue generation in the pipeline schemes. A quantitative comparison between architectures must take into account the effective power consumed by the building blocks. For 90-nm CMOS technology, all architectures with one or more op-amps are power expensive. Even if the op-amp can be scaled along the pipeline, the quantitative estimation for various pipeline architectures leads to large power, and the same applies to the two-step scheme. Thus, we focused on the subranging scheme without the residue amplifier.

Typical subranging ADCs [7] do not generate the residue, but they identify a set of fine references around the range of the sampled input voltage to convert the fine code. The fine reference voltages for the fine comparators are connected through the MUX switches to the appropriate internal tap points within the selected coarse segment of the reference ladder by the quantized coarse code. As a result, a large fan-out of the MUX switches is required, and they may cause large parasitic, limiting the speed of quantization. Based on this, we choose to quantize the fine code through the residue generated by the subtraction of the held input, in the capacitive DAC array, following the principle of switched-capacitor charge redistribution.

Three different schemes of subranging ADC with 9-bit $(10-1$ bit for digital correction) and an expected sampling rate of 90 MS/s were compared. Two of the schemes use the cascade of two Flashes (FL-FL) and the third is a Flash plus a SAR (FL-SA), whose timing definition is shown in Fig. 1. The first FL-FL scheme utilizes the same time for the two Flashes, and then the quantization period of the first scheme becomes $2 \cdot T = T_{\rm S}/3$, where T and $T_{\rm S}$ represent the period of one SAR conversion cycle and the quantization period of FL-SA, respectively. In addition, the second FL-FL scheme employs a longer conversion time in the second-stage Flash (same as the SAR). As the second-stage Flash requires a much higher resolution than the first-stage, even with the digital correction technique, the overall energy efficiency can be improved by allowing a longer conversion time to balance the power consumption in the two stages.

The power estimation performance uses heuristic equations that account for the power of the T/H, the comparators, and the resistive reference generator. Speed-accuracy prerequisites impose specific values for the transconductances, which provide the transistor bias currents assuming a given overdrive voltage $(I_D = g_m V_{\rm ov}/2)$. The results summarized and shown in Fig. 2 show that the FL-SA scheme obtains the best performances, even if only the comparators' energies are counted in the FL-FL ADCs. The power of FL-SA ADC has its minimum with both 5-bit in the Flash and the SAR, where the architecture's advantage is manifest for the used technology and given specifications. However, different conditions possibly favor other schemes. Actually, this is what happens with more traditional schemes enjoying a given optimum range of utilization.

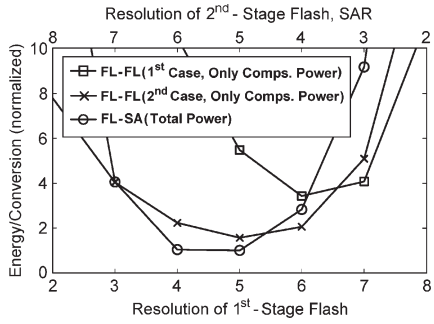

Fig. 2. Theoretic energy versus resolution division of proposed 9-bit FL-SA ADC and FL-FL ADCs (All normalized to a 5-bit first-stage Flash, 5-bit SAR level).

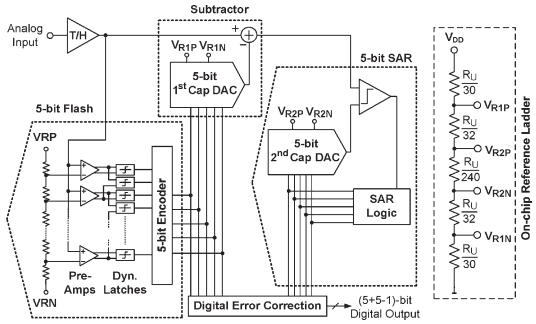

Fig. 3. Block diagram of the $(5+5-1)$-bit Flash-SAR subranging ADC.

III. Architecture Description

The result of the previous section leads to the architecture of Fig. 3, which is a $(5+5-1)$-bit FL-SA ADC. It includes a 5-bit first-stage Flash ADC, a 5-bit first-stage DAC (first-DAC), a 5-bit second-stage SAR ADC with an embedded N-bit second-stage DAC (second-DAC), a front-end track-and-hold amplifier (T/H), which samples the input signal for both Flash and SAR, and an on-chip reference ladder to charge/discharge the first-DAC and the second-DAC.

The digital error correction relaxes the requirement of Flash comparators in the coarse stage. Moreover, the offset of the SAR comparator is not critical as it is just required not to saturate the quantization range in the fine stage. Accordingly, the largest error allowed for the FL-SA ADC to tolerate the Flash and SAR comparators' offsets with 1-bit overlap in the digital error correction is given by

$$\varepsilon_{FL-SA} = \sqrt{\varepsilon_{FL}^2 + \varepsilon_{SA}^2} = \frac{V_{FS}}{2^{5+1}} \tag{1}$$

where V_{FS} is the dynamic range of the FL-SA ADC and ε_{FL} and ε_{SA} are the random offset errors of Flash and SAR comparators, respectively. If the Flash and SAR comparators are designed with the same matching tolerance, i.e., $\varepsilon_{FL} = \varepsilon_{SA}$, then the largest offset of Flash and SAR comparators can be given by

$$\varepsilon_{FL} = \varepsilon_{SA} = \frac{V_{FS}}{\sqrt{2} \cdot 2^{5+1}}. \tag{2}$$

To quantify the power consumption and performance of the FL-SA scheme of Fig. 3, its building blocks have been designed

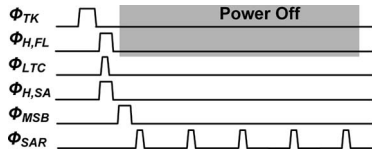

Fig. 4. Clock diagram of the proposed FL-SA ADC.

assuming a 0.9-V supply voltage, 9-bit resolution, and 90 MS/s sampling rate. The technology used in the implementation is a conventional 90-nm CMOS process with multiple metal and MiM capacitors. The design details of this technology is presented next.

A. Clock Diagram

The proposed converter is controlled by 6 phases generated from a main clock, as shown in Fig. 4. The phase, Φ_{TK}, determines the tracking of the input voltage. It is followed by the hold, during $\Phi_{H,FL}$, for the Flash section. The phase Φ_{LTC} drives the latches of the Flash. $\Phi_{H,SA}$, that coincides with $\Phi_{H,FL}$, and stores the held input signal on the first-DAC. During Φ_{MSB}, the held input is subtracted to generate the residue on the first-DAC by the coarse 5-bit MSB from the Flash. Finally, Φ_{SAR} controls the SAR operation. The signal from the track-and-hold is not necessary after the storing of the held signal on the Flash section and first-DAC, so it is switched off for sparing power. The clock generator uses a suitable inverter chain to get the main phases and consumes a reduced amount of power.

B. Track-and-Hold Amplifier

A T/H suitable for this design is the power-scalable proposed in [8]. It includes an adaptive power controller for regulating its bias current. It is also used to avoid drawing static power when the T/H is idle during the SAR conversion phase. Since the T/H's working time frame is much smaller than the whole conversion period, the method allows large power savings. The value of the sampling capacitor C_S is 500 fF to render the kT/C noise contribution negligible. The bandwidth of the T/H is optimized to drive about 2 pF loading capacitance, which is equivalent to the first-DAC capacitive array and the input parasitic capacitance of the Flash comparators.

C. Flash ADC

A well-known technique that allows minimum power is interpolation, which is used in the 5-bit Flash that employs 16 preamplifiers with 32 interpolating dynamic latches, as shown in Fig. 5. The preamplifier of Fig. 6(a) is a single-stage differential amplifier with resistive load. The preamplifier, whose gain is around 10, is used also for limiting the kickback of the cascaded dynamic latch [9], as shown in Fig. 6(b). The converter uses auto-zero [6] to reduce the comparators' offsets and to keep the common-mode voltage of the preamplifier input at an optimum value. As mentioned in Section II, the largest offset allowed for the Flash and SAR comparators with 1-bit overlap in the digital error correction is 6-bit. The transistors' dimensions in the comparators are designed to suppress sufficiently the dominating offset, implying that these will be also insensitive to the input-referred noise. Each dynamic latch in the Flash is connected with a NAND-gate based SR latch to lock quickly the regenerated output from the comparator. Bubble error correction logic removes sparkles from the thermometer code. Finally, there is a thermometer-gray-binary encoder to transform the thermometer code to a 5-bit binary code.

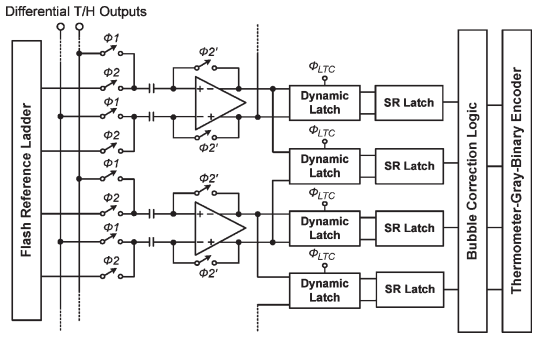

Fig. 5. Interpolated comparators with input auto-zeroing and encoding circuits in the Flash implementation.

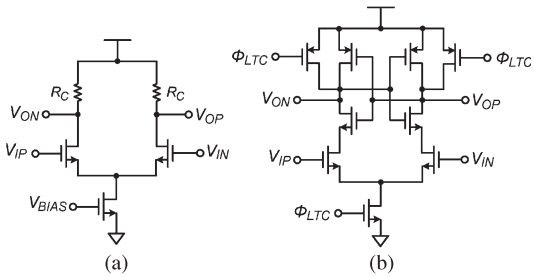

Fig. 6. (a) Resistive-loaded preamplifier. (b) Dynamic latch.

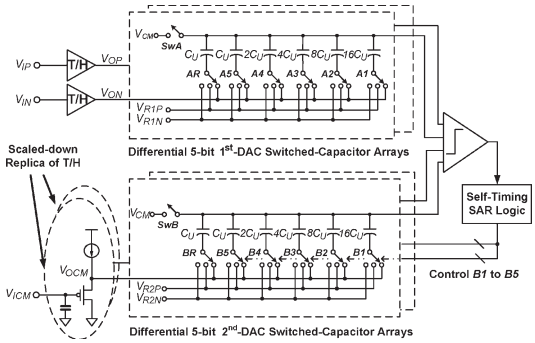

Fig. 7. Capacitor arrays of the first-DAC and second-DAC.

D. Residue Processing and Capacitive DAC Arrays

After determining the MSB, it is necessary to generate the residue from subtracting the held input, which can be obtained from the first-DAC of Fig. 7 that is capacitance-based and uses the charge redistribution principle. The second-DAC (also capacitance-based) operates together with the SAR to approximate the residue into the fine code. Both DACs are differential, binary-weighted capacitor arrays. The value of the unit capacitance C_{U} is 50 fF, which is enough to render the kT/C noise negligible. Moreover, the total capacitance of the first and second differential DACs is 6.4 pF. The simulation result shows that the matching between the capacitive DACs approached a 10-bit resolution. The capacitor arrays of the two DACs, shown in Fig. 7, use two different differential pairs with reference

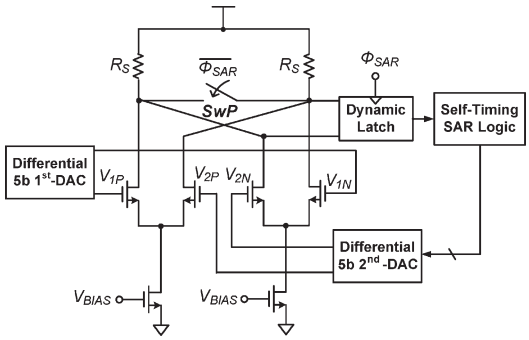

Fig. 8. Four-input fully-differential comparator of the SAR.

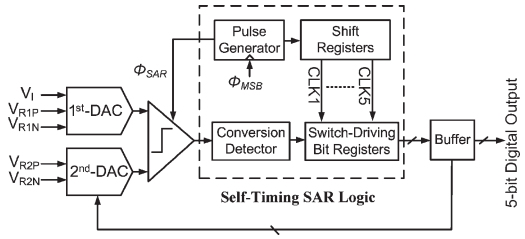

Fig. 9. Self-timing SAR logic implementation.

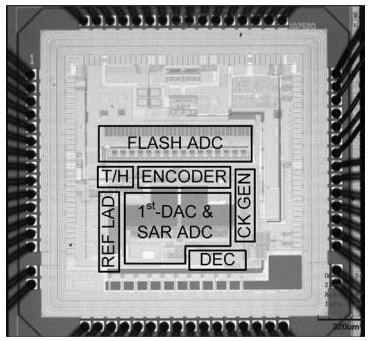

Fig. 10. Chip micrograph.

voltages V_{R1P}, V_{R1N}, V_{R2P}, V_{R2N}, which are provided by the same on-chip reference ladder, avoiding the division error between two sources of reference generation. In fact, each tap resistor of the ladder is paralleled by a great quantity of large-size ($2\ \mu\text{m} \times 10\ \mu\text{m}$) unit resistors R_U (shown in Fig. 3) to diminish the process mismatch. Thus, the precision of the on-chip reference ladder has been designed to surpass 10-bit. The references V_{R1P} and V_{R1N} for the first-DAC are equal to those used in the Kelvin divider of the Flash. Since the references V_{R2P} and V_{R2N} for the second-DAC must resolve the last 5-bit, their values correspond to 1/16 of the dynamic range. Besides, the analog switches are implemented with the Standard-V_T PMOS and NMOS transistors in a CMOS configuration and their dimensions are designed large enough to minimize the on resistances.

The reset of the capacitive array of the second-DAC occurs at $\Phi_{H,SA}$ when the capacitive array of the first-DAC samples the input. The operation is done through a replica of the T/H scaled to match the loads. The choice equalizes the sampling conditions of the first-DAC and the second-DAC. Also, the voltage V_{ICM} (provided off-chip) at the input of the scaled T/H should give an equal output common-mode voltage V_{OCM} to the main T/H.

E. SAR ADC

In the proposed FL-SA A/D converter, the SAR must convert the difference between the second-DAC and the first-DAC used to generate the residual. The difference is performed at the input of the SAR comparator that uses four input terminals, as shown in Fig. 8. There are two differential pairs with resistive loads to implement the preamplifier, and its outputs drive the dynamic latch. A switch SwP resets the preamplifier every successive approximation cycle and the operation recovers from overdrive and eliminates the memory effect. The two differential input pairs of the preamplifier are connected to the top plates of the differential first-DAC and second-DAC. Then, the equivalent input voltage of the preamplifier becomes $(V_{1P} - V_{1N}) - (V_{2P} - V_{2N})$, where $V_{1P} - V_{1N}$ is the subtracted residue of the coarse step and $V_{2P} - V_{2N}$ is the successive approximated voltage of the SAR from bit-cycling.

F. Self-Timing SAR Logic and Digital Output

The SAR operates with a self-timing control. The self-timing SAR logic provides the command to the comparator when the bit is likely determined. This avoids the extra clock for the phase Φ_{SAR} but just uses Φ_{MSB} to trigger and start the SAR operation. Therefore, the scheme of Fig. 9 uses a pulse generator, shift registers, a conversion detector, and bit registers to obtain the self-timing SAR logic. After the coarse quantization by the Flash, the pulse generator, which is a self-trigger inverter chain loop, produces the self-timing strobe phase Φ_{SAR} and activates the shift registers to generate multiple shifted clocks CLK1 to CLK5, switching the bit registers. The pulse generator was tested with a process corner simulation to verify its circuit function.

The self-timing operation can be impaired by a possible meta-stability of the comparator. To avoid this effect, the pulse generator is made independent of the SAR comparator output by using the conversion detector described in [10]. The circuit verifies a meta-stability state of the comparator and, in case there is a meta-stable condition, it brings high the output of the conversion detector. This does not correspond to an error because it is supposed that the input is close to the threshold by less than half LSB. The solution is different from the asynchronous scheme used in [11], where each asynchronous bit-cycling clock phase is generated by the preceding bit comparison. Exactly, the asynchronous clock phase generation from [11] is triggered through the NAND gate of the comparator differential output while there is a decision in the comparator. However, there is a risk of the NAND gate not being able to provide a transfer condition while the comparator's outputs appear to be the same in a meta-stability state. As a result, the following bit-cycling clock phases of the comparator become weaker and weaker; worse, it can even vanish once the comparator is meta-stable.

The results of each SAR cycle are stored in the switch-driving bit registers [10]. The block also ensures a fast charging path from the comparator to the second-DAC. The final SAR registers contents are used for digital error correction and are combined with the MSB to build the overall output code.

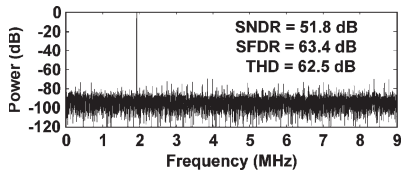

Fig. 11. Measured FFT spectrum at $f_{in} = 1.9$ MHz (decimated by 5).

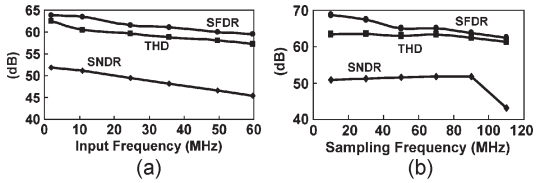

Fig. 12. Measured SNDR, SFDR and THD (a) versus input frequencies at $f_S = 90$ MHz. (b) versus sampling frequencies at $f_{in} = 1.9$ MHz.

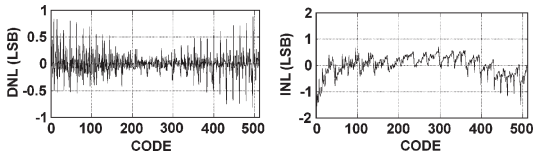

Fig. 13. Measured DNL/INL.

IV. Experimental Verification

The proposed FL-SA ADC was simulated and fabricated in a 90-nm single-poly 9-metal (1P9M) CMOS process and the chip micrograph is shown in Fig. 10. The active core area of the circuit is 0.64 mm^2. The reference ladders of the ADC are implemented with nonsilicide P+poly resistor. The routing wires connecting unit capacitors are laid out symmetrically to balance parasitic capacitances. The layout uses inter-digitized and common-centroid techniques [6]. Moreover, the signals travel over balanced fully-differential paths throughout the entire chip.

The measurements show that the converter works properly as predicted in the design, especially when consuming the expected power, and it is fully functional up to 9-bit 90 MS/s while operating with a 0.9-V supply. Fig. 11 shows the output FFT spectrum for a 0.9 $V_{\mathrm{p-p}}$ 1.9 MHz input signal while the peak SNDR/SFDR and THD are 51.8/63.4 dB and 62.5 dB, respectively. Fig. 12(a) and (b) shows the measured SNDR, SFDR, and THD versus input and clock frequencies. The curves, meanwhile, show that the effective resolution bandwidth (ERBW) is about 30 MHz. Fig. 13 shows the measured static performance where the DNL is 0.87/$-$0.81 LSB and the INL is 0.71/$-$1.55 LSB. The result corresponds to the expected matching accuracy of the used unit capacitors in the SAR converter. The total dissipated power of the prototype ADC is 13.5 mW while the T/H consumes 2.5 mW. The Flash consumes 4.3 mW (Flash comparators take around 3.5 mW), the SAR consumes 1.2 mW (SAR comparator around 0.6 mW), the clock generation consumes 0.5 mW, and the on-chip reference ladder consumes 5 mW.

Table I shows the performance summary and comparisons with the state-of-the-art pipelined and subranging ADC designs [1]–[3], [7] with similar specifications. The design from [3] was implemented with a 65 nm HPA CMOS process (High Performance Analog - special option).

TABLE I
Performance Summary and Comparisons

	ISSCC'07 [1]	CICC'07 [2]	ISSCC'08 [3]	ISSCC'08 [7]	This Work
CMOS Process	90 nm	0.13 μm	65 nm (HPA)	90 nm	90 nm
Resolution	10-bit	10-bit	10-bit	8-bit	9-bit
Speed	80 MS/s	60 MS/s	100 MS/s	300 MS/s	90 MS/s
DNL/ INL	0.8/1.0 LSB	0.35/0.49 LSB	0.1/0.2 LSB	N/A	0.87/1.55 LSB
SNDR	55 dB	56 dB	59 dB	46.3 dB	51.8 dB
Supply Voltage	0.8 V	0.8 V	1.2 V	1.2 V	0.9 V
Input Range	1.2 V_{p-p}	0.8 V_{p-p}	1 V_{p-p}	1.4 V_{p-p}	0.9 V_{p-p}
Power	6.5 mW	19.2 mW	4.5 mW	34 mW	13.5 mW
FOM_1= P /(2^{ENOB}·f_S)	200 fJ/conv.	625 fJ/conv.	62 fJ/conv.	680 fJ/conv.	472 fJ/conv.
FOM_2= P /(2^{ENOB}·2·*ERBW*)	280 fJ/conv.	1.12 pJ/conv.	70 fJ/conv.	780 fJ/conv.	700 fJ/conv.

V. Conclusion

The competitive power consumption performance of a SAR architecture has been extended with a subranging architecture using a Flash in front of the SAR. The SAR speed limit doubles by reducing the accuracy from 9 bit to 5 bit. The overall resolution is then restored by a 5-bit Flash. The use of the digital correction technique costs one bit but relaxes the specifications of the Flash. The experimental verification of this design demonstrates the following benefits: low supply voltage, 0.9 V, reaching 9-bit at 90 M/s Nyquist ADC with a conventional 90-nm CMOS technology and total power consumption as low as 13.5 mW. The Figure-of-Merits (FOMs), defined as $FOM_1 = \mathrm{Power}/(2^{\mathrm{ENOB}} \cdot f_S)$, is 472 fJ/conversion and $FOM_2 = \mathrm{Power}/(2^{\mathrm{ENOB}} \cdot 2 \cdot ERBW)$ is 700 fJ/conversion.

Acknowledgment

The authors would like to thank the Associate Editor and anonymous reviewers for their insightful comments and suggestions.

References

[1] M. Yoshioka, M. Kudo, T. Mori, and S. Tsukamoto, "A 0.8 V 10 b 80 MS/s 6.5 mW pipelined ADC with regulated overdrive voltage biasing," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 452–453.

[2] Y. J. Kim, H. C. Choi, S. W. Yoo, S. H. Lee, D. Y. Chung, K. H. Moon, H. J. Park, and J. W. Kim, "A re-configurable 0.5 V to 1.2 V, 10 MS/s to 100 MS/s, low-power 10 b 0.13 μm CMOS pipeline ADC," in *Proc. CICC*, Sep. 2007, pp. 185–188.

[3] M. Boulemnakher, E. Andre, J. Roux, and F. Paillardet, "A 1.2 V 4.5 mW 10 b 100 MS/s pipeline ADC in a 65 nm CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 250–251.

[4] M. Elzakker, E. Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9 μW 4.4 fJ/conversion-step 10 b 1 MS/s charge-redistribution ADC," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 244–245.

[5] J. Craninckx and G. Van der Plas, "A 65 fJ/conversion-step 0-to-50 Ms/s 0-to-0.7 mW 9 b charge-sharing SAR ADC in 90 nm digital CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 246–247.

[6] F. Maloberti, *Data Converters*. Berlin, Germany: Springer-Verlag, 2007.

[7] Y. Shimizu, S. Murayama, K. Kudoh, and H. Yatsuda, "A split-load interpolation-amplifier-array 300 MS/s 8 b subranging ADC in 90 nm CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 552–553.

[8] H. G. Wei, U-F. Chio, Y. Zhu, S. W. Sin, S. P. U, and R. P. Martins, "A power scalable 6-bit 1.2 GS/s flash ADC with power on/off track-and-hold and preamplifier," in *Proc. IEEE ISCAS*, May 2008, pp. 5–8.

[9] L. Sumanen, M. Waltari, and K. Halonen, "A mismatch insensitive CMOS dynamic comparator for pipeline A/D converters," in *Proc. IEEE ICECS*, Dec. 2000, pp. I-32–I-35.

[10] U-F. Chio, H. G. Wei, Y. Zhu, S. W. Sin, S. P. U, and R. P. Martins, "A self-timing switch-driving register by precharge-evaluate logic for high-speed SAR ADCs," in *Proc. IEEE APCCAS*, Dec. 2008, pp. 1164–1167.

[11] M. S. Chen and R. W. Brodersen, "A 6b 600 MS/s 5.3 mW asynchronous ADC in 0.13 μm CMOS," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2006, pp. 574–575.