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A Three-Level Soft-Switching Active Power Filter with DC Self-Balancing Capability

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Abstract – *The three-level neutral-point-clamped (NPC) inverter was applied in active power filters (APFs). The three-level NPC inverter has the structure of split dc capacitors. So the existing dc neutral point can be directly utilized as the ground return in a three-phase four-wire system. DC bus voltage unbalance has been one of the major problems of three-level NPC inverters. In addition, high voltage and current stresses during switching cause higher system losses and lower efficiency. In this paper, a generalized three-level quasi-resonant dc-link (QRDCL) inverter is proposed, which has both the soft-switching and dc voltage self-balancing capabilities. The switching sequence for all the power switches in the proposed three-level QRDCL inverter is designed. The inverter is controlled by the 3-dimensional direct pulse width modulation with embedded auxiliary switches triggering. The proposed generalized three-level QRDCL inverter is applied in a three-phase four-wire APF. Simulation results and experimental results verified that the proposed system can achieve dc-link balance and switching losses reduction simultaneously. The efficiency of the proposed active power filter is improved and the high voltage stress during switching is released.*

Keywords: *Active Filters, DC Unbalance, Quasi-Resonant DC-Link, Soft-Switching Template*

Nomenclature

C_m, L_m	Clamp capacitor and inductor in the DC balance module
C_{r1}, L_{r1}	Resonant capacitor and inductor in the upper quasi-resonant module
C_{r2}, L_{r2}	Resonant capacitor and inductor in the lower quasi-resonant module
ΔV_{dc}	Initial voltage difference between C_m and the upper or the lower DC bus voltage
V_{cr}	Resonant voltage across the capacitor C_{r1} or C_{r2}
i_{cr}	Resonant current passes through the capacitor L_{r1} or L_{r2}
i_{Lm}	Current passes through the inductor L_m in the DC balance module
V_{dc}	DC bus voltage of the three-level inverter
T	The oscillating period of the quasi-resonant module

I. Introduction

The three-level neutral-point-clamped (NPC) inverter was applied in active power filters for achieving higher voltage and higher power [1][2]. A three-level NPC inverter can be employed in three-phase three-wire systems, as well as three-phase four-wire systems [3]-[5]. Since the switching devices of a three-level inverter share half of the dc bus voltage, the voltage stresses across the switching devices are reduced in comparison with a two-level inverter. The three-level inverter also provides more available output vectors that can improve the harmonic contents by selecting appropriate switching vectors.

Switching loss and switching noise degrade the efficiency of the power converters and would induce other problems, such as power dissipation and electromagnetic interference. Power losses dissipate in the form of heat. The increasing thermal stress of the power electronic devices affects its performance, and may shorten the lifetime of the power electronic devices. Consequently, the size of snubber circuits and heat sinks need to be increased. To apply soft-switching techniques are essential to overcome these problems[6]-[10]. Several soft-switching techniques have been proposed for three-level inverter [9]-[13]. In this paper, the quasi-resonant dc-link (QRDCL) module in [15] is adopted since it uses a small number of auxiliary components and is easier to control. Zero voltage condition is generated by the QRDCL module for achieving the zero voltage switching of the main switches in the three-level NPC inverter. Severe dv/dt of the power devices is released and the switching losses could be reduced.

The DC-link unbalance is another important issue of the three-level NPC inverter [16]. The unbalanced dc-link leads to a shifted voltage at the virtual ground and deteriorates the performance of the three-level inverter. Various approaches have been proposed to control the neutral point voltage. Some methods add additional dc

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control loop in the pulse width modulation (PWM) [17]-[19]. The design of the control loop is critical because it determines the voltage-balancing dynamic of the system and may produce instability under some operating conditions. By applying additional natural balancing circuits to the three-level NPC inverter, the dc voltage can also be controlled [20]-[22]. The dc voltage self-balancing module in [22] was originally proposed for generalized multilevel topology. It constructs by two power switches and one capacitor and is easy to control. This dc self-balancing module can also be applied to the three-level NPC inverter to achieve the dc link voltage balance.

In this paper, a generalized QRDCL three-level inverter is proposed, which include both the QRDCL module for soft-switching and dc voltage self-balancing module. The two modules affect the operation of each other, as a result, the dc self-balancing module in [19] needs to be modified. Since more power switches are added to the proposed three-level inverter, the switching sequence needs careful design to guarantee both soft-switching and dc-link self-balancing abilities are achieved. The effect on the output of the three-level inverter should also be kept as small as possible. The proposed switching sequence is combined with 3-dimensional direct pulse width modulation (3D DPWM) [23][24] to control the generalized QRDCL thee-level inverter. The generalized QRDCL three-level inverter is applied to a three-phase four-wire active power filter (APF) to achieve harmonic current, reactive current and neutral current compensation.

The structure and basic operational principle of the proposed generalized three-level quasi-resonant dc-link inverter is introduced in section II.

The detailed switching sequences for the main switches and auxiliary switches in the proposed inverter are explained in section III.

When the soft-switching and dc self-balancing is embedded with the 3D direct PWM, the corresponding control system is also proposed in this section. The generalized three-level QRDCL inverter is applied to a three-phase four-wire APF. The simulation verifications are given in section IV, including the results for demonstrating the soft-switching and dc self-balancing capabilities. The experimental results of the APF prototype are provided in section V.

II. Generalized Three-Level Quasi-Resonant DC-Link Inverter

In order to equip a three-phase four-wire three-level inverter with soft-switching and voltage self-balancing abilities, a generalized QRDCL three-level inverter is proposed, as shown in Fig. 1.

The QRDCL circuit is constructed by two symmetrical modules which can operate independently. The inductor L_r and the capacitor C_r are small energy storage devices. During the dc resonance, the voltage of capacitor C_r decreases to zero when the energy in the capacitor transfers to the inductor.

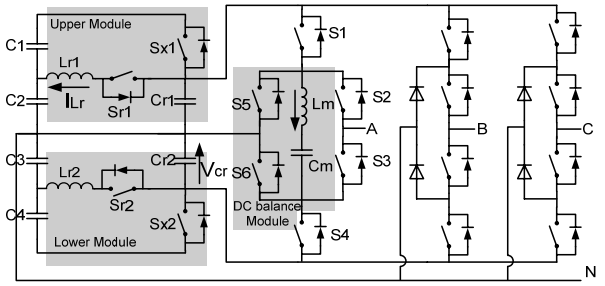


Fig. 1. The generalized quasi-resonant dc-link three-level inverter

The oscillating period is determined by (1):

$$T = \pi\sqrt{L_r C_r} \tag{1}$$

The upper module and the lower module could resonant voltages across the capacitors C_{r1} and C_{r2} respectively during the switching intervals. Once the zero voltage condition appears, the inverter's main switches are triggered and can achieve zero voltage turn on and turn off.

Except the QRDCL module, a dc self-balancing module is also included in the proposed three-level inverter. Switches $S5$, $S6$ and the capacitor C_m are the clamping devices which used to balance the dc capacitors' voltages. Table I lists four possible switching combinations of the leg A of the generalized three-level QRDCL inverter.

TABLE I
SWITCHING TABLE OF GENERALIZED THREE-LEVEL INVERTER

Output Voltage	S1	S2	S3	S4	S5	S6	Capacitors in Parallel
Vdc/2	1	1	0	0	0	1	Upper dc-link capacitor
0	1	0	1	0	0	1	Upper dc-link capacitor
0	0	1	0	1	1	0	Lower dc-link capacitor
-Vdc/2	0	0	1	1	1	0	Lower dc-link capacitor

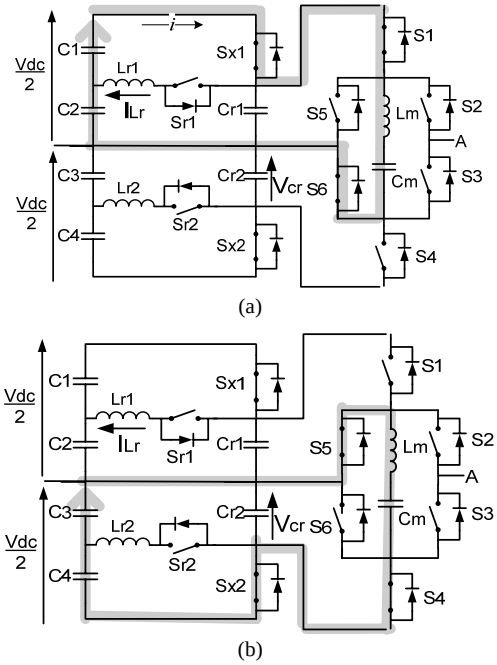
When switches $S1$, $S6$ are gated on, the output voltage of the inverter is positive $V_{dc}/2$ or zero. Capacitors C_m and the upper dc-link capacitors are connected in parallel as illustrated in Fig. 2(a). When switches $S4$ and $S5$ are triggered, the output voltage of the inverter is negative V_{dc} /2 or zero.

Capacitors C_m and the lower dc-link capacitors are connected in parallel, as illustrated in Fig. 2(b). The C_m connecting to the upper and lower dc-link capacitors alternately results in voltage equality of the upper and lower dc buses.

In this paper, the dc voltage balance module in conventional generalized converter is modified by adding an inductor L_m. The inductor L_m could limit the inrush current when two unbalanced capacitors are connected in parallel.

According to Fig. 2(a), (2) are obtained:

$$\begin{cases} L_m \dfrac{di}{dt} = u_{C1} + u_{C2} - u_{cm} \\ C_1 \dfrac{du_{C1}}{dt} = -i \\ C_2 \dfrac{du_{C2}}{dt} = -i \\ C_m \dfrac{du_{Cm}}{dt} = i \end{cases} \quad (2)$$



Figs. 2. The operation modes of dc self-balancing module (a) Parallel with upper dc-link capacitor (b) Parallel with lower dc-link capacitor

It is assumed C_1=C_2=2C_m, the initial current is zero and the initial voltage differences is ΔV_{dc} , the current in the balancing circuits and the voltage differences are obtained:

$$i = \Delta V_{dc} \sqrt{\frac{C_m}{2L_m}} \cdot sin\left(\sqrt{\frac{2}{L_m C_m}} t \right) \quad (3)$$

$$\begin{aligned} \Delta v_{dc} &= u_{C1} + u_{C2} - u_{cm} = \\ &= \Delta V_{dc} \sqrt{\frac{C_m L_m}{2}} \cdot cos\left(\sqrt{\frac{2}{L_m C_m}} t \right) \end{aligned} \quad (4)$$

According to (3) and (4), the time to reach the dc balance is only determined by the capacitor and inductor values. Even a large dc unbalance exists, the dc voltage could be balanced in one forth cycle. Hence, only one phase leg adopting the dc balancing module is sufficient to obtain the dc link voltage self-balancing for the three-phase inverter. The dc self-balancing module can be connected to any leg of the three-level inverter. In Fig. 1, the dc self-balancing module connects to phase A and the other two phase legs are the same as traditional diode-clamped structure As a generalized solution, this dc self-balancing module can also be applied to single-phase, four-leg or even back-to-back three-level converters to achieve dc voltage self-balancing.

However, the operation of the QRDCL circuit is affected when the dc self-balancing module is added. When the QRDCL circuit operates to produce zero dc voltages, the voltages of C_{r1} and C_{r2} are decreased. Without the dc control module, the voltage across C_{r1} and C_{r2} reaches zero during resonance. The dc control module is connected to one of the phase leg. The two free-wheeling diodes of switches S1 and S4 on that phase are turned on when the voltage across C_{r1} and C_{r2} drops to lower than half of the original value. The capacitor C_m is connected in parallel to the dc bus even both switches S5 and S6 are opened. As a result, the resonant voltage could not reach zero in the proposed generalized three-level QRDCL inverter. Instead, it decreases to a value lower than half of the original capacitor voltage. The resonant voltage and currents of the QRDCL modules in the proposed three-level inverter are illustrated in Fig. 3.

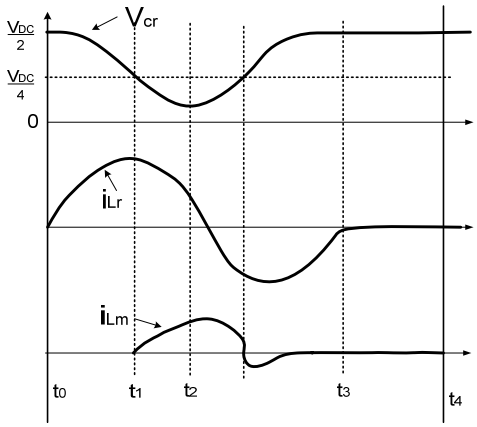


Fig. 3. The resonant voltages and currents of QRDCL module in the proposed inverter

As mentioned in previous discussions, the conventional generalized converter is modified by adding an inductor L_m.

During the soft-switching process, the inductor Lm acts as a snubber which can block the energy recharged by capacitor C_m, so that a lower resonant voltage is achieved. With carefully selected parameters for each module, the voltages across the resonant capacitors could reach a value close to zero during the resonant period.

In order to keep the resonant voltage of the upper and the lower QRDCL modules in-phase, switches S5 and S6 of the dc control module should be turned-off during dc-link resonance.

If either S5 or S6 is turned on during the resonance, the equivalent resonant capacitance is changed, which results in asynchronous of achieving minimum voltage for the upper dc bus and lower dc bus. Hence, switches S5 and S6 are hard switched off before the dc-link resonance. In addition, switches S2 and S3 in the dc voltage self-balance

leg could not be soft-switched as they are clamped by capacitor C_m. All the other switches in the proposed generalized QRDCL three-level inverter are soft-switched.

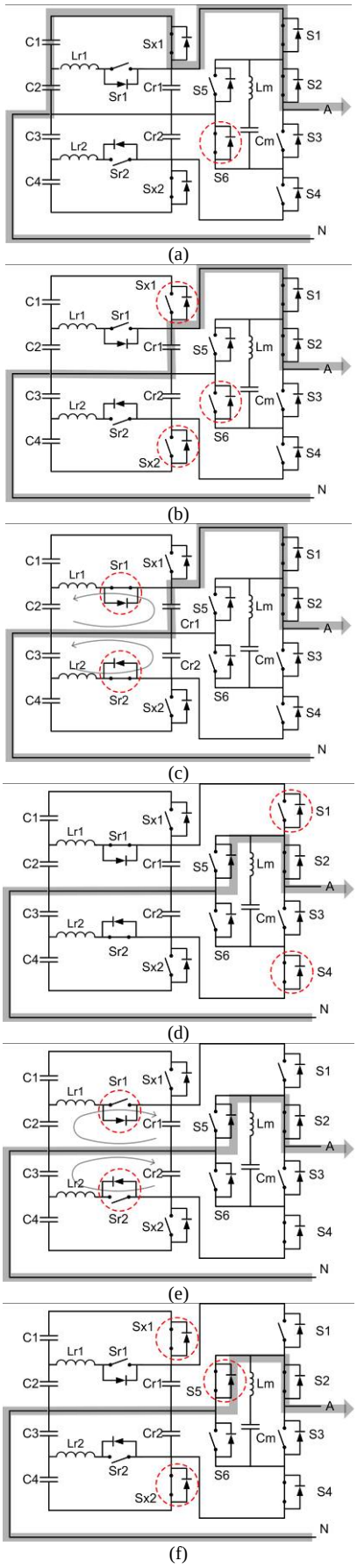
III. Control the Generalized Three-Level QRDCL Inverter

In the proposed generalized three-level QRDCL inverter, the power switches in the QRDCL module and the dc self-balancing module also needs to be triggered by the controller except the main switches. Hence, a properly designed switching sequence is important.

The switching sequence of the proposed generalized three-level QRDCL inverter from one switching state to another is explained in this section. The time section is divided as shown in Fig. 3.

It is assumed that the output voltage of the inverter is changed from $V_{dc}/2$ to zero. The other situations also follow the same procedure for triggering the QRDCL module and the dc control module. The operational modes of the proposed inverter in each time interval are shown in Figs. 4.

- $t < t_0$, Fig. 4(a). Inverter is in steady state and output voltage is positive $V_{dc}/2$. Auxiliary switches Sx1 and Sx2 were closed. Resonant capacitors are paralleled with the dc-link capacitors. The balancing capacitor C_m was connected in parallel with the upper dc-link capacitor since the auxiliary switch S6 is closed. The voltages of the upper dc-link capacitor and C_m were balanced.
- $t = t_0$, Fig. 4(b). Preparation of changing the output state of the inverter. Auxiliary switches S5 and S6 must be turned off before the resonance began. Then, switches Sx1 and Sx2 are opened to trigger the dc-link resonance.
- $t_0 < t < t_2$, Fig. 4(c). Auxiliary switches Sr1 and Sr2 are closed for voltage resonance, and the voltages of the resonant capacitors C_{r1} and C_{r2} start decreasing. However, At t_1, the voltages decreased to half of the original values. The capacitors C_{r1} and C_{r2} begin to be recharged by the balancing capacitor C_m through the anti-parallel diodes of S1 and S4. As a result, the minimum voltage of the resonant capacitors could not reach zero.
- $t = t_2$, Fig. 4(d). The minimum resonant voltage is detected. Inverter main switches S1 is turned off and S4 is turned on. The output state of the inverter is changed from positive $V_{dc}/2$ to zero. Since the dc-bus voltage is decreased, the switching losses of the inverter are reduced.
- $t_2 < t < t_3$, Fig. 4(e). During the second half of the resonance, the voltage across the capacitors C_{r1} and C_{r2} are recharged. Auxiliary switches Sr1 and Sr2 are turned off under zero voltage since the anti-parallel diodes of Sr1 and Sr2 are conducted.



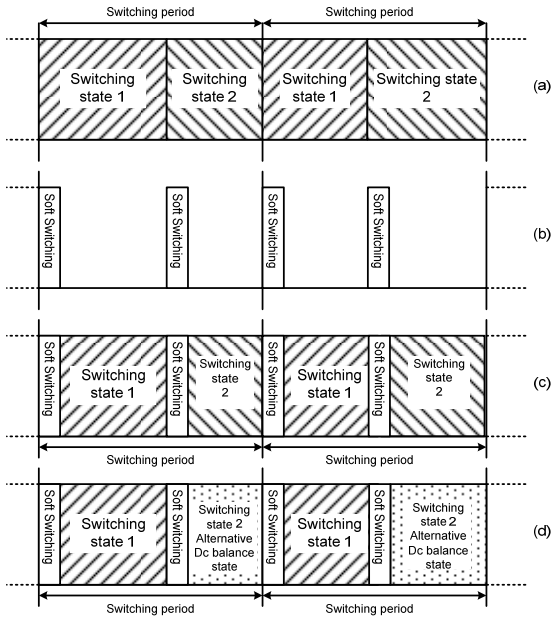
Figs. 4. Switching transient of the proposed three-level QRDCL inverter

- $t_3 < t < t_4$, Fig. 4(f). Auxiliary switches Sx1 and Sx2 can perform zero voltage closing when the resonant voltage returned to its original value. The resonance process is completed. Auxiliary switch S5 is closed in order to let the balancing capacitor C_m connects in parallel with the lower dc-link capacitor. The balancing capacitor C_m is connected in parallel with upper dc-link capacitor and lower dc-link capacitor alternatively. The dc self-balance of the proposed inverter is achieved.
- Under this switching sequence, the quasi-resonant dc-link and the dc control module could work together in the proposed generalized three-level QRDCL inverter. Most of the switches can be soft commutated and the overall switching losses of the inverter can be reduced. The dc voltage of the upper and lower dc bus of the three-level inverter is also self-balanced.

Figs. 5 show the switching sequences of the conventional inverter and the proposed generalized three-level QRDCL inverter. Normally, two switching states are adopted in a switching period to achieve the voltage-second approximation in a conventional three-level inverter, as illustrated in Fig. 5(a). When the QRDCL module operates, the time section for soft-switching is added between two switching states, as in Figs. 5(b) and (c). When the dc self-balancing module also operates, an alternative switching state are selected for the dc self-balancing module for the two neighboring sections with different switching states. The overall switching distribution in a switching period of the proposed generalized QRDCL three-level inverter is shown in Fig. 5(d).

The corresponding control chart of the proposed generalized QRDCL three-level inverter is given in Fig. 6. The generalized 3D direct Pulse-Width Modulation (PWM) is employed in this paper [23]. The 3D direct PWM has less calculation process than the conventional space vector modulation (SVM), especially for multilevel inverter.

The QRDCL modules are activated when the switching pattern of the inverter is to be changed. The incoming PWM signals are held on a latch device, and are released as soon as the minimum voltage condition is detected. A threshold value is selected in the control system for activating the voltage self-balancing unit. In addition, QRDCL modules feed back its operating state to the voltage self-balancing unit to avoid the interacting between the two modules.



Figs. 5. The switching distribution of (a) a conventional inverter, (b) QRDCL resonant process, (c) QRDCL inverter and (d) the proposed generalized three-level QRDCL inverter

IV. Simulation Results

The proposed generalized quasi-resonant dc-link three-level inverter is applied to a three-phase four-wire active power filter. The system configuration is shown in Fig. 7.

The proposed APF is used to compensate the harmonic currents, reactive power and neutral current in a three-phase four-wire system. Instantaneous reactive power theory is employed to calculate the reference current for compensation [25]. Table II lists the parameters of the simulation system.

The internal switches could switch the rectifiers between full-wave mode and half-wave mode. The dc offset exists in the neutral current when the nonlinear load operates in half-wave rectifying mode. When the APF compensate for this neutral current, a large dc voltage variation occurs.

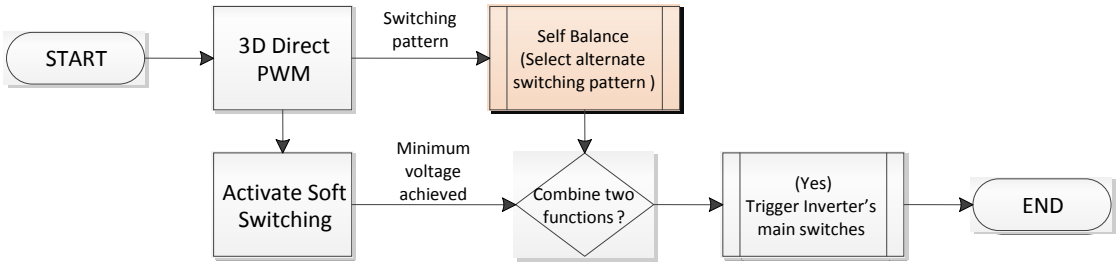


Fig. 6. Control diagram of the generalized three-level QRDCL inverter

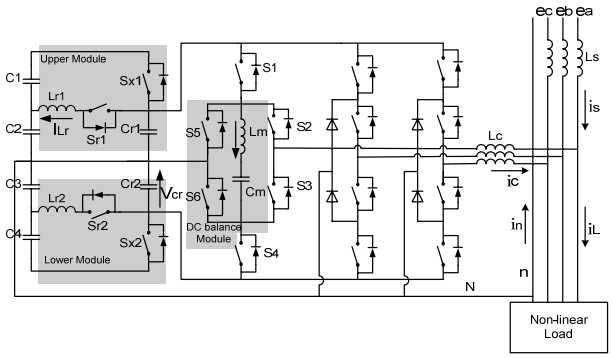


Fig. 7. System configuration of the APF using generalized QRDCL three-level inverter

TABLE II
SYSTEM PARAMETERS OF THE SIMULATION MODELS

Parameters	Symbols	Value
Nonlinear currents (rms)	I_a, I_b, I_c	1.46 A
Neutral current (rms)	I_n	1. 64 A
DC bus voltage	V_{dc}	160 V
Resonant inductor	L_r	5 μH
Resonant capacitor	C_r	0.5μF
Balancing inductor	L_m	6μH
Balancing capacitor	C_m	5000 μF
Switching frequency	f_s	5000 Hz

The nonlinear loads are shown in Fig. 8, which include three single-phase full-wave rectifiers.

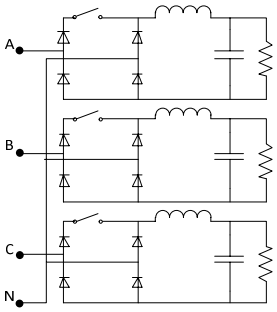


Fig. 8. The three-phase four-wire nonlinear load

The total harmonic distortion of the nonlinear load in full-wave rectifying mode is over 30%, in which the most significant harmonic is third order. The power factor of the nonlinear load is around 0.8. Fig. 9 shows the phase currents and neutral current of the system before compensation.

Before the dc voltages self-balancing function was activated, the dc link voltages deviated quickly as illustrated in Fig. 10. The compensation performance was deteriorated significantly when the dc link voltages were unbalance.

Once the self-balancing module is triggered, the dc link voltages were balanced immediately and the compensation performance of APF is improved. Fig. 11 illustrates the phase currents and neutral current after compensation by hard-switching.

Fig. 12 shows the system currents after compensation by the proposed generalized QRDCL three-level APF.

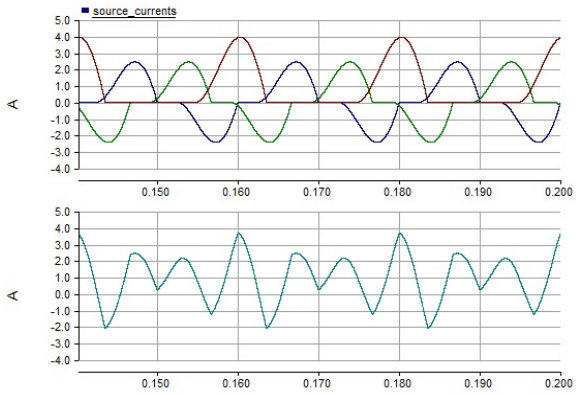


Fig. 9. The nonlinear phase currents and neutral current before compensation

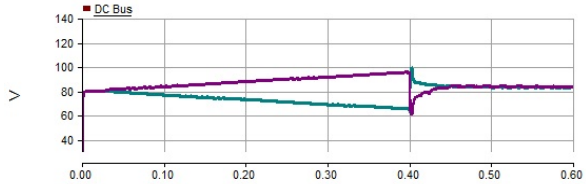


Fig. 10. The upper and lower dc-link voltages

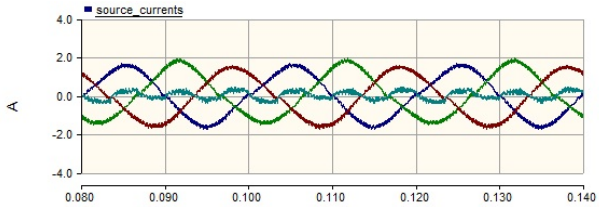


Fig. 11. The system phase currents and neutral current after compensation by hard switching

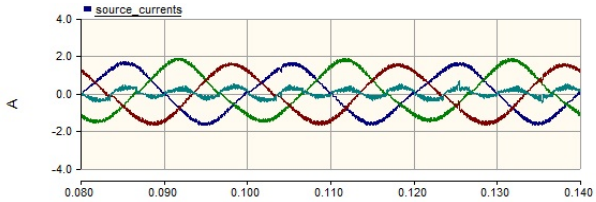


Fig. 12. The system phase currents and neutral current after compensation by soft-switching

Figs. 13 to 15 show the switching losses of the proposed generalized QRDCL three level inverter when it is applied in the three-phase four-wire APF. The losses of one of the main switch are shown in Fig. 13. The switching losses of the auxiliary switches Sx and Sr of the soft-switching module are shown in Figs. 14 and 15 respectively.

Moreover, Table III lists the compensation performance of the proposed APF under hard switching and soft-switching conditions, and the average losses of each critical switch. The simulation results show that the

proposed generalized QRDCL three-level active power filter can successfully compensate the harmonic currents and reactive power. At the same time, the dc voltages are self-balanced and the switching losses of whole APF are reduced by 20.8%. In addition, the high voltage and current stress across the switches during the switching are also released.

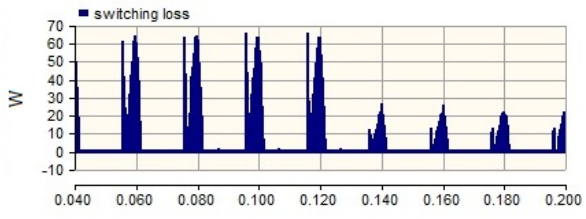


Fig. 13. The switching losses of one of the APF's main switch

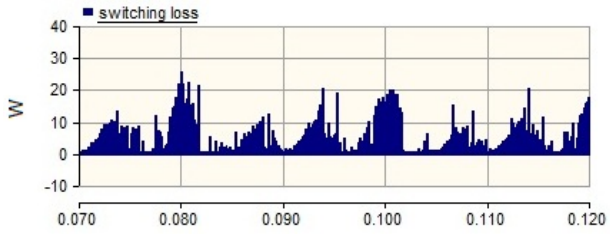


Fig. 14. The switching losses of one of the auxiliary switch of a soft-switching module (Sx)

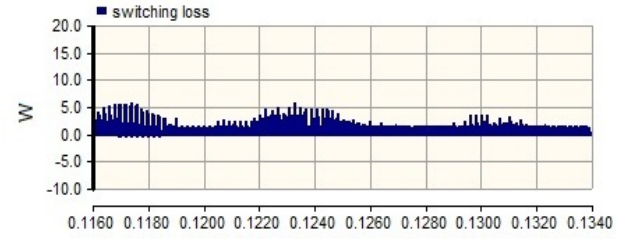


Fig. 15. The switching losses of one of the auxiliary switch of a soft-switching module (Sr)

TABLE III
THE COMPENSATION PERFORMANCE AND SWITCHING LOSSES

	Before Compensation	Hard Switching	Soft-switching
Phase current	1.42A	1.07A	1.08A
Neutral current	1.72A	0.19A	0.23A
Power factor (DPF)	0.83	0.99	0.99
Current THD	36%(Full wave rectifier) 66%(Half wave rectifier)	8.5%	9.2%
Balanced dc voltages	-	82.7V, 83.6V	84.3V, 85V
Avg. switching losses (APF's main switch)	-	0.083W*12	0.025W*10+0.083*2
Avg. switching losses (Sx)	-	-	0.089W*2
Avg. switching losses (Sr)	-	-	0.077W*2
Avg. switching losses (self-balance switch)	-	0.097W*2	0.097W*2
Total switching losses	-	1.19W	0.942W

V. Experimental Results

V.1. Prototype of the Proposed Three-Level QRDCL APF

The prototype of the proposed generalized QRDCL three-level inverter was built and was applied in a three-phase four-wire APF. The system configuration is shown in Fig. 7 and the non-linear loads for testing are as shown in Fig. 8. The photo of the prototype is shown in Fig. 16 and the corresponding control system block diagram is given in Fig. 17. The TI TMS320F2812 controller and Xilinx XC3S400 FPGA are selected to implement the control system.

V.2. Switching Losses Evaluation

Fig. 18 shows the switching transients of an inverter's main switch under hard switching condition, i.e. the QRDCL modules are not triggered. The transient voltage reaches twice of the nominal voltage and oscillates very quickly during the switching. Current overshot is also recorded as given in Fig. 18. The switching losses of the main switch of the three-level inverter could be measured by multiplying the instantaneous voltage and instantaneous current.

Fig. 19 shows the switching losses of the main switch by multiplying the voltage and current, in which the average switching losses in one period (50Hz) is approximately 1.49W. The total switching losses under hard switching include the losses of the twelve main switches of the three-level converter and the losses of the two switches in the dc self-balancing module. The switching losses are recorded and given in Table IV.

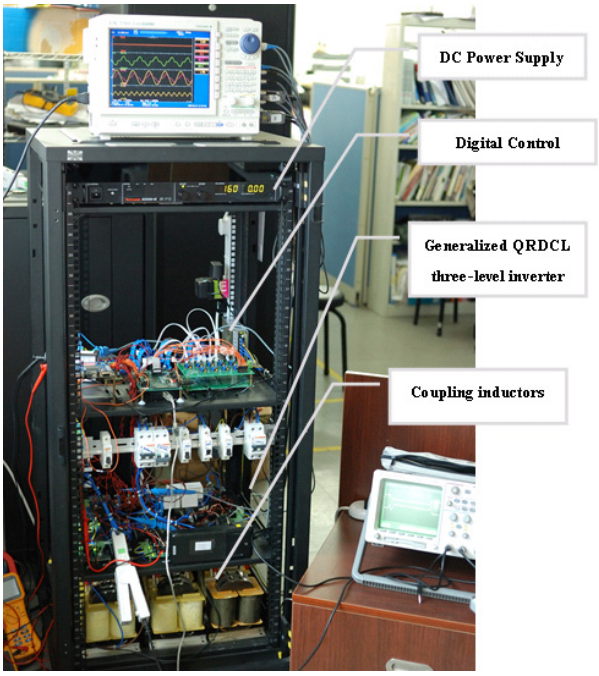


Fig. 16. Prototype of the three-phase four-wire APF

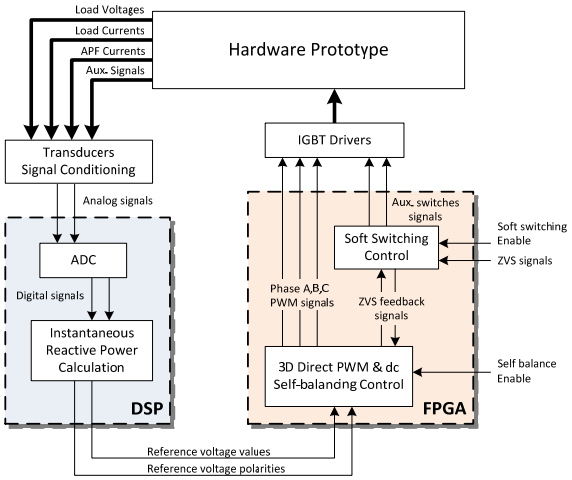


Fig. 17. Structure of the digital control systems

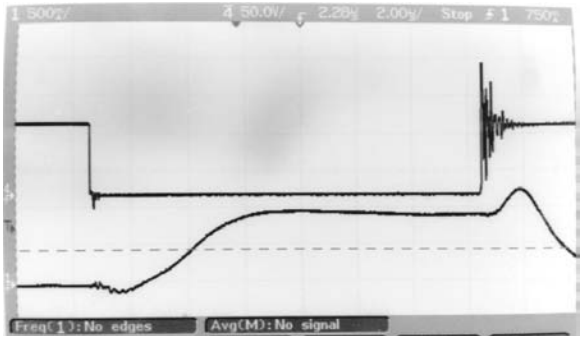


Fig. 18. The switching transient of a switch in hard-switching

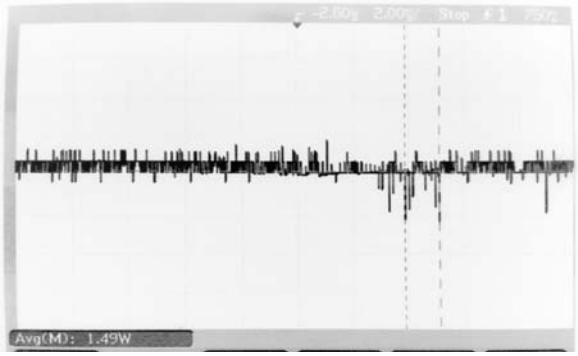


Fig. 19. The average switching losses of a inverter's main switch

After the QRDCL modules operate, the cross section of transient voltage and current of the switching devices was significantly reduced. Fig. 20 shows the switching transients of an inverter's main switch in soft-switching and the corresponding switching losses are shown in Fig. 21. It could be seen from Fig. 20 that the high transient voltage and current overshot are removed by applying the soft-switching technique. The recorded average switching losses of the main switches in the three-level converter was 0.48W, which is about 32% of the losses during hard switching. As two main switches are clamped by the dc self-balancing module, their switching losses keep the same as hard-switching. Only the switching losses of ten main switches are reduced. The switching losses of the auxiliary switches in QRDCL circuit and dc self-balancing module are also recorded.

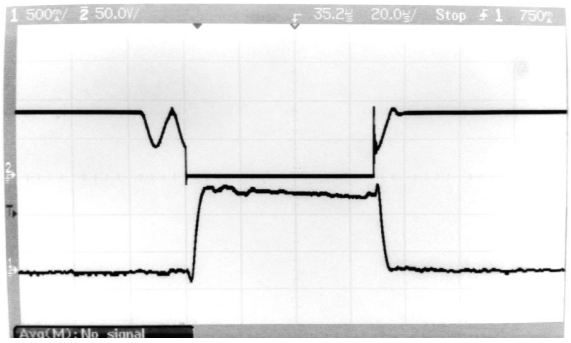


Fig. 20. The switching transient of soft-switching

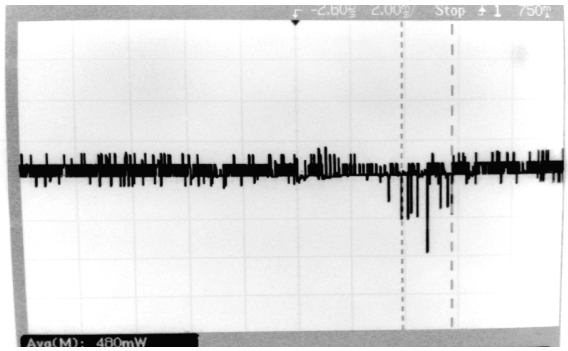


Fig. 21. The average switching losses of inverter's main switch in soft-switching

The switching losses for hard switching and soft-switching are compared in Table IV. According to the experimental results, the overall switching losses are reduced by 18. 5%.

TABLE IV
THE COMPARISON OF SWITCHING LOSSES BETWEEN HARD AND SOFT-SWITCHING

	Hard Switching	**Soft-switching**
Inverter's main switch (per switch)	1.49W	0.48W
Auxiliary switches (self-balance)	2.55W×2	2.55W×2
Auxiliary switches (per module)	–	2.15W, 0.77W
Overall switching losses	22.98W (1.49×12+2.55×2)	18.72W (0.48×10+1.49×2+2.15×2 +0.77×2+2.55×2)

V.3. DC Voltage Control and Compensation Performance

The currents of the non-linear loads in the experiments are shown in Fig. 22. As dc offset exists in the neutral current, the DC-link voltages deviates when the APF compensates the unbalanced load currents without dc voltage control. The source current of phase A after

compensation and the unbalanced dc link voltages are shown in Fig. 23. The dc voltages were set as ±80V under normal condition, however the dc voltages were deviated to +94V, –66V after 5 seconds.

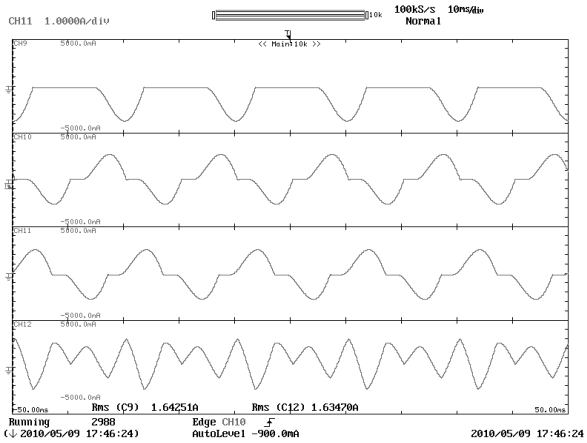


Fig. 22. The phase currents and neutral current of nonlinear loads

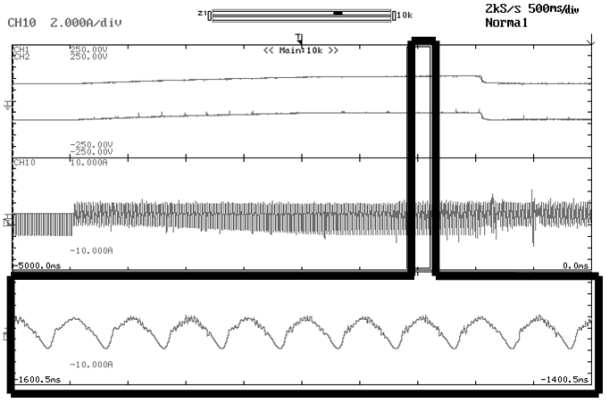


Fig. 23. The dc voltages and system currents during compensation without dc control

Once the dc voltage self-balancing module is activated, the dc voltages were balanced and the dc unbalance was controlled in a very short time. Fig. 24 shows the source current of phase A and the dc link voltages after triggering the dc self-balance module.

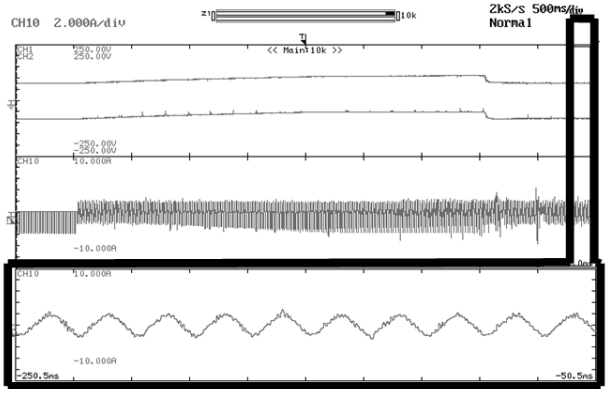


Fig. 24. The dc voltages and system currents after compensation with dc control

Figs. 25 and 26 show the source currents before and after compensation for the other two phases and the neutral currents. The compensation performance are given in Table V and also compared with hard-switching situation. Results indicate that the soft-switching module only slightly affect the compensation performance of the three-phase four-wire active power filter. The proposed generalized QRDCL three-level APF could compensate harmonics, reactive current and neutral currents simultaneously in a three-phase four-wire system.

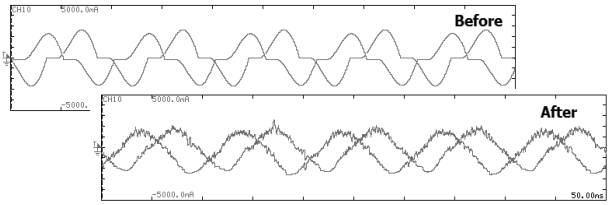


Fig. 25. The system phase currents before and after compensation

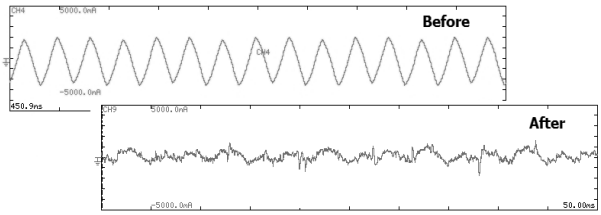


Fig. 26. The system neutral current before and after compensation

TABLE V
THE COMPENSATION PERFORMANCE

	Before Compensation	Hard Switching	Soft-switching
Phase current	1.45 A	1.38A	1.39A
Neutral current	1.37 A	0.7A	0.75A
Power factor (DPF)	0.81	0.99	0.99
I THD	36%	8.6%	9%

VI. Conclusion

In this paper, a generalized QRDCL three-level inverter is proposed and is applied to a three-phase four-wire active power filter. The proposed generalized QRDCL three-level inverter has the capability of soft-switching and dc self-balancing. With the proposed switching sequences, the QRDCL module and dc self-balancing module could work together in the three-level inverter. Simulation and experimental results are provided to show the validity of the proposed inverter and its control strategy. However, the output of the three-level inverter is slightly affected when the dc balance module operates. The initial cost of the QRDCL modules is high compared to the saving through switching losses when the inverter rating is small. The QRDCL module not only reduced the switching losses but also releases the voltage stresses across the main switches, which is good for the safe operation of the power switches. The proposed generalized QRDCL three-level APF could compensate harmonics, reactive current and neutral

currents simultaneously in a three-phase four-wire system.

Acknowledgements

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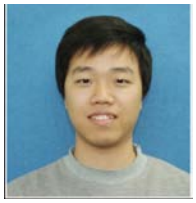

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