Pre-emphasis transmitter (0.007 mm^2, 8 Gbit/s, 0–14 dB) with improved data zero-crossing accuracy in 65 nm CMOS

Y. Chen, P.-I. Mak, L. Zhang, H. Qian and Y. Wang

A pre-emphasis transmitter with improved data zero-crossing accuracy is described. It is achieved via data re-synchronisation using a set of extended true single-phase clock latches before output combining, constituting a robust, area- and power-efficient solution. Fabricated in 65 nm CMOS, the full-rate one-tap pre-emphasis transmitter measures a total jitter of 33.12 ps up to an 8 Gbit/s data rate, and 25.04 to 38.75 ps under a 0–14 dB reconfigurable pre-emphasis range. The achieved output swing is as large as 550 mV$_{pp}$, and the active area is just 0.007 mm^2.

Introduction: To facilitate low-power data communications over long printed circuit board traces or coaxial cables, the data generated by the transmitter must be properly pre-emphasised to overcome frequency-dependent channel loss because of the skin effect and dielectric loss. A typical pre-emphasis transmitter consists of two parts: a 'data-delay array' based on latches, and an 'output combiner' for summating the different taps and controlling the amount of pre-emphasis [1, 2]. For implementation of the former, as shown in Fig. 1, the extended true single-phase clock (E-TSPC) logic is more favourable than the current-mode logic (CML) in terms of power efficiency. The details have been studied in [1], showing that a 10 Gbit/s TSPC latch can be 10 × more power efficient than its CML counterpart. Regrettably, unlike the CML latch which can be differentially structured to minimise the systematic mismatch between differential outputs, the E-TSPC latch suffers from structural mismatches in generating the differential outputs (Q and QB), showing poor data zero-crossing accuracy which eventually leads to higher jitter and less eye opening at the receiver side. This Letter introduces a new data re-synchronisation technique suitable for a E-TSPC-based data-delay array. Both simulation and experimental results are provided to demonstrate the feasibility and robustness of the technique against process and temperature variations, and over a wide range of data rates.

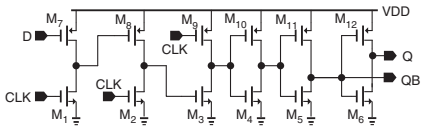

Fig. 1 *Typical E-TSPC latch*

Pre-emphasis transmitter with improved data zero-crossing accuracy: The proposed transmitter (Fig. 2) is based on a full-rate architecture to exploit fully the digital speed capability of fine linewidth CMOS, and is immune to duty clock distortion of the master clock (CLK). To further save power and area, the pre-emphasis exploits only one-tap to minimise the latch counts and parasitic effects in the output combiner. The front stage is a CML-to-CMOS buffer which converts the input signal into a rail-to-rail logic signal stream, which is then fed into the data-delay arrray made by cascaded E-TSPC latches. The first-stage E-TSPC latch is to sample and shape the data, whereas the fourth-stage E-TSPC latch is to balance the loading effect at the output of the third-stage E-TSPC latch. Although both main data and one unit interval (1-UI) data can be created with this delay array, their differential data ($V_{o1p,n}$ and $V_{o2p,n}$) suffer from mismatches because of the asymmetrical operation of E-TSPC latches. To address this problem, four E-TPSC latches were added physically closer to the output combiner to re-synchronise the four data streams. As such, not only the data-delay difference (unavoidable in the physical layout) can be minimised, but also the data waveform can be reshaped in a better manner. This hardware overhead is fair as the E-TSPC latch is extremely area and power efficient, as mentioned before. After re-synchronisation, the zero-crossing-improved outputs ($V_{o3p,n}$ and $V_{o4p,n}$) are summated at the output combiner, where the tap cofficients (α_0 and α_1) can be reconfigured to offer a wide pre-emphasis range.

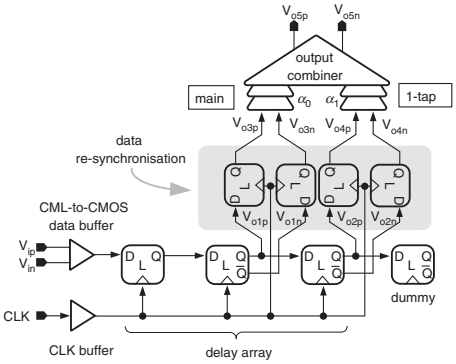

Fig. 2 *Proposed pre-emphasis transmitter*
Four E-TSPC latches perform data re-synchronisation, improving the data zero-crossing accuracy

The improvement achieved by the technique is assessed first by simulations. With an 8 Gbit/s pseudorandom binary sequence data (PRBS 2^7–1) as the input, the 1-UI eye diagrams of V_{o1p}–V_{o1n} and V_{o3p}–V_{o3n} under the slow–slow (SS) corner and 27°C are obtained, as shown in Fig. 3. $V_{o1p,n}$ suffers from a zero-crossing error of 164.2 mV, but is significantly reduced to 2.55 mV at $V_{o3p,n}$ after re-synchronisation. The effects of temperature and process variations are reported in Fig. 4. Before re-synchronisation, the minmum $V_{os1,diff}$ ($|V_{o1p}$–$V_{o1n}|$) is 50.54 mV at the SS corner (–40°C), whereas the maximum $V_{os1,diff}$ is 594.4 mV at the slow NMOS fast PMOS (SNFP) corner (125°C). On the contrary, $V_{os2,diff}$ is within 8 mV in all cases after re-synchronisation, substantiating the robustness of the technique.

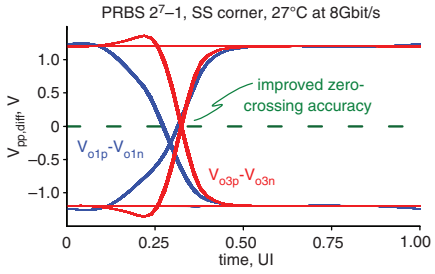

Fig. 3 *Simulated 1-UI eye diagram of main path, showing improved zero-crossing accuracy from V_{o1p}–V_{o1n} to V_{o3p}–V_{o3n}*

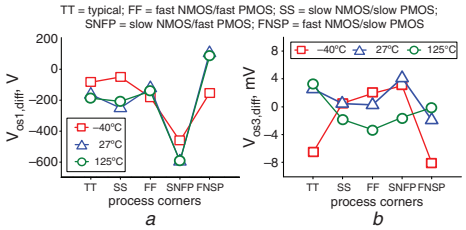

Fig. 4 *Simulation results under 8 Gbit/s (PRBS 2^7–1)*
a Before data re-synchronisation at $V_{o1p,\,n}$
b After data re-synchronisation at $V_{o3p,\,n}$

Experimental results: The pre-emphasis transmitter fabricated in 65 nm CMOS occupies an active area of 0.007 mm^2 (Fig. 5). Each E-TSPC latch, sized with a fan-out-of-2 driving capability, occupies a 54 μm^2 die size and draws 0.72 mW at a data rate of 8 Gbit/s. The output combiner is a three-stage differential-pair amplifier with resistive loads, operating as a CML output buffer with controllable bias currents for reconfiguring the pre-emphasis range. Both the input and the output pads are tailored for double-wire bonding to facilitate high-speed testing. The data input with a PRBS of 2^7–1 is generated by the J-BERT N4903B. The output eye diagrams are captured via the MSOX 93204A Infiniium oscilloscope at 2 and 8 Gbit/s corresponding to 0 and 10 dB pre-emphasis as shown in Fig. 6. These eye diagrams illustrate the symmetrical data waveform and precise zero crossing, proving the efficacy of the adopted re-synchronisation. The measured total jitter increases from 25.04 to 38.75 ps whereas the pre-emphasis

increases from 0 to 14 dB (Fig. 7*a*), because of the more data-dependent jitter contribution. The total jitter varies from 29.72 to 33.12 ps under 2 to 8 Gbit/s data rates (Fig. 7*b*). The power consumed by the delay array with the added re-synchronisation part is 5.05 mW. Table 1 compares this work with a recent art [3] targeting a similar application. This design is favoured for its higher data rate and smaller die size. Since this work targets more output swing and pre-emphasis, the power budget of the output combiner is higher than [3].

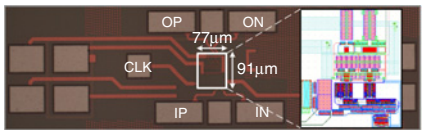

Fig. 5 *Chip photo of fabricated pre-emphasis transmitter*

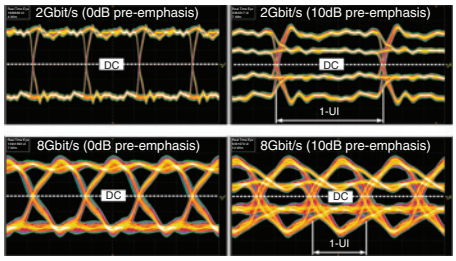

Fig. 6 *Measured eye diagrams at 2 Gb/s (upper) and 8 Gb/s (lower) with 0 and 10 dB pre-emphasis*

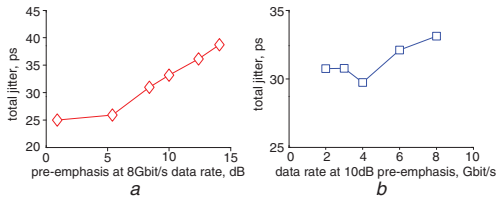

Fig. 7 *Measured results*

a Total jitter against pre-emphasis at 8 Gbit/s data rate
b Total jitter against data rate at 10 dB pre-emphasis

Table 1: Performance summary and comparison

Parameters	[3] TCAS-II'12	This work
Technology	90 nm CMOS	65 nm CMOS
Data rate (Gbit/s)	2–6	**1–8**
Supply voltage (V)	1.2	1.2/1
Output swing ($mV_{pp,diff}$)	300	**550**
Pre-emphasis range (dB)	0–6	**0–14**
Die size (mm^2)	0.035	**0.007**
Power (mW)	7.32	5.05 + 22.85[a]

[a]Consumed by output combiner

Conclusion: We propose a pre-emphasis transmitter with improved data zero-crossing accuracy via E-TSPC-based data re-synchronisation. The key performances have been simulated and verified experimentally in 65 nm CMOS. This work has demonstrated promising potential for performance enhancement of wireline transceivers in nanoscale CMOS.

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One or more of the Figures in this Letter are available in colour online.

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