A 0.0045-mm^2 32.4-μW Two-Stage Amplifier for pF-to-nF Load Using CM Frequency Compensation

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***Abstract*—This brief reports an embedded capacitor multiplier (CM) frequency compensation technique to realize an extremely compact micropower two-stage amplifier for wide capacitive load (C_L) drivability. It features: 1) a valuable left half-plane zero to enhance the closed-loop stability over a wide range of C_L; 2) no extra bias circuit and power, as the CM is embedded into the first stage of the amplifier, and 3) only one very small (subpicofarad) compensation capacitor improving the transient settling and area efficiency. Detailed analytical treatments of the amplifier offer the critical insights for device sizing and optimization. Fabricated in 0.18-μm CMOS, the amplifier measures 3.06-MHz unity-gain frequency (UGF), 1.76-V/μs average slew rate (SR), and 74° phase margin (PM) at 20-pF C_L, and 0.22-MHz UGF, 0.049-V/μs SR, and 59.8° PM at 15-nF C_L. The die size is 0.0045 mm^2, and power is 32.4 μW at 1.2 V. Competitive large- and small-signal figures of merit are achieved with respect to the state of the art.**

***Index Terms*—Capacitive load, capacitor multiplier (CM), CMOS, frequency compensation, stability, two-stage amplifier.**

I. Introduction

Extremely compact micropower CMOS amplifiers with wide capacitive load (C_L) drivability have found extensive applications in chemical sensors and liquid crystal display drivers [1], [2]. For amplifiers having three or more stages, their performances are tightly related to the frequency compensation scheme applied [3]. In fact, very few three-stage amplifiers are capable to drive pF-to-nF C_L at small power and area, due to the closed-loop stability constraints at either light or heavy C_L [4]. In contrast, two-stage amplifiers exhibit simpler tradeoffs among the major metrics such as dc gain, gain-bandwidth (GBW) product, power and area with frequency compensation. However, most existing frequency compensation schemes for the simple two-stage Miller amplifier were focused on eliminating the unwanted right half-plane zero, rather than extending the range of C_L drivability [5].

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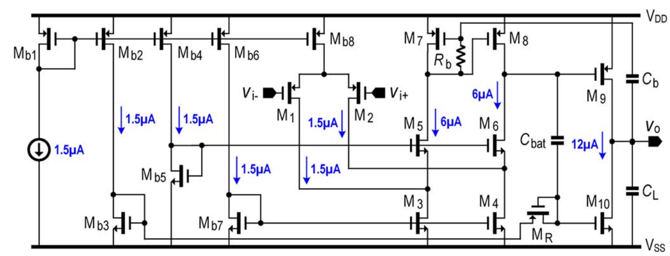


Fig. 1. Schematic of the proposed two-stage amplifier with embedded CM frequency compensation.

In this brief, we report a two-stage amplifier capable of driving a wide range of C_L, while achieving high power and area efficiencies. Previously, current buffer Miller compensation (CBMC) was optimized to realize a two-stage amplifier stable for any C_L [6]. However, to attain the small C_L stability, the current buffer has to dissipate a significant amount of power to push up the associated parasitic pole, and the measured step response at 10-pF C_L still exhibited a superimposed high-frequency ringing. Moreover, when C_L becomes heavy enough ($>$ 100 pF), the Miller capacitor must be increased to uphold the first-stage dc gain [6]. A large Miller capacitor penalizes not only the die area but also the power and slew rate (SR). To alleviate such tradeoffs, a capacitor multiplier (CM) can be applied to reduce the physical size of the capacitor and power. The current-mirror-based CM in [7] features simple realization, but it was hard to achieve a high multiplication factor under low power budget. Although there were many other alternatives [8] that can boost the multiplication factor by at least one order of magnitude, they inevitably produced low-frequency poles that limit the amplifier's GBW. In addition, existing current-buffers or CM realizations require add-on bias circuits, while inducing extra voltage offset, noise, and parasitic capacitances [8].

The described two-stage amplifier is based on the embedded CM frequency compensation scheme [8], but is architecturally improved via exploring a new design freedom to eliminate the GBW-limiting shunt compensation capacitor, while preserving the stability at small C_L. A modified class-AB output stage is also proposed to reduce the parasitic capacitance and save power. A complete *local feedback loop* (LFL) analysis [4] and a design procedure are proposed to optimize the performance of the amplifier over a wide range of C_L.

II. Proposed Two-Stage Amplifier With Embedded CM Frequency Compensation

A. Schematic

The schematic of the proposed two-stage amplifier with embedded CM frequency compensation is depicted in Fig. 1.

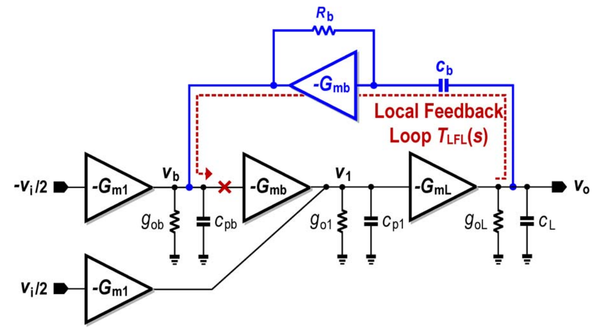


Fig. 2. Small-signal equivalent model of the proposed two-stage amplifier.

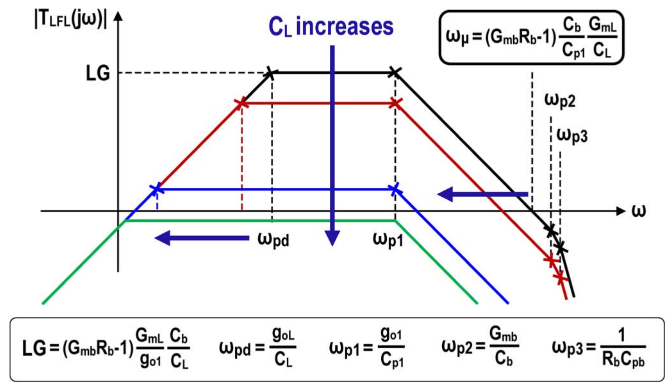


Fig. 3. LFL magnitude responses of the proposed two-stage amplifier under increasingly large C_L.

The first stage uses a folded-cascode structure ($M_1 - M_8$ and M_{b8}). The embedded CM is realized via R_b, C_b and the reuse of the current mirror M_{7-8}. Unlike the realization in [8] entailing an extra compensation capacitor, C_b is solely responsible here for saving area and avoiding GBW reduction, particularly at large C_L. In addition, the light C_L drivability is not sacrificed because of the design freedom given by the embeddable CM, which will be detailed later. M_9 and M_{10} form the output stage of the amplifier. In order to obtain symmetrical rising and falling SRs, a class-AB output stage is employed, and it is realized by adding $C_{\rm bat}$ and a diode-connected PMOS transistor M_R [9]. During the dynamic operation, the first stage's output will vary noticeably. Since M_R operates as an extremely large resistor, the time entailed to (dis)charge $C_{\rm bat}$ will be quite long. Hence, the voltage variation at the gate of M_9 can be transferred to that of M_{10} with negligible loss. $M_{b1} - M_{b8}$ form the basic current sources and mirrors, providing a proper bias current for the amplifier.

Fig. 2 depicts the amplifier's small-signal equivalent model. The two G_{m1} represent the transconductances of M_1 and M_2. $G_{\rm mb}$ is the transconductance of M_{7-8}, while $G_{\rm mL}$ is the sum of M_9 and M_{10} transconductances, accounting the ac effect of the class-AB output stage. The output conductance of each stage is denoted by $g_{\rm ob}$, g_{o1}, and $g_{\rm oL}$, respectively. $C_{\rm pb}$, C_{p1}, and C_{p2} lumped into the load capacitor C_L model the parasitic capacitance at the corresponding nodes. The small C_b amplified by the embedded CM generates the required effective capacitance, which via the LFL ensures the two poles associated with v_1 and v_o to split apart, producing widely spaced dominant and nondominant poles under light-to-medium C_L conditions.

B. LFL Transfer Function

Conventional direct circuit analysis [4] cannot offer enough insights to optimize the amplifier's pole-zero arrangement when analyzing the stability of the amplifier over a wide range of C_L. The LFL analysis is employed here to guide the design phase, particularly at light-C_L condition. As shown in Fig. 2, the LFL induced by the embedded CM is broken at node v_b. In addition to the assumption, i.e., $1/G_{\rm mb} < R_b \ll 1/g_{\rm ob}$, for the embeddable CM, the LFL transfer function $T_{\rm LFL}(s)$ is derived, assuming that the gain of each stage is $\gg$1, and $C_{\rm pb}$, $C_{p1} \ll C_b \ll C_L$, i.e.,

$$T_{\rm LFL}(s) \approx \frac{-sG_{\rm mL}(G_{\rm mb}R_b - 1)C_b}{g_{o1}g_{\rm oL}\left(1+\frac{s}{\omega_{\rm pd}}\right)\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}+\frac{s^2}{\omega_{p2}\omega_{p3}}\right)}. \quad (1)$$

The conceptual magnitude responses of $T_{\rm LFL}(s)$ are shown in Fig. 3 over different values of C_L. The LFL's dominant pole is $\omega_{\rm pd}$, while the first nondominant pole is ω_{p1}. ω_μ is the LFL's UGF, and the other two high-frequency poles stemming from the embedded CM are ω_{p2} and ω_{p3}, respectively, which can be configured in a complex form to boost the LFL's phase margin (PM).

As illustrated in Fig. 3, ω_μ might locate close to ω_{p2} and ω_{p3} under a small C_L. If C_L is further decreased, the LFL's PM will deteriorate and degrade the LFL's stability, which imposes a significant magnitude peak in the overall transfer function of the amplifier. In the time domain, this will result in the step response exhibiting a long-lasting high-frequency oscillation [4]. To quantify the limit of low C_L drivability, the PM of the LFL, i.e., $PM_{\rm LFL}$, is calculated as

$$PM_{\rm LFL} \approx 90^\circ - \tan^{-1}\frac{\frac{\omega_\mu}{\omega_{p2}}}{1-\frac{\omega_\mu^2}{\omega_{p2}\omega_{p3}}}. \quad (2)$$

Solving (2) and substituting the expressions of ω_μ, ω_{p2}, and ω_{p3}, the minimum C_L under a given $PM_{\rm LFL}$ is given by

$$C_{L\_\min} \approx \frac{2(G_{\rm mb}R_b - 1)G_{\rm mL}R_bC_b}{\left(\sqrt{1+\frac{4G_{\rm mb}R_b}{(\tan PM_{\rm LFL})^2}\frac{C_{\rm pb}}{C_b}}-1\right)\tan PM_{\rm LFL}}\frac{C_{\rm pb}}{C_{p1}} \quad (3)$$

where $C_{L\_\min}$ is not much vulnerable to process variations because $C_{\rm pb}$ is mainly determined by the gate capacitance of M_8 that partially tracks C_{p1} (mostly arises from M_9 and M_{10}). To enhance the small C_L drivability, it was proposed in [8] to upscale C_{p1} via shunting an extra capacitor. Although the MOS capacitor (MOSCAP) realization incurs less area overhead, it substantially lowers the position of ω_{p1}, thereby limiting the GBW. Particularly, as C_L becomes very large, ω_{p1} comes into the first nondominant pole of the amplifier. Instead, the approach of selecting a smaller $G_{\rm mb}R_b - 1$ is explored in the proposed amplifier to balance the light C_L drivability with a large GBW.

Since ω_μ, ω_{p2}, and ω_{p3} control the high-frequency portion of the amplifier's overall transfer function while ω_μ determines its first nondominant pole [4], a larger ω_μ results in a larger PM for the amplifier. When C_L is increased, ω_μ moves toward lower frequencies, as shown in Fig. 3. Although $PM_{\rm LFL}$ is improved, the amplifier's PM is degraded. The trend continues until the midband LFL gain (LG) becomes no more than unity, which is expressed as

$$\mathrm{LG} = (G_{\mathrm{mb}}R_b - 1)\frac{G_{\mathrm{mL}}C_b}{g_{o1}C_L} \leq 1. \tag{4}$$

As LG continues to reduce with increasingly large C_L, the LFL completely fails to shape the amplifier's frequency response, i.e., the amplifier degenerates into a simple two-stage amplifier without Miller compensation. The overall transfer function should then be resorted to assess the stability.

C. Overall Transfer Function

As the wide-range C_L variation forces the LFL to be either effective or ineffective under different scenarios, the overall transfer function of the proposed amplifier should be studied according to different cases.

1) Case 1: When C_L is small (LG $\gg 1$), the LFL takes control over the frequency response below ω_μ. The overall transfer function $A_v(s)$ can be calculated as

$$A_v(s) \approx \frac{A_{\mathrm{DC}}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_d}\right)\left(1+\frac{s}{\omega_\mu}+\frac{s^2}{\omega_\mu\omega_{p2}}+\frac{s^3}{\omega_\mu\omega_{p2}\omega_{p3}}\right)} \tag{5}$$

where A_{DC} is the dc gain $G_{m1}G_{\mathrm{mL}}/g_{o1}g_{\mathrm{oL}}$; ω_d is the dominant pole $g_{o1}g_{\mathrm{oL}}/G_{\mathrm{mL}}(G_{\mathrm{mb}}R_b - 1)C_b$; and the GBW is $G_{m1}/(G_{\mathrm{mb}}R_b - 1)C_b$. A useful left half-plane (LHP) zero $\omega_z = 2G_{\mathrm{mb}}/[(G_{\mathrm{mb}}R_b + 1)C_b]$ is created, which can be used to improve the PM of the amplifier, i.e., PM_{overall}, at light-to-medium C_L conditions. Unlike CBMC that relies on the LFL to create an LHP zero, the presence of such LHP zero is due to the existence of the direct feedforward signal path from the input to the output formed by R_b and C_b (see Fig. 2). As previously discussed, for small values of C_L that can maintain a reasonable PM_{LFL}, the amplifier shows enough PM_{overall} as ω_μ, ω_{p2}, and ω_{p3} locates much higher than the GBW.

If C_L is large to reduce ω_μ to be much less than ω_{p2} and ω_{p3} while still ensures LG $\gg 1$, it means that the first nondominant pole of the amplifier, i.e., ω_μ, can be factored out from the third-order polynomial in (5), simplifying $A_v(s)$ to

$$A_v(s) \approx \frac{A_{\mathrm{DC}}\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_d}\right)\left(1+\frac{s}{\omega_\mu}\right)\left(1+\frac{s}{\omega_{p2}}+\frac{s^2}{\omega_{p2}\omega_{p3}}\right)} \tag{6}$$

and PM_{overall} is given by

$$PM_{\mathrm{overall}} \approx 90^\circ - \tan^{-1}\frac{\mathrm{GBW}}{\omega_\mu} + \tan^{-1}\frac{\mathrm{GBW}}{\omega_z} - \tan^{-1}\frac{\frac{\mathrm{GBW}}{\omega_{p2}}}{1-\frac{\mathrm{GBW}^2}{\omega_{p2}\omega_{p3}}}. \tag{7}$$

As C_L is increased, ω_μ is reduced, while ω_d, ω_z, ω_{p2}, and ω_{p3} all remain unchanged, resulting in a lower PM_{overall}.

2) Case 2: When C_L is exceedingly large and forces LG $\ll 1$, the amplifier can be well approximated by a two-pole system, and the overall transfer function is given by

$$A_v(s) \approx \frac{A_{\mathrm{DC}}}{\left(1+\frac{s}{\omega_{\mathrm{pd}}}\right)\left(1+\frac{s}{\omega_{p1}}\right)} \tag{8}$$

where ω_{pd} and ω_{p1} correspond to the dominant and nondominant poles of the amplifier, respectively, and the GBW is $G_{m1}G_{\mathrm{mL}}/g_{o1}C_L$. PM_{overall} is reformulated into

$$PM_{\mathrm{overall}} \approx 90^\circ - \tan^{-1}\frac{\mathrm{GBW}}{\omega_{p1}} = 90^\circ - \tan^{-1}\frac{G_{m1}G_{\mathrm{mL}}G_{\mathrm{P1}}}{g_{o1}^2 C_L}. \tag{9}$$

If C_L is further increased, ω_{pd} will continue to reduce in frequency and the GBW follows. As ω_{p1} is fixed, PM_{overall} is improved, and the amplifier becomes more stable. Hence, the proposed amplifier is unconditionally stable for any larger C_L.

3) Case 3: The aforementioned analysis of PM_{overall} versus C_L implies that there is a minimum PM_{overall}, i.e., $PM_{\mathrm{overall\_min}}$ that occurs at LG $= 1$. The corresponding C_L is given by

$$C_L = \frac{G_{\mathrm{mL}}(G_{\mathrm{mb}}R_b - 1)C_b}{g_{o1}}. \tag{10}$$

Intuitively, this condition can be explained as the LFL just begins to lose the control over the amplifier's frequency response, and it contributes equally with the output stage to form the dominant pole of the amplifier. Thus, ω_{pd} shifts to $g_{\mathrm{oL}}/2C_L$, while ω_{p1} is moved up to $2g_{o1}/C_{p1}$. Substituting (10) into (9) with the shifted ω_{pd} and ω_{p1}, $PM_{\mathrm{overall\_min}}$ is evaluated as

$$PM_{\mathrm{overall\_min}} = \tan^{-1}\frac{4g_{o1}(G_{\mathrm{mb}}R_b - 1)C_b}{G_{m1}C_{p1}}. \tag{11}$$

There are several ways to achieve a good $PM_{\mathrm{overall\_min}}$. One possibility is to limit the gain of the first stage, while degrading the offset and noise performances of the amplifier. In addition, C_{p1} can be reduced to improve $PM_{\mathrm{overall\_min}}$ at the expense of the small C_L drivability. However, the optimum solution would be to preserve a reasonably large $(G_{\mathrm{mb}}R_b - 1)C_b$, which is the major advantage of the proposed embedded CM compensation allowing the use of a small C_b and therefore less G_{mb} (i.e., less power), when compared with the CBMC in [6].

III. Other Considerations and Design Procedure

A. Class-AB Output Stage

When C_L is very large, e.g., in the order of nanofarads, the SR of an amplifier should be limited at the output stage. Hence, it is highly desirable to configure the output stage of a wide-range C_L amplifier in a class-AB mode. The employed class-AB output stage [9] relies on C_{bat} working as a level shifter (i.e., a floating battery) to propagate voltage variations at the gate of M_9 to that of M_{10}. The accuracy of the voltage transfer demands both large C_{bat} and small parasitic capacitance at the gate of M_{10}. Unlike the realizations in [8] and [9] that connect the gate of M_{10} to that of M_3, M_{10} is separately biased by M_{b3}, which can be sized with a smaller channel length than that of M_3, considerably reducing the parasitic capacitance. The transconductance of M_{10} can be thus more efficiently utilized. In addition, a large C_{bat} is beneficial to boost the gain at low frequencies. In the layout design, the top plate of C_{bat} is connected to the gate of M_{10}, reducing the added parasitic capacitance.

The saturation voltage of M_9 should be sized the same as that of M_{10}, so that they can provide the same amount of (dis)charging current during transients to obtain a symmetrical SR. In addition, a relatively low saturation voltage, which is another reason to bias M_{10} independently, benefits the voltage spike reduction at the input of the output stage, decreasing or avoiding the conduction of parasitic diode in M_R and itself.

B. Noise

For simplicity, only thermal noise is accounted since the same method can be applied to analyze the flicker noise. As the noise contribution from the output stage, such as M_9, M_{10}, and M_R, is greatly suppressed by the gain of the first stage, the input-referred noise is dominated by the first stage and can be given by

$$\overline{v_{n,T}^2} = \frac{8\kappa_B T\gamma}{g_{m1}}\left[1 + \frac{g_{\mathrm{m3}}}{g_{m1}} + \frac{g_{\mathrm{m7}}}{g_{m1}}\left(1 + \frac{g_{\mathrm{m7}} R_b}{2\gamma}\right)\right]. \quad (12)$$

Since R_b forms a shunt feedback between the gate and the drain of M_7, its noise voltage is directly amplified by M_8 and adds at the first stage's output, which manifests as the last term in (12). Thus, R_b cannot be chosen too large to significantly degrade the noise performance. In this design, R_b adds 36.5% input-referred thermal noise.

C. Design Procedure

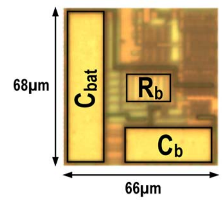
There are several performance tradeoffs when C_L is varying. It is desirable to have a clear design procedure to balance the metrics under a variety of C_L. The first step is to place the poles of the embeddable CM. To boost the PM_{LFL} and, hence, the low C_L drivability as much as possible, ω_{p2} and ω_{p3} are set to be equal, achieving a 45° PM for the LFL inside the embeddable CM itself. Then, resolving (2) results in

$$\omega_{p2} = \omega_{p3} = \frac{\tan PM_{\mathrm{LFL}} + \sqrt{(\tan PM_{\mathrm{LFL}})^2 + 4}}{2}\omega_{\mu}. \quad (13)$$

The next step is to determine the capacitor multiplication factor $G_{\mathrm{mb}}R_b - 1$. At nominal C_L, e.g., 100 pF in this design, the amplifier follows the overall transfer function in (6). PM_{overall} is recalculated with $\omega_{p2} = \omega_{p3}$ and given by

$$PM_{\mathrm{overall}} \approx 90^\circ - \tan^{-1}\frac{\mathrm{GBW}}{\omega_\mu} + \tan^{-1}\frac{G_{\mathrm{mb}}R_b + 1}{2}\frac{\mathrm{GBW}}{\omega_{p2}} - \tan^{-1}\frac{\frac{\mathrm{GBW}}{\omega_{p2}}}{1 - \left(\frac{\mathrm{GBW}}{\omega_{p2}}\right)^2}. \quad (14)$$

With specified PM_{LFL}, PM_{overall}, and GBW/ω_u, $G_{\mathrm{mb}}R_b$ can be evaluated by simultaneously solving (13) and (14). For example, PM_{LFL} and PM_{overall} target 80° and 65°, respectively, while $\omega_{\mu,\mathrm{Proposed}}$ is set to roughly 1.5× GBW, $G_{\mathrm{mb}}R_b$ is ~ 4 in this design. The minimum C_b is determined from the estimated C_{pb}, C_{p1}, and g_{o1} to maintain $PM_{\mathrm{overall\_min}} > 45°$. Consequently, the estimated values of G_{m1}, G_{mb}, and G_{mL} are calculated according to the expressions of GBW, ω_u, and ω_{p2}. Following the aforementioned steps, the key parameters of the proposed amplifier are $G_{m1} = 33.4\ \mu$S, $G_{\mathrm{mb}} = 103.8\ \mu$S, and $G_{\mathrm{mL}} = 428.9\ \mu$S, respectively. The typical value of C_b is set to be 0.556 pF, with R_b being 38.5 kΩ, targeting a GBW of ~3 MHz at $C_L = 100$ pF.



Device	Size (μm)	Device	Size (μm)
M_1/M_2	8 x (3.6/0.5)	M_{10}	8 x (1.6/0.8)
M_3/M_4	5 x (1.6/1.6)	M_R	(0.42/0.42)
M_5/M_6	6 x (2.4/0.4)	C_b	0.556 pF
M_7/M_8	6 x (3/0.54)	C_{bat}	1 pF
M_9	12 x (3/0.54)	R_b	38.5 kΩ

Fig. 4. Die photo of the amplifier (left) and its key device sizes (right).

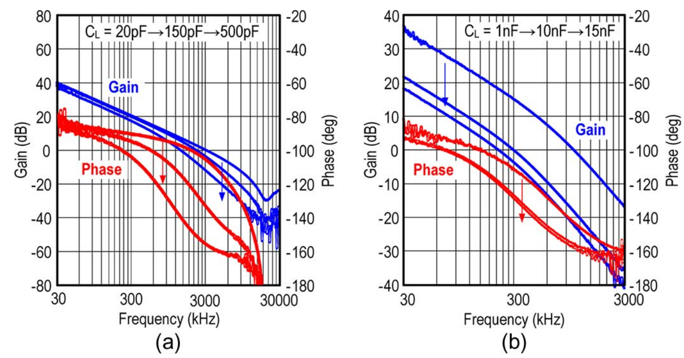


Fig. 5. Measured ac responses of the proposed two-stage amplifier at (a) $C_L = 20$, 150, and 500 pF. (b) $C_L = 1$, 10, and 15 nF.

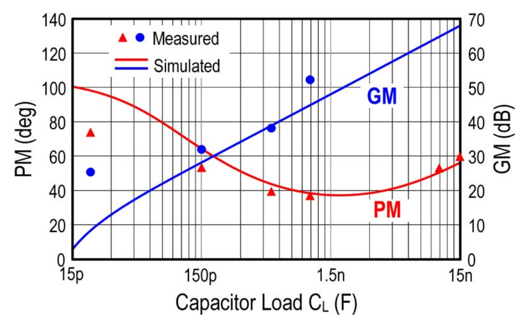


Fig. 6. Measured and simulated PM and GM curves over a wide range of C_L. The discrepancy at small C_L is likely due to the uncertain capacitances of the PCB traces and testing cables.

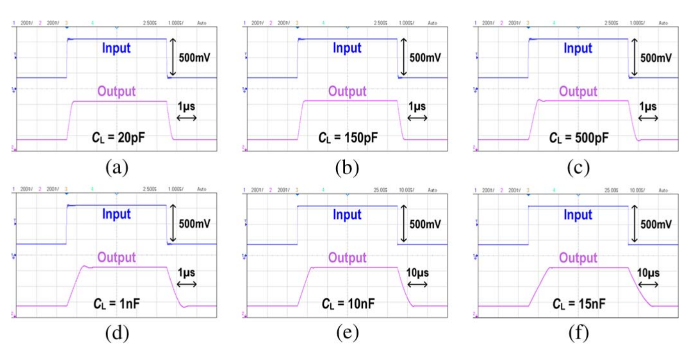


Fig. 7. Measured 500-mV step responses at: (a) $C_L = 20$ pF; (b) $C_L = 150$ pF; (c) $C_L = 500$ pF; (d) $C_L = 1$ nF; (e) $C_L = 10$ nF; and (f) $C_L = 15$ nF.

IV. Measurement Results

The amplifier was fabricated in 0.18-μm CMOS (see Fig. 4), and the die size is 0.0045 mm^2, which is dominated by C_{bat} rather than R_b and C_b in the embedded CM compensation. C_{bat} and C_b are metal–insulator–metal capacitors. R_b is made

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work						JSSC'13 [4]				ISSCC'14 [10]
Technology	**0.18 μm CMOS**						0.35 μm CMOS				0.18 μm CMOS
Chip Area (mm^2)	**0.0045**						0.016				0.007
Power @ V_{DD} (μW)	**32.4 @ 1.2 V**						144 @ 2 V				6.3 @ 0.9 V
Estimated DC Gain (dB)	**82**						>100				>100
Input-Referred Noise Density (nV/√Hz @ 100 kHz)	**130**						174				N/A
Capacitive Load C_L (pF)	**20**	**150**	**500**	**1,000**	**10,000**	**15,000**	1000	5,000	10,000	15,000	500
UGF (MHz)	**3.06**	**2.26**	**1.41**	**1.05**	**0.30**	**0.22**	1.37	1.24	1.06	0.95	1.34
Phase Margin (°)	**74.0**	**53.4**	**39.5**	**37.0**	**53.1**	**59.8**	83.2	69.8	57.2	52.3	52.7
Gain Margin (dB)	**25.4**	**32**	**38.2**	**52.3**	**>60**	**>60**	9.8	16.6	17.0	18.1	N/A
Average SR (V/μs)	**1.76**	**1.77**	**1.26**	**0.75**	**0.076**	**0.049**	0.59	0.50	0.30	0.22	0.62
Average 1% T_S (μs)	**0.36**	**0.35**	**0.70**	**1.20**	**6.98**	**11.0**	1.28	1.71	3.66	4.49	1.12
FOM_S (MHz·pF/mW) *	**1,889**	**10,463**	**21,759**	**32,407**	**92,593**	**101,852**	9,514	43,056	73,889	98,656	106,349
FOM_L (V/μs·pF/mW) #	**1,086**	**8,194**	**19,444**	**23,148**	**23,457**	**22,685**	4,097	17,326	20,833	22,917	49,206

*FOM_S = (GBW · C_L) / Power   #FOM_L = (SR · C_L) / Power

up of high-resistive polyresistors. The static current excluding the bias circuitry is 27 μA at 1.2 V. The wide-C_L drivability is verified in the frequency domain first, as shown in Fig. 5(a) and (b). With $C_L = \sim 20$ pF [input capacitance of the equipment, electrostatic discharge, and printed circuit board (PCB) trace], the GBW reaches 3.06 MHz and the PM is 74°, but the gain margin (GM) is 25.4 dB due to the reduced PM_{LFL}. When C_L is increased to 500 pF, the GBW is reduced to 1.41 MHz. The measured PM (39.5°) is close to the simulated value, which is $\sim 44°$. At 1-nF C_L, the amplifier approaches to the minimum PM condition with the measured 37.0° PM having $< 2°$ deviation from the simulation result. The measured GM is 38.2 dB. When C_L is further increased to 15 nF, the PM starts to recover with a value of 59.8°, while the GM is > 60 dB. The overall tendency is plotted in Fig. 6, which aligns well with the simulations.

The transient settling behaviors of the amplifier are verified via a 500-mV step stimulus. For $C_L = \sim 20$ pF [see Fig. 7(a)], there exhibit no overshoot and ringing, indicating that the amplifier is adequately stable and consistent with the results given in Fig. 5. The measured positive and negative SRs are respectively 1.84 and 1.67 V/μs, which are dominated by the current to (dis)charge C_b. When C_L is increased to 1 nF [see Fig. 7(d)], the output response shows both overshoot and undershoot, but their magnitudes are only $\sim$3%. The SRs are determined by the maximum amount of dynamic current provided by the output stage, which correspond to 0.712 V/μs for the positive and 0.789 V/μs for the negative steps. As C_L is as large as 10 nF [see Fig. 7(e)] and 15 nF [see Fig. 7(f)], the outputs become more and more stable. Particularly at $C_L =$ 15 nF, there is no visible ringing, overshoot, or undershoot. The SRs are proportionally reduced by $\sim 15\times$. The detailed performances are summarized in Table I and compared with recent advanced three-stage works. At large C_L, the UGF and PM of the proposed amplifier show relatively large variation in comparison with that in [4]. However, they may not be crucial for sensor interface applications. Rather, the proposed amplifier achieves the widest C_L drivability and occupies the smallest die area, while the FOM_S and FOM_L stay competitive at various C_L values.

V. CONCLUSION

In order to enlarge the C_L drivability of a two-stage amplifier with small power and area, an improved version of embedded CM frequency compensation has been introduced. The first stage of the amplifier features the embedded CM minimizing the size of the physical compensation capacitors, improving the SR, and creating a useful LHP zero to enhance the stability. No extra bias circuit and power are required by the embedded CM. Detailed analytical treatments, design procedure, and silicon verification validated the feasibility of the proposed amplifier.

REFERENCES

[1] R. F. B. Turner, D. J. Harrison, and H. P. Baltes, "A CMOS potentiostat for amperometric chemical sensors," *IEEE J. Solid-State Circuits*, vol. SSC-22, no. 6, pp. 473–478, Jun. 1987.

[2] W.-J. Huang, S. Nagayasu, and S.-I. Liu, "A rail-to-rail class-B buffer with DC level-shifting current mirror and distributed Miller compensation for LCD column drivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1761–1772, Aug. 2011.

[3] R. G. H. Eschauzier and J. H. Huijsing, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*. Dordrecht, The Netherlands: Kluwer, 1995.

[4] Z. Yan, P.-I. Mak, M.-K. Law, and R. P. Martins, "A 0.016-mm^2 144-μW three-stage amplifier capable of driving 1-to-15 nF capacitive load with $> 0.95 -$ MHz GBW," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 527–540, Feb. 2013.

[5] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*., 5th ed. Hoboken, NJ, USA: Wiley, 2009, pp. 643–649.

[6] R. J. Reay and G. T. A. Kovacs, "An unconditionally stable two-stage amplifier," *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 591–594, May 1995.

[7] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.

[8] Z. Yan, P. -I. Mak, and P. R. Martins, "Two-stage operational amplifiers: Power-and-area efficient frequency compensation for driving a wide range of capacitive load," *IEEE Circuits Syst. Mag.*, vol. 11, no. 1, pp. 26–42, Jan.–Mar. 2011.

[9] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. J. Lopez-Martin, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 568–571, Jul. 2006.

[10] W. Qu, J.-P. Im, H.-S. Kim, and G. -H. Cho, "A 0.9 V 6.3 μW multistage amplifier driving 500 pF capacitive load with 1.34 MHz GBW," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 290–291.