A Multiphase Switched-Capacitor DC–DC Converter Ring With Fast Transient Response and Small Ripple

Yan Lu, *Member, IEEE*, Junmin Jiang, *Student Member, IEEE*, and Wing-Hung Ki, *Member, IEEE*

***Abstract*— A fully integrated step-down switched-capacitor dc–dc converter ring with 123 phases has been designed that could achieve fast dynamic voltage scaling for the microprocessor of wearable devices. The symmetrical multiphase converter ring surrounds its load in the square and supplies power to the on-chip power grid that is easily accessible at any point of the chip edges. The frequency of the V_{DD}-controlled oscillator is adjusted through its supply voltage V_{DD}, which allows the unity-gain frequency to be designed higher than the switching frequency. The converter ring has been fabricated in a low-leakage 65-nm CMOS process. This converter achieves a response time of 3 ns, a reference tracking speed of 2.5 V/μs, and a minimum output ripple of 2.2 mV. The peak efficiency is 80% at the power density of 66.6 mW/mm^2, and the maximum power density is 180 mW/mm^2.**

***Index Terms*— Amplifier, charge pump, converter ring, dc–dc converter, dynamic voltage and frequency scaling (DVFS), low dropout (LDO) regulator, multiphase, *N*-path filter, switched-capacitor power converter (SCPC), voltage-controlled oscillator (VCO).**

I. Introduction

TO EXTEND the battery cycle of a wearable device, the technique of dynamic voltage and frequency scaling (DVFS) is widely adopted [1], of which the CPU/GPU supply voltage (V_{DD}) and the clock frequency are increased to achieve high performance and decreased in the idle period to save energy. In a fine-grained power management scheme, V_{DD} is set to different values (ranging from 1.1 to 0.6 V, for example) to satisfy different performance requirements. The settling times of transiting between different V_{DD} levels are also included in the processing time of the task and should be minimized. In particular, settling times to higher V_{DD} have to be fast to meet performance requirements; otherwise, user experiences will be degraded. Hence, to support the dynamic voltage scaling (DVS) scheme, dc–dc converters and/or low-dropout (LDO) voltage regulators with fast reference tracking are needed [2]–[4].

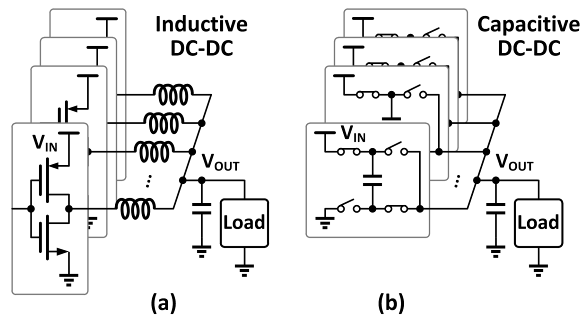


Fig. 1. Multiphase (a) inductive and (b) capacitive dc–dc converters.

Microprocessors driven by fully integrated power converters with fast transient responses are needed for miniaturized devices [5], [6]. However, as shown in Fig. 1, conventional inductive dc–dc converters need one or more inductors that are hard to be integrated and will occupy large chip or printed circuit board area. The energy transfer between inductor and capacitor could be lossless, and the ideal efficiency of the inductive dc–dc converter is 1, which is favorable, especially for higher power consumption, such as 10–100 W. On the other hand, due to the charge redistribution loss, the efficiency of the capacitive dc–dc converter resembles that of the linear regulator [7], which is proportional to the actual output voltage over the ideal no-load output voltage [8]. With the advancement in fabrication processes, the capacitor density has been significantly increased, for example, an ultrahigh power density of 5 W/mm^2 has been demonstrated in [9] with deep-trench capacitors. Losses due to parasitic capacitors can also be reduced by appropriate topological considerations and circuit techniques [5], [10], [11]. In addition, switched-capacitor (capacitive) power converters (SCPCs) can adopt the multiphase architecture for ripple reduction easily with very little power and area overhead [12]. Thus, SCPCs are preferred for full integration in nanometer processes at low power levels [13]. Moreover, a capacitive dc–dc converter can achieve faster transient response compared with its inductive counterpart. Note that an inductive dc–dc converter with voltage-mode control contains an *LC* filter that is of second order, and needs a complicated compensation scheme to extend the bandwidth and maintain stability, while the

Manuscript received January 10, 2016; revised May 10, 2016 and August 12, 2016; accepted October 11, 2016. Date of publication November 7, 2016; date of current version January 30, 2017. This paper was approved by Associate Editor Gyu-Hyeong Cho. This work was supported in part by the Research Grant Council of Hong Kong under Project T23-612/12-R, in part by the Macau Science and Technology Development Fund (FDCT), and in part by the Research Committee of University of Macau.

Y. Lu is with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, (e-mail: yanlu@umac.mo).

J. Jiang and W.-H. Ki are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: eeki@ust.hk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2016.2617315

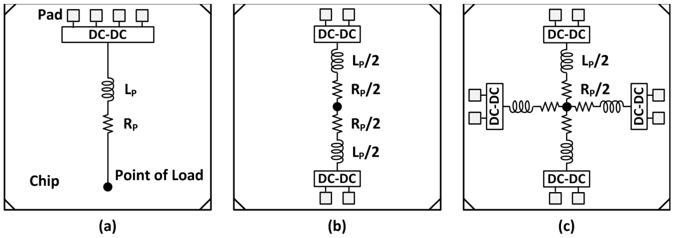


Fig. 2. Parasitic resistance of the supply routing with on-chip dc–dc converter(s), supplied from (a) one side, (b) two sides, and (c) four sides.

switched-capacitor power stage is only of first order. Although the power stage of an inductive dc–dc converter with current-mode control can be considered as first order, the changing of V_{OUT} has a 90° phase delayed compared with the changing of the inductor current I_L. In this regard, a capacitive dc–dc converter is more suitable for realizing fast DVS with full integration.

The goal of a power distribution system is to deliver the required current across the whole chip to the load circuits while maintaining the voltage level necessary for proper operation of the digital loads. Nevertheless, a large dc current I_{dc} will introduce *IR* drop due to the parasitic resistance R_P of the V_{DD} network, and fast transient current will cause V_{DD} variation due to the parasitic inductor L_P of the power buses and bond wires. The overall ΔV_{DD} is approximately $I_{\mathrm{dc}}R_P + L_P \cdot di/dt$ that will cause clock jitter and affect the logic delay of the load [14]. In addition, asynchronous circuits that are highly dependent on the sequence of signals are more sensitive to supply variations than synchronous circuits. Obviously, as shown in Fig. 2, supplying the load in the center from opposite sides could reduce the worst case R_P and L_P to one-fourth of that by supplying from only one side of the chip. R_P and L_P could further be reduced using more dc–dc converters in parallel, as shown in Fig. 2(c). However, each dc–dc converter needs a control block that is area and power consuming. In this paper, we propose a symmetrical multiphase dc–dc converter ring that surrounds the load in the square, as shown in Fig. 3 [3]. Now, the load can easily get access to the power supply through any point on the chip edges. The in-rush current is reduced by the distributed multiphase configuration and also by employing higher V_{IN} (lower I_{IN}) compared with an LDO. The converter ring helps reducing the number of power and ground pads while maintaining good noise performance for V_{DD} and Gnd nodes.

Conventionally, the unity-gain frequency (UGF) of the control loop of a dc–dc switching converter (either inductive or capacitive) is designed to be at least six times lower than the switching frequency F_S. It is worth noting that increasing the phase number N will not only reduce the output voltage ripple but also enable the control loop to respond at every T/N of the switching period T. Hence, by designing a multiphase interleaving SCPC, the effective switching frequency is much increased, and it becomes possible to achieve a control-loop UGF that is higher than F_S.

This paper is organized as follows. The original concept and considerations of the layout-oriented converter ring design

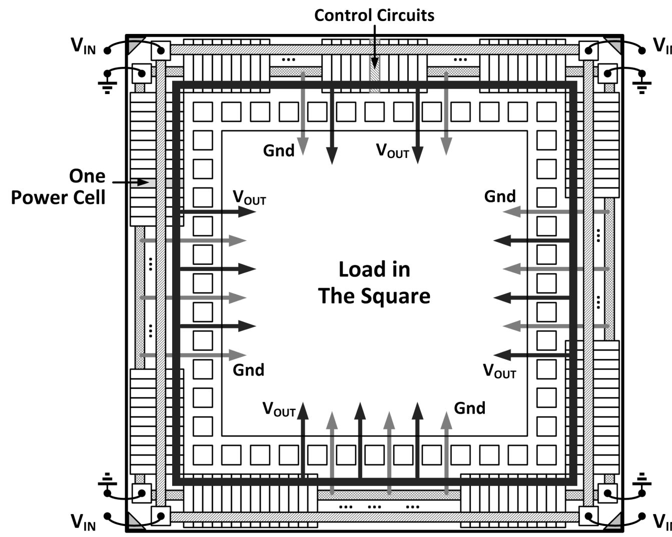


Fig. 3. Conceptual layout of the proposed multiphase converter ring.

are introduced in Section II. Circuit implementation issues are discussed in Section III. Analysis of the pseudocontinuous-time SCPC is presented in Section IV, followed by the measurement results in Section V. Finally, conclusions are drawn in Section VI.

II. Layout-Oriented Design Considerations

This design was inspired by the St. Peter's Square of Vatican City, which is surrounded by 284 columns along the perimeter of the Square. With reference to Fig. 3, one may regard each power cell as one column, and the loads are distributed within the square. Each power cell delivers a predesigned maximum power and constitutes one interleaving phase. The power cells are then concatenated to form a dc–dc converter ring. The number of phases is determined by the total power of the loads and the geometry of the chip. In this prototype, there are 30 phases on the "top" edge and 31 phases on the other edges, making 123 phases in total. The control circuitry occupies the area of only one power cell. It is evident from the layout that the converter ring is symmetrical. At each corner of the chip, there is one V_{IN} pad and one Gnd pad such that all power pads stay clear of the bonding pads of the loads.

The system architectures of the conventional and the proposed multiphase SCPCs are shown in Fig. 4(a) and (b), respectively. For both SCPCs, the switching frequency F_S determines the output voltage V_{OUT}, and F_S is generated by a voltage-controlled oscillator (VCO). The conventional SCPC has a centralized current-starved (CS) VCO with a fixed supply voltage (V_{LDO}), while V_{OUT} is compared with the reference voltage V_{REF} to generate the control voltage V_{CTRL} in determining the bias current of the inverters, which in turn determines F_S. Note that the clock phases are distributed to the loads that are scattered over the whole chip through a routing maze, and there could be serious path mismatches that defeat the ripple cancellation effect. For the proposed multiphase SCPC, F_S is determined by the supply voltage

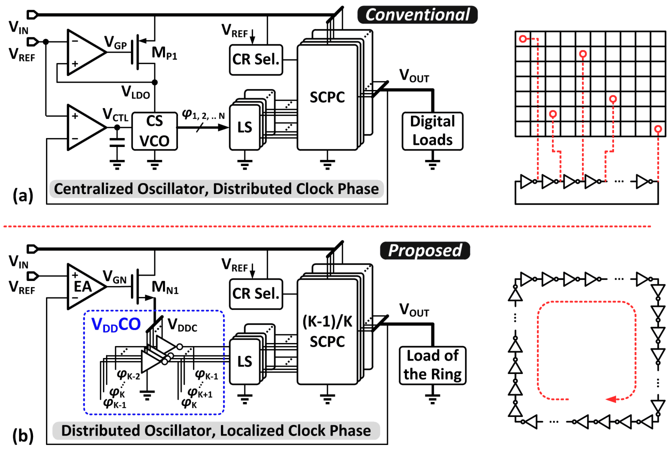


Fig. 4. System architectures of (a) conventional and (b) proposed multiphase SCPC.

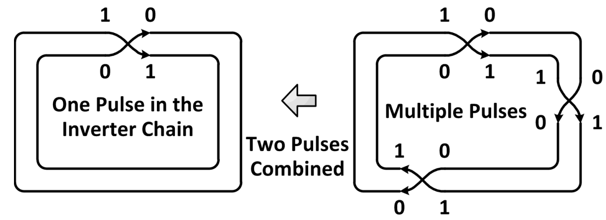


Fig. 5. Conceptual diagram of multiple pulses in a long inverter chain.

of the VCO (V_{DDC}), which is in turn controlled by the error amplifier (EA) through comparing V_{OUT} with V_{REF}. The VCO consists of many VCO cells that are distributed evenly along the perimeter of the chip, and the proposed distributed V_{DD}-controlled oscillator (V_{DD}CO) is driven by the nMOS buffer. The localized clock phases are the outputs of the distributed inverters among the VCO cells. Note that each current VCO cell is driven by its previous VCO cell, and the phase differences among the cells are significantly reduced. Hence, more phases can be used. Meanwhile, the proposed SCPC can realize the conversion ratios (CRs) of 1/2, 2/3, and 3/4 (($K-1$)/K)) upon the command of the CR selector.

For the distributed ring oscillator architecture, the power cells can either be distributed (as implemented in this design) or gregarious. When the power cells are distributed, the process and temperature gradients across the chip and the mismatches in *IR* drop from the supply to each delay cell may result in phase mismatches and larger voltage ripple. Nevertheless, with reduced equivalent parasitic inductors and resistors, smaller output voltage ripples are still expected. In addition, when the power cells are distributed, the overall switching frequency reflects the averaged process and temperature variations of the whole chip. In other words, the process and temperature gradients are embedded into the output frequency of the ring oscillator. In this sense, the distributed scheme might be more immune to process variations.

A. Phase Number Selection

Modifying the current phase number of 123 into other numbers can be easily achieved through minor revisions of the chip layout. When the phase number is large already, say 100+, the exact number of phases becomes less important as the output ripple is small enough. Besides, more phases means more inverters in the ring oscillator that limit the maximum output frequency. One potential problem is exciting multiple pulses in a very long inverter chain, like having multiple waves running through a soccer stadium, as illustrated in Fig. 5. The output frequency of the oscillator will be several times higher than that of the designed single-pulse case. However, no multiple pulsing is observed in the measurement results. The explanation is as follows. Assume that there are multiple pulses in the inverter chain. One pulse will catch up with its preceding pulse due to noise sooner or later, and the pulses will then coalesce. Finally, only one pulse will remain in the chain.

B. Phase Mismatch

Although phase mismatch could be reduced because of the distributed ring oscillator, phase mismatch could still occur due to the process, supply, and temperature gradients. It is obvious that the most serious phase mismatches occur at the power cells that are located at the corners, because the routing lengths of these four inverters are longer than those of the other inverters. To simulate the phase mismatch effects, one 5-fF capacitor is intentionally added to one of the inverters in the V_{DD}CO, as shown in Fig. 6. The 5-fF capacitor results in 80 ps longer in inverter delay, which is 30% of the duration of one phase. As shown in Fig. 6(a), the simulated output voltage ripple without phase mismatch for the 123-phase converter is only 65 μV, but V_{OUT} drops 2.6 mV after a phase mismatch of Ph$\langle 1\rangle$. The delay between the V_{OUT} drop and the phase mismatch is caused by the delays of the level shifter (LS) and the gate drivers. A circuit model that imitates the effect conservatively is shown in Fig. 6(b). Although the phase mismatch occurs only at Ph$\langle 1\rangle$, all the power cells are actually delayed by this phase mismatch. Therefore, when one power cell is not switched punctually due to phase mismatch, it is modeled as disconnecting the input source from the load. The switch S_O is turned OFF for the duration of the additional delay, which is 80 ps in this case. A 3.7-mV V_{OUT} variation is observed as shown in Fig. 6(c). In this conservative model, the V_{OUT} variation can be calculated by

$$\Delta V_{\mathrm{OUT}} = V_{\mathrm{OUT}}(1 - e^{-\Delta t_d/\tau}) \tag{1}$$

where Δt_d is the phase mismatch time, $\tau = R_L C_L$ is the time constant of the output node, and C_L includes the capacitance of the flying capacitors that are connected to the output node and the intrinsic capacitance from the load.

C. Global Routing Considerations

The converter ring was designed using a 65-nm 1-poly-8-metal low-leakage (LL) process with metal 8 being the only thick metal. We targeted at making the converter ring slim fit for the load, with a width of only 120 μm. Since lower metal layers are all reserved for the flying capacitors C_F using

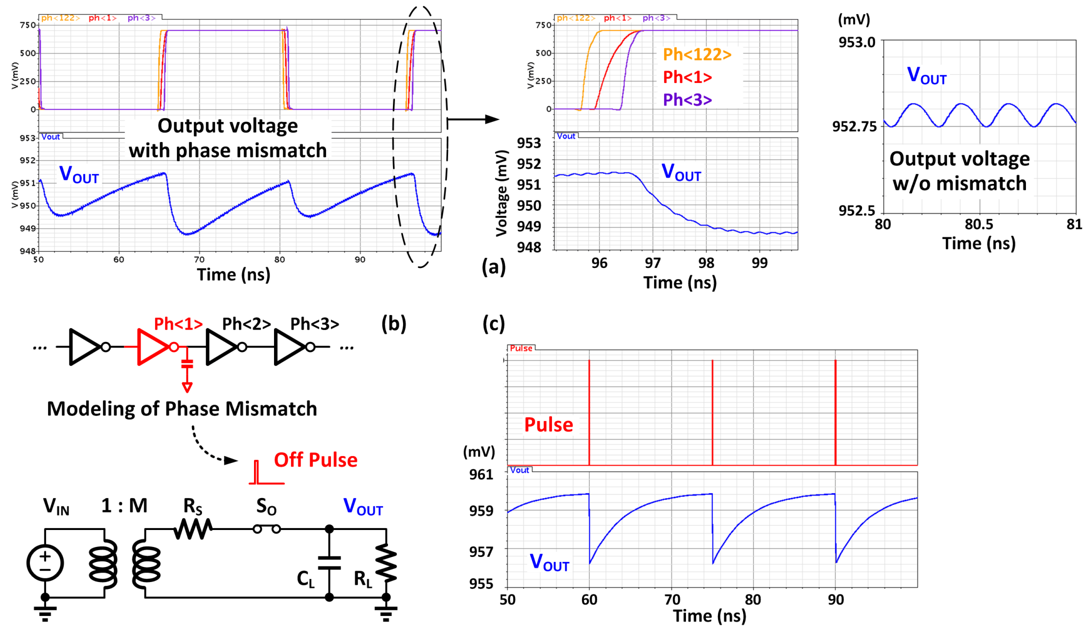


Fig. 6. (a) Simulated output voltage waveforms with and without phase mismatch. (b) Circuit model of phase mismatch. (c) Output waveform with the proposed model.

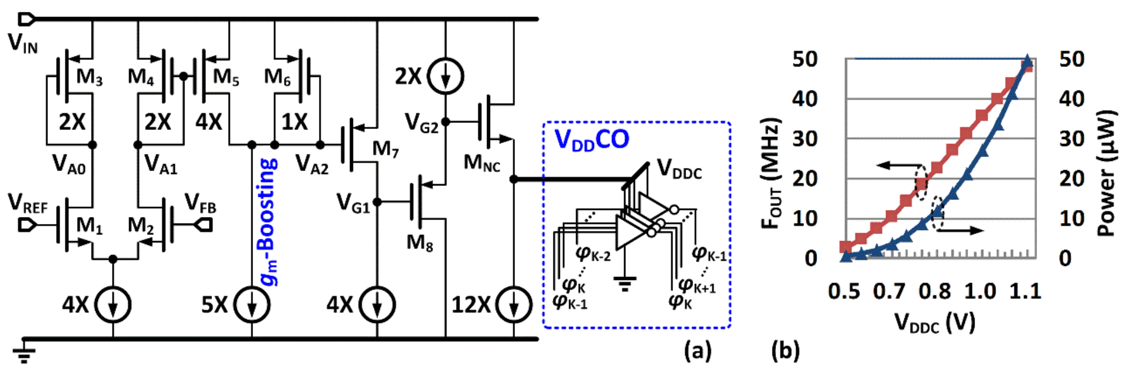


Fig. 7. (a) Schematic of the EA and V_{DD}CO. (b) Simulated output frequency and power consumption versus the control voltage V_{DDC}.

stacked MIM and MOM capacitors, the thick metal 8 layer is used for the three high-current routings of the input (V_{IN}), the output (V_{OUT}), and the Gnd terminals, assisted by the aluminum (Al) layer for pads that has a comparable sheet resistance and current handling capability as the thick metal. Besides, metal 1 with contacts to the substrate is also used for the Gnd path. Metal 2 is used for the internal supply rails (V_{DDL} and V_{SSH}) that conduct much less current, and metal 3 is used for the internal signal V_{DDC}.

III. Circuit Implementations

A. V_{DD}-Controlled Oscillator

With reference to Fig. 7(a), the EA with an nMOS source-follower buffer stage is used to drive the V_{DD}CO with VCO cells that are distributed around the ring and localized to every SCPC power cell. This makes the V_{DD}CO free of matching and routing problems. The simulation results in Fig. 7(b) show that the output frequency F_{OUT} of the V_{DD}CO is approximately linearly proportional to V_{DDC}. The proposed V_{DD}CO is more power efficient than the conventional CS VCO for the following reasons. The power consumption of a ring oscillator is given by

$$P_{VCO} = C_P \cdot V_{DD}^2 \cdot F_{OUT} \tag{2}$$

where C_P is the parasitic capacitance of the oscillator. To obtain the same maximum F_{OUT} with the same number of inverter stages, the CS VCO needs a higher V_{DD} than that of the V_{DD}CO because for each stage, it has two more current sources and thus larger parasitic capacitance. For lower F_{OUT}, the power consumption of a CS VCO decreases linearly as its V_{DD} is fixed, while that of the V_{DD}CO decreases at a cubic rate, as can be explained by taking a closer look at Fig. 7(a). As the V_{DD}CO is driven by the source-follower M_{NC} that handles all the current of the V_{DD}CO, the power consumption of the V_{DD}CO including M_{NC} is given by

$$P_{V_{DD}CO} = C \cdot V_{DD}^2 \cdot F_{OUT} \cdot \frac{V_{IN}}{V_{DDC}} = C \cdot V_{DDC} \cdot F_{OUT} \cdot V_{IN} \tag{3}$$

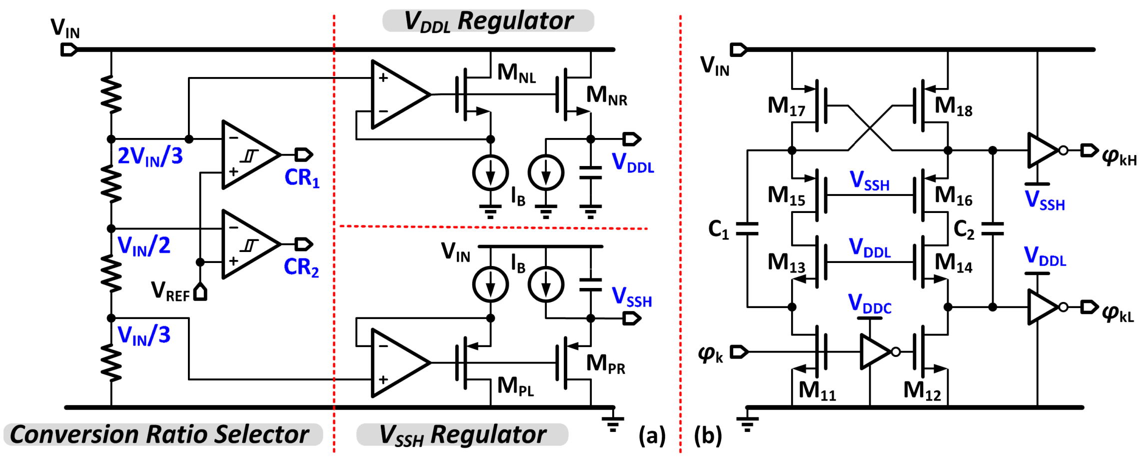


Fig. 8. Schematics of (a) CR selector and two internal rail voltage regulators and (b) LS dealing with three voltage domains.

with $V_{\text{DD}} = V_{\text{DDC}}$. Thus, the power consumption of the V_{DD}CO including M_{NC} decreases at a square rate with respect to V_{DDC} and F_{OUT}, as F_{OUT} is approximately linearly proportional to V_{DDC}.

B. High-Speed Error Amplifier

The high-speed EA, as shown in Fig. 7(a), consists of a differential input stage, a g_m-boosting stage, a gain stage, and two buffer stages. M_5 and M_6 form the g_m-boosting stage [15], to improve the dc gain without introducing additional low-frequency poles [16]. The dc gain of the EA is calculated as

$$A_{\text{EA}} \approx g_{\text{m2}} \cdot \frac{1}{g_{\text{m4}}} \cdot g_{\text{m5}} \cdot \frac{1}{g_{\text{m6}}} \cdot g_{\text{m7}} \cdot r_{\text{O7}} = 8 \cdot g_{\text{m2}} \cdot r_{\text{O7}} \tag{4}$$

where the boosting gain is 8 V/V. The final buffer stage M_{NC} drives the V_{DD}CO that can be modeled as a relatively large capacitive load in parallel with an adaptive resistive load. In heavy load conditions, F_{OUT} increases and the V_{DD}CO will draw more current from M_{NC} and lower the output impedance of the V_{DDC} node, and the corresponding pole shifts to higher frequencies. Hence, the V_{DDC} node is automatically adaptively biased by driving the V_{DD}CO, which improves stability for the output-pole-dominated case. With V_{IN} ranging from 1.6 to 2.2 V, all the transistors in this design are low-voltage (1.2 V) devices. Thus, all the internal nodes of the EA have pole frequencies in the gigahertz range. The input of the EA is connected to the nearest point of the V_{OUT} network by assuming that the V_{OUT} information can spread fast enough across the chip with wide metals, and even faster if an on-chip power grid is available.

During the startup process, the converter tends to operate at a higher F_S. Eventually, V_{G2} is equal to V_{IN}, M_8 is in deep subthreshold region, V_{G1} is close to V_{IN}, the gate-to-drain voltage of M_8 is large, and M_8 is vulnerable to breakdown. To solve this problem, M_8 should be a high-voltage I/O device. A better solution is to replace M_8 with a super source follower [17], which not only reduces the risk of breakdown but also increases the speed of the EA.

C. Internal Supply Rail Generators and Conversion-Ratio Selector

As shown in Fig. 8(a), two internal supply rails, V_{DDL} and V_{SSH}, are employed so that 1.2-V devices can be used and switching loss is reduced at the same time. The internal rails do not need to have very accurate values; hence, V_{DDL} and V_{SSH} are generated by the replica regulators that have outputs equal to $2V_{\text{IN}}/3$ and $V_{\text{IN}}/3$, respectively, derived from the resistor divider of V_{IN}. Each replica regulator consumes only 7.5 μA.

Two hysteresis comparators with built-in offset compare V_{REF} with $2V_{\text{IN}}/3$ and $V_{\text{IN}}/2$ to determine the CR for the $(K-1)/K$ SCPC. High-voltage (2.5-V) devices have to be used because the supply voltage of the comparators is V_{IN}. The outputs of the CR selector, CR_1 and CR_2, are then shifted to the voltage domains of [V_{DDL}, Gnd] and [V_{IN}, V_{SSH}] that power up the SCPC power cells using only 1.2-V devices.

D. Three-Domain Level Shifter

Every clock phase needs one energy-efficient LS that has short propagation delay. Fig. 8(b) shows our proposed improved LS that efficiently converts the signal from the input domain of [V_{DDC}, Gnd] to the output domains of [V_{IN}, V_{SSH}] and [V_{DDL}, Gnd] simultaneously in one conversion. Cascoding M_{13}–M_{16} with gate biases of V_{DDL} and V_{SSH} can prevent device breakdown. Although the variation of V_{DDC} would affect the propagation delay of the LS, it is acceptable to have longer delay at lower V_{DDC} since the switching frequency is also lower.

E. Power Cell of the SCPC

As derived in [7], the efficiency of the SCPC is linearly proportional to $V_{\text{OUT}}/(\text{CR} \times V_{\text{IN}})$ when switching loss is ignored. Thus, more voltage CRs would result in a flatter efficiency curve covering a wider input/output voltage range [18]. A simplified schematic of the power cell of the $(K-1)/K$ SCPC is shown in Fig. 9(a). For CR = 1/2, only C_{F1} is used as the flying capacitor, and C_{F2} and C_{F3} are connected between V_{IN} and V_{OUT} and serve as C_L. For CR = 2/3, C_{F1} and C_{F2} are

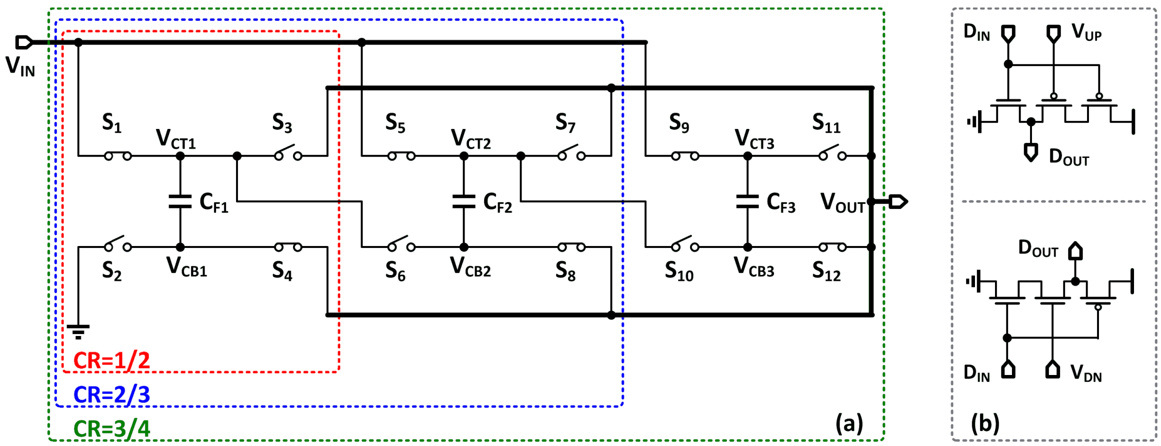


Fig. 9. (a) Simplified schematic of the $(K-1)/K$ SCPC. (b) Schematic of the 3T-based inverters.

TABLE I
SUMMARY OF THE OPERATION OF THE SWITCHES FOR EACH CR

CR	CR = 1/2		CR = 2/3		CR = 3/4	
Phase	*Charge*	*Discharge*	*Charge*	*Discharge*	*Charge*	*Discharge*
S1	**ON**	OFF	**ON**	OFF	**ON**	OFF
S2	OFF	**ON**	OFF	**ON**	OFF	**ON**
S3	OFF	**ON**	OFF	OFF	OFF	OFF
S4	**ON**	OFF	**ON**	OFF	**ON**	OFF
S5	**ON**	**ON**	**ON**	OFF	**ON**	OFF
S6	OFF	OFF	OFF	**ON**	OFF	**ON**
S7	OFF	OFF	OFF	**ON**	OFF	OFF
S8	**ON**	**ON**	**ON**	OFF	**ON**	OFF
S9	**ON**	**ON**	**ON**	**ON**	**ON**	OFF
S10	OFF	OFF	OFF	OFF	OFF	**ON**
S11	OFF	OFF	OFF	OFF	OFF	**ON**
S12	**ON**	**ON**	**ON**	**ON**	**ON**	OFF

flying capacitors, and only C_{F3} is used as C_L. For CR = 3/4, all C_{F1}, C_{F2}, and C_{F3} are used as flying capacitors.

The connections of the switches for each CR are summarized in Table I. In particular, S_3 switches only when CR = 1/2; S_7 switches only when CR = 2/3; S_6 switches when both CR = 2/3 and 3/4; and S_9–S_{12} switch only when CR = 3/4. In this configuration, the flying capacitors are connected in series in the discharging phase that has lower equivalent capacitances. Thus, although more capacitors are used for larger CRs, the output capability of each CR is similar.

To realize nonoverlapped timing and consequently to eliminate the shoot-through current and the reverse current, three-transistor (3T)-based inverters are used to drive the switches S_1–S_{12}, as shown in Fig. 9(b). The 3T inverters that drive the nMOS (pMOS) switches consist of two pMOS (nMOS) to turn ON the switches slowly. Meanwhile, if the additional terminal V_{UP} or V_{DN} is controlled by another signal, the 3T inverter driving the nMOS can be considered as a single-side NOR gate, and that driving the pMOS is a single-side NAND gate.

Fig. 10 shows the full schematic of the power cell of the $(K-1)/K$ SCPC. The clock phase φ_K comes from the previous power cell, and is applied to the current power cell as φ_{K+1} after one inverter delay. In one power cell, C_{F1}, C_{F2}, and C_{F3} are 13 pF each, and are constructed by stacking MOS, MOM, and MIM capacitors. Turn-on sequences of the switches are also controlled by the 3T inverters through sensing the voltages on the C_{F1}, $C_{F2,}$ and C_{F3} either top or bottom plate. For example, S_3 (S_6) will be turned ON when V_{CT1} is low at CR = 1/2 (2/3), and S_{10} and S_{11} will be turned ON when V_{CT2} is low at CR = 3/4.

IV. CONTROL-LOOP ANALYSIS

There are many benefits of designing the dominant pole of a voltage regulator to be its output pole p_O, as discussed in [19]. To satisfy the stability requirement, the UGF of the internal-pole-dominated case has to be a few decades lower than p_O. On the other hand, the UGF of the p_O-dominated case is higher than p_O. Thus, the maximum achievable UGF of the p_O-dominated case is higher than that of the internal-pole-dominated case. Furthermore, with a large load capacitor at the

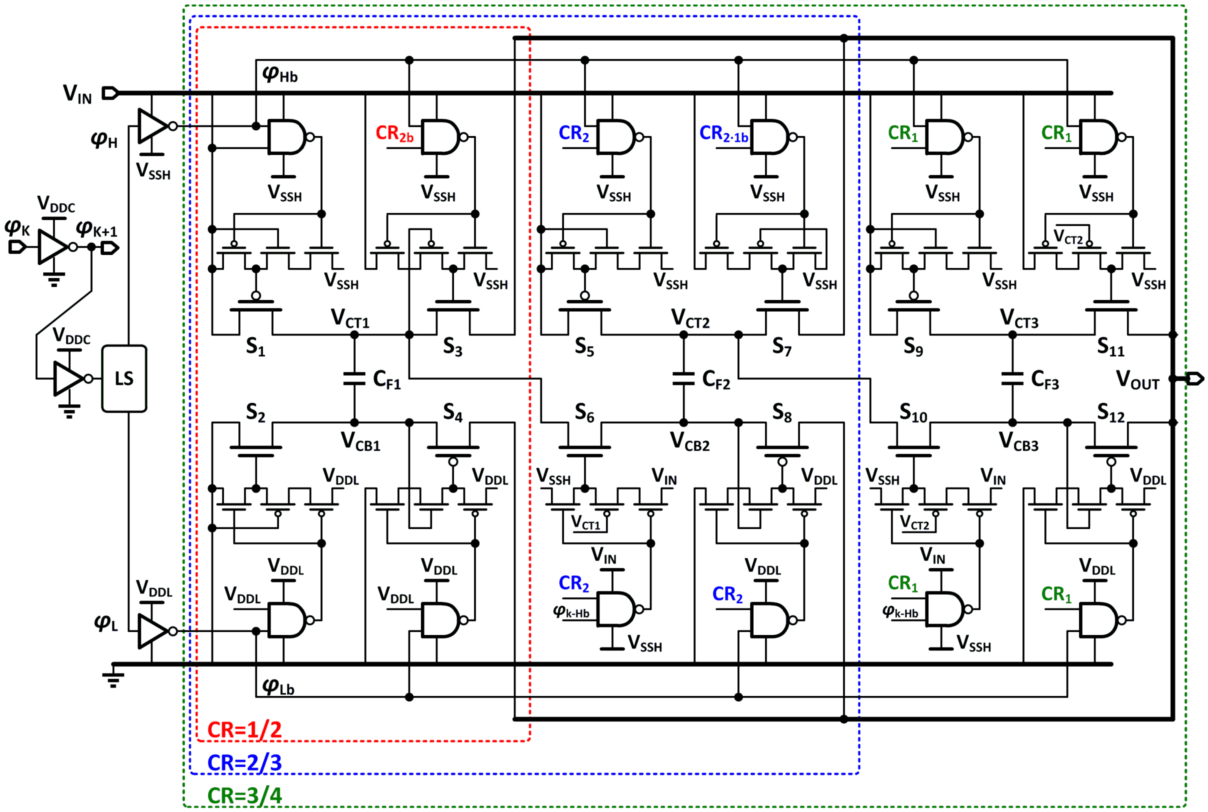


Fig. 10. Schematic of unit cell of the $(K-1)/K$ SCPC.

output node, the output voltage ripple is smaller. More importantly, capacitive digital loadings would result in a large load capacitor that gives a low p_O frequency, making the internal-pole-dominated case more difficult to be compensated for.

A. Conventional Loop Design

A rule-of-thumb design of the UGF of the control loop of a switch-mode power converter is 1/6 of the switching frequency F_S to satisfy linearization requirement [20]. The linearized small-signal model becomes inaccurate when the frequencies of interest approach one-half of F_S in the single-phase converter case [21]. In a conventional SCPC, the dominant pole of the control loop is located at the VCO input node. If the converter switches to operate in pulse-frequency modulation (PFM), then F_S is low at the light load condition. Thus, the bandwidth is limited and the transient response is slow. To achieve fast load response, an additional 3.3 GHz clock was proposed in [5] to trigger a fast loop that bypasses the main integrator loop when the output voltage drops too much. However, the reference tracking speed of a converter that implements DVS depends on the bandwidth of the main loop, not the fast loop. Moreover, such a high-frequency clock may not be available in low-power applications such as Internet-of-things and wearable devices.

In [7] and [8], the steady-state characteristics of the power stage of an SCPC are modeled as

$$V_{\mathrm{OUT}} = M \cdot V_{\mathrm{IN}} - a_0 \frac{I_{\mathrm{OUT}}}{C_F F_S} \tag{5}$$

where M is the CR, a_0 is a topology-dependent charge multiplier coefficient, and C_F is the value of the total flying capacitance. However, the factor F_S that is being modulated as in the denominator makes it hard to be linearized. Thus, the frequency-to-output gain K_{SCPC} is dependent on the operating point. In [22], the SCPC was modeled by its delivered charge (or current), and thus F_S was modeled to be linearly proportional to I_{OUT}. This assumption is valid in a constant-load-current mode, or when V_{OUT} is well regulated with a resistive load.

B. AC Response Simulation and Discussion

The small-signal model of the converter ring is shown in Fig. 11(a). Two locations are identified to compute the frequency responses of the EA, the power stage, and the loop gain function. Since the SCPC stage is a switching stage and the frequencies of interest are close to or higher than the switching frequency, the averaged model may not be accurate at high frequencies. Therefore, to verify the validity of the averaged model of our multiphase converter ring, time-domain ac response simulations have been carried out, such that the transfer functions of the continuous part and the switching part can be investigated separately, and then be considered together to arrive at the total ac characteristics. Fig. 11(b) shows the simulation results with heavy and light loads. At heavy load, for example, $R_L = 10\ \Omega$, and F_{OUT} is regulated to around 33 MHz. Small signals of 40 $\mathrm{mV_{PP}}$ at different frequencies were injected at V_{G2}, and the one at 150 MHz was attenuated by the power stage to appear at V_{OUT} with a magnitude

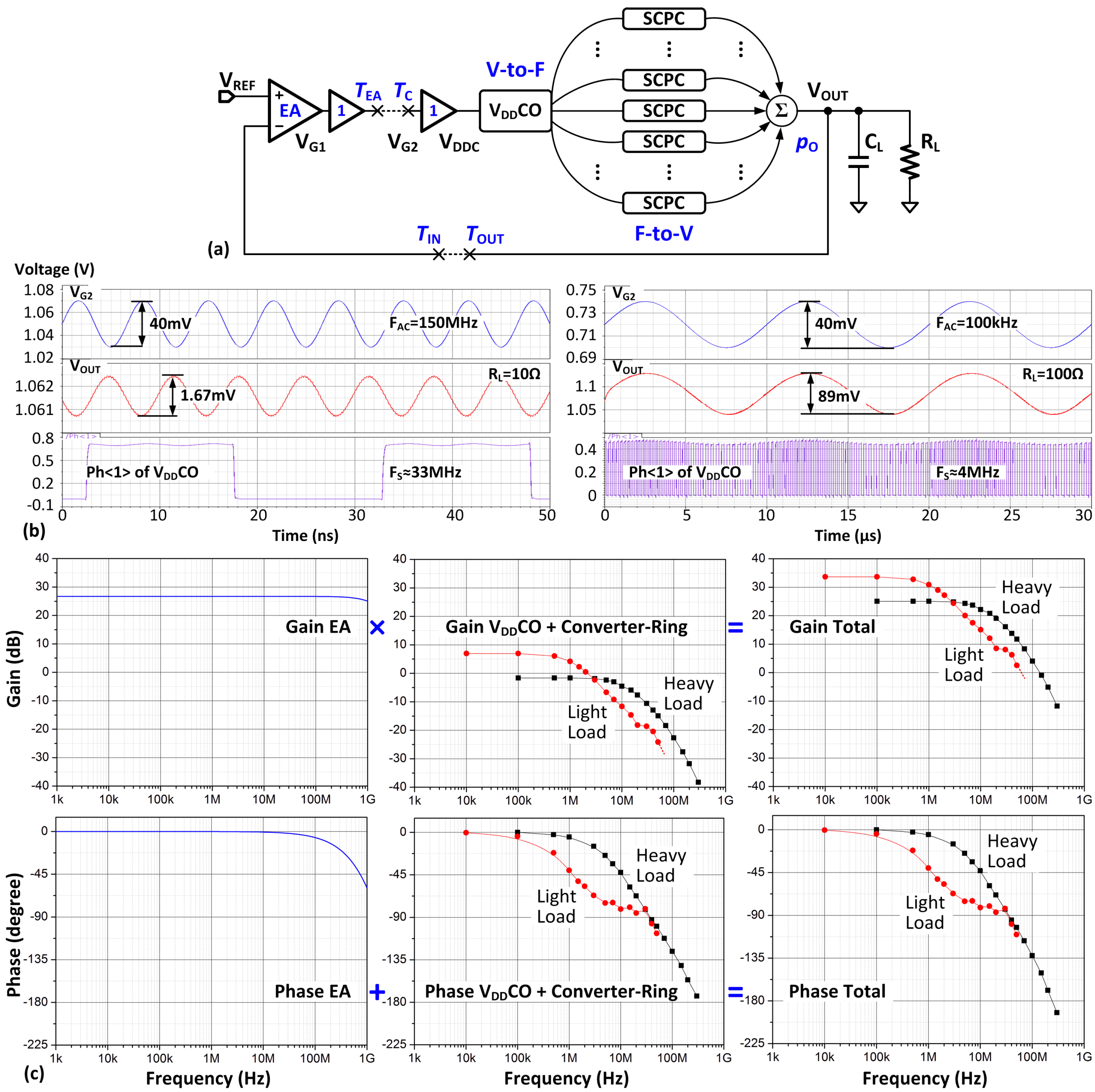


Fig. 11. (a) Small-signal model of the pseudocontinuous-time multiphase SCPC. (b) Time-domain ac response simulation waveforms with $R_L = 10$ and 100 Ω, respectively. (c) Bode plots of the EA, the power stage with V_{DD}CO, and the total loop response.

of 1.67 mV_{PP}. Other frequency points were obtained similarly, and are compiled in Fig. 11(c). At light load, for example, $R_L = 100$ Ω, and F_{OUT} is regulated to around 4 MHz. The small signal of 40 mV_{PP} at 100 kHz injected at V_{G2} emerged at V_{OUT} with a magnitude of 89 mV_{PP}. Similarly, other frequency points were obtained, and are compiled in Fig. 11(c). The EA has a dc gain of 27 dB that is insensitive to the change in the load. A few high-frequency poles in the gigahertz range can be detected by the phase shift that occurs in the 100 MHz–1 GHz range. The converter ring with the V_{DD}CO has a low-frequency output pole that changes with the load and a second pole at slightly higher than 100 MHz that is caused by the switching nature of the power stage. In terms of stability, the worst case occurs at heavy load with a UGF of 150 MHz and a phase margin of 30°. Note that the UGF of 150 MHz is achieved with the converter switching at 33 MHz only, meaning that the UGF can be a few times higher than the switching frequency.

The VCO here (V_{DD}CO) does not contribute any low-frequency pole to the loop, unlike it does in a phase-locked loop, because the small-signal information here is the frequency and not the phase. Nevertheless, the multiphase switched-capacitor power stage can be considered as a phase-integrating block that converts both phase and frequency information into V_{OUT} or I_{OUT} (depending on how it is modeled). Here, V_{DDC} is a low-impedance node and the associated pole p_C is located at high frequency, while the output pole p_O becomes the dominant pole. Using the multiphase topology, the control loop can respond to external variations at every fraction of the switching period (T), which

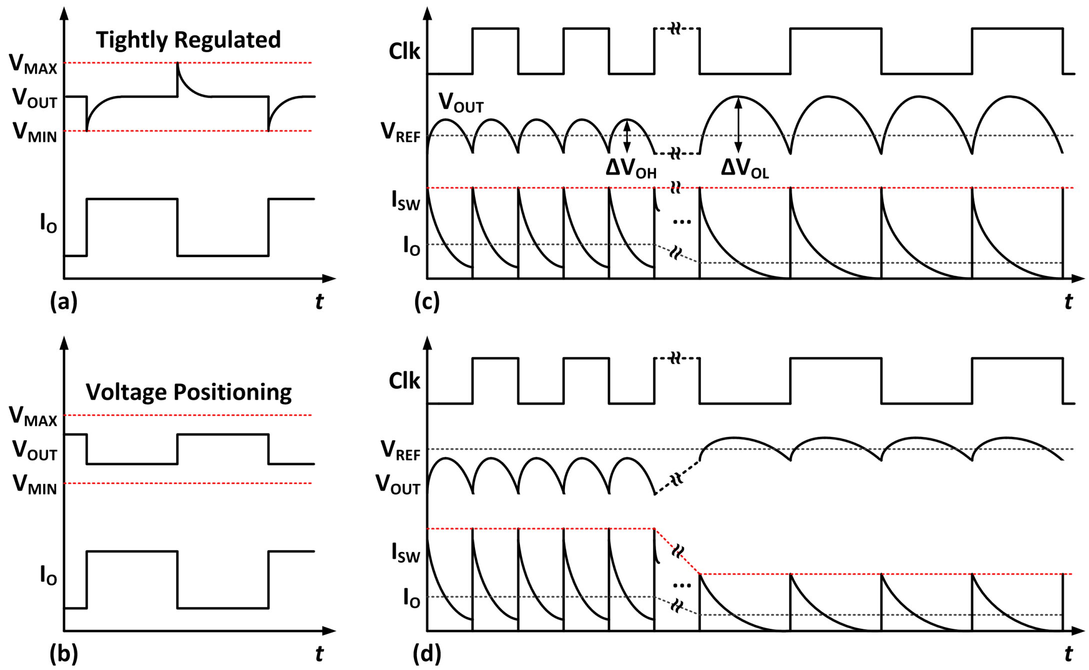


Fig. 12. Conceptual waveforms of V_{OUT} and I_{OUT}. (a) With tightly regulated V_{OUT}. (b) With voltage positioning. (c) Ripple increases when I_{OUT} decreases with PFM. (d) Ripple decreases when I_{OUT} decreases with PFM and voltage positioning.

is $T/123$ in our case. In fact, the discrete-time power stage can be considered as a pseudocontinuous-time power stage.

Although the effect of bandwidth extension has been studied for the multiphase PWM buck converters [23]–[25], it is not applicable for the PFM case of this design. As discussed in [23], in a PWM controller, the EA output voltage is sampled by the PWM comparator (which compares the EA output and the ramp signal), and the perturbation on the EA output will generate harmonics at the PWM comparator output due to sampling effect. The low-frequency harmonic components that limit the control-loop bandwidth can be canceled by the multiphase topology. However, the canceling effects will be degraded due to phase mismatch. Thus, previous works on multiphase buck converters achieved only a UGF slightly higher than F_S [24], limited by the PWM comparator's sampling effect [23] and the small number of phases. On the other hand, there is no such sampling process in the PFM control of this design. When V_{DDC} changes, the frequency (or the inverter delay) of every phase will be changed simultaneously that ensures pseudocontinuous-time operation. Therefore, the multiphase switched-capacitor dc–dc converter ring could achieve a UGF a few times higher than F_S.

C. Voltage Positioning

Voltage positioning [26] is employed to reduce the V_{OUT} peak-to-peak variation during load transient and also to relax the dc loop-gain requirement. As shown by the conceptual waveforms of the V_{OUT} and I_{OUT} in Fig. 12(a) and (b), the voltage droop is the intentional drop of the output voltage as it drives a load. Employing the droop in a voltage regulation circuit increases the headroom for load transients.

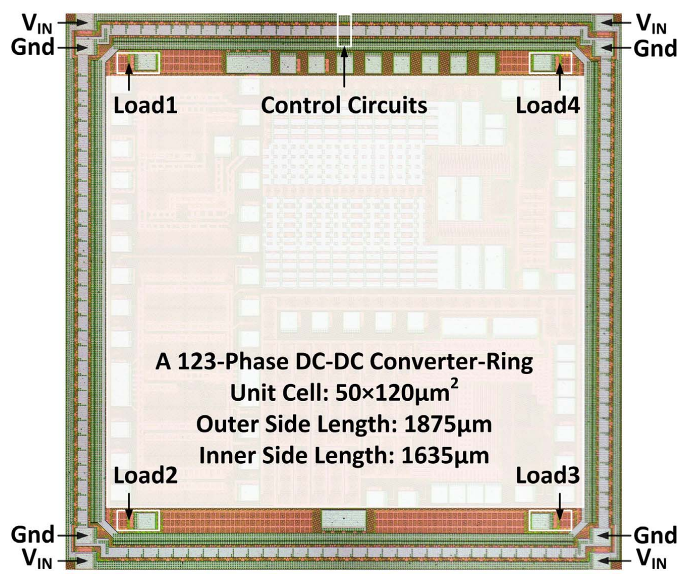


Fig. 13. Chip micrograph of the dc–dc converter ring.

From Fig. 12(c) and (d), we found that the voltage positioning scheme can also lower the output voltage ripple at light load conditions. Fig. 12(c) shows the case of an SCPC working in PFM without voltage positioning, and the ripple increases when I_{OUT} decreases. This is because the peak current that transfers charge between the flying capacitor and C_L is decided by V_{DS} of the switches and is constant in the tightly regulated case [27]. On the other hand, the peak current that transfers the charge between two capacitors drops in the voltage positioning case as shown in Fig. 12(d), as V_{OUT} in light load increases and V_{DS} of the switches is lower. Note that

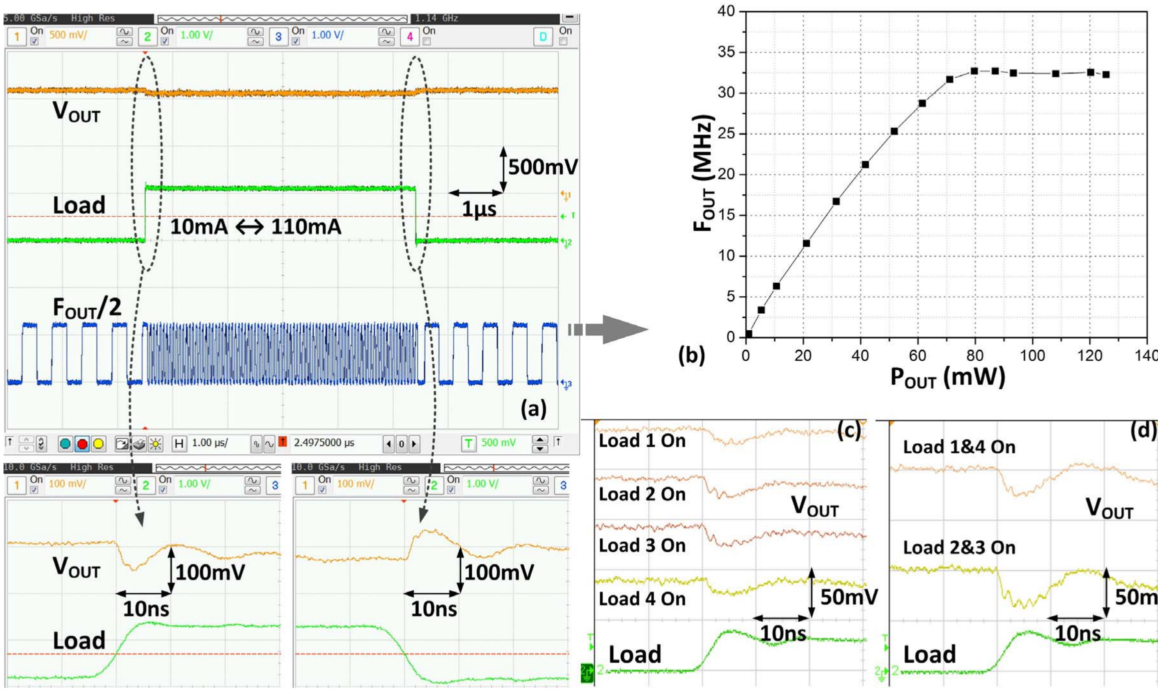


Fig. 14. (a) Measured load transient response with switching all on-chip loads. (b) Switching frequency versus output power of the converter ring. (c) Load transient with switching one of the on-chip loads. (d) Load transient with switching two of the on-chip loads.

with the joint effects of PFM and voltage positioning, the output ripples are not monotonous with respect to the load current.

V. Measurement Results

The converter ring was fabricated in a 65-nm LL CMOS process with an effective area of 0.84 mm^2 excluding the load and pads for testing. The chip micrograph is shown in Fig. 13. The power cell measures 50×120 μm^2. The length of the outer side of the converter ring is 1875 μm, and the length of the inner side is 1635 μm. At each corner of the chip, an on-chip load of 25 mA with edge times of 100 ps was fabricated for measuring fast transients and proof of concept. The loads have not been placed in the center of the chip because the shaded silicon area is occupied by other projects.

Fig. 14(a) shows the measured load transient waveforms sensed from the large pad on the bottom center of the chip. The measurement conditions were $V_{\mathrm{IN}} = 2$ V, $V_{\mathrm{OUT}} = 1.1$ V, CR $= 2/3$, and the four on-chip loads worked together to give a load current that changed between 10 and 110 mA. The output voltage undershoot and overshoot ΔV_{OUT} were within 58 mV. The loop response time is around 3 ns, corresponding to a UGF of over 100 MHz, without using an extra gigahertz clock. The V_{DD}CO frequency, as shown in Fig. 14(b), was measured to be ranging from 250 kHz to 33 MHz for the entire load range. To investigate the impacts of the V_{OUT} sensing location and the load location on the measured waveforms, the on-chip loads on different corners were partially enabled during the load transient measurements, and the V_{OUT} waveforms are compared and shown in Fig. 14(c) and (d). The V_{OUT} waveforms show only small differences in undershoot, while the loop response time remains unchanged.

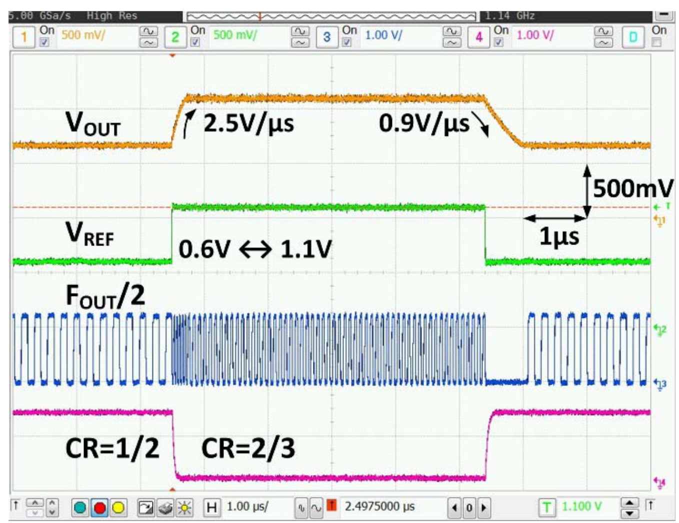


Fig. 15. Measured reference tracking waveforms of the converter ring.

Fig. 15 shows the measured reference-tracking waveforms with V_{REF} changing between 0.6 and 1.1 V, and with CR switching automatically between 1/2 and 2/3. A load capacitor C_L of 2 nF is integrated on-chip to mimic the load capacitance of the microprocessor. The reference up-tracking and down-tracking speeds were 2.5 and 0.9 V/μs, respectively, making this design fit for fast DVS. Note that the reference-tracking speed depends on the value of C_L, and more time is needed to drive larger capacitive digital loads.

Since the output ripple of the proposed SCPC is quite small and hard to be measured by an oscilloscope that has a noise

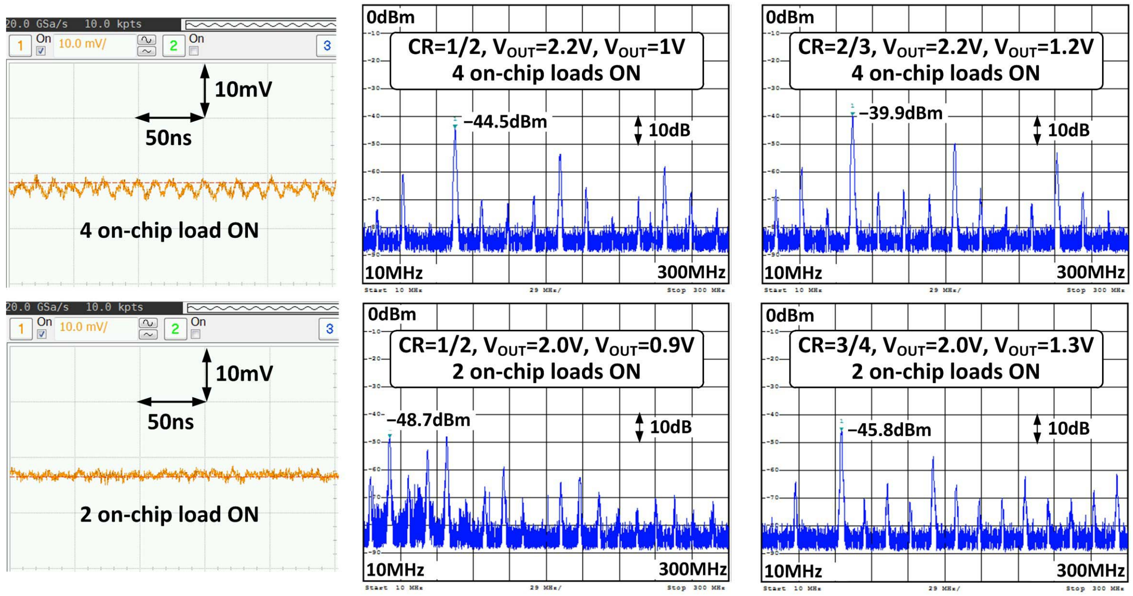


Fig. 16. Measured steady-state output ripple and output spectrum at different conditions.

TABLE II
COMPARISON WITH STATE-OF-THE-ART BULK-CMOS SCPC WORKS

Publication	[28] JSSC '11	[12] ISSCC '12	[5] ISSCC '13	[6] JSSC '14	This work
Process	32nm SOI	90nm	65nm	22nm Tri-gate	**65nm**
Conv. Ratios	2/3, 1/2, 1/3	1/2, 2/3	1/3, 2/5	1/2, 2/3, 4/5, 1	**1/2, 2/3, 3/4**
Phase No.	32	41	18	8	**123**
V_{IN}	2	1.2-2V	3-4V	1.225V	**1.6-2.2V**
V_{OUT}	0.5-1.2V	0.7V	1V	0.45-1V	**0.6-1.2V**
F_S @η_{Peak}	300MHz*	50MHz	N/A	250MHz	**33MHz**
η_{Peak}	79.8%	81%	74.3%	82.7%	**80.0%**
Power Density	860mW/mm^2	39mW/mm^2	190mW/mm^2	250mW/mm^2	**180mW/mm^2**
$P_{OUT,Max}$	600mW*	10mW	162mW	25mW	**152mW**
Ripple Range	N/A	3.8mV-N/A	N/A	43mV-125mV*	**2.2mV-30mV**
ΔV_{OUT} @T_{Edge}	N/A	N/A	76mV @50ps	N/A	**58mV @100ps**
DVS Speed	N/A	N/A	N/A	N/A	**2.5V/µs**

*Estimated from figure.

floor of several millivolts, a spectrum analyzer that has a relatively lower noise floor was used instead. Fig. 16 shows the output ripples in the time domain and the output spectrums at different CRs with all and half of the on-chip loads being turned on. To obtain the peak-to-peak ripple voltage (V_{PP}) from the spectrums, the amplitudes and frequencies of the highest three tones were recorded and Fourier transform was performed, and the corresponding output ripple amplitudes were obtained. The measured output ripples with one, two, three, or four on-chip loads are summarized in Fig. 17. As discussed in Section IV-C, the output ripple amplitude depends on the load current, switching frequency, and control loop characteristics. Lower V_{PP} was observed at the boundaries of changing CRs, as V_{DS} of the switches was reduced in these cases. Ground routing and noise coupling affect the ripple amplitude. The minimum ripple measured is 2.2 mV$_{PP}$, and the maximum is below 30 mV$_{PP}$.

Measured efficiencies for different load and CR conditions are shown in Fig. 18. All CRs give a similar output capability, and the optimum I_{Load} is around 50 mA. The maximum power density of 180 mW/mm^2 was measured at CR = 1/2 and V_{IN} = 2.2 V. The power density decreases at low V_{IN} (and results in a high CR of 3/4), and the lowest peak power density was measured to be 130 mW/mm^2 at which the efficiency was 75.8%. Fig. 19 shows the measured efficiencies versus V_{OUT}, with V_{IN} = 2.0 V and I_{Load} = 50 mA. Fig. 20 shows the measured efficiencies versus V_{IN} with I_{Load} = 50 mA, V_{REF} = 0.9 V for CR = 1/2 and 2/3, and V_{REF} = 1.1 V for

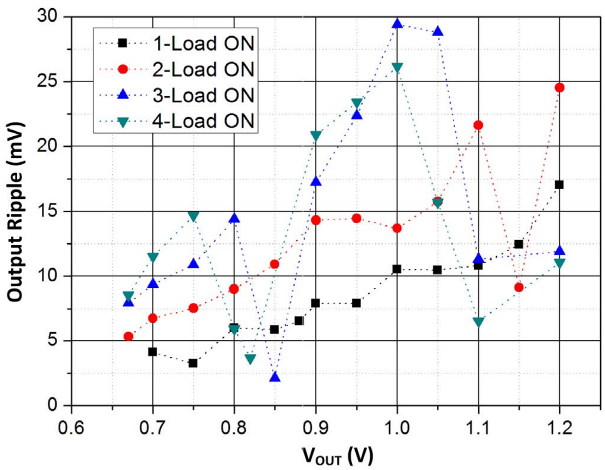


Fig. 17. Measured output ripple voltages with different on-chip loading conditions.

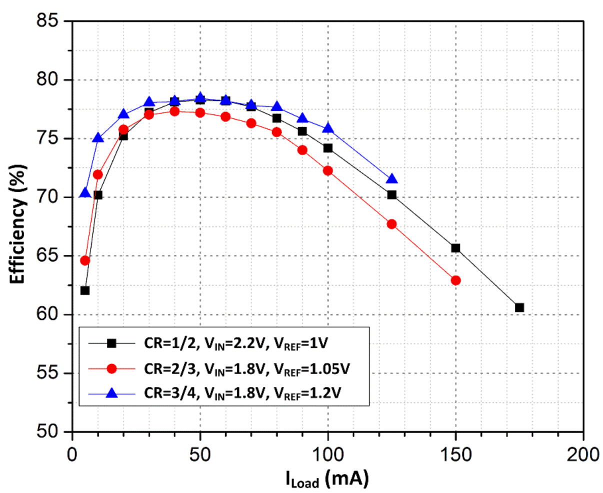


Fig. 18. Measured efficiencies for different CRs.

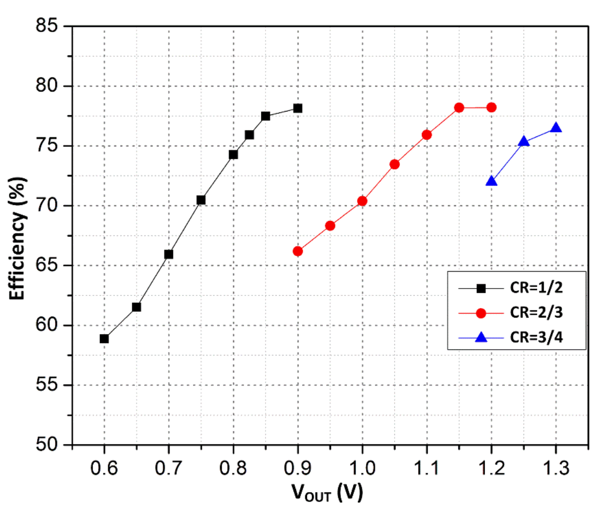


Fig. 19. Measured efficiencies versus V_{OUT}, at $V_{\mathrm{IN}} = 2.0$ V and $I_{\mathrm{Load}} = 50$ mA.

CR = 2/3 and 3/4, respectively. The peak efficiency is 80% at the power density of 66.6 mW/mm^2.

Performance comparison with state-of-the-art bulk-CMOS SCPC designs is listed in Table II. This paper has a minimum output voltage ripple of 2.2-mV and achieves small ΔV_{OUT} during load transients with fast switching on-chip loads. Moreover, V_{OUT} tracks V_{REF} in the submicrosecond range that is good for fast DVS applications.

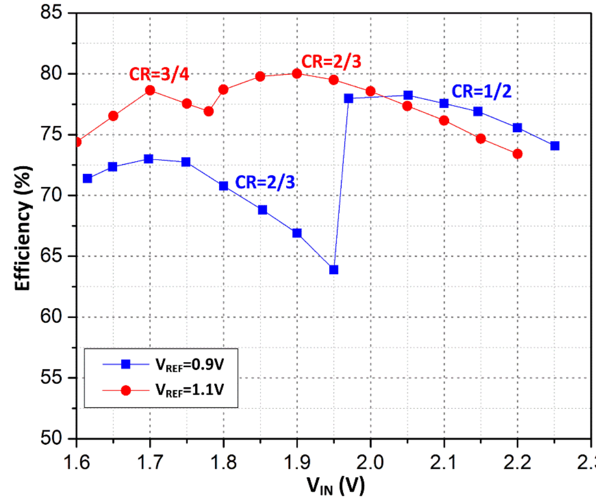


Fig. 20. Measured efficiencies versus V_{IN} with $I_{\mathrm{Load}} = 50$ mA, and $V_{\mathrm{REF}} = 0.9$ and 1.1 V, respectively.

VI. Conclusion

By adopting the multiphase ring-shaped topology and the V_{DD}CO, this is the first attempt to design an SCPC with a control-loop UGF higher than the switching frequency. The dominant pole is designed to be located at the output node of the SCPC driven with a high-speed EA. As a result, fast-transient response is obtained without using high switching frequency nor an additional high-frequency (GHz) clock. Special layout considerations have been taken for global routing and bonding, such that the proposed scheme can be easily incorporated into existing SoC applications. We further anticipate that a multiphase dc–dc converter grid could be a possible power management solution for a multicore processor array with flip-chip packaging.

References

[1] W. Kim, D. Brooks, and G.-Y. Wei, "A fully-integrated 3-level DC-DC converter for nanosecond-scale DVFS," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 206–219, Jan. 2012.

[2] S. S. Kudva and R. Harjani, "Fully integrated capacitive DC–DC converter with all-digital ripple mitigation technique," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1910–1920, Aug. 2013.

[3] Y. Lu *et al.*, "A 123-phase DC-DC converter-ring with fast-DVS for microprocessors," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.

[4] Y. Lu, W.-H. Ki, and C. P. Yue, " An NMOS-LDO regulated switched-capacitor DC–DC converter with fast-response adaptive-phase digital control," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1294–1303, Feb. 2016.

[5] H.-P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm^2 at 73% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2013, pp. 372–373.

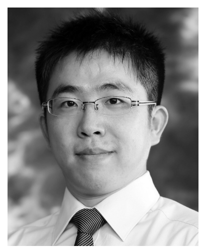
[6] R. Jain *et al.*, "A 0.45–1 V fully-integrated distributed switched capacitor DC-DC converter with high density MIM capacitor in 22 nm Tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[7] W.-H. Ki, F. Su, and C.-Y. Tsui, "Charge redistribution loss consideration in optimal charge pump design," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2005, pp. 1895–1898.
[8] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.
[9] T. M. Andersen *et al.*, "A feedforward controlled on-chip switched-capacitor voltage regulator delivering 10W in 32nm SOI CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.
[10] W.-H. Ki *et al.*, "Analysis and design strategy of on-chip charge pumps for micro-power energy harvesting applications," in *VLSI-SoC: Advanced Research for Systems on Chip*. Berlin, Germany: Springer, 2012, pp. 158–186.
[11] J. Jiang, Y. Lu, C. Huang, W.-H. Ki, and P. K. T. Mok, "A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2015, pp. 1–3.
[12] G. V. Piqué, "A 41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2012, pp. 98–100.
[13] G. Villar-Piqué, H. J. Bergveld, and E. Alarcon, "Survey and benchmark of fully integrated switching power converters: Switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4156–4167, Sep. 2013.
[14] K. A. Bowman, C. Tokunaga, T. Karnik, V. K. De, and J. W. Tschanz, "A 22 nm all-digital dynamically adaptive clock distribution for supply voltage droop tolerance," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 907–916, Apr. 2013.
[15] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.
[16] M. Ho, K. N. Leung, and K.-L. Mak, "A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2466–2475, Nov. 2010.
[17] P. R. Gray, P. Hurst, S. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed. New York, NY, USA: Wiley, 2009, pp. 212–214.
[18] Y. Lu, W.-H. Ki, and C. P. Yue, "Input-adaptive dual-output power management unit for energy harvesting devices," in *Proc. IEEE 55th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2012, pp. 1080–1083.
[19] Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65ns-response-time 3.01ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2014, pp. 306–307.
[20] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY, USA: Springer Science+Business Media, 2001.
[21] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," in *Proc. IEEE Power Electron. Specialists Conf.*, Jun./Jul. 1981, pp. 349–369.
[22] Y. K. Ramadass, A. A. Fayed, and A. P. Chandrakasan, "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.
[23] Y. Qiu, K. Yao, Y. Meng, M. Xu, F. C. Lee, and M. Ye, "Control-loop bandwidth limitations for multiphase interleaving buck converters," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Exposit. (APEC)*, vol. 2. Feb. 2004, pp. 1322–1328.
[24] S. Xiao, W. Qiu, G. Miller, T. X. Wu, and I. Batarseh, "Adaptive modulation control for multiple-phase voltage regulators," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 495–499, Jan. 2008.
[25] F. C. Magallanes, D. Aguglia, C. A. de Martins, and P. Viarouge, "Review of design solutions for high performance pulsed power converters," in *Proc. 5th Int. Power Electron. Motion Control Conf. (EPE/PEMC)*, Sep. 2012, pp. DS2b.14-1–DS2b.14-6.
[26] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.
[27] L. G. Salem and R. Jain, "A novel control technique to eliminate output-voltage-ripple in switched-capacitor DC-DC converters," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2011, pp. 825–828.
[28] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

Yan Lu (S'12–M'14) received the B.Eng. and M.Sc. degrees in microelectronic engineering from the South China University of Technology, Guangzhou, China, in 2006 and 2009, respectively, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2013.

He was an IC Design Engineer with Silicon Laboratories, Shenzhen, China, in 2011. He was a Visiting Scholar with the IC Design Group, University of Twente, Enschede, The Netherlands, in 2013. He has been an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, since 2014. His current research interests include analog and mixed-signal circuit design, wireless power transfer, fully integrated power converters, and voltage regulators.

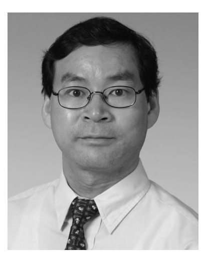
Dr. Lu served as a Technical Program Committee Member of several IEEE conferences and a Reviewer for many journals/conferences. He was a recipient of the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2013–2014.



Junmin Jiang (S'09) received the B.Eng. degree in electronic and information engineering from Zhejiang University, Hangzhou, China, in 2011. He is currently pursuing the Ph.D. degree at The Hong Kong University of Science and Technology, Hong Kong.

He was an Assistant Researcher Intern with the LS&C Department, Philips Research China, Shanghai, China, in 2013. He joined the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, in 2013. He was a Visiting Scholar with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China, in 2015. His current research interests include power IC design, especially in switched capacitor power converter design.

Mr. Jiang was a recipient of the Analog Devices Inc. Outstanding Student Designer Award and the ISSCC Student Travel Grant Award in 2015.



Wing-Hung Ki (S'86–M'91) received the B.Sc. degree in electrical engineering from the University of California at San Diego, La Jolla, CA, USA, in 1984, the M.Sc. degree in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 1985, and the Ph.D. degree in electrical engineering from the University of California at Los Angeles, Los Angeles, CA, USA, in 1995.

In 1992, he joined Micro Linear Corporation, San Jose, CA, USA, as a Senior Design Engineer with the Department of Power and Battery Management, where he was involved with the design of power converter controllers. In 1995, he joined The Hong Kong University of Science and Technology, Hong Kong, where he is currently a Professor with the Department of Electronic and Computer Engineering. His current research interests include power management circuits and systems, switched-inductor and switched-capacitor power converters, low dropout regulators, wireless power transfer for biomedical implants, and analog IC design methodologies.

Prof. Ki served as an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II—EXPRESS BRIEFS from 2012 to 2013 and as a member of the International Technical Program Committee of the IEEE International Solid-State Circuits Conference from 2010 to 2014.