A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection

Yan Lu, *Member, IEEE*, Yipeng Wang, *Student Member, IEEE*, Quan Pan, *Member, IEEE*, Wing-Hung Ki, *Member, IEEE*, and C. Patrick Yue, *Fellow, IEEE*

***Abstract*—A fully-integrated low-dropout regulator (LDO) with fast transient response and full spectrum power supply rejection (PSR) is proposed to provide a clean supply for noise-sensitive building blocks in wideband communication systems. With the proposed point-of-load LDO, chip-level high-frequency glitches are well attenuated, consequently the system performance is improved. A tri-loop LDO architecture is proposed and verified in a 65 nm CMOS process. In comparison to other fully-integrated designs, the output pole is set to be the dominant pole, and the internal poles are pushed to higher frequencies with only 50 μA of total quiescent current. For a 1.2 V input voltage and 1 V output voltage, the measured undershoot and overshoot is only 43 mV and 82 mV, respectively, for load transient of 0 μA to 10 mA within edge times of 200 ps. It achieves a transient response time of 1.15 ns and the figure-of-merit (FOM) of 5.74 ps. PSR is measured to be better than -12 dB over the whole spectrum (DC to 20 GHz tested). The prototype chip measures 260×90 μm^2, including 140 pF of stacked on-chip capacitors.**

***Index Terms*—Amplifier, flipped voltage follower, low dropout regulator (LDO), power supply rejection (PSR).**

I. Introduction

SWITCH MODE power converters in power management units generate high levels of switching noise. A linear regulator can filter out the noise and provide a clean supply voltage to drive noise-sensitive circuits such as trans-impedance amplifiers (TIA) or low-noise amplifiers (LNA) in wireline and/or wireless communication front-end systems [1], [2], as well as critical paths in VLSI chips [3]. Therefore, high performance low dropout regulators, commonly known as LDOs, are indispensable in a system-on-a-chip (SoC) due to their ripple free, fast transient response and good power supply rejection (PSR) characteristics. In general, differential analog circuit loads need an LDO with high PSR; digital circuit loads need an LDO with fast load transient response [3]; while single-ended analog/RF circuit loads need an LDO with both high PSR and fast line and load transient responses [2].

Off-chip LDOs or on-chip LDOs with off-chip decoupling capacitors are commonly used for rejecting supply noise. However, an off-chip capacitor cannot effectively reduce the supply noise at the point-of-load, due to the bond-wire effect.

Manuscript received June 24, 2014; revised September 26, 2014 and November 03, 2014; accepted December 02, 2014. Date of publication January 06, 2015; date of current version February 23, 2015. This paper was recommended by Associate Editor A. Mazzanti.

Y. Lu was with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China. He is now with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China (e-mail: yanlu@umac.mo).

Y. Wang, Q. Pan, W.-H. Ki, and C. P. Yue are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2014.2380644

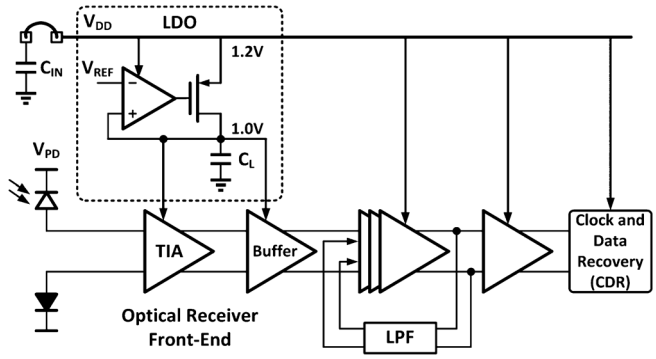


Fig. 1. An optical receiver with embedded LDO.

Thus, fully-integrated area-efficient LDOs are highly desirable for point-of-load power delivery and multi-voltage systems [4]. In addition, supplying power to individual noise-sensitive and/or noise-generating building blocks with separate LDOs can improve the system performance considerably. Fig. 1 shows an LDO embedded in an optical receiver that helps improving the front-end sensitivity [5], [6]. The single-ended (or pseudo-differential) TIA has only one photodetector, and supply variations would degrade its sensitivity severely [2]. The data rate of an optical receiver could be over 10 Gb/s, the digital output buffer and/or clock and data recovery circuits will generate GHz on-chip noises, thus, the LDO needs to have PSR for the frequency range from DC to 20 GHz in such system.

With a large off-chip output capacitor, say 1 μF, small ripples due to load transients can be achieved and bandwidth can be extended using techniques such as load-current dependent boost current [7], dynamically-biased buffer impedance attenuation (BIA) [8], adaptively-biased super current mirror [9], and multiple small-gain stages in nanometer processes [10]; while high PSR can be achieved using feed-forward ripple cancellation techniques [11]. However, for fully-integrated LDOs, large load capacitors are no longer available, and both transient response and PSR will degrade significantly. Small form factor and low cost are the driving factors for full integration. Many fully-integrated LDOs with limited on-chip capacitance (a.k.a. capacitorless LDOs) have been proposed in the past decade [12]–[19]. To make a comparison, a figure-of-merit (FOM) of LDOs is defined in [13] and widely adopted by other researchers. It reads

$$\mathrm{FOM} = T_{\mathrm{R}} \frac{I_{\mathrm{Q}}}{I_{\mathrm{MAX}}} = \frac{C \times \Delta V_{\mathrm{OUT}}}{I_{\mathrm{MAX}}} \times \frac{I_{\mathrm{Q}}}{I_{\mathrm{MAX}}}, \qquad (1)$$

where I_{Q} is the quiescent current, and the response time T_{R} is a function of the total on-chip capacitance C, load-transient glitches of the output voltage ΔV_{OUT} and the maximum load current I_{MAX}. To achieve full integration, some specifications have to be sacrificed. In [13], a folded cascode stage was used to increase the DC gain, and a considerably large current (6%) was

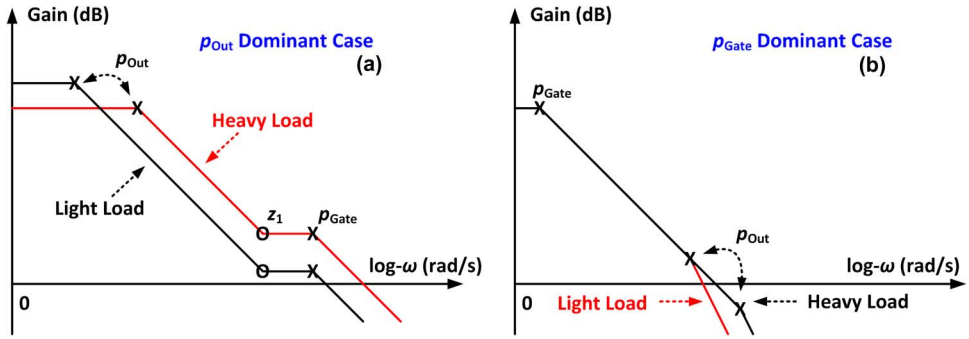


Fig. 2. Magnitude plot of a generic LDO with two low frequency poles: (a) with p_{Out} being its dominant pole; and (b) with p_{Gate} being its dominant pole.

TABLE I
LDO CATEGORIZATION BY DOMINANT POLE LOCATION

Integration	With Off-Chip Cap.		Fully-On-Chip	
Dominant pole	p_{Gate}	p_{Out}	p_{Gate}	p_{Out}
Process Scaling	No	Yes	No	Yes
Limit on $I_{O,Min}$	Yes	No	Yes	No
UGF	×	–	–	√
Transient ΔV_{OUT}	–	√	×	–
PSR	–	√	×	–
I_Q	√	–	√	×

used to move the non-dominant poles to high frequencies, resulting in a mediocre current efficiency of 94%. A cascode structure with 600 mV dropout voltage was employed in [14] that significantly improved the PSR performance, but also considerably degraded the transient response. A single transistor control LDO based on the flipped voltage follower (FVF) topology, which is the simplest FVF architecture, provided stable voltage regulation for a wide range of output capacitor values including the output capacitor-less case in [15], but it was sensitive to process, voltage and temperature (PVT) variations, and was not fast enough with 160 mV load-transient undershoots observed. The FVF with folded cascode stage was also employed in [16] with slew-rate enhancement circuit that responded to 100 ns load-transient edges; however, its PSR degraded to 0 dB before reaching 1 MHz. An ultra-fast response comparator-based regulator in 45 nm SOI process was proposed in [17] that consumed 12 mA of quiescent current and required an on-chip deep-trench capacitor of 1.46 nF, and its intrinsic 10 mV ripple is not suitable for supplying the RF/analog front-end systems. [25] was using a non-inverting gain stage for higher loop gain and Miller compensation for stability, but only provides simulations results with 100 ns edge times.

From the literature review above, we conclude that there is a gap between the performances of fully-integrated and non-fully-integrated LDOs. An area-efficient LDO with ultra-fast response and full spectrum PSR is in high demand. In this research, a tri-loop LDO is proposed that achieves an FOM of 5.74 ps and PSR of better than −12 dB over the whole spectrum (DC to 20 GHz tested). The basic idea of this design is to take advantage of the advanced processes by keeping most of the limited available capacitance at the output node for better PSR and transient response, and pushing the internal poles to be higher than the unity-gain frequency (UGF) by using buffer impedance attenuation (BIA) and flipped voltage follower (FVF) techniques. Consequently, the performance is improved with process scaling. In the proposed tri-loop architecture, the BIA technique is integrated into the FVF structure with the output node being the dominant pole, and a tri-input error amplifier (EA) is proposed to improve the DC accuracy.

This paper is organized as follows. Considerations of the proposed architecture and the existing circuit techniques are discussed in Section II. Circuit implementation, stability and PSR analyses of the proposed tri-loop LDO are discussed in Section III. Measurement results of the prototype chips are presented in Section IV, followed by conclusions in Section V.

II. ARCHITECTURAL CONSIDERATIONS

A. Dominant Pole Considerations

For an LDO, the largest capacitors are the output filtering capacitor $C_{\rm L}$ and the parasitic gate capacitor $C_{\rm g}$ of the power MOS transistor. Hence, there are at least two low-frequency (LF) poles on the left-half-plane (LHP): the pole at the output node $p_{\rm Out}$, and the pole at the gate of the power MOS $p_{\rm Gate}$, as sketched in Fig. 2 with either $p_{\rm Out}$ or $p_{\rm Gate}$ being the dominant pole. The pole $p_{\rm Out}$ would shift to a lower frequency when the load resistance increases and vice versa. Basically, LDOs with an off-chip filtering capacitor are designed to be $p_{\rm Out}$ dominant [7], [9]–[11], while all fully-integrated analog "capacitor-less" LDOs have an internal dominant pole $p_{\rm Gate}$ [12]–[16], [18], [19]. Thus, LDOs can be classified by the need for an off-chip capacitor or not, or they can be classified by being output-pole dominant or internal-pole dominant. Therefore, there are 4 combinations of which the pros and cons are summarized in Table I and discussed as follows.

There are many benefits in designing $p_{\rm Out}$ as the dominant pole by using most of the available capacitance at the output node. First of all, a larger output capacitor filters out power supply noise and glitches and serves as a buffer for load-transient current changes, resulting in a smaller $\Delta V_{\rm OUT}$. Second, as discussed in [20], because the output voltage is well regulated by the control loop at low frequency, and the noise is bypassed to ground by $C_{\rm L}$ at high frequency, the worst case PSR would occur at medium frequency. Thus, increasing both the output capacitance and the loop bandwidth (that is, the unity-gain frequency UGF) would improve the PSR. Third, $p_{\rm Out}$ moves to lower and lower frequency as the load current decreases, which is better for the loop stability comparing to the internal-pole dominant case. In fact, the zero-load condition is not even discussed in many output-capacitor-less designs, and instead, a minimum load current $(I_{\rm O,Min})$ is needed to satisfy stability requirements. If $C_{\rm L}$ is reduced to satisfy stability requirements, the high frequency PSR performance will be degraded, and is not acceptable in our application.

For the $p_{\rm Out}$ dominant case, pole-zero cancellation is usually used to extend the loop bandwidth and to enhance the stability. The LHP zero z_1 may be generated by the equivalent

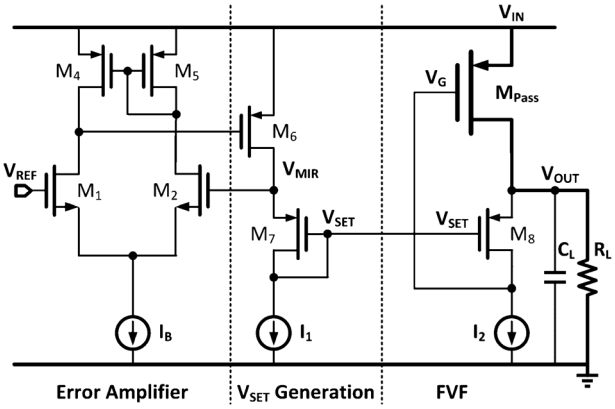


Fig. 3. The single-transistor-control LDO based on the FVF topology.

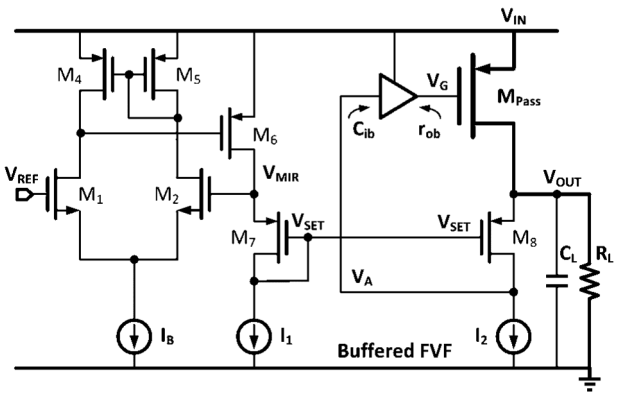


Fig. 4. The FVF based LDO with inserted buffer.

series resistance (ESR) of $C_{\rm L}$ or by a high-pass feedback network as proposed in [12]. Alternatively, the non-dominant pole $p_{\rm Gate}$ may be pushed to frequencies higher than the UGF by circuit techniques mentioned in [7]–[10]. The only drawback with the $p_{\rm Out}$ dominant case is that a relatively high quiescent current is needed to push the internal poles to higher frequencies. This requirement can be relaxed by using advanced processes that have lower parasitic capacitance. The transistors will have smaller feature sizes, and the internal poles could be moved to higher frequencies with the same bias current. At the same time, smaller $C_{\rm L}$ can be used and results in smaller chip area and higher UGF. To summarize, an LDO being $p_{\rm Out}$ dominant can benefit from the process scaling that is one of the most desirable characteristics in integrated-circuit design. The proposed architecture will be introduced in Section III.

B. Flipped Voltage Follower

The replica biasing technique is widely used in source-follower based or flipped-voltage-follower (FVF) based LDOs for supplying power to digital ICs with ultra-fast load-transient responses [21], [13]. The schematic of a single-transistor-control LDO based on FVF in [15] is shown in Fig. 3 as an example. This circuit can be divided into three parts: the error amplifier (EA), the $V_{\rm SET}$ generation and the flipped voltage follower. For simplicity, we assume $I_1 = I_2$ and $(W/L)_7 = (W/L)_8$. The mirrored voltage $V_{\rm MIR}$ is controlled to be equal to $V_{\rm REF}$ by the EA, and $V_{\rm SET}$ is generated from $V_{\rm MIR}$ by the diode-connected $\rm M_7$. Followed by a FVF, $V_{\rm OUT}$ is set by $V_{\rm SET}$ through $\rm M_8$, and it is a mirrored voltage of $V_{\rm MIR}$. In the FVF, $\rm M_8$ act as a common-gate amplifying stage from $V_{\rm OUT}$ to $V_{\rm G}$.

Obviously, there are two low-frequency poles ($p_{\rm Gate}$ and $p_{\rm Out}$) in the FVF when a relatively large on-chip $C_{\rm L}$ (ranging from 100 pF to 1 nF) is used to handle the load current that ranges from 0 to 10 mA. This topology is very difficult (if not impossible) to be stable if $p_{\rm Out}$ is the dominant pole. In [15], $p_{\rm Gate}$ dominant is adopted using a small $C_{\rm L}$ (or even no $C_{\rm L}$). In [13], $p_{\rm Gate}$ dominant is also adopted with an ESR zero; adaptive voltage positioning by intentionally setting $V_{\rm OUT}$ to a lower value at heavy load was used. However, lower $V_{\rm OUT}$ is undesirable for analog loads.

Another issue associated with this structure is the DC accuracy of $V_{\rm OUT}$. The offset voltage between $V_{\rm REF}$ and $V_{\rm OUT}$ can be divided into two parts. First, there is an offset between $V_{\rm REF}$ and $V_{\rm MIR}$ that consists of systematic and random offsets of the EA. Second, the mismatches between the voltage mirror ($\rm M_7$ and $\rm M_8$) and the bias currents (I_1 and I_2) will generate an offset between $V_{\rm MIR}$ and $V_{\rm OUT}$. Hence, the FVF-based topology has low immunity to PVT variations. Moreover, the loop gain of the FVF is low, which results in poor load regulation. Nevertheless, due to its potential for fast transient response and low voltage characteristics, the FVF structure is used as the starting point, and improvements will be discussed in Section III.

C. Buffer Impedance Attenuation

To realize the LDO with $p_{\rm Out}$ dominant, $p_{\rm Gate}$ in Fig. 3 should be pushed to high frequency not only by using large bias current I_2 but also with additional circuitry. A buffer can be inserted between the gain stage with high output impedance and the power stage with large input capacitance [8], as shown in Fig. 4. The buffer presents low input capacitance to $V_{\rm A}$ and low output impedance to $V_{\rm G}$, pushing the two poles at $p_{\rm A}$ and $p_{\rm Gate}$ to high frequencies. In this design, the output capacitor $C_{\rm L}$ is 130 pF, the bias current I_2 is 20 μA, and the buffer consumes another 20 μA at light load (60 μA at heavy load), and all the above help pushing $p_{\rm Gate}$ to the GHz range. The remaining problem is the low DC accuracy of $V_{\rm OUT}$.

III. Proposed Tri-Loop Low-Dropout Regulator

In this research, a fully-integrated tri-loop low-dropout regulator designed in a 65 nm CMOS general purpose (GP) process is proposed to achieve ultra-fast transient response and full spectrum (DC to 20 GHz tested) power supply rejection with limited chip area, current budget and voltage headroom [22]. The transistor-level schematic is shown in Fig. 5.

A. Tri-Loop Architecture

To increase the DC accuracy of the FVF-based LDO, a third loop is introduced through using a tri-input EA. In previous architectures, only $V_{\rm MIR}$ is fed forward to generate $V_{\rm OUT}$, and $V_{\rm OUT}$ is not fed back to the EA. Now, the EA compares $V_{\rm REF}$ with both $V_{\rm MIR}$ and $V_{\rm OUT}$, and the W/L ratios of the three input transistors $\rm M_1$, $\rm M_2$ and $\rm M_3$ are $(\rm W/L)_1$: $(\rm W/L)_2$: $(\rm W/L)_3$ = 4: 1:3 such that $V_{\rm OUT}$ is computed to be

$$\left(V_{\rm REF} - \frac{1}{4}V_{\rm MIR} - \frac{3}{4}V_{\rm OUT}\right) \times {\rm A_{EA}} = V_{\rm OUT} \tag{2}$$

$$V_{\rm MIR} = V_{\rm OUT} + \Delta {\rm V}, \tag{3}$$

where $\rm A_{EA}$ is the gain of the EA (including the $V_{\rm SET}$ generation stage), and ΔV is the voltage difference between $V_{\rm MIR}$ and $V_{\rm OUT}$ due to PVT and load variations. By substituting (3) into (2), and assuming ${\rm A_{EA}} \gg 1$, we have

$$\begin{aligned} V_{\rm OUT} &= \frac{\rm A_{EA}}{1+{\rm A_{EA}}}V_{\rm REF} - \frac{\Delta {\rm V} \cdot {\rm A_{EA}}/4}{1+{\rm A_{EA}}} \\ &\approx V_{\rm REF} - \frac{\Delta {\rm V}}{4}, \end{aligned} \tag{4}$$

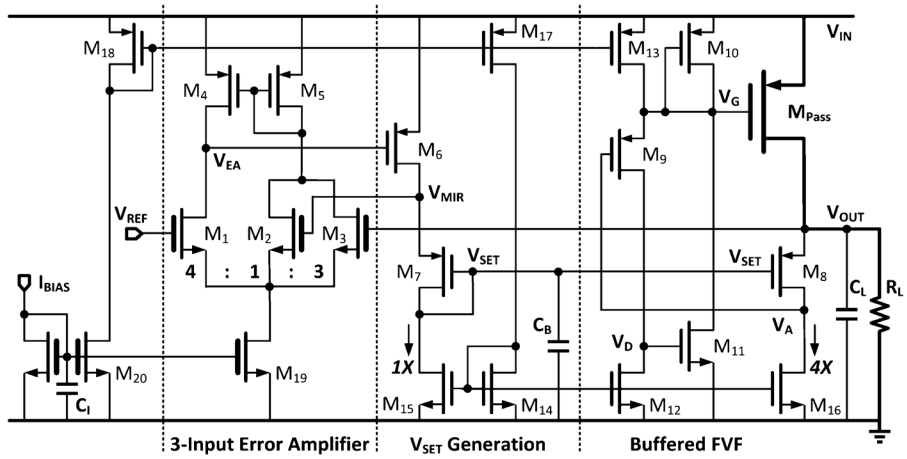


Fig. 5. Transistor level schematic of the proposed fully integrated tri-loop LDO.

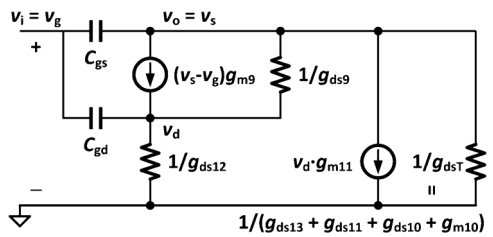


Fig. 6. Small-signal model of the buffer.

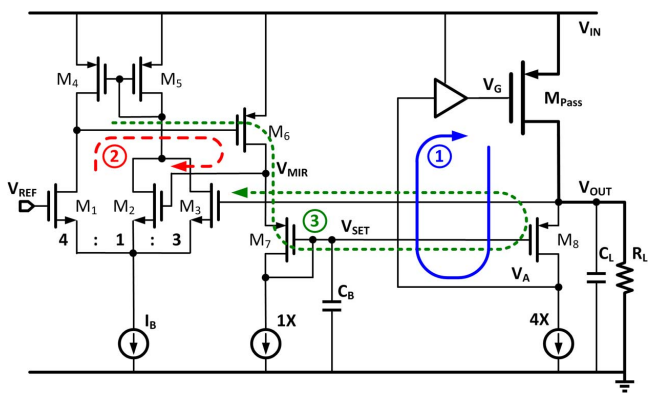


Fig. 7. Simplified diagram of the three loops in the proposed LDO.

$$V_{\mathrm{MIR}} = \frac{\mathrm{A_{EA}}}{1+\mathrm{A_{EA}}}V_{\mathrm{REF}} + \frac{3\Delta\mathrm{V}\cdot\mathrm{A_{EA}}/4}{1+\mathrm{A_{EA}}} + \frac{\Delta\mathrm{V}}{1+\mathrm{A_{EA}}} \approx V_{\mathrm{REF}} + \frac{3\Delta\mathrm{V}}{4}. \quad (5)$$

Therefore, V_{OUT} is closer to V_{REF} than V_{MIR} by setting the size ratio of $\mathrm{M_2}$ and $\mathrm{M_3}$ to be 1:3.

B. Circuit Implementation

Since the EA is not in the high-speed path, the input transistors of the EA and its tail current mirror are implemented with 2.5-V I/O devices for DC gain and ESD considerations. Different symbols are used to distinguish the I/O devices from the 1-V core devices in Fig. 5. All on-chip MOS capacitors are I/O devices to avoid gate leakage current if thin-oxide (1.0 V) devices are used. Transistors in the FVF stage are all thin-oxide devices for fast response. To suppress off-chip noise, a 2 pF C_{I} is added at the bias input node I_{Bias}, and may not be needed if I_{Bias} is generated on-chip. To save static current, the ratio of $\mathrm{M_7}$ and $\mathrm{M_8}$, and that of their bias currents, is set to be 1:4, as V_{SET} is in the low-speed path that does not need much current, but V_{A} is in the high-speed path and needs more current.

The buffer used for impedance attenuation consists of $\mathrm{M_9}$ through $\mathrm{M_{13}}$, and three parameters are of concern: the input capacitance C_{iB}, the output resistance r_{oB}, and the DC gain $\mathrm{A_B}$. The small-signal model of the buffer is shown in Fig. 6. The input capacitance of the circuit can be computed by noting that

$$C_{\mathrm{iB}}\Delta\mathrm{V_g} = C_{\mathrm{gs}}\Delta\mathrm{V_{gs}} + C_{\mathrm{gd}}\Delta\mathrm{V_{gd}}, \quad (6)$$

and in the small-signal limit, (6) can be rewritten as

$$C_{\mathrm{iB}} = (1 - v_{\mathrm{s}}/v_{\mathrm{g}})\cdot C_{\mathrm{gs}} + (1 - v_{\mathrm{d}}/v_{\mathrm{g}})\cdot C_{\mathrm{gd}}, \quad (7)$$

where C_{gs} and C_{gd} are the gate-to-source and gate-to-drain capacitances of $\mathrm{M_9}$. The voltage gains are calculated as

$$\mathrm{A_B} = \frac{v_{\mathrm{s}}}{v_{\mathrm{g}}} = \frac{1}{\left(1 + \frac{1}{\mathrm{A_1}} + \frac{2}{\mathrm{A_1A_2}}\right)} \quad (8)$$

with

$$\mathrm{A_1} = \frac{g_{\mathrm{m9}}}{g_{\mathrm{ds9}}} \quad (9)$$

$$\mathrm{A_2} = \frac{(g_{\mathrm{m11}} + g_{\mathrm{ds12}})}{g_{\mathrm{dsT}}} \quad (10)$$

$$g_{\mathrm{dsT}} = g_{\mathrm{m10}} + g_{\mathrm{ds10}} + g_{\mathrm{ds11}} + g_{\mathrm{ds13}}. \quad (11)$$

and

$$\frac{v_{\mathrm{d}}}{v_{\mathrm{g}}} = \frac{v_{\mathrm{d}}}{v_{\mathrm{s}}}\frac{v_{\mathrm{s}}}{v_{\mathrm{g}}} = -\frac{1}{\mathrm{A_2}}\frac{v_{\mathrm{s}}}{v_{\mathrm{g}}} = -\frac{\mathrm{A_1}}{\mathrm{A_1A_2} + \mathrm{A_2} + 2} \quad (12)$$

Here, $\mathrm{A_1}$ is the intrinsic gain of $\mathrm{M_9}$, and $-\mathrm{A_2}$ is the gain from the drain to the source of $\mathrm{M_9}$. Assume $\mathrm{A_1}$ and $\mathrm{A_2}$ to be much larger than 1, then $\mathrm{A_B} \approx 1$. Combining (7), (8) and (12), we have

$$C_{\mathrm{iB}} = \frac{\mathrm{A_2}+2}{\mathrm{A_1A_2} + \mathrm{A_2} + 2}C_{\mathrm{gs}} + \left(1 + \frac{\mathrm{A_1}}{\mathrm{A_1A_2} + \mathrm{A_2} + 2}\right)C_{\mathrm{gd}} \approx \frac{1}{\mathrm{A_1}}C_{\mathrm{gs}} + \left(1 + \frac{1}{\mathrm{A_2}}\right)C_{\mathrm{gd}} \approx C_{\mathrm{gd}}. \quad (13)$$

Since $\mathrm{M_9}$ operates in the saturation region, most of the channel charge is associated with the source, which means that C_{gs} is much larger than C_{gd}, and hence, C_{iB} is small. The output resistance of the buffer r_{oB} is given by

$$r_{\mathrm{oB}} = \frac{1}{\mathrm{A_3}(g_{\mathrm{m9}} + g_{\mathrm{ds9}}) + g_{\mathrm{dsT}}}, \quad (14)$$

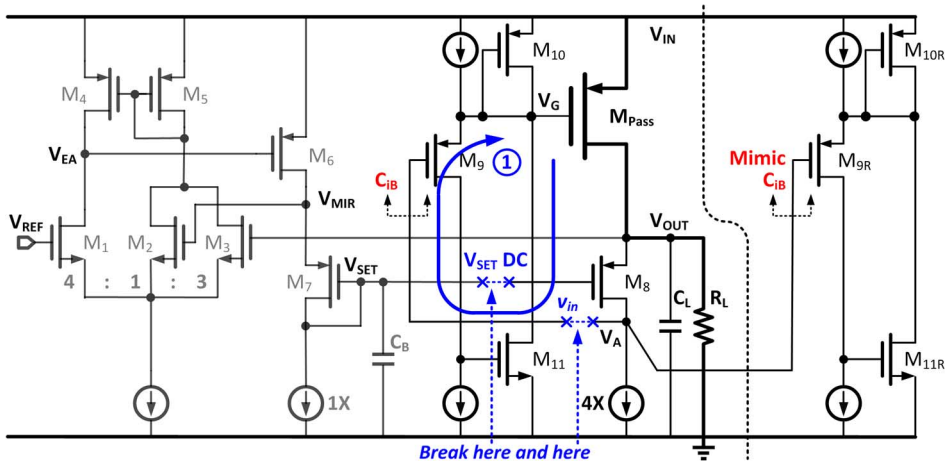


Fig. 8. Break Loop-1 with replica buffer to mimic its input capacitance.

where $A_3 = (g_{m11} + g_{ds12})/(g_{ds12} + g_{ds9})$. This gain needs to be increased to further attenuate r_{oB}. Note that g_{dsT} includes the term g_{m10} from M_{10}, and lowering r_{oB} by increasing g_{m10} also increases the pull-up capability of the buffer.

A fundamental design trade-off is identified between the DC gain and the frequency response: to satisfy the assumption that $A_1, A_2 \gg 1$, the channel length L of M_9 should be long for $A_1 \gg 1$, and the L of M_{11} should be long for $A_2 \gg 1$; to reduce C_{gs} and C_{gd}, L of M_9 and M_{11} should be short. In this design, the minimum L is used for M_9 and M_{11} for speed consideration, and M_{11} operates in the sub- or near-threshold region (in light or full load conditions, respectively) to give a larger g_{m11} to increase A_2 and A_3. The gate capacitance of M_{11}, which would generate an additional pole p_D at node V_D, is neglected in the analyses above. This non-dominant pole p_D is located in the GHz range as verified by the following AC simulations and transient measurements.

C. Stability Analyses

The signal paths of each loop are superimposed on the schematic shown in Fig. 7. Each loop has a different function: Loop-1 is an ultra-fast low-gain loop with p_{Out} being its dominant pole, and non-dominant poles p_{Gate} and p_A are pushed to the GHz range by the buffer impedance attenuation technique; Loop-2 is composed of the EA and the diode-connected M_7 and is a slow loop that generates the voltages of V_{MIR} and V_{SET}; Loop-3 has V_{OUT} fed back to the EA such that the DC accuracy is improved. In other words, Loop-1 is used to deal with the fast load-transient current, while Loop-3 is used to enhance the V_{OUT} DC accuracy. To simulate the loop response of each loop, three simulation setups are configured and described as follows.

Setup 1: As shown in Fig. 8, the signal path of Loop-1 is broken between V_A and the buffer input. The AC small signal is injected to the buffer input and the output is observed at V_A. To isolate the influence from Loop-2 and Loop-3, the path from M_7 to M_8 is also broken. To maintain the DC bias point, a DC voltage V_{SET} is applied to the gate of M_8. And to account for the loading effect, a replica buffer stage is added to V_A to mimic C_{iB}.

Setup 2: Loop-2 and Loop-3 are broken from V_{MIR} to M_2 and from V_{OUT} to M_3, respectively, as shown in Fig. 9. The AC small signal is injected into the EA through M_2 only. Now, the AC response of Loop-2 can be obtained at V_{MIR}, and the response of Loop-3 can be obtained at V_{OUT}, simultaneously.

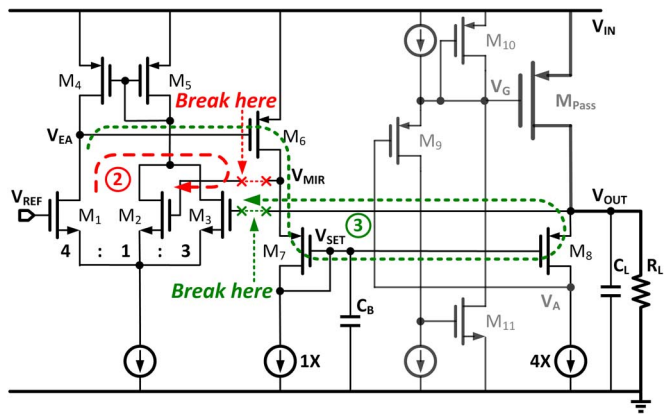


Fig. 9. Break Loop-2 and Loop-3 simultaneously for stability analysis.

Loop-2 and Loop-3 can be considered together because they both contain the error amplifier in their respective loops.

Simulation results of these two setups are combined in Fig. 10, which shows the Bode plots of the three loops at heavy load condition with $R_L = 100\ \Omega$. When V_{OUT} is 1.0 V, Loop-1 has a DC gain of 21 dB and its UGF_1 is 600 MHz, with a phase margin (PM_1) of 60°. Loop-2 has one dominant pole located at V_{SET} and a non-dominant pole located at V_{EA}, and $PM_2 = 80°$. Loop-3 has two non-dominant poles located at V_{OUT} and V_{EA}, respectively, and PM_3 is only 20°. Nevertheless, the stability of the circuit is determined by the system loop gain, not individual loop gains. A third loop-breaking setup for stability analysis is shown in Fig. 11, and described as follows.

Setup 3: Loop-2 and Loop-3 contain the error amplifier, and by breaking the loops between V_{EA} and the gate of M_6 we have

$$v_{ea} = \frac{g_{m2}(r_{o1}\|r_{o4})}{1 + sC_{EA}(r_{o1}\|r_{o4})}(v_{mir} + 3v_{out}) \tag{15}$$

$$\frac{v_{mir}}{v_{ac}} \approx \frac{-g_{m6}(r_{o6}\|r_{o15})}{1 + sC_B(r_{o6}\|r_{o15})} \tag{16}$$

$$\frac{v_{set}}{v_{mir}} \approx \frac{1}{1 + 1/A_7(s)} \tag{17}$$

$$\begin{aligned}\frac{v_{out}}{v_{mir}} &\approx \frac{1}{1 + 1/A_8 - 1/A_P(s)(r_{o16}\|r_{o8})} \cdot \frac{1}{1 + 1/A_7(s)} \\ &\approx \frac{1}{1 + 1/A_8} \cdot \frac{1}{1 + 1/A_7(s)} = \frac{A_8}{1 + A_8} \cdot \frac{A_7(s)}{1 + A_7(s)},\end{aligned} \tag{18}$$

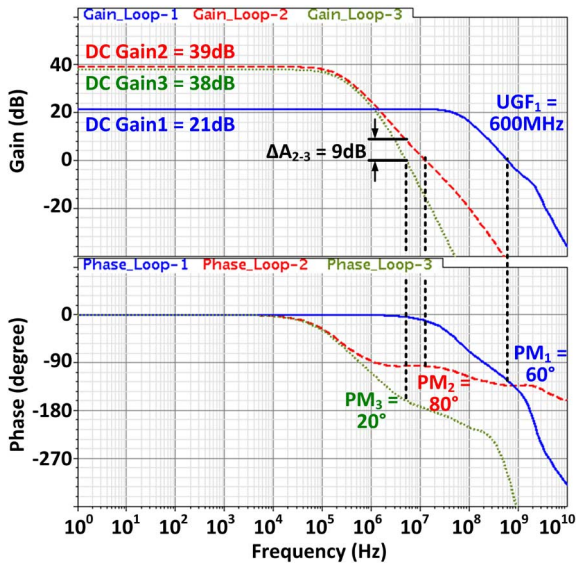


Fig. 10. Simulated frequency response of the three loops of the proposed LDO with $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 1.0$ V and $R_{\rm L} = 100\ \Omega$.

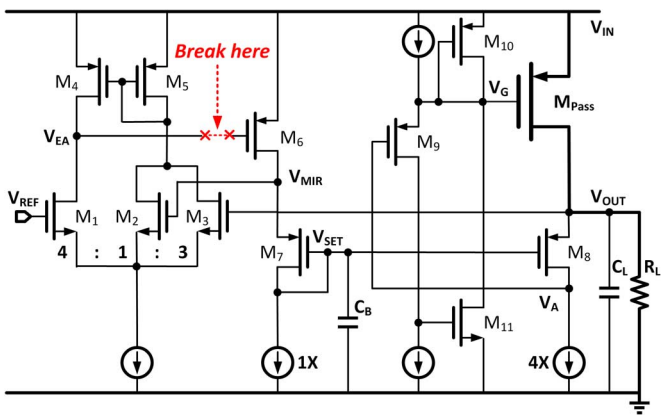


Fig. 11. Break the loop at the EA output.

with

$$\mathrm{A}_7(s) = \frac{g_{\rm m7} r_{\rm o15}}{(1 + sC_{\rm B} r_{\rm o15})} \tag{19}$$

$$\mathrm{A}_8 = g_{\rm m8} r_{\rm o8} \tag{20}$$

$$\mathrm{A}_{\rm P}(s) = \frac{g_{\rm mP}(r_{\rm oP} \| R_{\rm L})}{1 + sC_{\rm L}(r_{\rm oP} \| R_{\rm L})}, \tag{21}$$

where $v_{\rm ac}$ is the AC signal injected at the gate of M_6, $C_{\rm EA}$ is the parasitic capacitance at the $V_{\rm EA}$ node, and $r_{\rm op}$ is the output resistance of $\mathrm{M}_{\rm Pass}$. The loop-gain transfer function of the entire LDO is given by (22), at the bottom of the page. There are three LHP poles and one LHP zero in the transfer function, while the dominant pole is generated by $C_{\rm B}$. The zero is generated by Loop-2, which is a shorter path compared to Loop-3. It is

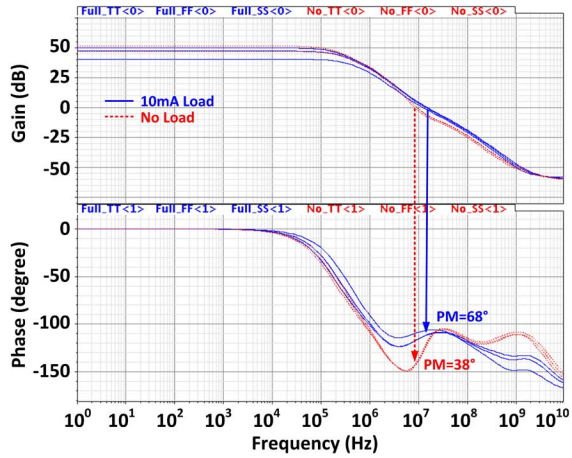


Fig. 12. Simulated Bode plot of the LDO with $V_{\rm IN} = 1.2$ V, and $V_{\rm OUT} = 1.0$ V, at the corners of TT at 25°, SS at 85° and FF at −20°.

a pole-zero tracking pair that makes the entire LDO stable in all loading conditions. The simulated Bode plots of Setup 3 in different corners are given in Fig. 12. The worst case phase margins are 68° at 10 mA loading ($R_{\rm L} = 100\ \Omega$) and 38° at no load condition, respectively.

In this research, the (W/L) ratio of M_2 and M_3 is aggressively set to be 1:3. This setting is to trade stability margin for better $V_{\rm OUT}$ DC accuracy. To gain more design margin for stability, the weighting of M_2 and M_3 could be set to 2:2 by satisfying with lower DC accuracy. Alternatively, in another extreme case, with M_2 (Loop-2) being removed and M_3 having the same size as M_1, the DC accuracy is maximized. However, the dominant pole of Loop-3 at $V_{\rm SET}$ has to be much lower than before, and the settling time of $V_{\rm OUT}$ will be much longer due to slow Loop-3.

D. Load Regulation

Curves of load regulation are shown in Fig. 13, with $(W/L)_2$:$(W/L)_3$ being set to 1:3, 2:2, and 1:0 (no Loop-3) respectively. In the case of no Loop-3, $V_{\rm OUT}$ changed by 34 mV when the load current is changed from 10 μA to 10 mA. For our proposed case of 1:3, $V_{\rm OUT}$ changed by only 11 mV with the same change in load current. DC accuracy is improved by about 3 times by adding Loop-3 without degradation in stability and speed performance. If the ratio of M_2 and M_3 is 2:2, $V_{\rm OUT}$ would change by 20 mV.

E. Power Supply Rejection

For many published works on fully-integrated LDOs with fast transient responses, performance on power supply rejection is usually not discussed. However, PSR is the most important specification of an LDO designed for noise-sensitive loads. Supply ripples are mainly due to the output voltage ripples from the pre-stage DC-DC converter and on-chip noise generated by

$$T(s) = \frac{v_{\rm ea}}{v_{\rm ac}} = \frac{-g_{\rm m2}(r_{\rm o1} \| r_{\rm o4}) g_{\rm m6}(r_{\rm o6} \| r_{\rm o15})}{(1 + sC_{\rm B}(r_{\rm o6} \| r_{\rm o15}))\,(1 + sC_{\rm EA}(r_{\rm o1} \| r_{\rm o4}))} + \frac{-3g_{\rm m2}(r_{\rm o1} \| r_{\rm o4}) g_{\rm m6}(r_{\rm o6} \| r_{\rm o15})}{(1 + sC_{\rm B}(r_{\rm o6} \| r_{\rm o15}))\,(1 + sC_{\rm EA}(r_{\rm o1} \| r_{\rm o4}))} \cdot \frac{\mathrm{A}_8}{1 + \mathrm{A}_8} \cdot \frac{\mathrm{A}_7(s)}{1 + \mathrm{A}_7(s)}$$

$$\approx \frac{-g_{\rm m2}(r_{\rm o1} \| r_{\rm o4}) g_{\rm m6}(r_{\rm o6} \| r_{\rm o15})(1 + 4g_{\rm m7} r_{\rm o15} + sC_{\rm B} r_{\rm o15})}{(1 + sC_{\rm B}(r_{\rm o6} \| r_{\rm o15}))\,(1 + sC_{\rm ea}(r_{\rm o1} \| r_{\rm o4}))\,(1 + g_{\rm m7} r_{\rm o15} + sC_{\rm B} r_{\rm o15})}. \tag{22}$$

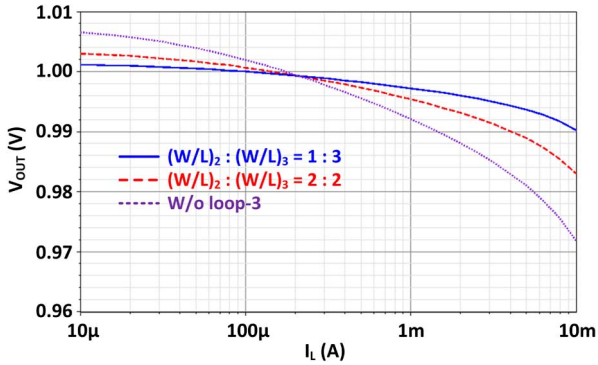


Fig. 13. Simulated $V_{\rm OUT}$ load regulation with $(W/L)_2$: $(W/L)_3$ being set to 1:3 and 2:2, respectively; plus the case without Loop-3.

the digital/driver circuits. Ripples generated by DC-DC converters could be higher than 100 MHz [23], while noise generated by digital circuits is in the GHz range. To achieve good PSR, stacked power transistors were used in [14] and [24] with large dropout voltages, sacrificing the LDO efficiency.

In this work, DC gain of Loop-1 has been sacrificed for fast transient response. Increase DC gain of Loop-1 needs additional stages that will introduce undesired LF poles. By setting $p_{\rm Out}$ as the dominant pole, most of the silicon area (capacitance) can be effectively used to stabilize $V_{\rm OUT}$ and reject noise from $V_{\rm IN}$. The simulated PSR curves of the proposed LDO with and without a 100 Ω $R_{\rm L}$ are shown in Fig. 14(a); and the PSR of the tri-loop regulator with and without $C_{\rm B}$, and the PSR of the regulator with only Loop-1 and $C_{\rm B}$, are plotted in Fig. 14(b), respectively. And. the equivalent model for the PSR of Loop-1 only [20] is plotted in Fig. 14(c).

$$\mathrm{PSR}_{\mathrm{Loop-1}} = \frac{v_{\rm out}}{v_{\rm dd}} \approx \frac{z_{\rm o-Loop1}}{r_{\rm dsP} + z_{\rm o-Loop1}} = \frac{1}{\left[1 + r_{\rm dsP} \mathrm{A}_{\mathrm{Loop-1}} / \left(r_{\rm dsP} \| R_L \| \frac{1}{sC_{\rm L}}\right)\right]}. \tag{23}$$

The ultra-fast Loop-1 provides a shunt path $z_{\rm o-Loop1}$ for the output node. At medium and high frequencies, the light-load PSR is better than the full-load PSR, as $C_{\rm L}$ can more effectively bypass the ripple to ground when it is in parallel with a larger $R_{\rm L}$. Although, the ultra-fast Loop-1 could response to the input ripple in the VHF (very high frequency, 30 MHz–300 MHz) range with the assistance of $C_{\rm L}$, the LDO with Loop-1 only have poor PSR at low frequencies. Based on the Loop-1 PSR, 9 dB improvement on PSR is achieved at frequencies lower than 1 MHz by the proposed tri-loop LDO. And. in FVF-based structures, $V_{\rm OUT}$ is mainly determined by $V_{\rm SET}$. Therefore, adding a bypass capacitor $C_{\rm B}$ (about 7 pF in this design) at the $V_{\rm SET}$ node could improve the PSR by filtering out the ripple that comes from $V_{\rm MIR}$ to $V_{\rm OUT}$. Adding $C_{\rm B}$ is effective in the medium frequency range (around 100 MHz to 1 GHz). Nevertheless, adding the $C_{\rm B}$ will lower the bandwidth of Loop-2 and -3, which is also the PSR corner frequency around 1 MHz. The long channel transistor M_{10} introduces an additional path from $V_{\rm IN}$ to $V_{\rm G}$ that slightly helping the PSR at high frequencies.

IV. Measurement Results

The measurement setup of the LDO with on-chip loading for load transient measurement is shown in Fig. 15(a). The on-chip $R_{\rm L}$ is connected in series with the switch S_1 (implemented by a 1.0 V device) driven by an on-chip inverter buffer, and the

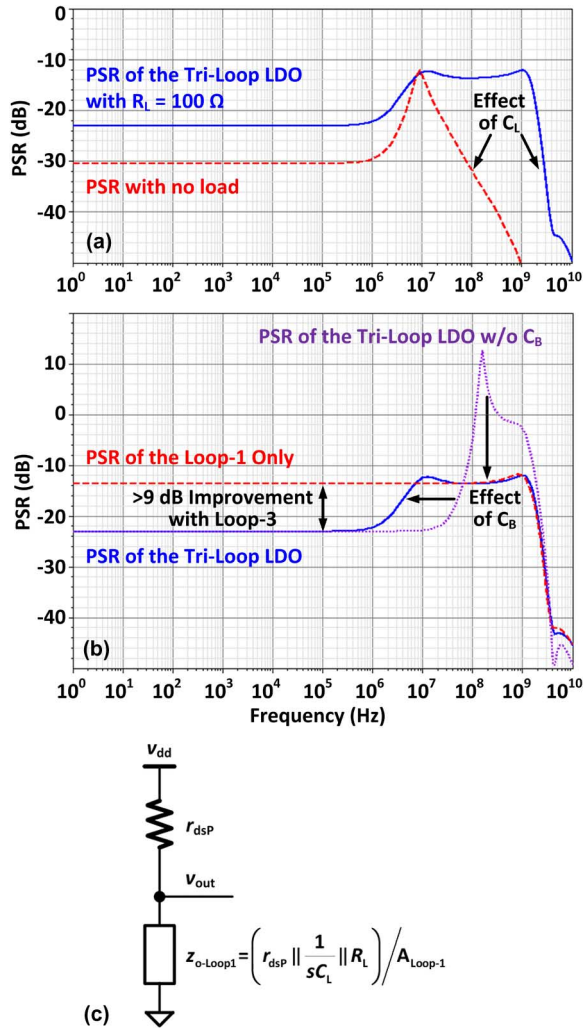


Fig. 14. (a) Simulated PSR of the proposed LDO; and (b) the PSR of Loop-1 only and the tri-loop regulator with or without $C_{\rm B}$, with $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 1.0$ V and $R_{\rm L} = 100$ Ω; and (c) the equivalent model for the PSR of Loop-1 only.

rising and falling edges $T_{\rm Edge}$ of the load current are less than 200 ps (in simulations they are 120 ps). The static currents of the chip with S_1 ON and with S_1 OFF are measured as $I_{\rm MAX}$ and $I_{\rm Q}$, respectively. The dropout voltage is measured to be 150 mV at $I_{\rm MAX}$ (the worst case). With chip-on-board setup, all the transient waveforms are collected by a pair of 7-GHz differential probes with input impedance of 50kΩ||0.32 pF connected to a 4-GHz oscilloscope. Single bond-wire is bonded to each input/output terminal of the prototype. The parasitic RLC low-pass filter consists of the 2n-H bond-wire inductance and the input impedance of the probe, and the cutoff frequency is over 6 GHz. With this setup, ultra-fast transient currents and voltages are generated and measured.

Two versions of the prototype chips of the proposed LDO are fabricated using 65 nm CMOS GP process. The micrographs of the stand-alone LDO with on-chip loading for characterization and the embedded LDO that serves as the power supply of the TIA of an optical receiver are shown in Fig. 15. Chip area of the stand-alone LDO is $260 \times 90\ \mu\mathrm{m}^2$, including 140 pF of on-chip capacitors and the circuit for generating load transients. Stacked MOS and MIM capacitors are used in the stand-alone version to reduce the silicon area, and only MOS capacitors are used in the embedded version, since the high-layer metal would affect the

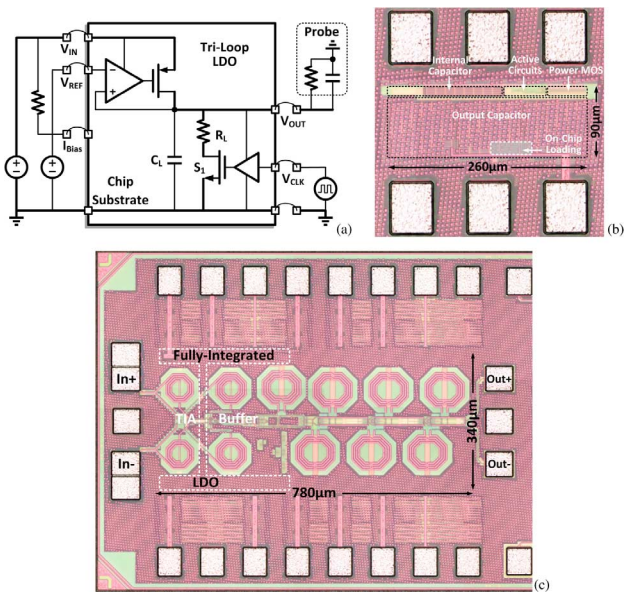


Fig. 15. (a) Testing setup of the LDO with on-chip load; and the micrographs of (b) the stand-alone proposed LDO with on-chip load and (c) the optical receiver with embedded LDO supplying its TIA (not in the same scale).

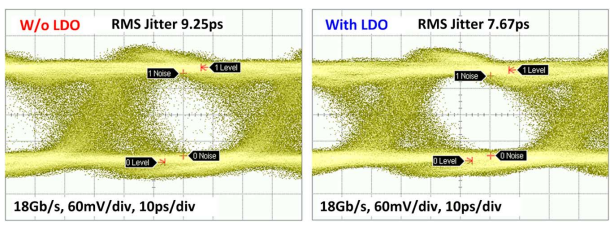


Fig. 16. The measured output data eye diagrams of the optical receiver for PRBS without or with the proposed tri-loop LDO supplying the front-end.

performance of the inductors in the receiver signal path. The measured 18 Gb/s output data eye diagrams of the optical receiver for pseudo-random binary sequence (PRBS) without and with the proposed tri-loop LDO supplying the front-end TIA are shown in Fig. 16. Note that, the without-LDO-case was directly supplied by off-chip 1.0 V supply with the same on-chip $C_{\rm L}$. The RMS jitter is reduced from 9.25 ps to 7.67 ps.

Fig. 17 shows the measured transient response of the output voltage $V_{\rm OUT}$ with on-chip load current change from 0 μA to 10 mA within 200 ps, with zoom-in details of the undershoot and overshoot voltages. With a quiescent current of only 50 μA, the measured undershoot voltage was 43 mV, and $V_{\rm OUT}$ recovered to its steady state value in 100 ns with the help of Loop-3 regulation. When the load current stepped from 10 mA to 0 μA, the measured overshoot voltage was 82 mV, and $V_{\rm OUT}$ was gradually discharged by the bias current of M_8, and then regulated by Loop-3 to its steady state value. The well-behaved transient waveforms of $V_{\rm OUT}$ confirmed the stability of the proposed tri-loop LDO. The FOM calculated according to (1) of [13] is 5.74 ps, and the response time is 1.15 ns. FOM is expected to be improved further with process scaling. Note that FOM improvement is not necessarily true for internal pole dominant cases, because low loop bandwidth is required by limiting $I_{\rm O,Min}$ for stability issue, as mentioned in Section II.

The measured transient waveforms at the worst case frequencies (5 MHz and 1 GHz) for evaluating the PSR are shown in Fig. 18. The PSR data at frequencies $\geq$ 2.5 GHz is measured by

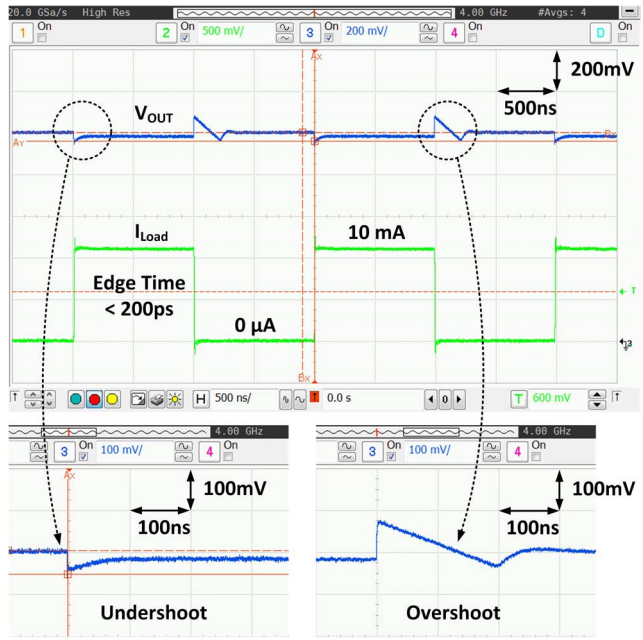


Fig. 17. Measured transient response with $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 1.0$ V, and on-chip loading change from 0 μA to 10 mA within edge times of 200 ps.

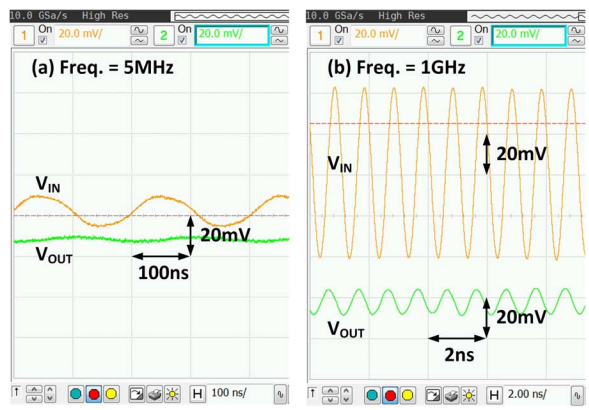


Fig. 18. Measured transient waveforms for PSR calculation at (a) 5 MHz and (b) 1 GHz, respectively.

a spectrum analyzer, and they are consistent with the data measured by transient waveforms at 2.5 GHz. The power supply rejection is better than -12 dB up to 20 GHz, and is suitable for high data rate wideband communication systems with digital buffers generating high frequency glitches on-chip.

Fig. 19 shows the summary of the measured PSR of the proposed LDO up to 20 GHz. For low frequencies, PSR is better than -21 dB; and the worst case occurs at 5 MHz with -12 dB rejection. PSR at 1 GHz is -15 dB. For frequencies higher than 2.5 GHz, PSR would be dominated by the ESR of the filtering capacitors ($C_{\rm L}$ and $C_{\rm B}$). Since the ESR zero is not needed in our proposed architecture, ESR of the on-chip capacitors is minimized in the layout design for good PSR. Due to the parasitic bond-wire effects and the substrate-to-PCB resistance, certain PSR variations are observed at the VHF region.

Performance comparison with state-of-the-art LDOs is summarized in Table II. Compared to previous ultra-fast transient response designs [13] and [17], response time on the order of nanosecond is achieved by the proposed architecture with much smaller $I_{\rm Q}$ and $C_{\rm L}$, and hence resulting in the best FOM. Furthermore, full spectrum PSR characterization is presented,

TABLE II
COMPARISON OF STATE-OF-ART LDOS

Publication	[9] ISSCC 2008	[10] JSSC 2010	[13] JSSC 2005	[17] JSSC 2012	[24] TCAS1 2014	[25] TCAS1 2014	This Work
C_L	Off-Chip		On-Chip				
Technology	0.35μm	90nm	90nm	45nm SOI	0.35μm	65nm	**65nm**
V_{OUT}	0.9V	0.9V	0.9V	0.9 to 1.1V	1.2V	1V	**1V**
Drop out	150mV	100mV	300mV	85mV	600mV	200mV	**150mV**
I_Q	4 to 164μA	9.3μA	6mA	12mA	44μA	23.7μA	**50 to 90μA**
I_{MAX}	50mA	50mA	100mA	42mA	12mA	50mA	**10mA**
Total Cap.	1μF	1μF	600pF	1.46nF	100pF	27pF	**140pF**
PSR	-50dB @1MHz	-35dB @10MHz	N/A	N/A	-38dB @50MHz	-53dB @1kHz	**-15.5dB @1GHz -12dB @5MHz**
ΔV_{OUT} @T_{Edge}	6.6mV @10ns	10mV @10ns	90mV @100ps	N/A	105mV @500ns	40mV @100ns*	**82mV @200ps**
DC Line Reg.	1.06mV/V	14mV/V	882mV/V**	27mV/V**	0.28mV/V	8.89mV/V	**37.1mV/V**
DC Load Reg.	0.061mV/mA	0.082mV/mA	0.9mV/mA	0.083mV/mA	0.68mV/mA	0.034mV/mA	**1.1mV/mA**
T_R	132ns	200ns	0.54ns	0.309ns*	N/A	N/A	**1.15ns**
FOM	10.6ps	37.2ps	32ps	62.4ps*	N/A	N/A	**5.74ps**

* Simulated results. ** Estimated from figure.

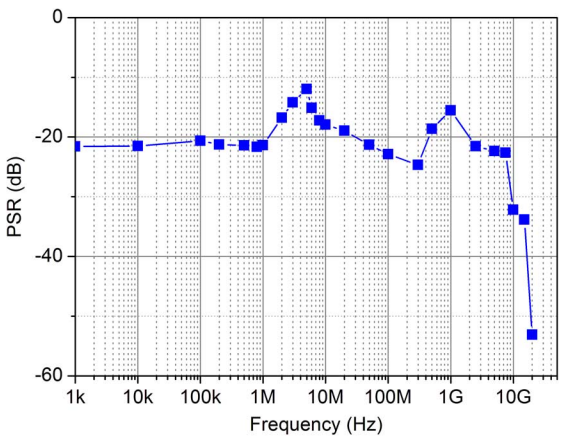


Fig. 19. Measured PSR up to 20 GHz with $R_L = 100\ \Omega$.

while other fully-integrated LDO regulators only present PSR at specific frequencies.

V. CONCLUSIONS

In this research, a fully-integrated low dropout regulator with fast transient response and full spectrum PSR characteristics for wideband communication systems is presented. Tri-loop architecture based on the flipped voltage follower and buffer impedance attenuation techniques is proposed and verified in 65 nm CMOS process. With the combined effects of the high-bandwidth Loop-1, C_L and C_B, full-spectrum PSR is achieved. With the additional Loop-3, V_{OUT} DC accuracy is improved by 3 times compared to the conventional FVF-based LDO. By comparing the performances and design methods of previous non-fully-integrated and fully-integrated LDO designs, a gap on transient and PSR performances has been identified and investigated in this research. This is the first attempt to design a fully-integrated LDO with certain PSR for the full-spectrum, while higher PSR is in demand for the future designs. As the FOM of this design scales with process, the proposed architecture will perform even better by using more advanced processes.

ACKNOWLEDGMENT

The authors would like to thank Prof. Philip K. T. Mok, Dr. Chen Huang, and Dr. Li Sun, for their valuable discussions, and also the anonymous reviewers for their comments and suggestions.

REFERENCES

[1] M. Jeong *et al.*, "A 65 nm CMOS low-power small-size multistandard, multiband mobile broadcasting receiver SoC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2010, pp. 460–461.

[2] T. Takemoto *et al.*, "A 25-Gb/s 2.2-W optical transceiver using an analog FE tolerant to power supply noise and redundant data format conversion in 65-nm CMOS," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 106–107.

[3] K. A. Bowman *et al.*, "A 22 nm all-digital dynamically adaptive clock distribution for supply voltage droop tolerance," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 907–916, Apr. 2013.

[4] S. Kose *et al.*, "Active filter-based hybrid on-chip DC-DC converter for point-of-load voltage regulation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 4, pp. 680–691, Apr. 2013.

[5] Y. Wang *et al.*, "A 3-mW 25-Gb/s CMOS transimpedance amplifier with fully integrated low-dropout regulator for 100 GbE systems," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2014, pp. 271–278.

[6] Q. Pan *et al.*, "A 48-mW 18-Gb/s fully integrated CMOS optical receiver with photodetector and adaptive equalizer," in *Proc. IEEE Symp. VLSI Circuits (VLSIC)*, Jun. 2014.

[7] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[8] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1732–1742, Aug. 2007.

[9] Y.-H. Lam and W.-H. Ki, "A 0.9 V 0.35 μm adaptively biased CMOS LDO regulator with fast transient responses," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2008, pp. 442–626.

[10] M. Ho, K. N. Leung, and K.-L. Mak, "A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2466–2475, Nov. 2010.

[11] M. El-Nozahi *et al.*, "High PSR low drop-out regulator with feed-forward ripple cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565–577, Mar. 2010.

[12] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[13] P. Hazucha *et al.*, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.

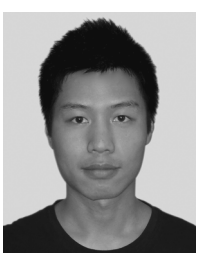
[14] V. Gupta and G. A. Rincon-Mora, "A 5 mA 0.6 μm CMOS Miller-compensated LDO regulator with -27 dB worst-case power-supply rejection using 60 pF of on-chip capacitance," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2007, pp. 520–521.

[15] T. Y. Man *et al.*, "Development of single-transistor-control LDO based on flipped voltage follower for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 5, pp. 1392–1401, May 2008.
[16] J. Guo and K. N. Leung, "A 6- μW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, Sep. 2010.
[17] J. F. Bulzacchelli *et al.*, "Dual-loop system of distributed microregulators with high DC accuracy, load response time below 500 ps, 85-mV dropout voltage," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 863–874, Apr. 2012.
[18] C. Zheng and D. Ma, "Design of monolithic CMOS LDO regulator with coupling and adaptive transmission control for adaptive wireless powered bio-implants," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2377–2387, Oct. 2011.
[19] E. N. Y. Ho and P. K. T. Mok, "Wide-loading-range fully integrated LDR with a power-supply ripple injection filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 6, pp. 356–360, Jun. 2012.
[20] V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE Int. SOC Conf.*, 2004, pp. 311–315.
[21] G. W. den Besten and B. Nauta, "Embedded 5 V-to-3.3 V voltage regulator for supplying digital IC's in 3.3 V CMOS technology," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 956–962, Jul. 1998.
[22] Y. Lu, W.-H. Ki, and C. P. Yue, "A 0.65 ns-response-time 3.01 ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 306–307.
[23] C. Huang and P. K. T. Mok, "An 82.4% efficiency package-bondwire-based four-phase fully integrated buck converter with flying capacitor for area reduction," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers (ISSCC)*, Feb. 2013, pp. 362–363.
[24] C. Zhan and W.-H. Ki, "Analysis and design of output-capacitor-free low-dropout regulators with low quiescent current and high power supply rejection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 2, pp. 625–636, Feb. 2014.
[25] X. L. Tan *et al.*, "A FVF LDO regulator with dual-summed miller frequency compensation for wide load capacitance range applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 5, pp. 1304–1312, May 2014.

Yan Lu (S'12–M'14) received the B.Eng. and M.Sc. degrees in microelectronic engineering from South China University of Technology in 2006 and 2009, respectively, and the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology in 2013.

He is an Assistant Professor in the State Key Laboratory of Analog and Mixed-Signal VLSI of University of Macau, Macao, since July 2014. His research interests include near-field coupled wireless power transfer, fully-integrated power converters and low dropout regulators.

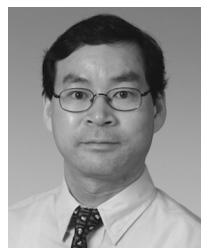
Dr. Lu is a recipient of the Outstanding Postgraduate Student of Guangdong (Canton) Province Award 2008, and the IEEE Solid-State Circuits Society Predoctoral Achievement Award 2013–2014.



Yipeng Wang received his B.S. degree in electrical engineering from Xiamen University, China, in 2010, and his M.S. degree in electronic and computer engineering from University of California, Santa Barbara, CA, USA, in 2012. He is currently pursuing his Ph.D degree at the Hong Kong University of Science and Technology with research in high speed wireline and wireless communication circuit.

Quan Pan (S'08) received his B.S degree in electrical engineering at University of Science and Technology of China in 2005; and M.S. degree in 2008. He received his PhD degree in electronic and computer engineering at the Hong Kong University of Science and Technology in 2014.

He was with MXTronics, Beijing, China, as a RFIC engineer in 2008 and 2009, working on GPS receiver. His research interests include high-speed optical transceiver, wireless and wireline circuit design, especially the high speed CDR and PLL design.



Wing-Hung Ki (S'86–M'91) received his B.Sc. degree from the University of California, San Diego, CA, USA, in 1984, the M.Sc. degree from California Institute of Technology, Pasadena, CA, USA, in 1985, and the PhD degree from the University of California, Los Angeles, CA, USA, in 1995, all in electrical engineering.

He joined Micro Linear Corporation, San Jose, CA, USA, in 1992, working on the design of power converter controllers. He then joined the Hong Kong University of Science and Technology in 1995, and is now a Professor in the Department of Electronic and Computer Engineering.

Dr. Ki served as an Associate Editor of TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2004–2005, 2012–2013), and he was a member of the International Technical Program Committee of the International Solid-State Circuits Conference (2010–2014). His research interests include switch mode power converters, switched-capacitor power converters, low dropout regulators, bandgap references, power management for energy harvesting and biomedical implants, and analog IC design methodologies.

C. Patrick Yue (S'93–M'98–SM'05–F'15) received the B.S.E.E. degree (with highest honors) from the University of Texas at Austin, TX, USA, in 1992, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1994 and 1998, respectively.

He is currently the Associate Provost for Knowledge Transfer and a Professor in Electronic and Computer Engineering Department at the Hong Kong University of Science and Technology (HKUST). He is the Founding Director of the HKUST-Qualcomm Joint Innovation and Research Lab and the School of Engineering Center for Industry Engagement and Internship. His current research interests include CMOS wireless and optical communication IC, smart LED SoC for visible light communication and micro-display, and wireless power transfer for biomedical implants.

Dr. Yue has contributed to over 100 peer-reviewed technical papers and two book chapters. He holds 13 U.S. patents. He was the co-recipient of the 2003 ISSCC Best Student Paper Award. He has been an editor of the IEEE Electron Devices Letter since 2011. He is a member of the IEEE Solid-State Circuit Society AdCom.