Adaptive On/Off Delay-Compensated Active Rectifiers for Wireless Power Transfer Systems

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***Abstract*—An adaptive on/off delay-compensation technique is proposed to improve the performance of CMOS active rectifiers for wireless power transfer (WPT) systems. The effects of the on/off delays on the performance of the active rectifiers with either a parallel-resonant or a series-resonant circuit at the secondary coil are studied, which include power conversion efficiency (PCE), voltage conversion ratio (VCR) and output voltage ripple. By adding two feedback loops to the active diodes to generate the switched-offset currents for the comparators adaptively, both on- and off-delays are compensated for accurately against PVT variations and mismatches. As a design example, a fully integrated active rectifier for biomedical applications with a parallel-resonant secondary was fabricated in a standard 0.35 μm CMOS process. With an AC input that ranges from 1.8 to 3.6 V, the measured VCR is higher than 90% and the measured PCE is higher than 89.1% for a load resistor of 500 Ω. In particular, the PCE is increased by 9% compared to the active rectifier without using the proposed technique.**

***Index Terms*—Active rectifier, comparator delay, delay compensation, inductive coupling, PVT variations, resonant wireless power transfer (R-WPT), reverse current control.**

I. Introduction

WIRELESS power transfer (WPT) using near-field magnetic coupling that pioneered by Tesla [1] has attracted extensive attention recently. It has a broad range of applications such as biomedical implants [2] and battery chargers of portable electronic devices [3] and electric vehicles [4]. WPT can be classified as inductive power transfer (IPT) and resonant wireless power transfer (R-WPT). In an IPT system, the primary coil and the secondary coil are placed close to each other with precise alignment, operating as a tightly coupled air-core transformer. In an R-WPT system, the technique of magnetic resonance [5] is used to compensate for leakage inductance so that power can still be efficiently transferred even the coils are loosely coupled. Industry consortia such as the Wireless Power Consortium (WPC), Power Matters Alliance (PMA), and Alliance for Wireless Power (A4WP) have been established. The specifications issued by WPC and PMA are generally regarded as IPT solutions, such as the "Qi" standard; while A4WP develops specifications for R-WPT that aim at providing spatial freedom and charging multiple devices concurrently [6].

Fig. 1 shows a typical power link of an R-WPT system. ISM band frequencies such as 6.78 or 13.56 MHz are usually selected as the resonant frequency f_s of the LC tank [3], [6]–[8]. The power amplifier drives the primary coil L_1 (with parasitic resistance R_{s_1}) to generate magnetic fluxes that induce an AC voltage at the secondary coil L_2 (with parasitic resistance R_{s_2}), and L_2 can either be parallel- or series-tuned by the capacitor C_2. The coupling coefficient k depends on the geometry, distance, and alignment of the coils. For loosely coupled coils, k can be lower than 0.1 [9]. The tuned circuit is then cascaded with a rectifier that converts the AC voltage to a DC voltage for powering up the loading circuits. The design of the rectifier affects the system efficiency, and higher energy loss may heat up an implant or a charger. Hence, passive diodes with forward voltage drops of 0.7 V are replaced by active diodes implemented by CMOS transistors and comparators, as shown in Fig. 2 [10]–[17]. The lower turn-on resistances result in higher voltage conversion ratio (VCR) and higher power conversion efficiency (PCE). However, when operating at a high frequency such as 13.56 MHz, propagation delays of comparators and gate drivers prevent the power transistors from being turned-on and off promptly, and degrade the performance of active rectifiers. The main challenge is thus to compensate for the propagation delays, and various schemes were proposed to tackle this problem [10]–[15].

In this research, an on/off delay-compensation technique is proposed to eliminate propagation delays of comparators and gate drivers adaptively. Inspired by the method suggested in [18], two feedback loops are added to the active diodes, and both turn-on delay (on-delay) and turn-off delay (off-delay) are fully compensated for with high precision against PVT variations and mismatches. The rest of this paper is organized as follows. Section II reviews two types of secondary tanks for R-WPT. The effects of on- and off-delays on the performance of the active rectifiers, such as PCE, VCR, and output voltage ripple, will be studied. Previous delay compensation schemes will also be discussed. The proposed on/off delay-compensation technique is introduced in Section III. Measurement results are presented in Section IV, and the research efforts are concluded in Section V.

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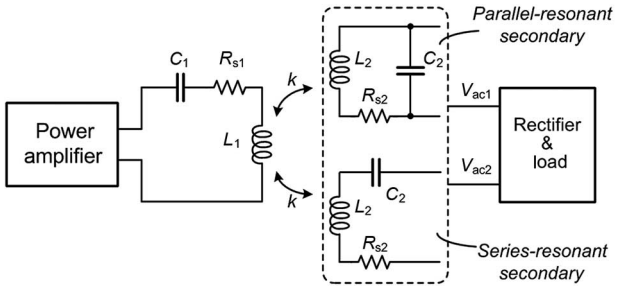

Fig. 1. Power link of an R-WPT system.

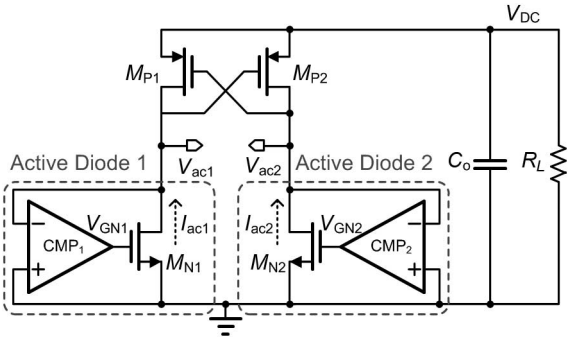

Fig. 2. Schematic of an active rectifier.

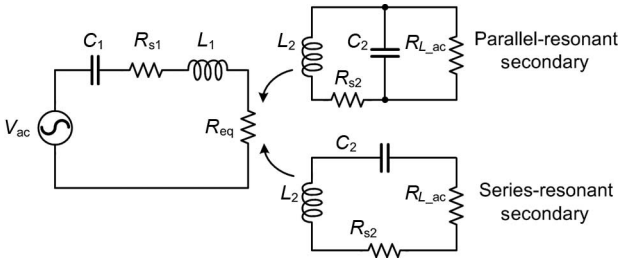

Fig. 3. Simplified equivalent circuit model of the power link.

II. Design Issues of Active Rectifiers for WPT

A. Parallel- or Series-Resonant Secondary

For an R-WPT system, there are two types of secondary tanks: 1) the parallel-resonant secondary (PS) tank and 2) the series-resonant secondary (SS) tank, as shown in Fig. 1. In either case, the subsequent rectifier and load can be modeled as a resistive load R_{L_ac}, and from the viewpoint of the primary, the secondary can be modeled as a reflected equivalent resistance R_{eq}, as shown in Fig. 3. The two resistances are given by [19]–[21]

$$R_{\mathrm{eq}} = \begin{cases} \dfrac{k^2 L_1}{L_2} R_{L\_\mathrm{ac}} \,(\mathrm{PS}) \\ \dfrac{\omega_s^2 k^2 L_1 L_2}{R_{L\_\mathrm{ac}}} \,(\mathrm{SS}) \end{cases} \tag{1}$$

where $\omega_s (= 2\pi f_s)$ is the resonant frequency of the LC tank in rad/s and f_s is also the switching frequency of the rectifier. The efficiency of the primary side is given by

$$\eta_{\mathrm{primary}} = \frac{R_{\mathrm{eq}}}{R_{s1} + R_{\mathrm{eq}}}. \tag{2}$$

The efficiency can be improved by maximizing R_{eq}, and thus the choice between the two types of secondary tanks can be determined by the load conditions of the secondary circuit [19], [20]. In general, for power transmission in the mW range with $R_{L\_\mathrm{ac}} \gg \omega L_2$, such as biomedical implants, the parallel-resonant secondary is preferred [8], [13], [14]. However, for power transmission of several watts with $R_{L\_\mathrm{ac}} \ll \omega L_2$, such as wireless battery chargers, the series-resonant secondary is better [3], [7]. The output characteristics of the secondary tanks are different: the parallel-resonant secondary behaves as a voltage-source and the series-resonant secondary behaves as a current-source [21], [22]. As a result, for the parallel-resonant secondary, the input voltage of the rectifier is a distorted sinusoidal wave. The conduction times of the power transistors depend on the output capacitor C_o and the load resistor R_L, and are usually much shorter than one cycle. For the series-resonant secondary, the input current is a sinusoidal wave, and the conduction time of each power transistor is half of the cycle. The input voltage is almost a square-wave, and the magnitude depends on R_L [23].

B. Effects of on/off Delay on the Performance of Active Rectifiers

With reference to Fig. 2, the operating principle of the active rectifier is as follows. When $V_{\mathrm{ac2}} - V_{\mathrm{ac1}} > |V_{tP}|$ (the threshold voltage of $M_{P1,2}$), M_{P2} is turned-on; and when $V_{\mathrm{ac1}} < 0$, the comparator CMP_1 turns-on M_{N1}, charging up V_{dc} by V_{ac}. After V_{ac1} swings above zero, M_{N1} is turned-off by CMP_1. During the next half of the AC input cycle, the other half of the rectifying circuit conducts in a similar fashion. Ideally, M_{N1} (M_{N2}) will be turned-on (off) once after $V_{\mathrm{ac1}}(V_{\mathrm{ac2}})$ swings below (above) 0. However, due to the propagation delays of the comparator and the gate driver, the actual scenario is different. As shown in Fig. 4, for the parallel-resonant secondary, the turn-on delay shortens the conduction time and increases the peak current [13]; and the turn-off delay results in reverse current that flows from the output capacitor back to the ground. For the series-resonant secondary, the turn-on delay enables the body-diode conduction of $M_{N1,2}$, and the turn-off delay also results in reverse current.

To investigate the effects of the on/off delays, the comparators $\mathrm{CMP}_{1,2}$ are modeled by verilog-A components with variable on- and off-delays. For simplicity, the power dissipation of the comparators is not included in the simulation. The parameters of the power links and the active rectifiers are listed in Table I. For the parallel-resonant secondary tank, the output capacitor of the active rectifier is chosen to be 2 nF so that it can be integrated on-chip. For the series-resonant secondary tank, due to the body-diode conduction of $M_{N1,2}$, $V_{ac1,2}$ swings low to around -0.7 V in the actual circuit. The large voltage difference makes the comparators respond quickly to turn-on $M_{N1,2}$. As a result, the on-delay of the comparator is usually very short, and it is fixed at 2 ns in the simulation.

Fig. 5 shows the simulation results of the PCE, the output voltage (V_{DC}), and the output voltage ripple (ΔV_{DC}) versus

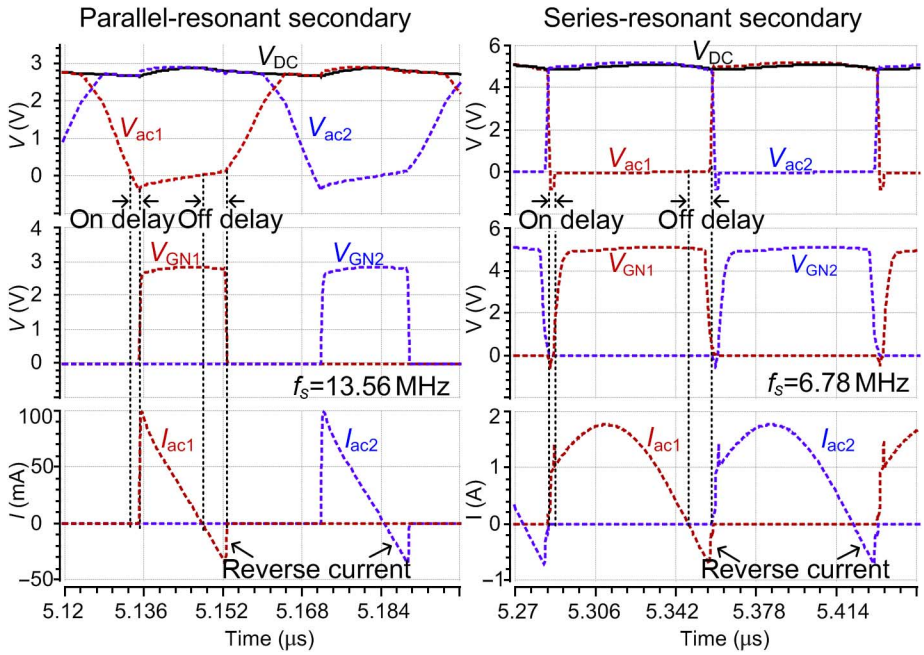

Fig. 4. Waveforms of active rectifiers.

TABLE I
PARAMETERS USED IN THE SIMULATIONS

Parameters		Parallel-resonant secondary	Series-resonant secondary
Power link	L_1 / R_{s1}	1 μH / 1 Ω	
	L_2 / R_{s2}	0.3 μH / 1 Ω	
	k	0.05	
	f_s	13.56 MHz	
Active rectifier	$M_{N1,2}$	625 μm / 0.35 μm	50 mm/0.5 μm
	$M_{P1,2}$	5000 μm / 0.35 μm	100 mm / 0.5 μm
	C_o	2 nF	0.47 μF
	V_{DC}	3.3 V	5 V

different delay durations, respectively. For the parallel-resonant secondary tank, both on- and off-delays degrade the PCE and the VCR of the active rectifier. The case for the off-delay at light load is even worse. ΔV_{DC} increases with the off-delay, but are not affected by the on-delay. For the series-resonant secondary tank, similar degradation due to the off-delay on V_{DC} and ΔV_{DC} can be observed. However, it is interesting to note that PCE is only slightly degraded, which is quite different from the case of using a parallel-resonant secondary tank. For the parallel-resonant tank, the off-delay increases the conduction time of the power transistors, resulting in extra conduction loss. Moreover, as the duration of the off-delay is comparable to the positive-current conduction time when operating at 13.56 MHz, this extra conduction loss is significant and the efficiency degradation is severe. For the series-resonant tank that works as a current-source, the off-delay only changes the current path and does not increase the conduction loss of the power transistors, so the efficiency degradation is limited. Fig. 6 shows the pie charts of the simulated power distribution of both types of secondary tanks when the off-delays are 0 and 6 ns, respectively. It can be shown that the portion of the conduction loss with respect to the total power is greatly increased (from 4.3% to 13.9%) by using the parallel-resonant tank, but is only slightly increased (from 3.7% to 5.7%) by using the series-resonant tank. However, the reverse current due to the off-delay significantly reduces the power-delivering capability of the series-resonant secondary (from 4.92 to 3.71 W). It means that more power has to be transferred from the primary to deliver the same output power due to the reverse current. Therefore, the power losses on $R_{s1,2}$ (in Fig. 3) will be increased and the efficiency of the whole R-WPT system will be degraded. Table II tabulates these effects. The di/dt noise is also an issue when considering the inductance of the off-chip bonding wires and pins of the package. The high slew rates of the current will generate voltage spikes between $V_{ac1,2}$ and ground. These spikes may inject noise into the substrate that degrades the performance of other noise-sensitive circuits implemented on the same chip, and they may even wrongly trigger the comparators, resulting in malfunction of the rectifier.

C. Review of Prior Delay Compensation Schemes

The above analysis shows that it is desirable to eliminate the on/off delays of the active rectifier, and various delay-compensation schemes have been proposed [10]–[16]. In [11] and [12], a constant offset is introduced to the comparators using unbalanced bias currents or asymmetrical input transistors to compensate for the off-delay, but the power transistor will also be turned-on later that increases the on-delay. In [10], an offset voltage is added only when turning-off the power transistor and is removed when turning it on. As both the comparator delay and the gate driver delay are highly affected by PVT variations, the constant or dynamic offset introduced in these techniques cannot accurately compensate for the off-delay under all conditions. In [13], a switched-offset biasing scheme is proposed for better controlling the reverse current. However, it still suffers from PVT variations and the design procedure is complicated. In [14] and [15], the on/off delays are both

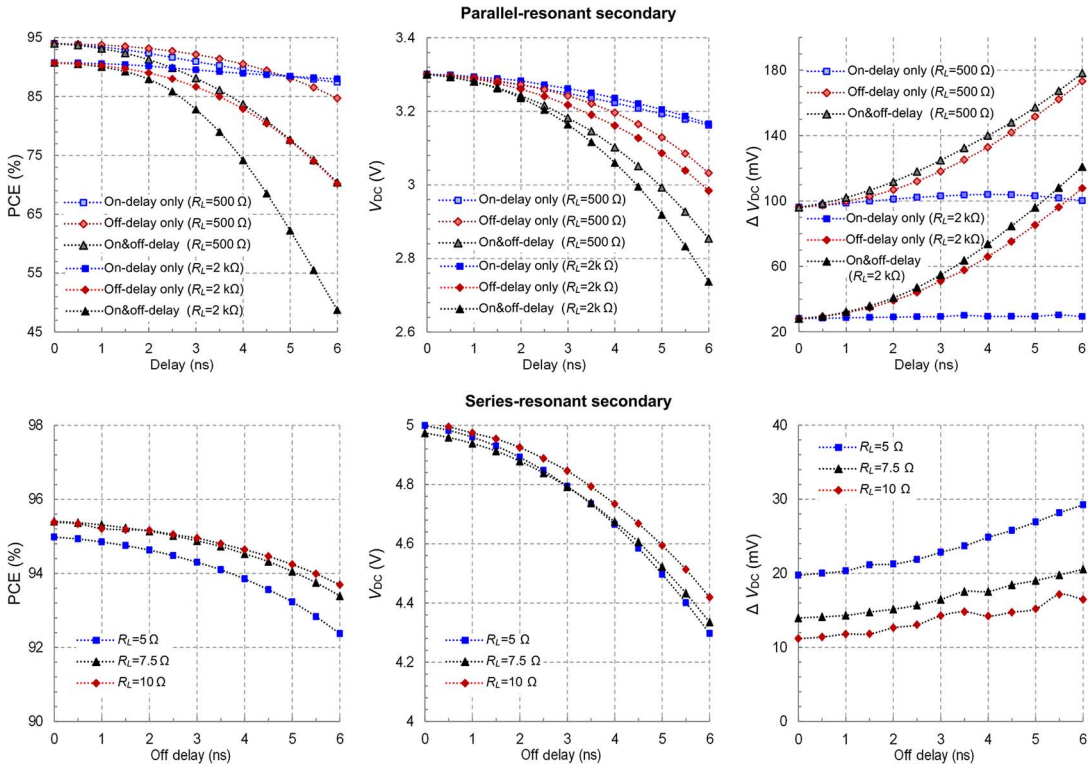

Fig. 5. Effects of on/off delay on the performance of the active rectifiers.

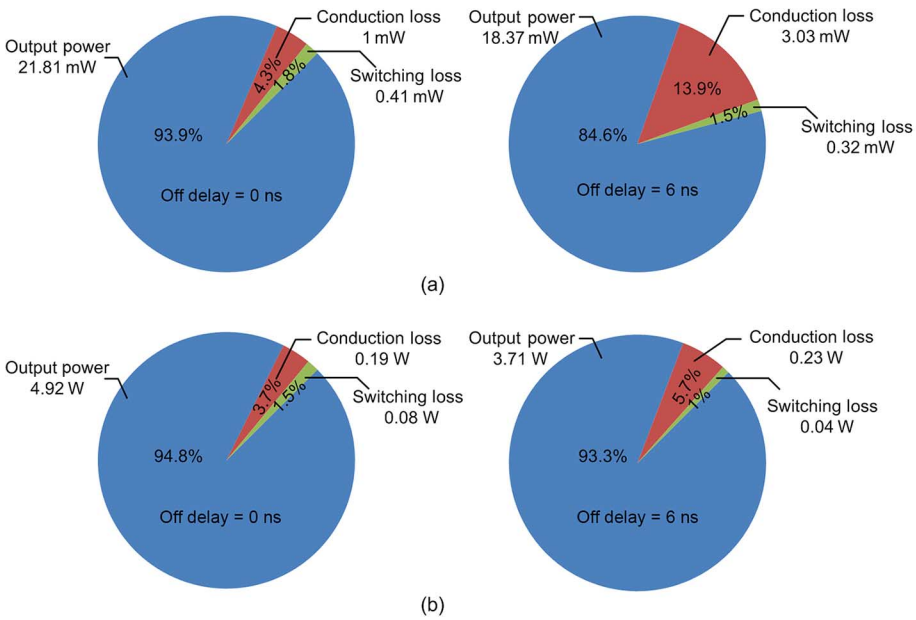

Fig. 6. Power distribution of the active rectifiers with (a) the parallel-resonant secondary; (b) the series-resonant secondary when the off-delays are 0 and 6 ns, respectively.

compensated for using similar schemes as in [11] and [12], and off-chip calibration is proposed to tune the offset [14]. In [16], a positive feedback loop is used to speed up the response of the comparators, but the delays are still larger than 3 ns. Hence, a solution that is insensitive to PVT variations is needed for high-performance active rectifiers. Next, we use the parallel-resonant secondary tank as an example to discuss the proposed adaptive on/off delay-compensation technique.

TABLE II
EFFECTS OF ON/OFF DELAY

Specification	Parallel-resonant secondary		Series-resonant secondary
	On delay	Off delay	Off delay
PCE	Medium	High	Low
V_{DC}	Medium	High	High
Δ V_{DC}	–	High	High

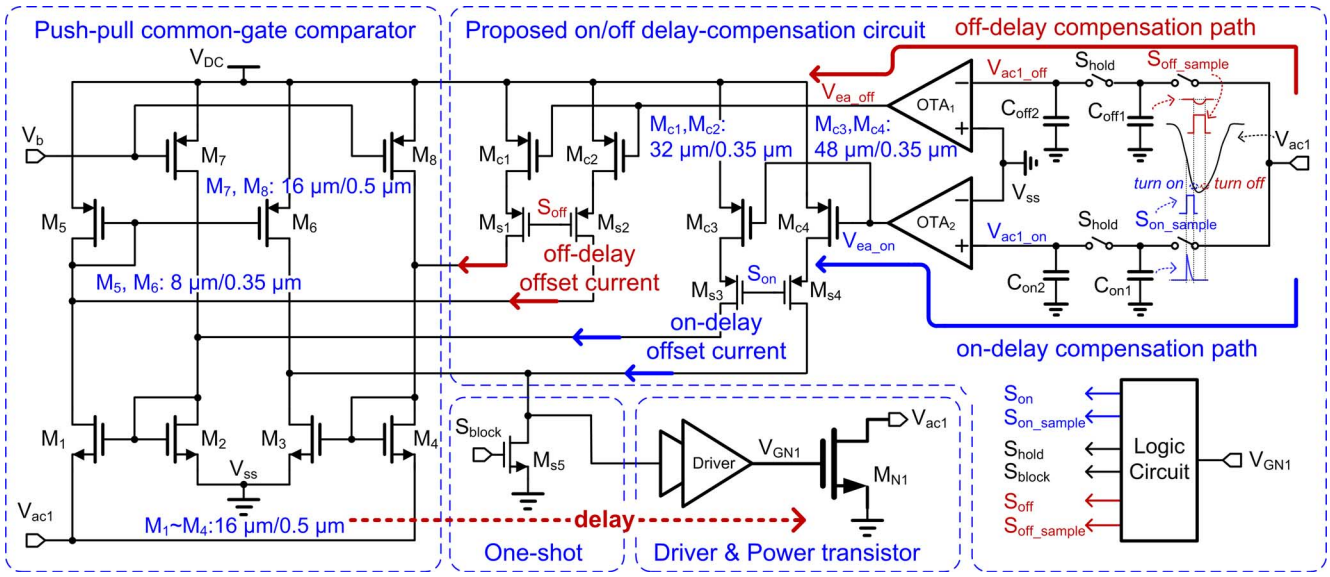

Fig. 7. Schematic of the active diode with the proposed adaptive on/off delay-compensation technique.

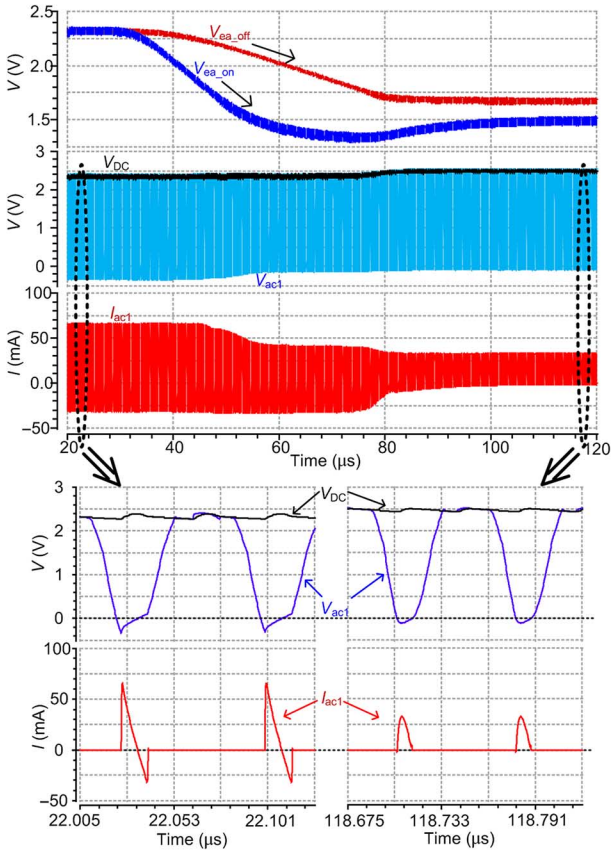

Fig. 8. Simulation results of the proposed technique.

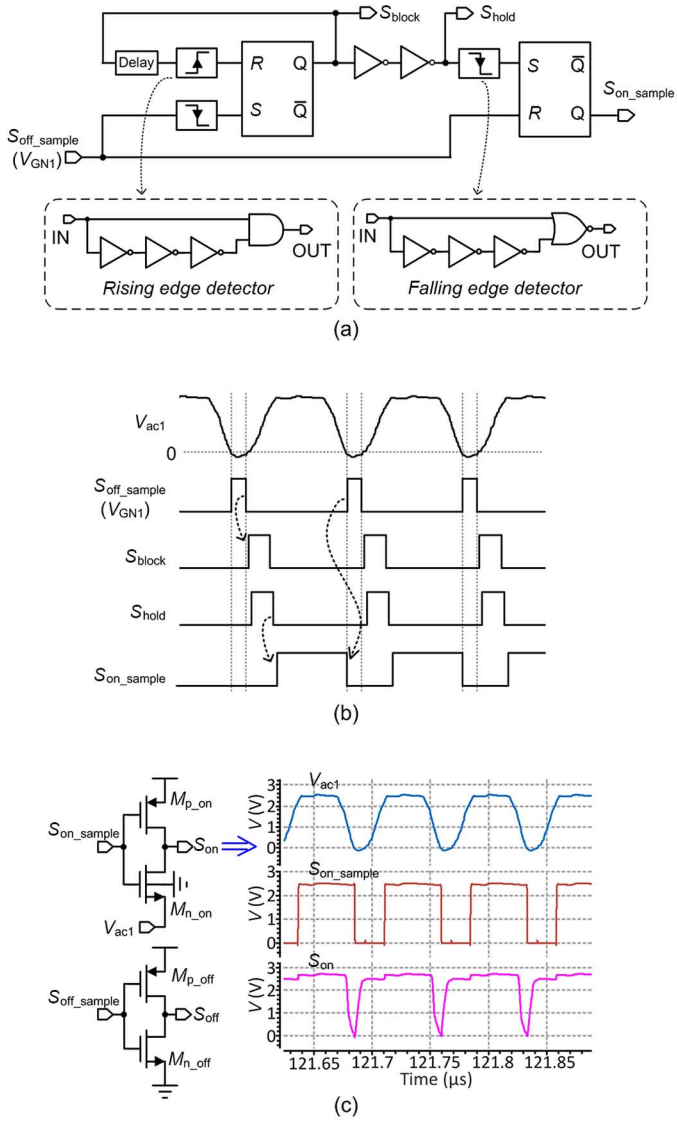

Fig. 9. (a) Control logic. (b) Timing diagram. (c) Simulated waveforms.

III. Adaptive On/Off Delay-Compensation Technique

A. Adaptive On/Off Delay-Compensation Technique

As discussed above, the switched-offset currents generated in [13] can only be optimized for a particular condition. Instead, if these currents can be generated adaptively according to the

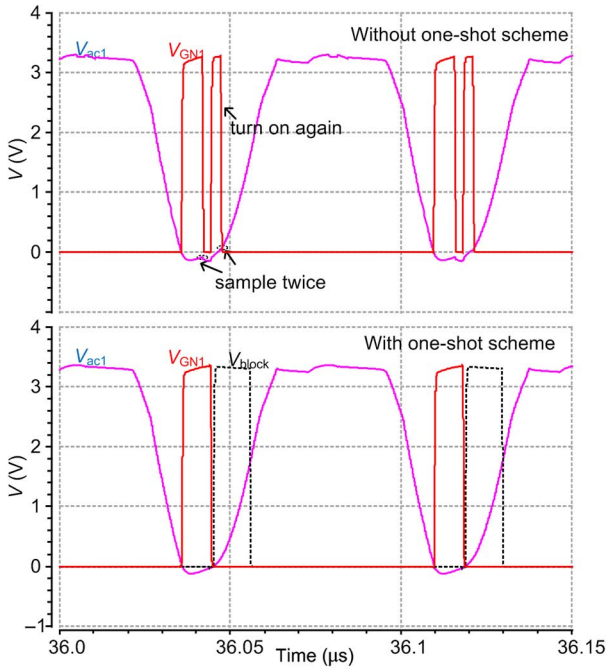

Fig. 10. Simulated waveforms with and without the one-shot scheme.

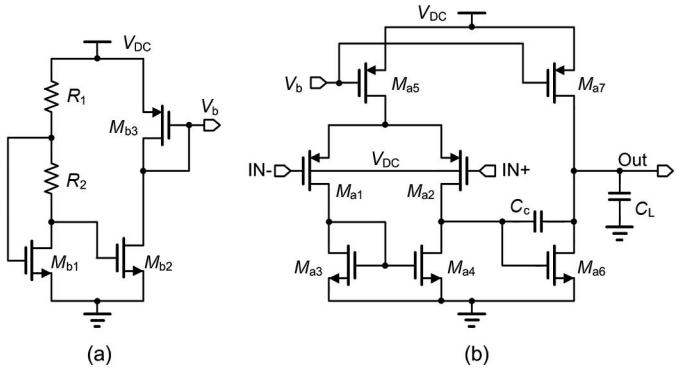

Fig. 11. Schematic of (a) peaking current source; (b) OTA.

working conditions, the on- and off-delays can be well compensated for despite PVT variations and mismatches. To adaptively generate the offset-currents, it is natural to introduce negative feedback, and Fig. 7 shows how this idea works. The proposed active diode consists of a conventional active diode (which includes a push–pull common-gate comparator [11], a gate driver and a power transistor) and the proposed adaptive on/off delay-compensation circuits. Two feedback loops are added to accurately generate the switched-offset currents for compensating both the on- and off-delays. Consider the off-delay compensation path as an example, and the operating principle of the proposed technique is as follows. The value of the voltage V_{ac1} is sampled by C_{off1} when S_{off_sample} is ON, and later the sampled voltage V_{ac1_off} is passed to be held on C_{off2} when S_{hold} is ON. Due to the off-delay, initially M_{N1} is turned-off later and V_{ac1_off} is higher than zero. The feedback amplifier OTA_1 compares V_{ac1_off} with ground, and drives V_{ea_off} to a lower value to increase the offset currents of M_{c1}

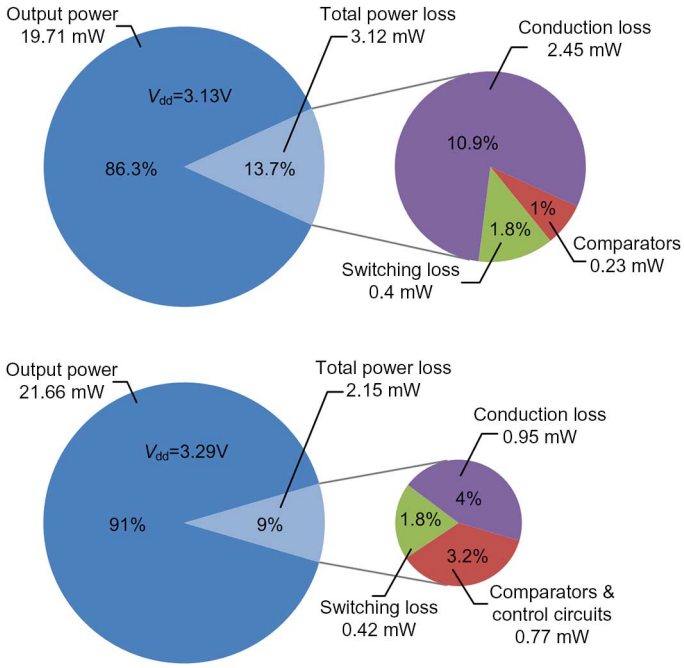

Fig. 12. Power distribution of the active rectifier. (a) Without the proposed technique. (b) With the proposed technique.

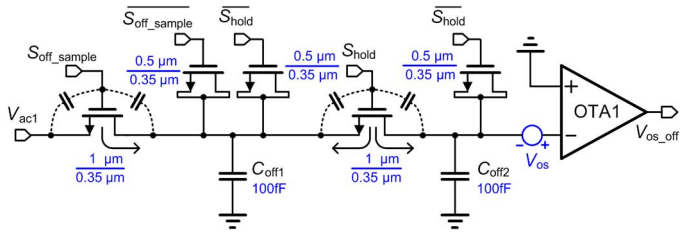

Fig. 13. Detailed schematic of the sampling circuit.

and M_{c2}. The sizes of $M_{c1,2}$ should be sufficiently large to generate enough offset-currents required by the feedback loop. As a result, M_{N1} will be turned-off earlier compared to the previous cycle. After several cycles, V_{ea_off} will be adjusted to the steady-state value so that V_{ac1_off} is equal to 0 V. A similar mechanism also applies to the on-delay compensation path. Fig. 8 shows the simulation results of the whole process. As feedback loops are used to force $V_{ac1\_on/off}$ to be exactly 0 V, both on- and off-delays are accurately compensated for against PVT variations and mismatches, as will be confirmed later.

Fig. 9 shows the control logic and its timing diagram. V_{GN1}, the gate signal of M_{N1}, is used to generated S_{off_sample}, S_{on_sample}, S_{hold}, and S_{block}, respectively. S_{off_sample} is the same signal as V_{GN1} so that the value of V_{ac1} when turning M_{N1} off can be sampled by C_{off1}. S_{on_sample} is terminated by the rising edge of V_{GN1} so that the value of V_{ac1} when turning M_{N1} on can be sampled by C_{on1}. S_{hold} should be designed not to overlap with S_{off_sample} and S_{on_sample}, and this is guaranteed by using the rising- and falling-edge detectors that are shown in Fig. 9(a). As the feedback loops do not need to be fast, the duration of S_{hold} is not critical, but it should be carefully designed

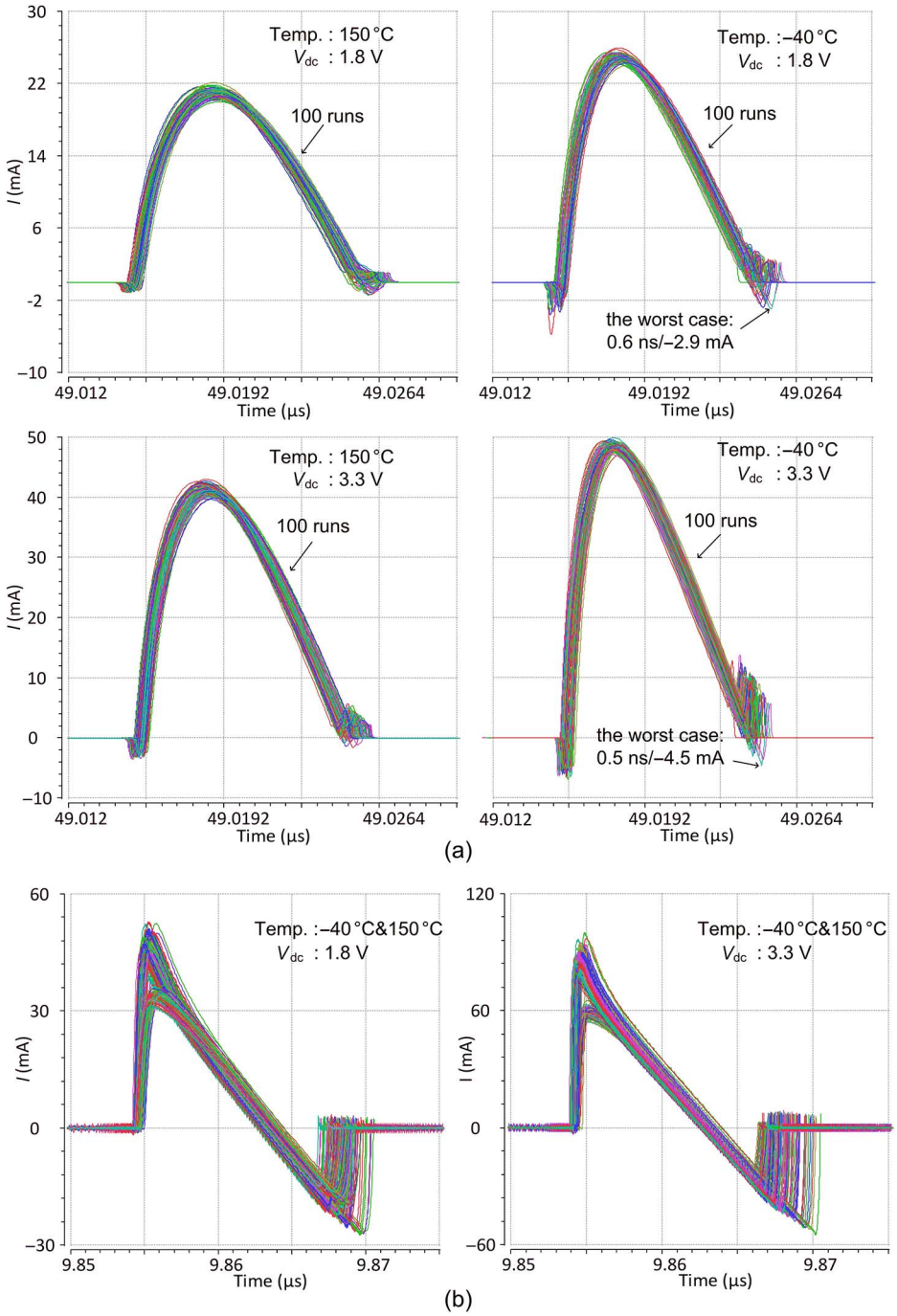

Fig. 14. Monte Carlo simulation waveforms of I_{ac1}. (a) With delay-compensation. (b) Without delay compensation.

to cover all PVT variations so that $\mathrm{S_{off\_sample}}$ can be properly generated under all conditions. As shown in Fig. 9(c), S_{on} and S_{off} are the complementary phases of $S_{\mathrm{on\_sample}}$ and $\mathrm{S_{off\_sample}}$, respectively. They are used to control the switches implemented by PMOS transistors $M_{\mathrm{s3,4}}$ and $M_{\mathrm{s1,2}}$ (in Fig. 7) to inject the offset currents into the comparator before turning M_{N1} on and off, respectively. The duration of the offset current for on-delay compensation is quite long and PCE will be degraded. To minimize the loss, we propose to connect the source terminal of M_{n_on} in Fig. 9(c) to V_{ac1} instead of to ground. Hence, the offset current for on-delay compensation will only be injected when V_{ac1} starts to decrease and this duration can be much shortened, as shown in Fig. 9(c). S_{block} is used to prevent the multiple-pulsing problem due to the switched-offset scheme [13]. The output of the comparator is shorted to ground for a short duration immediately after M_{N1} is turned-off. This simple one-shot scheme ensures that M_{N1} switches only once every cycle and C_{off1} samples the correct value. Let us consider the case when $V_{\mathrm{ea\_off}}$ is somehow lower than the correct value, and the offset current generated for off-delay compensation is too large. As shown in Fig. 10, if the one-shot scheme is not implemented, M_{N1} is turned-off too early and will be turned-on again

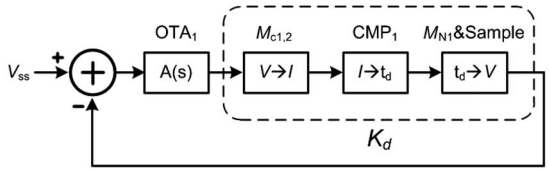

Fig. 15. Small-signal model of the off-delay compensation loop.

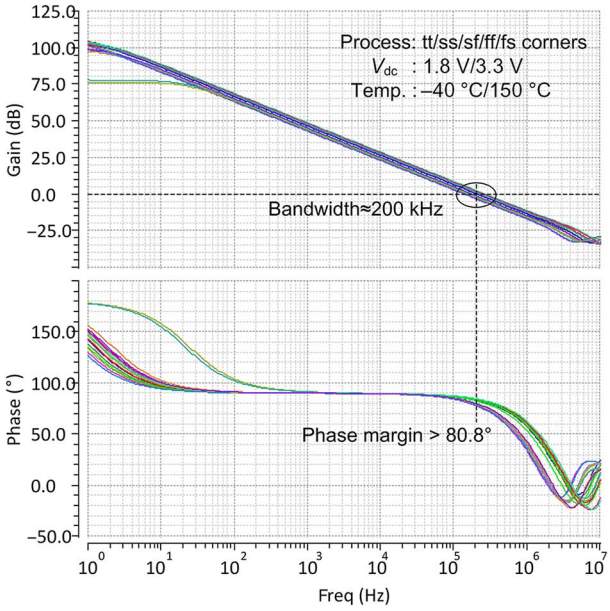

Fig. 16. Bode plots of OTA_1 under different PVT conditions.

after the offset current is removed. In such a case, V_{ac1} will be sampled by C_{off1} twice in each cycle, with a negative and a positive value, respectively. The feedback loop settles to a wrong value when the averaged sampled value is equal to zero, and multiple-pulsing problem sustains. If the one-shot scheme is implemented, M_{N1} cannot be turned-on again and V_{ac1} is only sampled once every cycle, which is a negative value in this case. The feedback loop will then drive $V_{\mathrm{ea\_off}}$ to a higher value to reduce the offset current. The duration of S_{block} is determined by the delay cell. It is preferred to be longer than the conduction time of M_{N1} and should be simulated for all corners to ensure the right timing against PVT variations.

Fig. 11 shows the schematics of the peaking current source that generates the bias currents and the feedback amplifier that is a transconductance amplifier (OTA). As the feedback loop does not need to be fast, the unity-gain bandwidth of the OTA is designed to be around 200 kHz only, consuming very low power (biasing current of 1 μA) and ensuring the stability of the feedback loop at the same time, as will be discussed in Section III-C.

Fig. 12 shows the pie charts of the simulated power distribution of the active rectifier at $R_L = 500\ \Omega$ with and without the proposed adaptive on/off delay-compensation technique. Without delay-compensation, power loss will be dominated by conduction loss. The case will be worse when accounting for the offsets and the post-layout parasitics of the comparators. With delay-compensation, conduction loss is much reduced by eliminating the on- and off-delays. The additional circuits consume only minute power, and the overall PCE is improved.

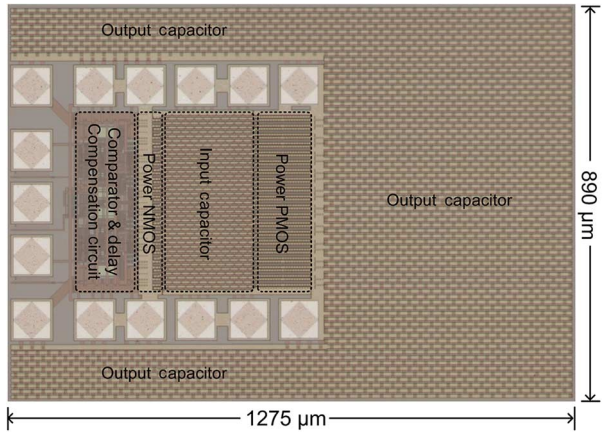

Fig. 17. Chip micrograph of the proposed active rectifier.

B. Accuracy Considerations of the Proposed Technique

There are mainly two error sources that affect the accuracy of the proposed technique: 1) the nonideal effects of the sampling switch, such as clock feed-through and channel charge injection and 2) the input offset voltage of the OTA. Fig. 13 shows the detailed schematic of the sampling circuit in Fig. 7. The sampling switches are implemented by NMOS transistors. To reduce the sampling error, the size of the switches is very small such that the parasitic capacitance is much smaller than $C_{\mathrm{off1,2}}$. To relieve these effects, dummy transistors with half the size of the switches are added [24]. To reduce the input offset voltage of the OTA, the size of the input transistors is designed to be large with careful layout. As such, the power transistors $M_{N1,2}$ will only be turned on/off slightly earlier or later than in the ideal case, and the effect on the overall performance is negligible. As mismatches of the input transistors of the comparators are accounted for by the feedback loops, they will not affect the performance of the rectifier. To evaluate the sensitivity of the proposed technique to PVT variations and mismatches, Monte Carlo simulations were performed under two extreme temperatures (-40 °C and 150 °C) and two extreme voltages (1.8 and 3.3 V), respectively. As shown in Fig. 14(a), the off-delays in the worst cases are only around 0.6 ns and 0.5 ns when the voltages are 1.8 V and 3.3 V, respectively. The corresponding reverse currents are only -2.9 and -4.5 mA, respectively. As a comparison, Fig. 14(b) shows Monte Carlo simulation results of the rectifier without the proposed technique, and it can be found that the delays are more sensitive to PVT variations.

C. Stability Analysis of the Proposed Technique

Without loss of generality, the stability of the off-delay compensation path shown in Fig. 7 will be analyzed. Fig. 15 shows the simplified small-signal model of the feedback loop. With reference to Fig. 7, $M_{\mathrm{c1,2}}$ converts $V_{\mathrm{ea\_off}}$ to be the offset currents, and they are injected to the comparator to change the off-delay of the comparator CMP_1. As a result, $M_{\mathrm{c1,2}}$ and CMP_1 can be modeled as a voltage-to-current block and a current-to-delay block, respectively. Furthermore, as different off-delays result in different reverse currents as well as different sampled voltages on C_{off2}, the power transistors

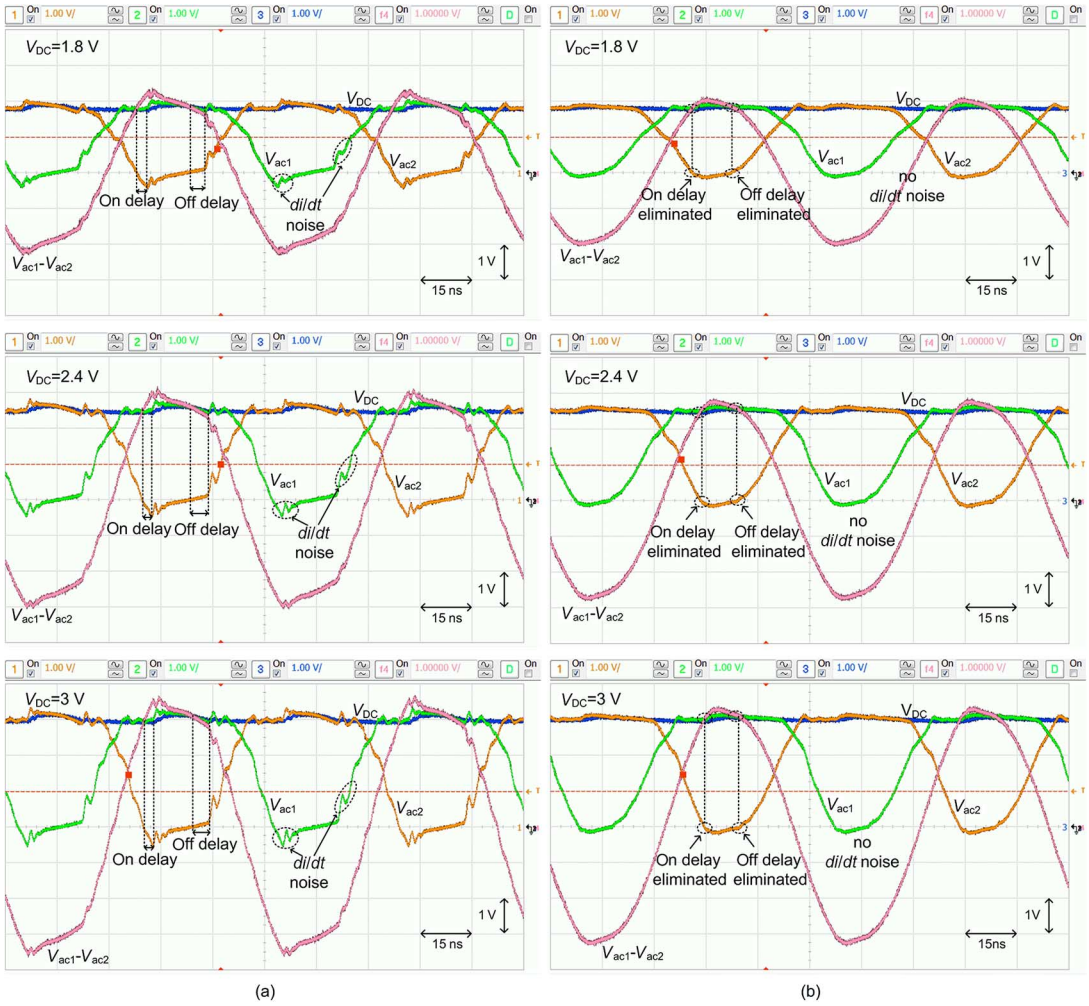

Fig. 18. Measured waveforms of the active rectifier when $R_L = 500\ \Omega$. (a) Without delay-compensation. (b) With delay-compensation.

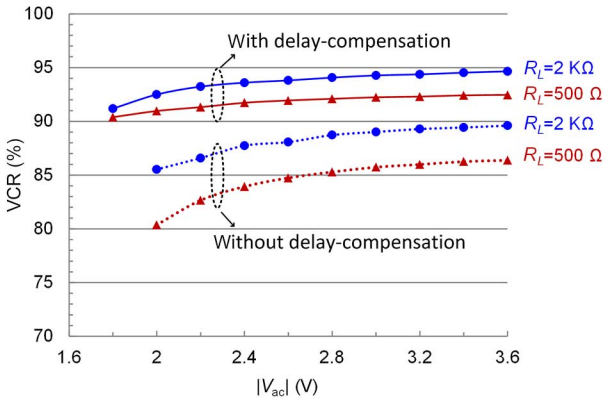

Fig. 19. Measured VCRs.

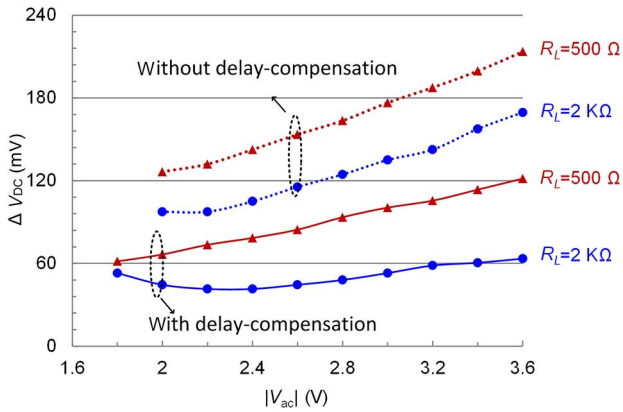

Fig. 20. Measured output voltage ripples.

$M_{\rm N1}$ and the sample-and-hold (*S/H*) circuits can be model as delay-to-voltage blocks. The pole due to the *S/H* circuit is located at f_s, much higher than the loop bandwidth and thus can be neglected. Therefore, the above three blocks can be grouped together and linearized as a gain of K_d approximately. The value of K_d is designed to be lower than one, and the loop stability is mainly determined by the transfer function of $\rm OTA_1$. Fig. 16 shows the Bode plots of the OTA under different PVT conditions. The phase margin is higher than 80.8°, and the loop stability is thus guaranteed.

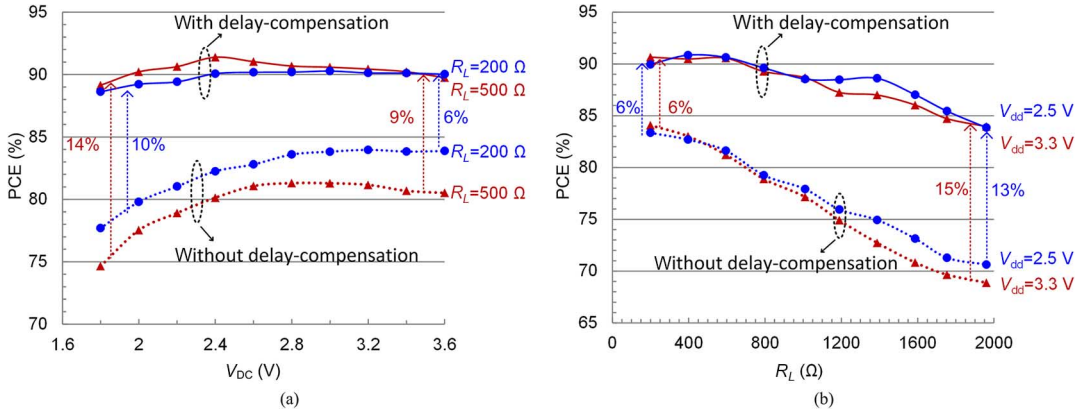

Fig. 21. Measured PCE under (a) different V_{DC} and (b) different R_L.

TABLE III
COMPARISON TO THE STATE-OF-THE-ART RECTIFIERS

	JSSC [11]	TCAS-I [14]	TCAS-II [12]	JSSC [16]	TBCAS [13]	JSSC [15]	**This Work**
Year	2009	2011	2012	2012	2014	2014	**2015**
Technology	0.35 μm	0.5 μm	0.18 μm	0.18 μm	0.35 μm	0.18 μm	**0.35 μm**
Frequency	1.5 MHz	13.56 MHz	13.56 MHz	6.78/13.56 MHz	13.56 MHz	13.56 MHz	**13.56 MHz**
Delay compensation	Off delay	On/off delay	Off delay only	On/off delay	Off delay only	On/off delay	**On/off delay**
Input range	1.2–2.4 V	3.3–5 V	0.9–2 V	N/A	1.5–4 V	1.15–1.35 V	**1.8–3.6 V**
Output cap.	1 μF	10 μF	10 μF	5.8 μF	1.5 nF	3*100 nF	**2 nF (on-chip)**
P_{OUT} (Max.)	43.3 mW	30.42 mW	3.2 mW	112.5 mW	24.8 mW	40 mW	**64.8 mW**
Voltage conversion ratio	0.94–0.95 (R_L = 2 kΩ) 0.82–0.84 (R_L = 100 Ω)	0.76–0.81 (R_L = 500 Ω)	0.82–0.89 (R_L = 1 kΩ)	N/A	0.873–0.93 (R_L = 1.8 kΩ) 0.79–0.89 (R_L = 500 Ω)	1.4–1.6 # (R_L = 100 Ω)	**0.912–0.946 (R_L = 2 kΩ) 0.904–0.924 (R_L = 500 Ω)**
Power conversion efficiency	82%–87% * (R_L = 500 Ω)	68%–80.2% (R_L = 500 Ω)	60%–81.9% (R_L = 1 kΩ)	93% * (w/ load chip)	82.2%–90.1% (R_L = 500 Ω)	72.5%–85% (R_L = 500 Ω)	**89.1%–91.4% (R_L = 500 Ω)**

#Voltage doubler;
*Simulated PCE

IV. MEASUREMENT RESULTS

The proposed fully integrated active rectifier was fabricated in a standard 0.35 μm CMOS process. Fig. 17 shows the chip micrograph that measures 1275 μm × 890 μm including the pads. The output capacitor of the active rectifier is integrated on-chip using a 2 nF MOS capacitor.

Fig. 18 shows the measured AC input and DC output waveforms of the active rectifier at different output voltages with a load resistor of 500 Ω. Without delay-compensation [Fig. 18(a)], the on/off delays can be clearly identified. Serious ringing was observed for the AC input waveforms, and the ringing inside the chip is expected to be even more serious. With delay-compensation [Fig. 18(b)], both the on- and off-delays were well eliminated in all cases, and the ringing disappeared, demonstrating the effectiveness and accuracy of the proposed technique. As shown in Fig. 19, the measured VCRs with the proposed technique are higher than 90% over the whole input range when $R_L = 500\ \Omega$ and 2 kΩ, improved by at least 5% when compared to the case without delay-compensation. The peak VCR is 94.6% when $R_L = 2$ kΩ. Fig. 20 shows the measured ΔV_{DC} under different conditions with and without delay-compensation. As expected, ΔV_{DC} is greatly reduced by eliminating the on/off delays.

The PCE was measured in the same way as discussed in [13]. As shown in Fig. 21(a), the measured PCEs with the output voltage that ranges from 1.8 to 3.6 V are higher than 88.6% when $R_L = 200\ \Omega$ and 89.1% when $R_L = 500\ \Omega$, respectively. Compared to the results of no delay-compensation, PCEs are improved by at least 6% and 9%, respectively. In Fig. 21(b), the measured PCEs with R_L that ranges from 200 Ω to 2 kΩ are both higher than 83.8% when $V_{\mathrm{DC}} = 2.5$ and 3.3 V. Compared to the results of no delay-compensation, PCEs are both improved by at least 6%.

Table III compares the performance of the proposed work with start-of-the-art active rectifiers. The proposed active rectifier achieves high PCE and high VCR over a wide output and loading range. More importantly, the proposed adaptive on/off delay-compensation technique is insensitive to PVT variations and mismatches, making it one of the most effective techniques in designing active rectifiers for WPT.

V. Conclusion

This paper presents an adaptive on/off delay-compensation technique for improving the performance of active rectifiers for WPT systems. The effects of on/off delays are studied with either a parallel-resonant or a series-resonant circuit at the secondary coil. By adding two feedback paths to the active diodes, the on/off delays are accurately compensated for under all conditions. A simple one-shot scheme is also used to prevent multiple pulsing of the power transistors. Compared to published delay-compensation schemes, the proposed technique is insensitive to PVT variations and mismatches. A fully integrated active rectifier that targeted at biomedical applications was fabricated in a standard 0.35 μm CMOS process and experimental results verified the effectiveness of the proposed technique. The proposed active rectifier achieves high PCE and high VCR over a wide output and loading range.

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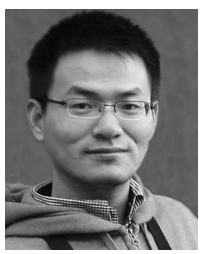

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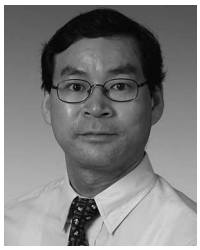

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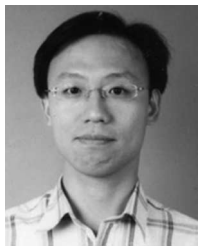

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