A 1-V 4-mW Differential-Folded Mixer With Common-Gate Transconductor Using Multiple Feedback Achieving 18.4-dB Conversion Gain, +12.5-dBm IIP3, and 8.5-dB NF

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***Abstract*— This article reports a novel differential-folded mixer with multiple-feedback techniques for performance enhancement. Specifically, we introduce the capacitor cross-coupled (CCC) common-gate (CG) transconductance stage to improve the noise figure (NF) at low power by boosting the effective transconductance, while enhancing the linearity via suppressing the second-order harmonic distortion. Typically, the created loop gain of the CCC can raise the third-order intermodulation (IM3) distortion, penalizing the input-referred third-order intercept point (IIP3). Here, we propose a positive and a second capacitive feedback into the CCC CG transconductor, not only to suppress the IM3 distortion current but also adds in design flexibility to the input transistors. Furthermore, the positive feedback also improves the input impedance matching, conversion gain, and NF through a flexible design criterion. Prototyped in a 0.13-μm process, the proposed mixer operating at 900 MHz dissipates 4 mW at 1 V. The measured double sideband (DSB) NF is 8.5 dB, the conversion gain (G_C) is 18.4 dB and the IIP3 is +12.5 dBm.**

***Index Terms*— Capacitive feedback, CMOS, high linearity, mixer, positive feedback, third-order intercept point (IIP3), third-order intermodulation (IM3) cancellation.**

I. Introduction

THE nonlinearity of a wireless receiver can be dominated by an active mixer due to the gain of the forefront low-noise amplifier (LNA). During frequency conversion, undesired harmonics are also generated that coexist with the weak desired signal, degrading the sensitivity of the receiver. Yet, most active-mixer topologies suffer from a tight tradeoff between the conversion gain (G_C), noise figure (NF), and linearity.

To achieve better linearity under high G_C and low NF, a number of recently reported active-mixer topologies are proposed with combined LNA into the transconductance stage of the mixer. In [1], a noise-canceling approach from [2] was adopted to achieve broadband input impedance matching and low NF simultaneously. The circuits in [3] and [4] adopt a resistive-feedback noise-canceling transconductor to enable wideband operation with low NF and high linearity.

Recently, several narrowband high-linearity active-mixer topologies based on second-order intermodulation (IM2) injection have been reported [5]–[7], achieving a third-order-intercept point (IIP3) beyond +9 dBm and consuming between 4 and 5.8 mW of power. However, this IM2 injection adopts an extra squaring circuit, which causes phase shift in the generated IM2 signals and deteriorates IIP3. Moreover, these works have been verified only through simulations extraction, without impedance matching at the input–output terminals.

Feedback is a widespread technique for linearizing circuits, but at the penalty of gain and noise degradation [8]–[11]. The second-order harmonic cancellation in capacitive cross-coupling (CCC) [8], positive feedback [9], and positive–negative feedback [10] can be applied to the common-gate (CG) transconductor to cancel the third harmonic, while breaking the tradeoffs between the input impedance matching and the NF. However, high linearity has to compromise with the gain and the power consumption. Recently, a high linearity and high gain dual capacitor cross-coupled (DCCC) transconductor with low power consumption has been reported [11]. Since the second feedback entails a direct voltage-to-current feedback loop between the drain and the source nodes of the CG transistor, it creates a correlation between the input impedance matching and the gain to the feedback capacitance C_{fb2}, and the load impedance Z_L, resulting in suboptimal linearity. Moreover, this passive capacitive feedback requires a large loop gain to linearize

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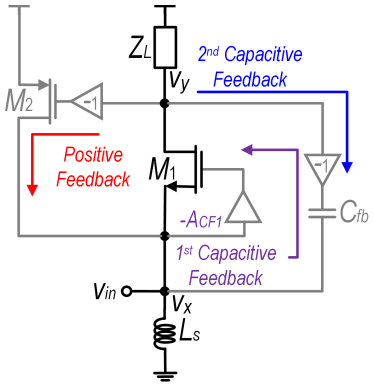


Fig. 1. Schematic of the proposed multiple-feedback transconductor. The first capacitive feedback reduces the NF by increasing g_m by a factor 2 while saving the power consumption. The positive feedback together with the second capacitive feedback suppress the IM3 distortion current and add flexibility to the design.

the nonlinearities of the main circuit when compared with the active feedback [12]. Thus, large load impedances can be explored as an off-chip element, while varying the value of C_{fb2} to provide the required loop gain with a minimum tradeoff between the gain and the input-impedance matching. Yet, these bulky inductor loads are not viable to be integrated as an on-chip component due to its low Q factor and large footprint. Besides, it adds noise and degrades the linearity of the circuit.

In this article, we propose to use another positive feedback loop for the DCCC transconductor to create an effective linearization, while creating additional design flexibility without compromising the interdependent performance metrics. Fig. 1 illustrates the single-ended model of our transconductance stage. Due to the nature of the CCC configuration, the first capacitive feedback structure improves the NF and reduces the second-order harmonic of the transconductor with low power consumption. The proposed positive feedback in conjunction with the second capacitive feedback cancels the third-order intermodulation (IM3) distortion while adding a new degree of freedom in the selection of the operating region of the input transistors while retaining the noise and G_C performances of the transconductance stage. Furthermore, the positive feedback scheme introduced into the DCCC CG transconductor also improves the input impedance matching, the NF, and the G_C performances with a flexible design criterion. We combine the proposed differential transconductor stage into a folded mixer successfully validating the concept. We also adopt an *LC*-folded configuration at the output of the transconductance stage to maintain a high drain-to-source voltage in the input transistors, while attenuating the low-frequency IM2 signal to improve the linearity of the mixer.

We organize this article as follows. Section II presents and analyzes in detail the proposed mixer. Section III summarizes the simulated and the measured results comparing them to the state-of-the-art mixer topologies, followed by the conclusions in Section IV.

II. Design and Analysis of the Proposed Multiple-Feedback Mixer

Fig. 2 shows the full schematic of the proposed mixer that implements the multiple feedback concept. The transistors M_1 and M_2 are the main transistors, whereas transistors M_4–M_7 form the pMOS-based LO switching quad and also construct a current-steering structure raising the design flexibility. The source of M_1 at one branch is cross-connected with the gate of M_1 at another branch through the capacitor C_{fb1}. The boosted CG transconductor effectively reduces the second-order distortion in the signal path due to the nature of the cross-coupling scheme, while doubling the transconductance g_{m1}. The cross-coupled capacitor C_{fb2} creates another passive feedback path other than the one created by C_{fb1}. The third feedback utilizes transistor M_2 which creates a current feedback to enhance the gain, the NF, and the input-impedance matching with an aid in the freedom of selection of g_{m1}. With the positive and second capacitive feedback, we are able to improve the linearity with the IM3 signal suppression.

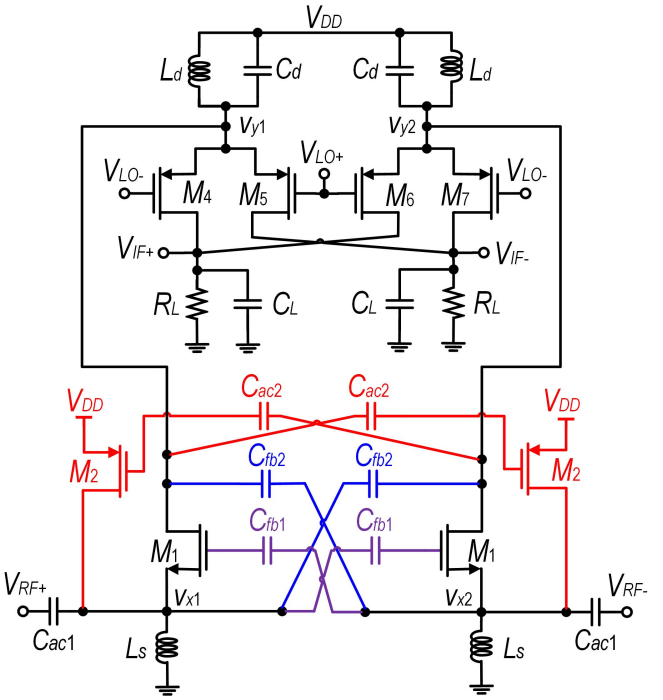


Fig. 2. Schematic of the proposed multiple-feedback differential-folded mixer (bias circuit not shown).

A. Input Matching and Effective Transconductance

Fig. 3 shows the equivalent half-circuit small-signal model of the proposed transconductance stage for the quantitative analysis. C_p is the total parasitic capacitance associated at the input pad, and at the source, and at the drain of M_1 and M_2. C_{dn} models the capacitive load defining the parallel combination of the dynamic and parasitic capacitors at the output node. We define the impedance Z_d by $R_{\rm sw}||j\omega L_d||(1/j\omega C_{dn})$, where $R_{\rm sw}$ is the output resistance of the switching transistors. $v_{x1,2}$ and $v_{y1,2}$ are the source and gate voltages of M_1, respectively. By setting $g_{m1}(1+A_{CF1}) \gg j\omega C_{fb2}$, the input impedance becomes

$$Z_{\rm in}(j\omega) = \frac{1}{g_{m1}(1+A_{CF1})\left(1+\frac{(j\omega C_{fb2}-g_{m2})Z_d}{1+j\omega C_{fb2}Z_d}\right)} \left\| \frac{1}{j\omega C_x} \right\| j\omega L_s \quad (1)$$

where $C_x = C_p + C_{fb2}$ and $A_{CF1} = (C_{fb1} - C_{gs1})/(C_{fb1} + C_{gs1})$. C_{gs1} is the gate–source capacitance of M_1. For $C_{fb1} \gg C_{gs1}$, $A_{CF1} \approx 1$. In practice, we select the value of L_s to resonate with the capacitance C_x at the operating frequency, and thus, the first term in (1) plays a key role in the input-impedance matching. Complementing the condition for input-impedance matching yields

$$g_{m1} = \frac{1}{2R_s(1 - g_{m2}R_{\rm sw})} \tag{2}$$

$$L_d = \frac{1}{\omega_o^2[C_{dn} + C_{fb2} + (C_{fb2}/g_{m2}R_{\rm sw})]} \tag{3}$$

where R_s is the terminating source resistance. When $g_{m2} = 0$, g_{m1} is constrained by the matching condition and the inductance L_d is significantly dependent on the capacitances C_{fb2} and C_{dn}. With the additional term $g_{m2}R_{\rm sw}$ due to the positive feedback, the input impedance can be varied, which also offers a degree of freedom in the selection of the values of C_{fb2} and L_d to set the reactance of the input impedance to zero. Comparatively, we reduce the required load inductance L_d to the value of the load inductance in the DCCC circuit. Thus, this allows the integration of L_d on-chip which reduces the silicon area.

It appears that the input-impedance matching condition imposes two boundaries on the feedback loops as follows: 1) $|(j\omega C_{fb2} - g_{m2})(Z_d||1/j\omega C_{fb2})| < 1$ which appears due to the input stability condition from (1) and 2) $g_{m2}R_{\rm sw} < 1$ which is due to the finite-input transconductance from (2).

At matching condition, the effective transconductance G_m $(=i_{\rm out}/v_s)$ of the proposed multiple-feedback transconductor will be

$$|G_m(\omega_o)| \approx \frac{g_{m1}}{\sqrt{1+\beta^2}} = \frac{1}{2R_s(1 - g_{m2}R_{\rm sw})} \cdot \frac{1}{\sqrt{1+\beta^2}} \tag{4}$$

where β denotes the ratio of $\omega_o C_{fb2}$ to g_{m2}, with β and g_{m1} directly related to the G_m of the transconductance stage. Thus, G_m is limited in the conventional DCCC architecture due the restricted g_{m1} in achieving input-impedance matching, as well as the selection of C_{fb2} in providing a high loop gain for good linearity. In the presence of positive feedback, g_{m1} can be increased to a higher value than that of the DCCC topology to reach a high G_m regardless of the input impedance matching.

The overall conversion gain G_C is

$$G_c(\omega_o) \approx \frac{2}{\pi} g_{m1}R_L \left(1/\sqrt{1+\beta^2}\right) \tag{5}$$

at the frequency of interest.

B. Stability

The multiple feedback in the CCC transconductor imposes a circuit stability analysis. This is often evaluated by a return ratio (RR) approach defined as the difference ratio of the output currents transconductor with and without the feedback [13]. Assuming $2g_{m1} \gg j\omega C_{fb2}$, the RR for the proposed transconductor will be

$$\text{RR} = \frac{2g_{m1}R_s}{1 + 2g_{m1}R_s}(j\omega C_{fb2} - g_{m2}) \left(Z_d \| \frac{1}{j\omega C_{fb2}}\right). \tag{6}$$

The second capacitive feedback and active feedback can work as a single negative or positive, depending on the selection of the feedback gain loop. We tune our design to have a positive feedback by setting the resultant $(j\omega C_{fb2} - g_{m2})[(1/j\omega C_{fb2})||Z_d]$ lower than 0. The stability condition of $0 < \text{RR} < -1$ can be guaranteed with a proper choice of the LC tank while meeting the input matched condition (1).

C. Noise Analysis

Under the input matching condition, the noise factor (F) of a single transconductance stage derived at ω_o is

$$F = 1 + \frac{\gamma}{\alpha}\frac{1 - g_{m2}R_{\rm sw}}{1 + A_{CF1}} + \frac{\gamma}{\alpha} g_{m2}R_s \tag{7}$$

where α is the ratio of the device transconductance to zero bias the drain-to-source conductance and γ is the coefficient of the gate noise. The second term represents the channel-noise contribution of M_1, reduced through A_{CF1} and the positive feedback. The third term shows noise induced by M_2 and it is decreased by using a small g_{m2}. Then, evidently the NF of the proposed transconductor is smaller than that of a typical DCCC transconductor.

D. Linearity

The transconductance stage will dominate the linearity in a down-conversion mixer if we assume that the switching stage is ideal. We use the simplified equivalent circuit of Fig. 3 to calculate the IIP3 of the proposed transconductance stage. We approximate C_{gs1} to a value much smaller than C_{fb1} in order that the second-order signal at v_{x1} has the same magnitude and phase of the second-order signal at the gate node of M_1 at another branch (see Fig. 2). Similarly, for the second-order signal at the v_{x2} and v_{g1} nodes, the second-order nonlinear transconductance of M_1 will be zero, $g'_{m1}v_{gs1}^2 \cong 0$ [11]. Hence, the nonlinear drain current of M_1 and M_2 can be modeled by the third-order Taylor series expansion as

$$i_{\rm ds1} \approx -g_{m1}(1 + A_{CF1})v_x - g''_{m1}(1 + A_{CF1})^3 v_x^3 + \cdots \tag{8}$$

$$i_{\rm ds2} = -g_{m2}v_y - g'_{m2}v_y^2 - g''_{m2}v_y^3 + \cdots \tag{9}$$

where $v_{\rm gs}$ and $v_{\rm ds}$ are gate–source and drain–source voltages, respectively. g_{mk}, g'_{mk}, and g''_{mk} are the fundamental transconductance, first- and second-order derivatives of the k transistor transconductance, respectively. From (8), the fundamental signal is amplified by the factor of $(1 + A_{CF1})$ due to the g_m-boosting feature of the CCC topology, and the second-order nonlinearity is reduced to zero, so that the second-order harmonic feedback effect to the IIP3 can be eliminated. Yet, the third-order transconductance increases by a factor of $(1 + A_{CF1})^3$ when compared with the conventional CG transconductor despite the reduction in the second-order distortion. The third-order nonlinear signal defines the IM3 distortion at low signal levels, and, thus, determines the IIP3 of the overall circuit. Therefore, it is outmost essential to minimize the third-order nonlinearity in the output current signal to raise the IIP3 significantly. The relaxed second-order nonlinear contribution to IIP3 in CCC topology will ease the cancellation process of third-order distortions.

To cancel the third-order distortion of the CCC transconductor implies the utilization of additional positive and second capacitive feedback in the CCC topology. With these additional feedback in the CCC transconductor, another IM3 component will appear at the drain current in addition to the generated IM3 distortion signal. By a proper selection of the biasing, the aspect ratio and capacitance C_{fb2} of the transistor M_2, an equal in magnitude and opposite in phase IM3 component appears with that in the main path at the output current of the transconductor, resulting in the total IM3 component to be smaller. In order to perform the nonlinear cancellation, the third-order coefficient, g_m'' of the transistors M_1 and M_2 must be opposite in phase to each other. With the inclusion of the second capacitive feedback, the operating region of the transistors M_1 and M_2 can be interchanged without degrading the other performances such as G_c, NF, and at the expense of minimal additional power. This will be explained in detail in the following description.

To theoretically verify the cancellation mechanism of the proposed technique, the equivalent small-signal circuit of the proposed transconductor as shown in Fig. 3 is analyzed using Volterra series. For weakly nonlinear operation, the output current of the transconductance stage can be presented as a function of the input voltage v_s by using Volterra series as

$$i_{\text{out}} = G_1(\omega) \circ v_s + G_2(\omega_1, \omega_2) \circ v_s^2 + G_3(\omega_1, \omega_2, \omega_3) \circ v_s^3 \tag{10}$$

where "$\circ$" represents the Volterra kernel operator, ω denotes the dependent frequencies, and G_1, G_2, and G_3 model the first-, second-, and third-order transconductance of the proposed transconductor, respectively.

With a lengthy derivation, reported in the Appendix, we obtain an expression for the Volterra kernels G_n that describe the nonlinearity of the proposed transconductor as

$$G_1(\omega) = -\frac{Z_d(\omega)}{R_s R_{\text{sw}}} \cdot \frac{g_{m1}(1 + A_{CF_1}(\omega)) - Y_{fb2}(\omega)}{V(\omega)} \tag{11}$$

$$G_2(\pm\omega_1, \mp\omega_2) = \frac{Z_d(\pm\omega_1 \mp \omega_2)}{R_{\text{sw}} V(\pm\omega_1 \mp \omega_2)} \times \begin{Bmatrix} [g_{m1}(1+A_{CF_1}(\pm\omega_1 \mp \omega_2)) - Y_{fb2}(\pm\omega_1 \mp \omega_2)] \\ \cdot g'_{m2} B_1(\pm\omega_1) B_1(\mp\omega_2) \end{Bmatrix} \tag{12}$$

$$G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2) = -\frac{Z_d(\pm 2\omega_1 \mp \omega_2)}{R_{\text{sw}} V(\pm 2\omega_1 \mp \omega_2)} \times \begin{Bmatrix} \left[\dfrac{1}{Z_T(\pm 2\omega_1 \mp \omega_2)} + Y_{fb2}(\pm 2\omega_1 \mp \omega_2)\right] \\ \cdot \left[g''_{m1}(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2))^3 A_1^2(\pm\omega_1) A_1(\mp\omega_2)\right] \\ + [g_{m1}(1+A_{CF_1}(\pm 2\omega_1 \mp \omega_2)) - Y_{fb2}(\pm 2\omega_1 \mp \omega_2)] \\ \cdot \left[g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2) \right. \\ \left. + 2g'_{m2} \overline{B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2)}\right] \end{Bmatrix} \tag{13}$$

where $Z_T = R_s || j\omega L_s || (1/j\omega C_x)$. In (13), the first product term represents the nonlinearity of M_1, where the third-order nonlinear coefficient g''_{m1} increases by $(1 + A_{CF1})^3$ in the presence of the CCC topology. While M_2 causes the additional second and third product terms. On the other hand, the second-order interaction term in (13) will be

$$\begin{aligned} &\overline{B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2)} \\ &= \frac{1}{3}[2B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2) + B_1(\pm\omega_2) B_2(\pm\omega_1, \mp\omega_1)] \\ &= \frac{1}{3} B_1^2(\pm\omega_1) B_1(\pm\omega_2) \times [2N(\pm\omega_1 \mp \omega_2) + N(\pm 2\omega_1)] \end{aligned} \tag{14}$$

where

$$N(\omega) = Z_d(w) \cdot \frac{g_{m1}(1 + A_{CF1}(\omega)) - Y_{fb2}(\omega)}{V(\omega)}. \tag{15}$$

The term $(2g_{m1} - Y_{fb2})$ in the numerator of $N(\omega)$ represents the feedback that C_{fb2} introduces between the input and output of the transconductor circuit. With an additional RF current source, composed by the parallel inductor L_d and capacitor C_{dn}, it is possible to minimize the low-frequency second-order distortion by decreasing the value of Z_d at the $\Delta\omega$ frequencies. Besides, the second-order nonlinear distortion still appears in the differential structure although with a negligible amount. Hence, $G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)$ in (13) can be approximated at the third-order distortion frequency as

$$G_3(\pm\omega_1 \pm \omega_1, \mp\omega_2) = \frac{Z_d(\pm 2\omega_1 \mp \omega_2)}{R_{\text{sw}} V(\pm 2\omega_1 \mp \omega_2)} \times \begin{Bmatrix} \left[\dfrac{1}{Z_T(\pm 2\omega_1 \mp \omega_2)} + Y_{fb2}(\pm 2\omega_1 \mp \omega_2)\right] \\ \cdot (1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2))^3 g''_{m1} A_1^2(\pm\omega_1) A_1(\mp\omega_2) \\ + [g_{m1}(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)) \\ - Y_{fb2}(\pm 2\omega_1 \mp \omega_2)] \\ \cdot g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2) \end{Bmatrix}. \tag{16}$$

In general, IIP3 can be described from (11) and (16) as

$$\text{IIP3}(\pm\omega_1, \pm\omega_1, \mp\omega_2) = \frac{1}{6}\frac{1}{R_s}\left|\frac{G_1(\omega_1)}{G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)}\right|. \tag{17}$$

$G_1(\omega_1)$ is typically fixed by the design parameters, and therefore the high IIP3 is achieved by reducing $G_3(\pm\omega_1, \pm\omega_1, \mp\omega_2)$. Referring to (17), if the second-order distortion is completely eliminated, IIP3 can be improved by minimizing the composite g_m''. As shown in Fig. 4, the sign of g_m'' changes from positive to negative as the operating region changes from the weak inversion to the strong inversion, with the changing spot $V_{\text{eff1,2}} = 80$ mV as the reference point. In (16), we can deduct from basic circuit theory that both A_1 and B_1 have the same signal. Therefore, by setting the coefficient transconductances of transistors M_1 and M_2, $g''_{m1,2}$ with opposite signal while varying the capacitor C_{fb2}, we can substantially reduce the IM3 distortion components.

To simplify the equation, we attribute to A_{CF1} an unity gain value. Thus, (16) implies that IM3 distortion can be canceled

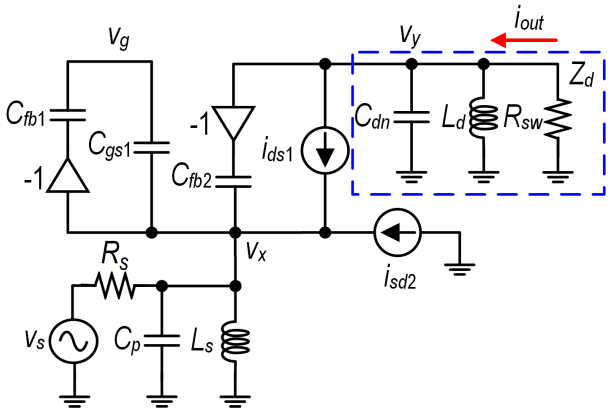


Fig. 3. Small-signal equivalent half circuit of the proposed transconductance stage.

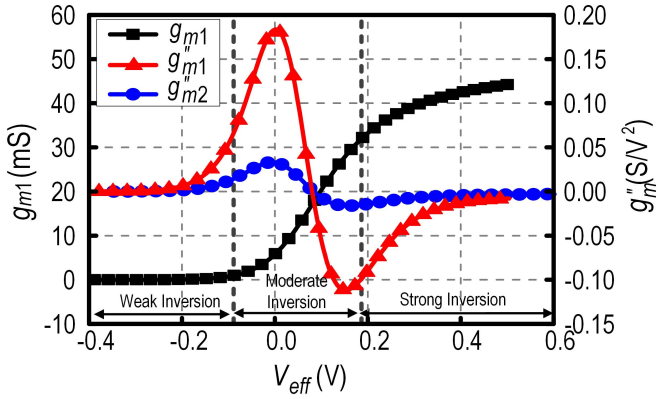


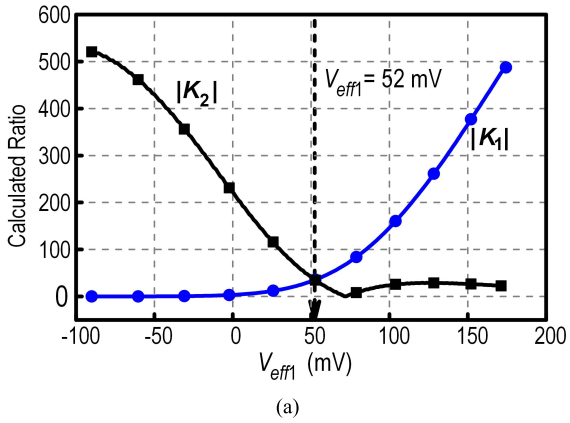
Fig. 4. Simulated g''_m of nMOS and pMOS transistors as a function of the gate overdrive voltage V_{eff}. $(W/L)_{1-2} = 60/0.13$ μm and $V_{\text{ds1,2}} = 1.0$ V.

if the following condition holds:

$$\frac{B_1^2(\pm\omega_1)B_1(\mp\omega_2)}{A_1^2(\pm\omega_1)A_1(\mp\omega_2)} = 8\frac{g''_{m1}}{g''_{m2}}\frac{(1/Z_T(\pm 2\omega_1 \mp \omega_2)) + Y_{fb2}(\pm 2\omega_1 \mp \omega_2)}{2g_{m1} - Y_{fb2}(\pm 2\omega_1 \mp \omega_2)}. \quad (18)$$

The ratio between the drain and source voltages of the input CG needs to match with the ratio of the component in the right-hand side of (18). As an initial step, we fix both capacitors C_{fb2} and gate biasing of M_2 according to the input-impedance matching and stability conditions leading to a negative value of g''_{m2}. Thus, the gate voltage of M_1 varies until we obtain the optimum gate overdrive voltage of M_1. Fig. 5(a) illustrates the plot used to find the optimum V_{eff1}, where the left and right terms in (18) are represented as K_1 and K_2, respectively. The maximum IM3 distortion cancellation should be obtained when the magnitude $K_1 = K_2$. To validate this, we perform the IIP3 simulation and measurement across V_{eff1} as shown in Fig. 5(b). The proposed mixer achieves an optimum IIP3 at V_{eff1} of 50 and 55 mV, respectively, which is reasonably close to the theoretical value of 52 mV predicted by Fig. 5(a).

An extensive set of simulations were carried out to determine how the IIP3 of the circuit varies at different operating



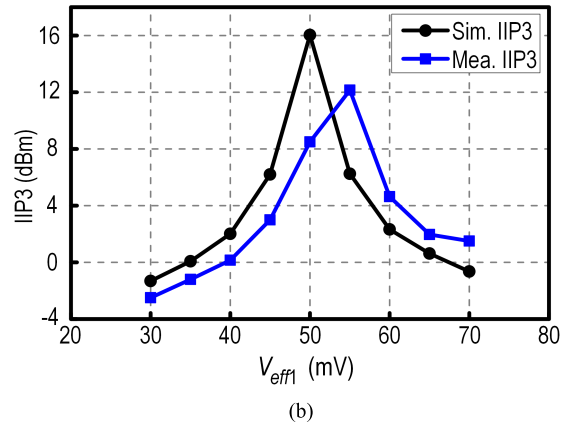


Fig. 5. (a) Calculated ratio based on (25). (b) Simulated and measured IIP3 of the proposed mixer with $W_1/L_1 = 125/0.13$ μm, $W_2/L_2 = 35/0.13$ μm, $C_{fb2} = 280$ fF, and $V_{\text{eff2}} = 150$ mV.

TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED MIXER

Parameter	$(W/L)_{4\text{-}7}$ (μm)	L_s (nH)	L_{d2} (nH)	Q_s	Q_d	C_d (fF)	C_{fb1} (pF)
Value	75/0.13	10	17	8.2	9.8	185	8.5

regions of M_1 and M_2. Fig. 6(a) and (b) illustrates the 3-D plot of the simulated IIP3 across the gate overdrive voltages of M_1 and M_2. We selected the capacitor C_{fb2} accordingly to provide the required magnitude in (18) to attenuate the third-order kernel of the transconductance stage output current. The size of the transistors is also optimized to provide the necessary g_m. In both designs, the capacitance C_{fb1}, inductance L_s, RF choke (L_d and C_d), load (R_L and C_L), and switching transistors are set to be the same, and their parameter values are listed in Table I.

As shown in Fig. 6, the high peaks of IIP3 are acquired for certain optimum bias point at which the complete distortion cancellation happens. For example, in case 1, for large V_{eff1} and low V_{eff2}, we achieve the high peak IIP3 value around $V_{\text{eff1}} = 130$ mV and $V_{\text{eff2}} = 40$ mV with $C_{fb2} = 390$ fF as illustrated in Fig. 6(a). In case 2, when M_2 is biased with a large V_{eff2} while reducing V_{eff1}, the optimal IIP3 is obtained at $V_{\text{eff1}} = 50$ mV and $V_{\text{eff2}} = 150$ mV with $C_{fb2} = 280$ fF, as shown in Fig. 6(b). Table II summarizes the device sizes and other performances at these selected points. For case 1, there

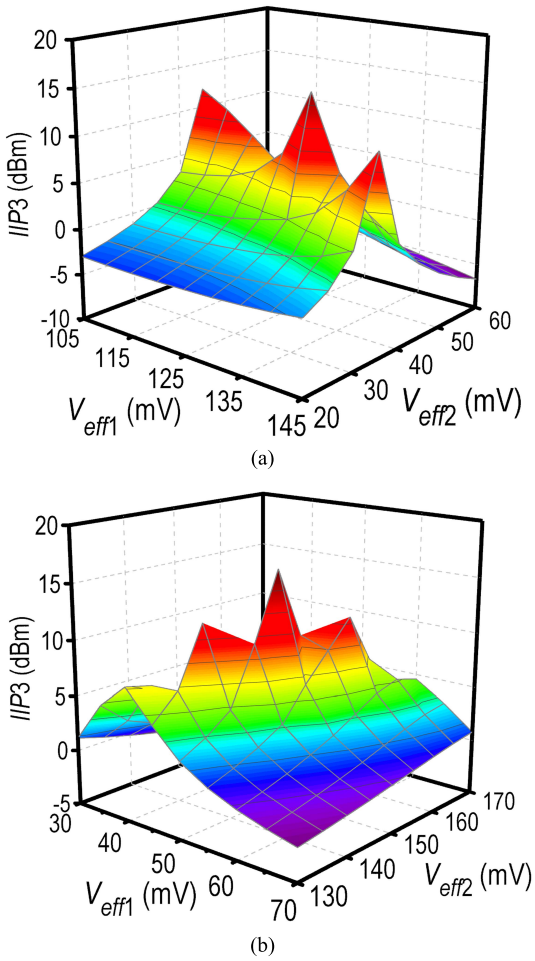


Fig. 6. Simulated IIIP3 of the proposed mixer when setting (a) $V_{\text{eff1}} > 80$ mV and $V_{\text{eff2}} < 80$ mV with $W_1/L_1 = W_2/L_2 = 60/0.13$ μm and $C_{fb2} = 390$ fF (case 1) and (b) $V_{\text{eff1}} < 80$ mV and $V_{\text{eff2}} > 80$ mV with $W_1/L_1 = 125/0.13$ μm, $W_2/L_2 = 35/0.13$ μm, and $C_{fb2} = 280$ fF (case 2).

TABLE II
MIXER IN DIFFERENT BIAS REGIONS

	V_{eff1} (mV)	V_{eff2} (mV)	g_{m1} (mS)	g_{m2} (mS)	C_{fb2} (*f*F)	W_1/W_2 (μm/μm)
Case 1	130	40	28	3.25	390	60/55
Case 2	50	150	28	4.9	280	125/32
	I_T (mA)	V_{DD} (V)	IIP3 (dBm)	G_C (dB)	NF (dB)	P1dB (dBm)
Case 1	4.4	1.0	15.0	18.1	8.2	-15.6
Case 2	4.0	1.0	16.0	18.4	8.3	-15.8

is a tiny drop in G_C (~0.3 dB) due to β increment according to (5). Besides, the NF is almost identical in both cases, as g_{m2} is in a tradeoff with noise. Furthermore, the achieved IIP3 is basically the same while maintaining G_C, NF, and P1dB performances. These characteristics imply that the design of the proposed transconductor allows the selection of the operating region in the input transistors through the choice of capacitance C_{fb2} and the gate biasing of transistor $M_{1,2}$.

Furthermore, the positive feedback in the DCCC transconductor provides higher linearity through the IM3 cancellation, which exhibits more flexibility in the simultaneous optimization of the input impedance matching,

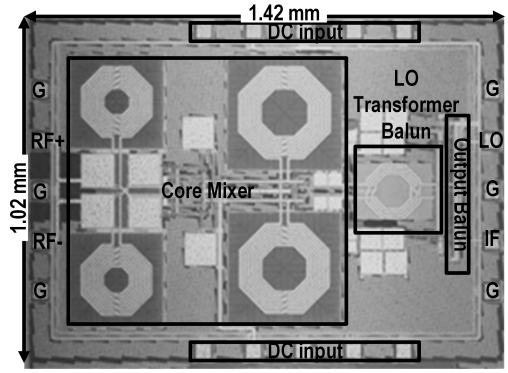


Fig. 7. Die microphotograph.

the conversion gain, and the NF instead of conquering the total gain through the conventional method in the DCCC circuit.

When the transistor operates in a moderate region, the required fundamental transconductance value is obtained through the increase in its device size which in turn increases the parasitic capacitance effect, however with the inductors located at the source and the drain of the transistor M_1, this effect can be nullified. However, the existence of the narrowband *LC* tank and the second capacitive feedback will limit the operating bandwidth. Therefore, this technique is suitable for narrowband applications.

III. Measurement Results and Comparison

The proposed mixer, implemented in 0.13-μm CMOS, follows the specifications and can be used as a building block for a down-conversion receiver IC in 900-MHz TV applications. Fig. 7 shows the die micrograph which occupies a die area of 1.42 × 1.02 mm^2 including the pads.

To characterize the performance, we utilized on-chip wafer probing. We also use an on-chip stacked 1:1 transformer-based balun at the LO input to provide a differential LO input signal with 0 dBm of input power, whereas we used an on-chip active buffer at the IF output to realize the 50-Ω output impedance matching for measurement purposes. The measurement uses an external RF balun to convert the single-ended RF signal into a differential output. The measured power consumption excluding the IF buffer is 4 mW at a supply voltage of 1 V.

Fig. 8 shows the measured and simulated RF input reflection coefficient (S_{11}) of the proposed down-conversion mixer. The measured $|S_{11}|$ is less than 15 dB at 900 MHz.

We designed and simulated the reported DCCC architecture and the proposed circuits to compare their performances, with the same transistor sizes and load impedances for a fair comparison. In DCCC, we optimized the capacitor C_{fb2} and the bias voltage of the input CG transistors to operate at 900 MHz. Fig. 9 exhibits the measured and simulated conversion gain across the RF frequency of the proposed mixer and the conventional DCCC transconductance-based mixer. There, the conversion gain is equal to 18.4 dB, which has been improved by ~3 dB with respect to the conventional DCCC mixer. Fig. 10 illustrates the measured and simulated double-sideband (DSB) NF. The simulated NF performance is better in the proposed mixer with a 2-dB improvement, indicating a

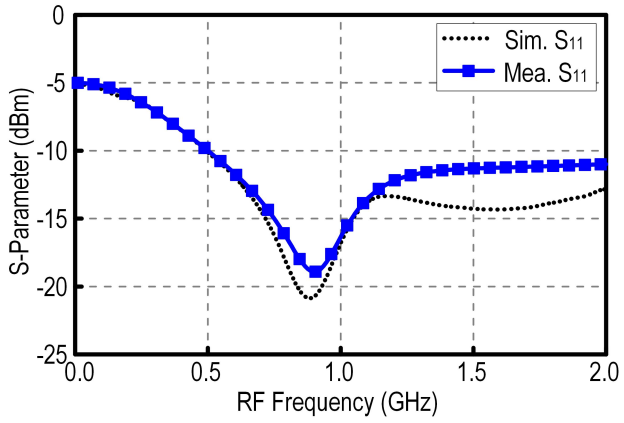


Fig. 8. Measured and simulated S_{11}.

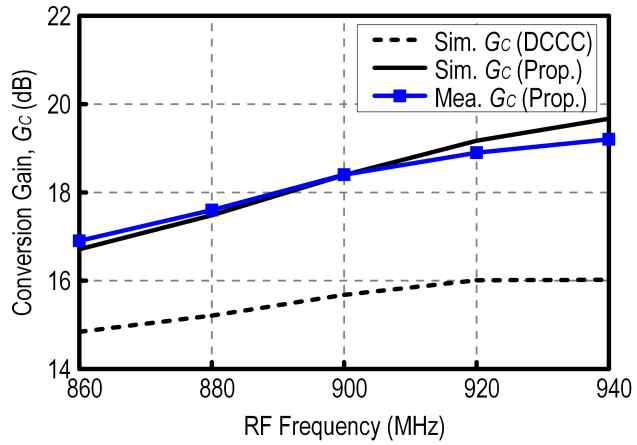


Fig. 9. Measured and simulated conversion gain versus RF frequency.

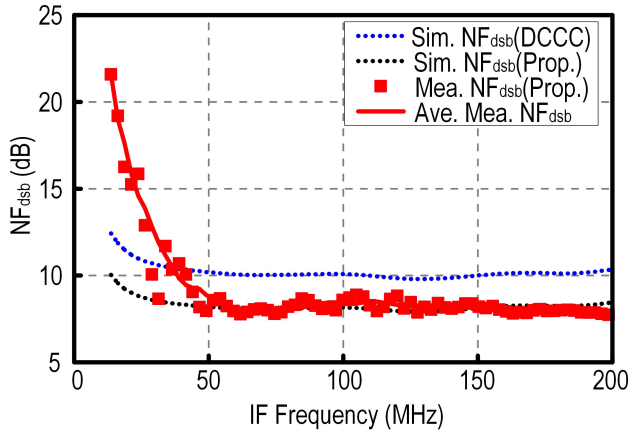


Fig. 10. Measured and simulated DSB NF versus IF frequency.

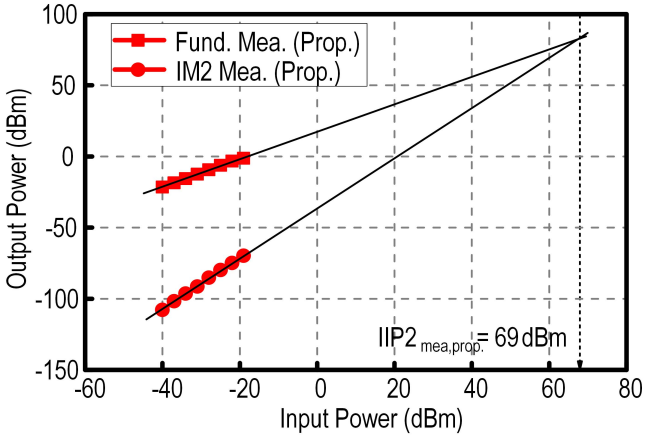


Fig. 11. Measured IIP2 of the proposed mixer.

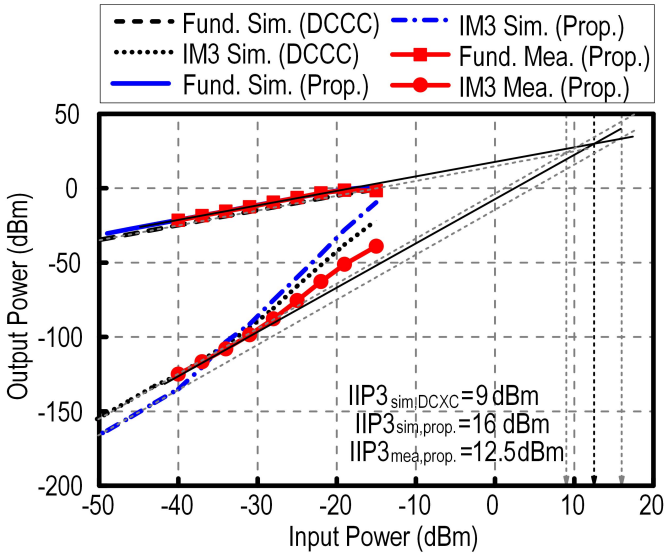


Fig. 12. Measured and simulated IIP3 results.

TABLE III
CORNER AND TEMPERATURE VARIATIONS IN THE PROPOSED CIRCUIT (SIMULATED)

Parameters	*IIP3 (dBm)*	*P1dB (dBm)*	*G_C (dB)*	*NF (dB)*	*Power (mW)*
FF@-40°C	13.5	-19.5	20.5	7.6	4.7
FF@85°C	14.5	-14.7	14.5	9.7	4.3
TT@27°C	16.0	-15.8	18.4	8.3	4.0
SS@85°C	15.2	-12.5	12.0	9.5	3.2
SS@-40°C	13.8	-16.1	21.3	7.1	3.5

measured DSB NF of ∼8.5 dB. The noise discrepancy between the measurement and simulation results at low frequency is mainly due to the starting operating frequency (10 MHz) of the noise analyzer which is in the vicinity of the operating IF frequency (50 MHz).

The measured input-referred second-order intercept point (IIP2) of the proposed mixer result is shown in Fig. 11, where it obtains 69 dBm of IIP2. The mixers IIP3 were obtained with a two-tone test, with the same amplitude and a frequency spacing of 1 MHz (900 and 901 MHz). Fig. 12 shows the measured and simulated IIP3 of the mixers. The measured IIP3 is +12.5 dBm. This value also indicates that the proposed mixer has −18.0 dBm measured 1-dB input compression point (P1dB). As expected, the proposed architecture shows better performances than the DCCC-based mixer. The discrepancy of the simulated and measure IIP3 point could be affected due

TABLE IV
PERFORMANCE SUMMARY AND BENCHMARK

Reference	Process (μm)	RF (GHz)	G_C(dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	FOM
[5]* VLSI'16	0.09	2.4	9.8#	15	-	+15.7	1.2	5.8	-14.9
[6]* VLSI'16	0.18	2.4	6.7	17	-	+9	1.6	4.6	-20.8
[7]* EL'14	0.09	2.4	22.1	13.2	-	+17.1	1.0	4	-4.6
[14]* TCAS-I'13	0.18	2.1	15	14	-	+15	1.8	8	-13.0
[15] TMTT'14	0.13	2.1	16.6	14.4	†-14.0	-5.24	1.0	2	-16.7
[16]* ISCAS'14	0.18	2.4	5	27**	-	+9	1.8	23.76	-38.8
[17] TMTT'13	0.13	0.3-1.2	8.8	4.8**	-8.8	-0.8	0.9	24	-19.6
[18] EL'16	0.18	0.1-2.5	8.9	9.6	-4	+5.8	1.8	3.74	-13.0
[19] JSSC'13	0.16	0.9	17.6	10.1**	†-18.0	11.8	1.8	19.62	-13.3
[20] EL'18	0.13	0.3-3.0	15.8	8.6**	-	10.1	1.2	3.1	-5.6
This work	**0.13**	**0.9**	**18.4**	**8.5****	**-18.0**	**+12.5**	**1.0**	**4.0**	-4.0

*Simulated results **DSB noise †Graphically estimated #Voltage conversion gain

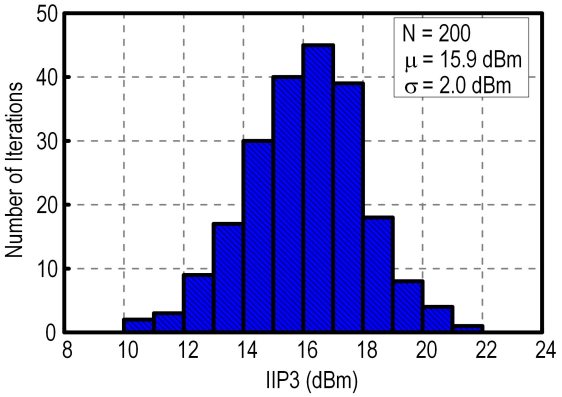


Fig. 13. IIP3 Monte Carlo simulation results of the proposed mixers.

to variation in the design parameters and also due to the constructive and destructive interferences of several nonlinearities.

Table III summarizes the simulation results in different process corner cases and temperature variations in the proposed circuit. Optimization of the overdrive voltages of M_1 and M_2 lead to a commendable performance even in worse case conditions (FF at 85 °C and SS at −40 °C). In addition, Fig. 13 plots the Monte Carlo simulation for IIP3 with process and mismatch variations.

Table IV summarizes the measured results of the proposed mixer in comparison with the state of the art recently reported in CMOS. The benchmark followed this figure of merit (FOM) [21]:

$$\mathrm{FOM} = 10\log\left(\frac{10^{(G_c(\mathrm{dB})/20)} \times 10^{(\mathrm{IIP3(dBm)}-10)/20}}{10^{(\mathrm{NF(dB)}/10)} \times P_{\mathrm{DC}}(\mathrm{mW})}\right). \quad (19)$$

The designed prototype mixer reaches the highest FOM which indicates the effectiveness of the proposed linearization technique without compromising other performances, like the conversion gain, the NF, and the power consumption.

IV. CONCLUSION

A novel multiple-feedback active mixer topology has been introduced with concurrent improvement of the linearity, NF, and conversion gain. The reduction of the second-order harmonics in the CCC topology, along with the doubling of the effective transconductance, allows this mixer to obtain low noise and low power. The additional third feedback composed by the positive feedback scheme contributes to the relaxation of the constraints inherent to the conventional DCCC CG transconductor. Prototyped in 0.13-μm CMOS, the mixer measures an IIP3 of +12.5 dBm in a two-tone test, together with an NF of 8.5 dB and a conversion gain of 18.4 dB at an IF = 50 MHz. The mixer consumes 4 mW at 1 V.

APPENDIX

In this section, the distortion cancellation mechanism is explained in detail by carrying out a Volterra series analysis based on the harmonic input method. This theoretical analysis facilitates the calculation of the frequency-dependent harmonic distortion coefficient and provides an expression for the IIP3 of the proposed transconductor. Referring Fig. 3, we conducted the complete derivation of the Volterra series kernels for proposed transconductance.

The node voltages can be expressed by Volterra kernels in terms of the excitation input voltage v_s as

$$v_x = A_1(\omega) \circ v_s + A_2(\omega_1, \omega_2) \circ v_s^2 + A_1(\omega_1, \omega_2, \omega_3) \circ v_s^3 \quad (20)$$

$$v_y = B_1(\omega) \circ v_s + B_2(\omega_1, \omega_2) \circ v_s^2 + B_1(\omega_1, \omega_2, \omega_3) \circ v_s^3 \quad (21)$$

$$\begin{vmatrix} \Sigma_{i=1}^{\{2,3\}}(g_{m1}(1 + A_{CF1}(\omega_i)) + Y_x(\omega_i) + Y_{fb2}(\omega_i) + Y_s) & \Sigma_{i=1}^{\{2,3\}} Y_{fb2}(\omega_i) - g_{m2} \\ \Sigma_{i=1}^{\{2,3\}}(g_{m1}(1 + A_{CF1}(\omega_i)) - Y_{fb2}(\omega_i)) & -\Sigma_{i=1}^{\{2,3\}}(Y_{fb2}(\omega_i) + Y_d(\omega_i)) \end{vmatrix} \begin{vmatrix} A_n(\omega_{1,\ldots,n}) \\ B_n(\omega_{1,\ldots,n}) \end{vmatrix}$$
$$= \begin{vmatrix} Y_s v_s + i_{\mathrm{ds1},NLn}^{n\in\{3\}} - i_{\mathrm{ds2},NLn}^{n\in\{2,3\}} \\ i_{\mathrm{ds1},NLn}^{n\in\{3\}} \end{vmatrix} \quad (26)$$

where $A_n(\omega_1, \omega_2, \ldots, \omega_n)$ and $B_n(\omega_1, \omega_2, \ldots, \omega_n)$ are the Laplace transforms of the nth-order Volterra kernels of v_x and v_y, respectively.

On the other hand, by applying Kirchhoff's current law (KCL) equations for each node of the circuit, the following set of equations will be obtained:

$$\frac{v_s - v_x}{R_s} = \frac{v_x}{Z_x(\omega)} - i_{\text{ds1}} + i_{\text{ds2}} + Y_{fb2}(\omega)(v_y + v_x) \quad (22)$$

$$\frac{v_y}{Z_d(j\omega)} = -i_{\text{ds1}} - Y_{fb2}(\omega)(v_y + v_x) \quad (23)$$

where Y_{fb2} is the admittance of the capacitor C_{fb2} and $Z_x(j\omega) = j\omega L_s || (1/j\omega C_p)$. From Fig. 3, a nodal equation at the drain node of transistor M_1 can be derived as

$$i_{\text{out}} = -v_y / R_{\text{sw}}. \quad (24)$$

From (24), the nth-order Volterra operator G_n that describes the nonlinearity of the proposed transconductance stage will be

$$G_n = -B_n / R_{\text{sw}}. \quad (25)$$

Therefore, $B_n(\omega_1, \omega_2, \ldots, \omega_n)$ needs to be computed to obtain the G_n Volterra operators in (10). We can solve (22) and (23) recursively to compute kernels in (20) and (21).

To obtain the nth-order response of the circuit, we established a matrix equation by referring (22) and (23) as shown in (26), at the bottom of the previous page. Y_s, Y_d, and Y_x are the admittances of R_s, Z_d, and Z_x, respectively. To acquire the first-order kernels, we set the excitation voltage $v_s = 1.0$ V and the nonlinear current sources $i_{\text{dsk,NL}n}^{n\in\{2,3\}}$ of the k transistor to 0. For the second- and third-order kernels, we include the respective nth-order current source $i_{\text{dsk,NL}n}$, $n\epsilon\{2, 3\}$ in the analysis with short-circuited excitation voltage ($v_s = 0$). $\sum_{i=1}^{\{2,3\}}(\pm\omega_i)$ represents the frequency dependence of the passive components for the second- and the third-order analyses; they will be $\pm\omega_1 \pm \omega_2$ or $\pm\omega_1 \pm \omega_2 \pm \omega_3$ to the respective nonlinearity order. Using Cramer's rule, we can solve the nth-order Volterra kernels.

The first-order Volterra kernels can be found from (26) as

$$A_1(\omega) = \frac{1}{R_s} \cdot \frac{1 + A_{CF2}(\omega)}{V(\omega)} \quad (27)$$

$$B_1(\omega) = \frac{Z_d(\omega)}{R_s} \cdot \frac{g_{m1}(1 + A_{CF_1}(\omega)) - Y_{fb2}(\omega)}{V(\omega)}. \quad (28)$$

The function $V(\omega)$ in the above equations is found to be

$$V(\omega) = (1 + A_{CF2}(\omega)) \times \left\{ \begin{array}{l} \dfrac{1}{Z_T(\omega)} + g_{m1}(1 + A_{CF1}(\omega)) \\ + \dfrac{A_{CF_2}(\omega) - A_{PF}(\omega)}{1 + A_{CF_2}(\omega)} \\ \cdot (g_{m1}(1 + A_{CF1}(\omega)) - Y_{fb2}(\omega)) \end{array} \right\} \quad (29)$$

where $A_{CF2} = j\omega C_{fb2} Z_d$ and $A_{\text{PF}} = g_{m2} Z_d$.

As mentioned earlier, to find the second-order Volterra kernels, the second-order nonlinear current source is applied with original input to zero. The second-order current source can be related with the second-order transconductance coefficient as follows:

$$i_{\text{ds2,NL2}} = g'_{m2} B_1(\pm\omega_1) B_1(\mp\omega_2). \quad (30)$$

According to (26), the second-order Volterra kernels $A_2(\pm\omega_1, \mp\omega_2)$ and $B_2(\pm\omega_1, \mp\omega_2)$ are then derived as

$$A_2(\pm\omega_1, \mp\omega_2) = \frac{1 + A_{CF2}(\pm\omega_1 \mp \omega_2)}{V(\pm\omega_1 \mp \omega_2)} g'_{m2} B_1(\pm\omega_1) B_1(\mp\omega_2) \quad (31)$$

$$B_2(\pm\omega_1, \mp\omega_2) = \frac{Z_d(\pm\omega_1 \mp \omega_2)}{V(\pm\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} [g_{m1}(1 + A_{CF_1}(\pm\omega_1 \mp \omega_2)) - Y_{fb2}(\pm\omega_1 \mp \omega_2)] \\ \cdot g'_{m2} B_1(\pm\omega_1) B_1(\mp\omega_2) \end{array} \right\}. \quad (32)$$

For a two-tone excitation at ω_1 and ω_2, the expression of third-order nonlinear current source is given by

$$i_{\text{ds1,NL3}} = -g''_{m1} A_1(\pm\omega_1) A_1(\pm\omega_1) A_1(\mp\omega_2) \quad (33)$$

$$i_{\text{ds2,NL3}} = 2g'_{m2} \overline{B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2)} + g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2). \quad (34)$$

Similarly, we can derive third-order Volterra kernels from matrix equation in (26) as shown in (35), at the bottom of this page, where the bar indicates the averaging of the transfer response over all possible permutations of the Laplace variables. The desired nth-order transconductance kernels G_n can be obtained by substituting the respective kernel B_n into (36), shown at the bottom of this page.

$$A_3(\pm\omega_1, \pm\omega_1, \mp\omega_2) = \frac{1 + A_{CF2}(\pm 2\omega_1 \mp \omega_2)}{V(\pm 2\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} \left(1 + \dfrac{A_{CF2}(\pm 2\omega_1 \mp \omega_2) - A_{PF}(\pm 2\omega_1 \mp \omega_2)}{1 + A_{CF2}(\pm 2\omega_1 \mp \omega_2)}\right) \\ \cdot \left[-g''_{m1}(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2))^3 A_1^2(\pm\omega_1) A_1(\mp\omega_2)\right] \\ + \left[g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2) + 2g'_{m2} \overline{B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2)}\right] \end{array} \right\} \quad (35)$$

$$B_3(\pm\omega_1, \pm\omega_1, \mp\omega_2) = \frac{Z_d(\pm 2\omega_1 \mp \omega_2)}{V(\pm 2\omega_1 \mp \omega_2)} \times \left\{ \begin{array}{l} \left[\dfrac{1}{Z_T(\pm 2\omega_1 \mp \omega_2)} + Y_{fb2}(\pm 2\omega_1 \mp \omega_2)\right] \\ \cdot g''_{m1}(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2))^3 A_1^2(\pm\omega_1) A_1(\mp\omega_2) \\ + [g_{m1}\left(1 + A_{CF_1}(\pm 2\omega_1 \mp \omega_2)\right) - Y_{fb2}(\pm 2\omega_1 \mp \omega_2)] \\ \cdot \left[\begin{array}{l} g''_{m2} B_1^2(\pm\omega_1) B_1(\mp\omega_2) \\ + 2g'_{m2} \overline{B_1(\pm\omega_1) B_2(\pm\omega_1, \mp\omega_2)} \end{array}\right] \end{array} \right\} \quad (36)$$

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