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A Reconfigurable and Extendable Digital Architecture for Mixed Signal Power Electronics Controller

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***Abstract*— This paper presents the design of a reconfigurable and extendable digital architecture for an integrated mixed signal power electronics (PE) controller as it could achieve better performances than the purely digital or analog PE controller. A computer-based configuration software interface for the controller is developed. This works aims to develop a user-interface design platform that can easily guide the controller function in feature-shared PE applications. Here, we simplify not only the design at the software level allowing controller hardware's swift reconfigurability to save development time, but also allow parallel processing and programmable on-the-fly ability. The proposed digital controller architecture is also easily extendable by adding more building blocks to realize additional PE applications and we designed and fabricated it in 65nm CMOS. Finally, we tested experimentally the proposed digital controller in power quality compensators to verify its reconfigurability and effectiveness. This digital architecture is fundamental for future mixed signal PE controller integration.**

***Index Terms*—Building block, digital controller, reconfigurable and extendable digital architecture, mixed signal PE controller.**

I. Introduction

In modern power electronics (PE) systems such as: power quality (PQ) compensators, uninterruptible power supplies (UPS), motor drivers, renewable energy conversion systems, etc. they all require a digital controller like a microcontroller unit, a digital signal processor (DSP), a field programmable gate array (FPGA), etc. to control on/off of the PE switches for performing the corresponding functionalities [1]-[3]. Usually, the large electrical signals of the PE systems are essentially converted into small analog signals through voltage or current sensors. Then, a signal conditioning circuit (SCC) and an analog-to-digital converter (ADC) is required to adapt the input voltage range of the digital controller.

Normally, a signal sensing system is designed with full-loading consideration for a digital controller. As a result, its resolution and signal to noise ratio cannot be adjusted for different loading situations, which significantly affects its performance. To overcome the above problem, the authors in [4] proposed a programmable gain control for the input signals by field-programmable analog array (FPAA) boards. In addition, the gain is computed by the digital controller (DSP or FPGA), and then sent to FPAA for the input signal adaptive gain modification when needed. This kind of mixed signal PE controller already significantly improves the PE system performances when compared with either analog or digital controller working alone [4]. This proves that an integrated solution of both analog and digital controllers is advantageous. But, this kind of mixed signal PE controller using FPAA-FPGA/DSP with an ADC (multi-PCBs) [4] has several disadvantages:

- Costly controller hardware;
- Significant space requirement;
- Complex wire connection, easily causing unstable operation;
- Time consuming programming for FPAA and FPGA/DSP;
- High power consumption;
- Control functions not easily reconfigurable;
- May bring up significant delay in feedback loop, thus affecting the loop stability and controller performance, etc.

In addition, more reconfigurable controller designs appeared for PE system applications [4]-[7]. However, the general controller architecture to be easily reconfigurable for other applications still lacks detailed study [4]-[7].

In this paper, we propose a reconfigurable and extendable digital controller architecture with its computer based user-interface and parallel processing ability for feature-shared PE applications, the proposed digital controller architecture can bring the following benefits.

1) Less Compile and Operation Time --- The controller possesses parallel processing ability among functional building blocks and also within each building block, thus achieving fast processing speed. As the building blocks within the proposed controller are ASICs, it does not need to be compiled when used, which is more convenient.
2) Swift Reconfigurability and Less Development Time --- With the configuration software interface, the controller can be swiftly configured for different PE applications by just controlling the connection sequence of the building blocks, thus reducing the development time and human resources

Manuscript received April 13, 2018; revised June 16, 2018 and July 18, 2018; accepted July 23, 2018. This work was supported in part by the Science and Technology Development Fund, Macao SAR (FDCT) (025/2017/A1) and in part by the Research Committee of the University of Macau (MYRG2017-00090-AMSV). (*Corresponding author: C.-S. Lam*)

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when compared with digital controllers that are time-consuming in terms of programming and debugging.

3) Easy Extendable Architecture --- The functional building blocks are arranged between input and output registers, thus this controller architecture is easily extendable by adding more building blocks to realize more PE applications.

II. Proposed Reconfigurable and Extendable Digital Controller Architecture

Fig. 1 shows the concept of the generalized and reconfigurable mixed signal PE controller integrated circuit (IC) with its computer configuration software interface. For the analog, mixed signal and the digital cores, they contain different functional building blocks. This mixed signal PE controller can miniaturize the overall PE controller system that usually requires many discrete signal conditioning boards, ADC chips, digital and/or analog controllers. It not only eases the design and optimization to save cost, but achieves several features: adaptive signal conditioning, programmability on-the-fly, bandwidth and accuracy real-time selective optimization, and simplicity of implementation, thus achieving better performance than the digital or analog PE controllers.

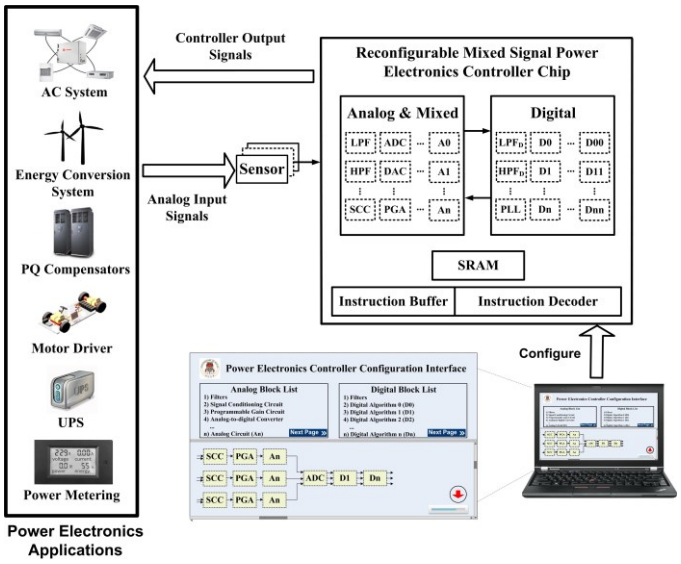

Fig. 1. Concept of generalized and reconfigurable mixed signal PE controller IC.

In Fig. 1, the analog parts can enhance the controller to obtain higher resolution, faster response and reduce digital calculation burden. As a result, the analog part is mainly composed of: SCC, analog programmable gain amplifiers (PGA), ADC/digital-to-analog converter (DAC), comparators (CMP) and analog filters such as low pass filters (LPF), high pass filters (HPF), etc., in which those operation parameters are controllable by pre-defined instructions and the digital part due to the operation and application requirements in series or/and parallel.

In this paper, from the concept of Fig. 1, Fig. 2 exhibits the reconfigurable and extendable digital controller architecture, with its control and connection concept. Its corresponding modules and their functions are given in TABLE I. The functional building blocks D0~Dn represent different algorithms for different PE applications. By controlling the connection sequence of D0~Dn through the configuration software interface, the proposed digital controller can be swiftly configured for different PE applications. TABLE II shows the algorithms of the building blocks configured for hybrid active power filter (HAPF) application. Moreover, the blocks D0~Dn can be controlled to process in sequence or in parallel.

TABLE I. Descriptions of Modules for the Proposed Controller

Modules	Functions
D0 ~ Dn	Different algorithms for PE applications
E0 ~ Ex	Input data storage (register) enable signals
Ex+1 ~ Ey	Output data storage (register) enable signals
R0 ~ Rx	Registers for storing input signals of D0 ~ Dn
Rx+1 ~ Ry	Registers for storing output signals of D0 ~ Dn
R_i0 ~ R_im	Registers for storing ADC input signals
Instruction Buffer	Buffer for storing programs
Instruction Decoder	Decoding engine for generating control signals for operation
MUX #x Select	Digital Multiplexers #x enable signals
MUX #x	Digital Multiplexers for selecting signals
SRAM	Store intermediate data
Digital Input Control	Selection of input data from ADC channels
Digital Output Control	Selection of data for output
UART	Sequential communication interface

Where y-x=x+1 in this design

TABLE II. Matching Blocks D0~D11 with HAPF Blocks

D0	*abc-αβ0*	D1	*Three Inst.pq*	D2	*LPF*
D3	*icαβ0*	D4	*αβ0-abc*	D5	*Lag π/2*
D6	*Single Inst.pq*	D7	*LPF_3*	D8	V_{dc_min}
D9	V_{dc}^{*}	D10	*DC_ctrl*	D11	*PWM*

A. Sequential Processing

For sequential processing, the building blocks D0~Dn operate in a sequential manner as shown in Fig. 3. For example, once the input data register enable signal (E0) of building block D0 is activated, the input signal for D0 will be stored in an input data register Register_in within the input data preparation cycle, then D0 can operate within a sequential processing cycle. Finally, once the output data register enable signal of D0 (Ex+1) is activated, the processed output data by D0 will be stored in the output data register Register_out within the processing done cycle. This operation cycle is repeated for other building blocks, in which the processed results will be stored in the Register_out one by one in a sequential manner. Fig. 3 illustrates the sequential connection process.

B. Parallel Processing

For parallel processing, the building blocks D0~Dn operate in a parallel manner as shown in Fig. 4. For example, once the input data register enable signals (E0~Ex) are activated, the input signals for D0~Dn will be stored in the input data register Register_in within the input data preparation cycle, then D0~Dn can operate in a parallel manner within a parallel processing cycle. Finally, once the output data register enable signals of D0~Dn (Ex+1~Ey) are activated, the processed output data by D0~Dn will be stored in the output data register Register_out simultaneously within the processing done cycle. Fig.4 illustrates the parallel connection process.

In the next section, we'll illustrate with several examples the proposed digital controller configured to control the HAPF and active power filter (APF) for PQ compensation.

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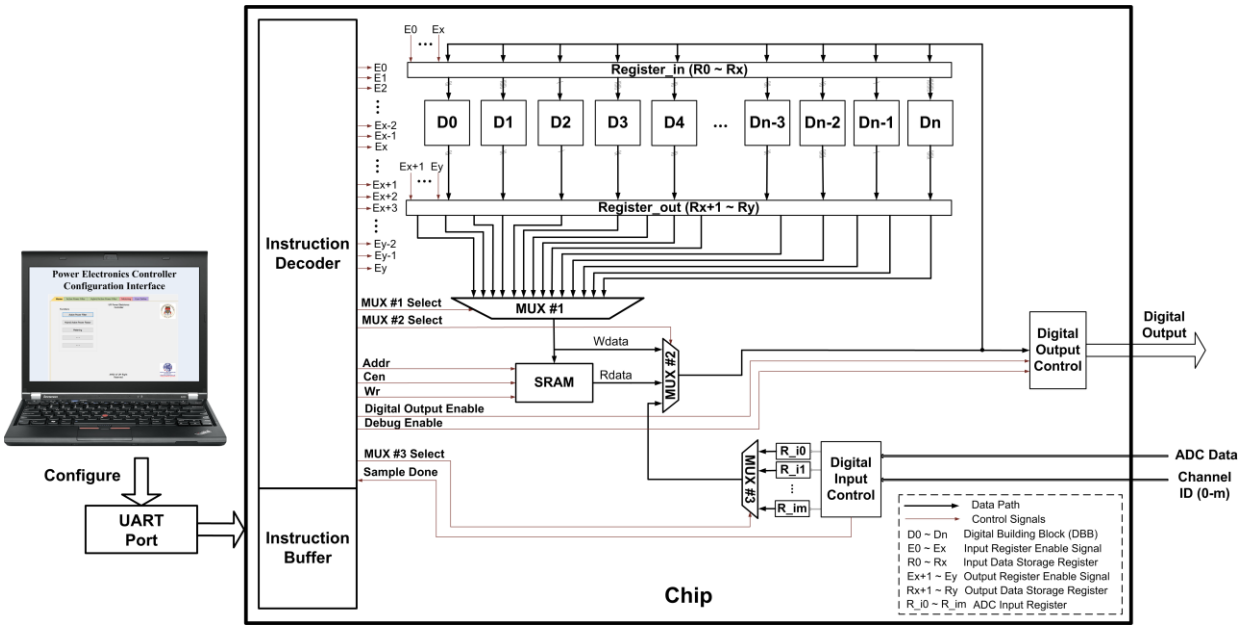

Fig. 2. Proposed reconfigurable and extendable digital controller architecture with its computer configuration software interface.

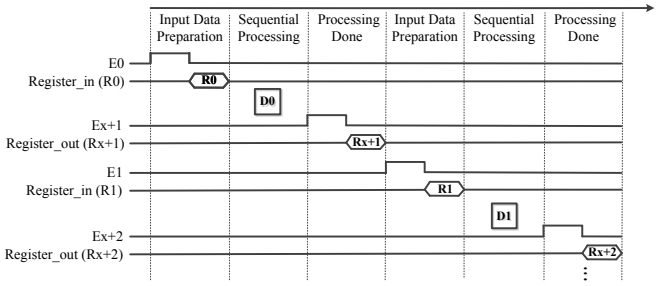

Fig. 3. Sequential processing.

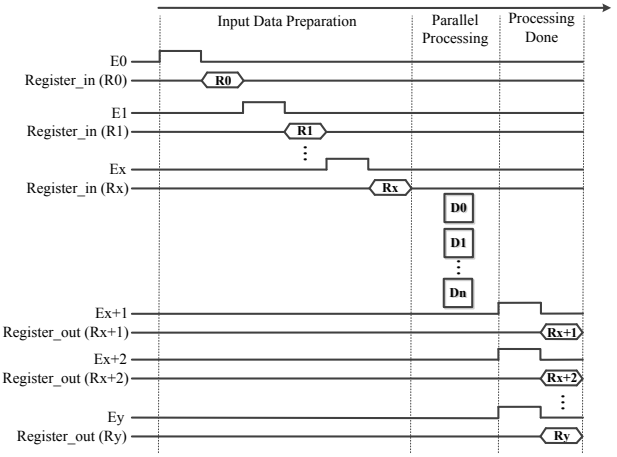

Fig. 4. Parallel processing.

III. Integrated Circuit Implementation

A. Operation Flow for a PQ Compensator

Fig. 5 presents a three-phase four-wire HAPF or APF with or without neutral inductor (PQ compensator) system, where the subscript '*x*' denotes phase *x* = *a, b, c, n*. The control algorithm for the HAPF or APF to calculate the reference compensating current i_{cx}^* is based on the three-phase and single-phase instantaneous PQ theory [8], [9]. Fig. 6 plots the block diagram of the HAPF or APF control algorithm [10], where it has 12 main building blocks (*abc-αβ0*, *Three Inst. pq*, *LPF*, *icαβ0*, *αβ0-abc*, *Lag π/2, Single Inst. pq, LPF_3,* V_{dc_min}, V_{dc}^*, *DC_ctrl*, *PWM*) to fulfill the whole calculation and control process. Each block can operate in parallel in case they have no dependency between each other. The final output signals from the PWM building block will generate the trigger signals to control the on/off of the switches T_{1x} and T_{2x} of the voltage source inverter (VSI) as in Fig. 5, in order to perform PQ compensation.

From TABLE II, we require a total of 12 building blocks for the proposed controller chip, obtained by matching the building blocks D0~D11 (Fig. 2) with those of the HAPF.

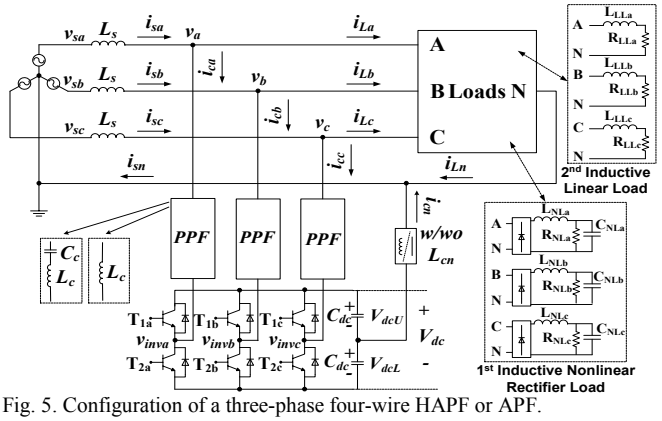

Fig. 5. Configuration of a three-phase four-wire HAPF or APF.

B. Clock Frequency Design

As the existing HAPF or APF experimental prototypes in the laboratory are using IGBT with its maximum switching frequency of 20kHz, the sampling frequency of the ADC for the proposed PE controller is set as 25kHz, then the switching frequency by using hysteresis PWM technique is limited to 12.5kHz, which is safe for the IGBT. Thus the input signal bandwidth is set to 12.5kHz, which means the sampling frequency of the ADC should be set at least 25kHz due to the

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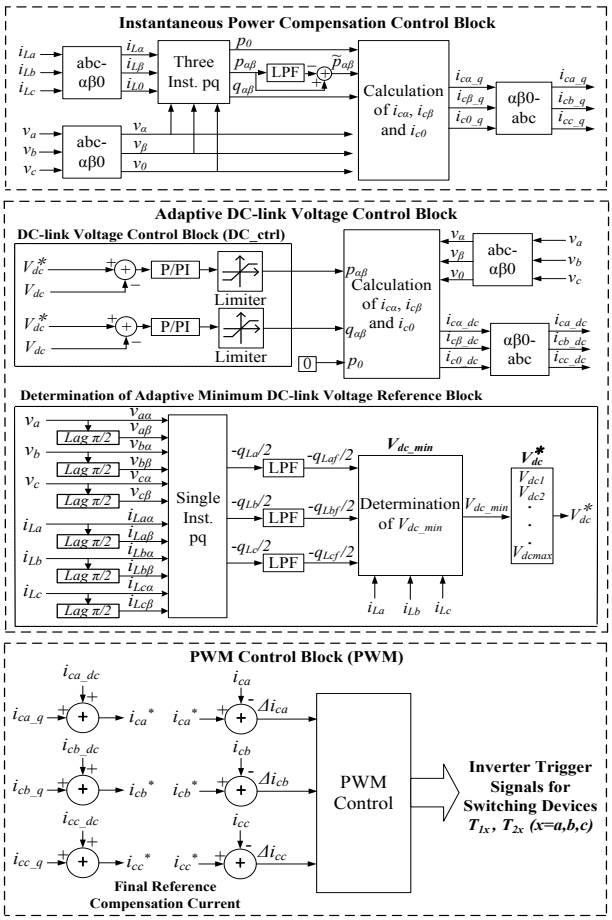

Fig. 6. Block diagram of HAPF or APF control algorithm.

Nyquist Sampling Theorem. That is 40,000ns in the sampling period, and the whole sampling period is composed of ADC conversion stage and the control algorithm processing stage. When the control algorithm process time is set to be equal to the ADC channels conversion time, that is 40,000ns/2 = 20,000ns, this yields the minimum ADC design requirement (25kHz). Assuming, at most 1,000 clock cycles for processing the most complex control algorithm of the controller IC, TABLE III summarizes the derivation process of the required clock frequency (=50MHz) for the proposed PE controller.

TABLE III. DERIVATION OF CLOCK FREQUENCY FOR THE PE CONTROLLER

ADC sampling period	ADC channels conversion period	Algorithm processing period	Processing cycles	Clock cycle
40,000ns	20,000ns	20,000ns	1000	20ns

IV. CONFIGURATION SOFTWARE INTERFACE

We achieve the configurability of the PE controller IC through a computer based configuration software interface developed on a Microsoft Visual Studio2013 platform. This configuration interface is just the beta version and we only design some feature-shared PE functions. In a future version, we can achieve more PE control functions with this interface.

V. EXPERIMENTAL VERIFICATION

A. PE Digital Controller IC and Testing PCB Description

The proposed PE digital controller architecture has been fabricated in 65nm CMOS, and the die size is 2mmx2mm including the PAD ring. The supply voltage is 1.2V, clock frequency is 50MHz, and maximum power dissipation is 840mW. Fig. 7 shows the die microphotograph and testing PCB of the proposed PE controller IC.

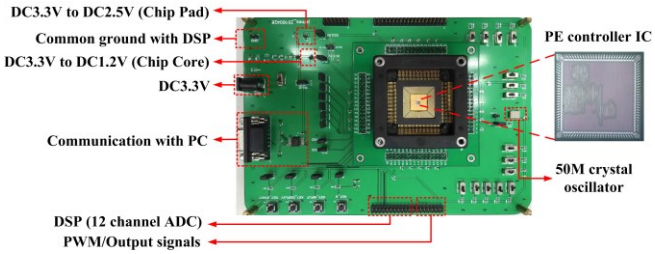

Fig. 7. Die microphotograph and testing PCB of the PE controller IC.

B. PE Controller IC Applied in a HAPF System

From Fig. 5, the proposed controller chip is tested as the digital control system of the HAPF. The ADC for the original controller DSP-TMS320F2812 in the HAPF is directly used to convert the analog input signals into digital signals. We used Mitsubishi IGBT intelligent power modules PM300DSA60 as the switching devices of the VSI, and their switching frequency limitation is at 20kHz. TABLE IV shows the system and HAPF parameters for experimental testing. Via [10], the minimum V_{dc} for compensating the experimental loadings can be obtained. Before compensation, the experimental power factor (PF), total harmonic distortion (THD_{isx}) of i_{sx} and system neutral current(i_{sn}) are 0.81, 28.8% and 2.01A during the 1st loading connected case and 0.85, 19.5% and 2.48A during the 1st and 2nd loadings connected case.

TABLE IV. SYSTEM AND HAPF PARAMETERS FOR EXPERIMENTS

System parameters		Physical values
System voltage & frequency	V_s, f	110V, 50Hz
Coupling inductor & capacitor	L_c, C_c	8mH, 50μF
Coupling neutral inductor	L_{cn}	5mH
DC capacitor	C_{dc}	3.3mF
DC-link voltage levels	V_{dcU}, V_{dcL}	20V, 40V, 60V, 80V
1st nonlinear loading A,B,C	R_{NLx}, L_{NLx}, C_{NLx}	43.2Ω, 35.0mH, 392μF
2nd linear loading A,B,C	R_{LLx}, L_{LLx}	60.0Ω, 50.0mH

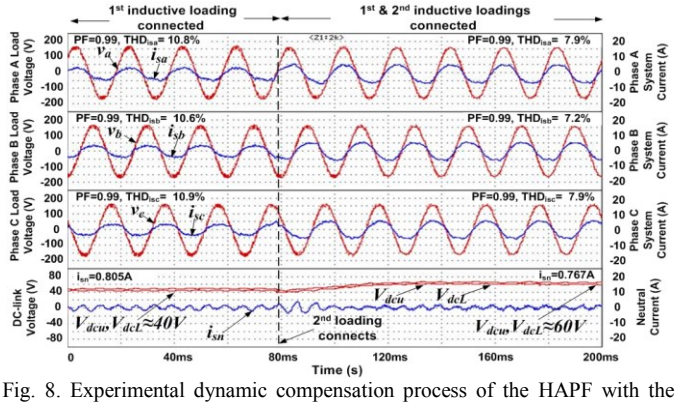

Fig. 8. Experimental dynamic compensation process of the HAPF with the proposed controller IC implemented with the adaptive V_{dc} control.

Fig. 8 plots the experimental dynamic compensation results of the HAPF with the proposed controller IC. We observe that the V_{dc} is adaptively controlled according to different loading

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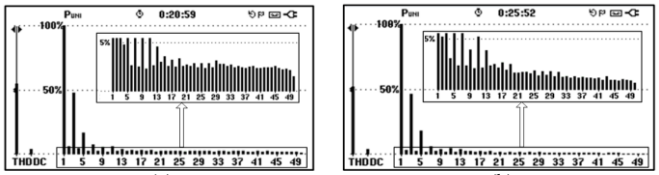
conditions. The experimental PF is improved to 0.99, with THD_{isx}<11%, and i_{sn} significantly reduced after compensation. Fig. 9 shows the frequency spectrum of the compensating current i_{cx} of phase *a* with fixed V_{dcU}, V_{dcL} =80V and adaptive V_{dc}, which shows that the proposed controller IC controlled HAPF with adaptive V_{dc} control can lower the switching noise.



(a) (b)

Fig. 9. Experimental frequency spectrum of i_{cx}: (a) fixed V_{dc}, (b) adaptive V_{dc}.

TABLE V illustrates the comparison among different digital controllers and the proposed controller based on the experimental results presented in this paper. From TABLE V, the HAPF with the proposed controller obtains shorter processing time and a slightly better THD_{isx} compensation performance.

TABLE V COMPARISON AMONG DIFFERENT DIGITAL CONTROLLERS AND THE PROPOSED CONTROLLER

	[11] DSP	[12] FPGA	This Work
Year	2003	2009	2018
Core calculation unit	ALU	LE	Building Block
Parallel processing architecture	No	Yes	Yes
Parallel running calculation unit	No	Yes	Yes
Processing time (cycles) for same PQ application	8000	343	343
THD_{isx} of source current i_{sx} after compensation	7.9%	8.2%	7.2%

C. Transient Response Testing of APF Application

Fig. 10 shows the experimental transient performance of the APF with the proposed controller IC, which shows a fast and smooth load transient response.

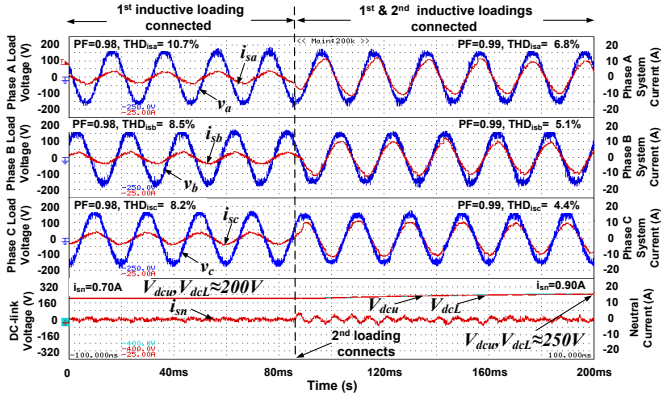


Fig. 10. The transient performance of APF with proposed controller IC.

D. Programmability On-The-Fly

Fig. 11 illustrates the programmability on-the-fly of the PE controller IC. When we adjust the sensor gain of v_a to be more accurate, the system performance can be significantly and smoothly improved (worst phase THD_{isx} from 20.1% to 5.7%).

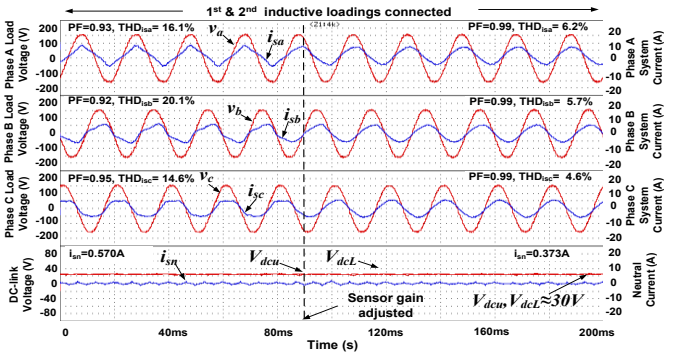


Fig. 11. Programmability on-the-fly of the proposed PE controller IC.

VI. CONCLUSIONS

In this paper, we have proposed a reconfigurable and extendable digital controller architecture for the mixed signal PE controller. Besides keeping the parallel computation characteristics, the connection strategy of the controller is simple, thus relaxing the long programming and debugging time when compared with the conventional digital controllers. We developed a computer-based configuration software interface, which allows the controller chip's reconfigurability and programmability on-the-fly. Lastly, we presented experimental results of using the controller IC to validate its reconfigurability and effectiveness. This digital controller architecture is fundamental for the future development of a generalized and reconfigurable mixed signal PE controller on chip.

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