IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 7, 2019, accepted December 21, 2019, date of publication December 24, 2019, date of current version January 6, 2020.

Digital Object Identifier 10.1109/ACCESS.2019.2962060

A 10.6-mW 26.4-GHz Dual-Loop Type-II Phase-Locked Loop Using Dynamic Frequency Detector and Phase Detector

ZUNSONG YANG, (Student Member, IEEE), YONG CHEN, (Member, IEEE), SHIHENG YANG, (Student Member, IEEE), PUI-IN MAK, (Fellow, IEEE), AND RUI P. MARTINS, (Fellow, IEEE)

State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau 999078, China
ECE, Faculty of Science and Technology, University of Macau, Macau 999078, China

Corresponding author: Yong Chen (ychen@um.edu.mo)

This work was supported in part by the University of Macau under Grant MYRG2017-00167-AMSV, and in part by the Macau Science and Technology Development Fund (FDCT)—SKL Fund.

ABSTRACT This paper reports a millimeter (mm)-wave type-II dual-loop phase-locked loop (PLL) with low-power and low-complexity design for improving jitter-power performance and power efficiency. Unlike the typical type-II single-loop PLL using a tri-state phase-frequency detector (PFD) plus a charge pump (CP) that has several limits in high-speed operation, our proposed PLL features a dual-loop scheme to enhance its performance and operating speed at low power. Specifically, we propose a dynamic frequency detector (FD) and a phase detector (PD) in conjunction with voltage-to-current converters (VICs) to avoid the typical current-mode-logic (CML) circuitry for static power reduction. Prototyped in 65-nm CMOS process, the entire PLL dissipates 10.6 mW, of which the dynamic FD and PD merely consume 0.28 mW. The integrated jitter is 415.6 fs_{rms} (10 kHz to 100 MHz) and the reference spur level is −53 dBc at a 26.4-GHz output.

INDEX TERMS CMOS, dual loop, phase-locked loop (PLL), frequency detector (FD), phase detector (PD), figure-of-merit (FoM), millimeter (mm)-wave, voltage-to-current converter (VIC), voltage-controlled oscillator (VCO), divider-by-4, dynamic latch.

I. INTRODUCTION

The continuous growth of data communications has pushed the operation speed of both wireline and wireless systems into the tens-of-GHz range (per lane or element). Their clock generation has to fulfill stringent jitter specifications in order to underpin dense data modulation schemes [1]–[11], where the phase-locked loop (PLL) remains as one of the most power-hungry building blocks. To achieve a better jitter-power performance, the development of millimeter (mm)-wave PLLs with low power and simpler hardware is of growing interest. The typical single-loop type-II PLL with a typical tri-state phase-frequency detector (PFD) has the benefits of design robustness and wide acquisition range when compared with its type-I counterpart. However, the dead-zone issue of the tri-state PFD can create a bottleneck in the operating speed when it drives the charge pump (CP). Prior work [9] reported the dual-loop type-II PLL using several power-hungry CML-based sub-blocks, such as divider-by-2, frequency detector (FD) and phase detector (PD). This paper presents the design of a dual-loop type-II PLL emphasizing on its dynamic FD and PD. Together with a high-performance multi-LC-tank VCO [12] and a low-power frequency divider chain, our PLL prototyped in 65-nm CMOS achieves an overall performance that compares favorably with the state-of-the-art.

Section II introduces our PLL and details its specific circuits, calculation of loop parameters and settling behavior. Section III summarizes the measurement results, and Section IV draws the conclusions.

The associate editor coordinating the review of this manuscript and approving it for publication was Woorham Bae.

II. PROPOSED DUAL-LOOP PLL ARCHITECTURE

A. OUR PLL ARCHITECTURE

Compared with the typical tri-state PFD-based single-loop PLL, the dual-loop PLL separately performs the frequency and phase detection, and aids reduction of power and phase noise while preserving a wide acquisition range.

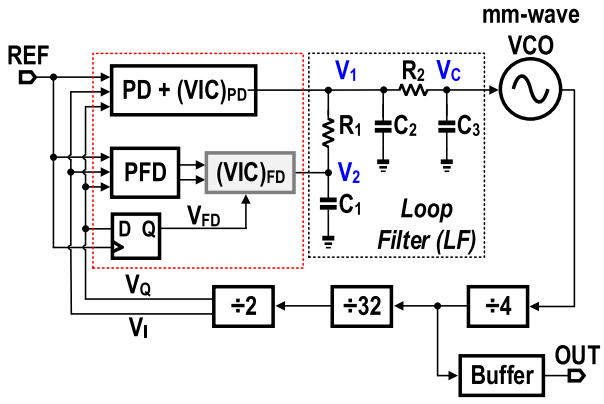


FIGURE 1. Proposed mm-wave PLL architecture with dual-loop detection.

Fig. 1 depicts the proposed dual-loop PLL decomposing the typical tri-state PFD into an FD with the $(VIC)_{FD}$ for frequency detection and a merged PD + $(VIC)_{PD}$ for phase detection. Together, they eliminate the dead-zone (DZ) issue and overcome the speed limits of the typical tri-state PFD. Compared to [9], the main differences are the design topology of FD. Herein, a D-flip-flop (DFF)-based tri-state PFD is utilized to correct frequency error and automatically turned off the $(VIC)_{FD}$ when the frequency is locked. Two detection loops are combined by a 3rd-order lowpass filter (LPF) to suppress the voltage ripple on the control side of the voltage-controlled oscillator (VCO). All LPF passives are on-chip. The output current of the PD injected into the LPF achieves fast phase-locking, while the FD will produce the polarity of the frequency error, namely, the VCO frequency greater or less than the locking frequency, and injects the current of $(VIC)_{FD}$ into C_1 for voltage integration, thus minimizing the frequency error in frequency locking. In the case of our dual-loop PLL design, we first optimize the loop parameters based on the phase-detection loop. And then the calculation method will be discussed later in Section II-E. The locking time may increase due to the settling process dominated by the frequency-detection loop. By properly setting the small current ratio ($< 4\times$) between $(V/I)_{FD}$ and $(V/I)_{PD}$, we can fully eliminate the instability risk. To reduce the entire PLL's power and enhance jitter performance, the VCO design is critical which is based on a multi-LC-tank topology using the 2nd-to-4th harmonic resonances to shape the impulse-sensitivity-function and reduce its RMS value [12]. Subsequently, a frequency divider chain has a total modulus of 256, corresponding to an mm-wave output frequency of 26.368 GHz with a 103-MHz external reference (REF) input. Note that the last divider-by-2 will provide the quadrature outputs, V_Q and V_I, to create the quarter-period pulse. They compare with the REF signal (V_{REF}) to modulate the pulse duration of the injection current for both phase and frequency detection loops.

The typical XOR-based FD and PD [9], [13] are based on the current-mode logic (CML) with small input/output swings to convert the phase and frequency error into the current. Their static biases regrettably penalize the total power consumption. Also, the CML topology suffers from the tail-current mismatch, inducing static phase error and jitter deterioration. However, extra voltage-bias circuitry is involved. To remedy it and save the static power, we propose the dynamic FD and PD enabling significant power reduction under a high-frequency REF input.

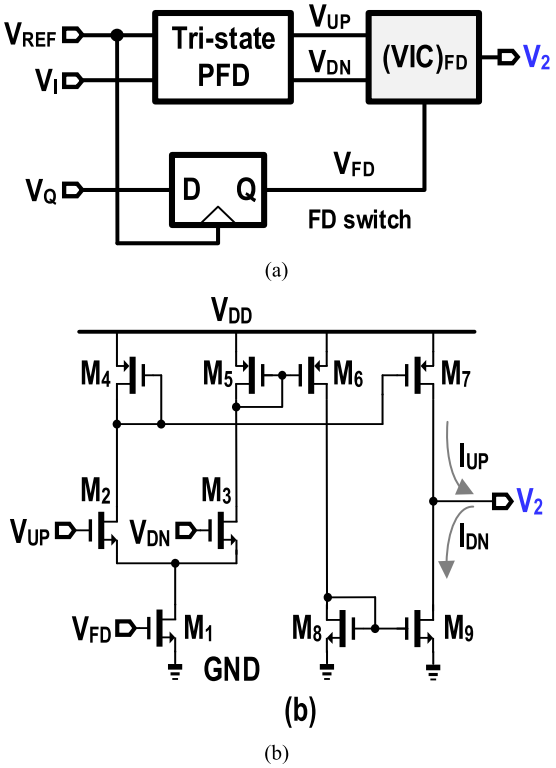


FIGURE 2. Schematic of the proposed (a) FD and (b) $(VIC)_{FD}$.

B. PROPOSED FD

Fig. 2(a) presents our proposed FD that detects the frequency error with a DFF-based tri-state PFD, which can secure a large acquisition range. Another DFF sampling V_Q by V_{REF} generates an indication signal (V_{FD}) to turn on/off the subsequent $(VIC)_{FD}$. If the two frequencies of V_{REF} and V_I are unequal, V_{FD} will be a pulse signal with two states: GND and VDD, to switch the $(VIC)_{FD}$ periodically. Fig. 2(b) shows the proposed $(VIC)_{FD}$ of the FD. When V_{FD} is in the GND state, the tail current source (M_1) turns off, while M_2 and M_3 work in the deep-triode or cutoff region, $(VIC)_{FD}$ is disabled, indicating that the impact of the FD on the entire PLL is blocked. Inversely, when V_{FD} is in the VDD state $(VIC)_{FD}$ will be activated.

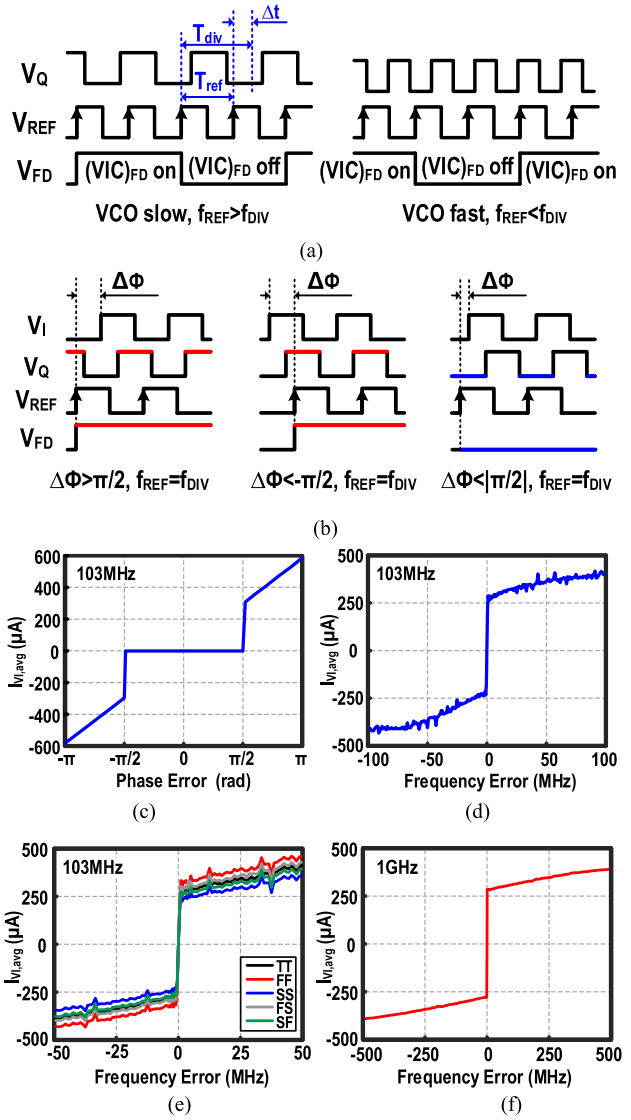


FIGURE 3. Operation of our FD: (a) frequency- and (b) phase-identification characteristics. Simulated (c) frequency- and (d) phase-detection curves of our FD at 103-MHz RFE. Simulated (e) frequency-detection curves under different corners at 103-MHz REF. Simulated (f) frequency-detection curve at 1-GHz REF. Different corners are denoted as Fast-Fast (FF), Slow-Slow (SS), Typical-Typical (TT), Fast-NMOS-Slow-PMOS (FS) and Slow-NMOS-Fast-PMOS (SF).

Fig. 3(a) plots the frequency-identification characteristic. If the VCO is slow ($f_{REF} > f_{DIV}$) and its output frequency is constant, the time difference between V_{REF} and V_Q within one detection cycle is $\Delta t = T_{DIV} - T_{REF}$. It will accumulate in each cycle due to the frequency error when the accumulated Δt reaches a half period of V_Q ($T_{DIV}/2$). The state of the V_{FD} will be flipped and the number of cycles that V_{REF} travels through is,

$$N = \frac{T_{DIV}/2}{\Delta t} = \frac{T_{DIV}/2}{T_{DIV} - T_{REF}} = \frac{T_{DIV}/2}{2\,(1 - f_{DIV}/f_{REF})} \quad (1)$$

Hence, the period of V_{FD} is,

$$T_{FD} = 2N \cdot T_{REF} = \frac{2T_{REF}}{2\,(1 - f_{DIV}/f_{REF})} = \frac{1}{f_{REF} - f_{DIV}} \quad (2)$$

Similarly, if the VCO is fast, the period of V_{FD} will be,

$$T_{FD} = \frac{1}{f_{DIV} - f_{REF}} \quad (3)$$

Therefore, $(VIC)_{FD}$ will be turned on/off with a period of T_{FD}.

Our FD also has the function of the phase-detection once the VCO output frequency is locked. Fig. 3(b) illustrates its phase-identification characteristic, indicating that the phase error ($\Delta\Phi$) determines the state of V_{FD}. Compared to the tri-state PFD with a dead-zone of $\pm\pi$ range [14] for the phase detection, Fig. 3(c) shows the simulated phase-detection curve of our FD with a dead-zone of $\pm\pi/2$ range. Our FD can reduce the phase error to a smaller value before turning off, which helps the PLL locking faster. When the phase error, $|\pi| > \Delta\Phi > |\pi/2|$, V_{FD} will be in the VDD state to enable $(VIC)_{FD}$ and integrate the VCO output frequency, thus reducing the phase difference. The $(VIC)_{FD}$ has turned off automatically when $\Delta\Phi < |\pi/2|$, which no longer contributes to the power consumption and noise. Then, the activation of the PD only happens for phase locking. For the simulated phase [Fig. 3(c)] and frequency [Fig. 3(d)] detection characteristic, within $\Delta\Phi < |\pi/2|$, the current injection is zero to disable the FD. As $|\pi| > \Delta\Phi > |\pi/2|$ and $f_{DIV} \neq f_{REF}$, the current of $(VIC)_{FD}$ injects hundreds of microamperes to aid fast frequency locking. Fig. 3(e) shows the simulated frequency-detection curves under different corners at 103-MHz REF. Additionally, we plot the simulated frequency-detection curve at 1-GHz REF, indicating that our FD is able to operate at a higher frequency.

C. PROPOSED AND-BASED PD

Fig. 4(a) presents our AND-based PD, which is similar to the $(VIC)_{FD}$ of the FD. Interestingly, the PD and its VIC are merged to reduce the number of transistors, thereby improving the power and operating speed. The overall PD + $(VIC)_{PD}$ contains only ten transistors that draw sub-1 mW in our design.

The up-current (I_{UP}) is determined by the pulses generated by the fixed phase error between V_I and V_Q, leading to a constant I_{UP} with a quarter-period REF pulse. The down-current (I_{DN}) is crucial to correct the phase error between V_{REF} and V_Q, resulting in the pulses whose widths are proportional to the phase error. Their behavior can be expresse as,

$$\begin{cases} \overline{\overline{V_I} + \overline{V_Q}} = I_{UP} = V_I \cdot V_Q \\ \overline{\overline{V_Q} + \overline{V_{REF}}} = I_{DN} = V_Q \cdot V_{REF} \end{cases} \quad (4)$$

where the above equations exhibit the equivalent behavior between the implementation in [9] and our solution. The left-sided term shows the PD operation using the power-hungry CML-based XOR gate [9] , furthermore, its function is determined by an extra voltage bias. Based on De Morgan's laws, our AND-based PD represents the same operations at the right-sided term. Once the PLL is locked, the UP/DN current in our PD maintains within a quarter

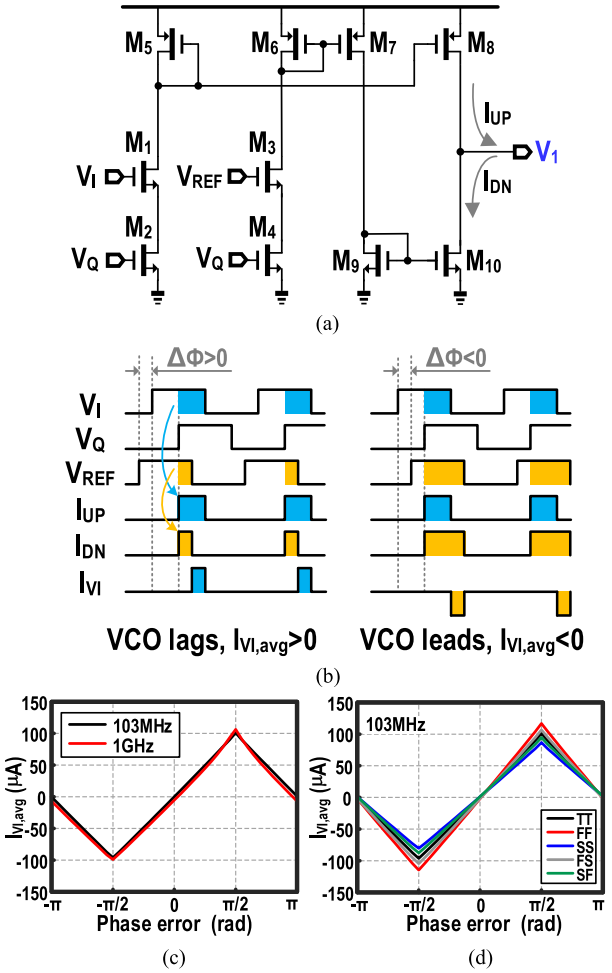


FIGURE 4. (a) Proposed AND-based PD + $(VIC)_{PD}$. (b) Its timing diagram. (c) Simulated phase-detection curves at 103-MHz and 1-GHz REF inputs. (d) Simulated phase-detection curves under different corners at 103-MHz REF.

period of REF. Compared to the CML-based PD that consumes static power, our PD reduces power consumption by four times.

Fig. 4(b) illustrates the timing diagrams of the proposed PD for leading and lagging conditions. When the VCO lags (i.e, $\Delta\Phi = \Phi_{REF} - \Phi_{DIV} > 0$), the rising edge of V_I lags behind V_{REF}, the overlapping area between V_Q and V_{REF} for generating I_{DN} is <1/4 cycle, pushing $(VIC)_{PD}$ to inject the current ($I_{UP} - I_{DN} > 0$) into the LF to raise the VCO frequency and minimize the phase error. When the VCO leads (i.e, $\Delta\Phi < 0$), vice versa, the rising edge of V_I leads V_{REF}, the overlapping area of V_Q and V_{REF} for generating I_{DN} is >1/4 cycle, pushing $(VIC)_{PD}$ to draw more current ($I_{UP} - I_{DN} < 0$) to decrease the VCO frequency for phase locking.

For the simulated phase-detection curves at 103-MHz and 1-GHz REF inputs [Fig. 4(c)] of our PD, as $\Delta\Phi < |\pi/2|$, the FD is disabled and the PD has a constant phase-detection gain (K_{PD}) of $0.4/2\pi$ mA/rad in the linear curve. The average output current ($I_{VI,avg}$) of the $(VIC)_{PD}$ reaches the maximum value $I_{VI,avg,max} = I_{UP(DN)}/4$ when $\Delta\Phi = |\pi/2|$. Since the

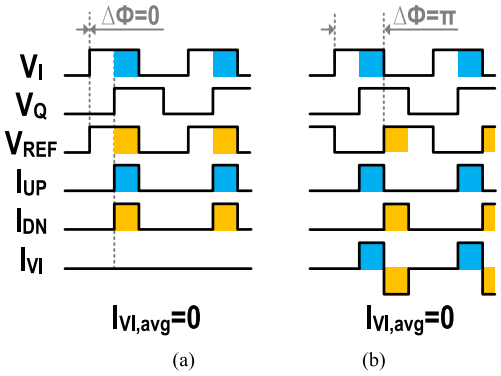


FIGURE 5. Timing diagram for our PD under different phase errors: (a) $\Delta\Phi = 0$ and (b) $\Delta\Phi = \pi$.

PD will be enabled all the time, leading to $\Delta\Phi > |\pi/2|$, the PD will repeat the linear curve periodically. Since the injection current of the PD is four times smaller than that of the FD, it will not dominate the loop for locking. Fig. 4(d) shows the phase-detection curves under different process corners at 103-MHz REF input.

The FD aids the PD to only operate at $\Delta\Phi < |\pi/2|$, since the PD curve repeats periodically, when $\Delta\Phi = 0$ ($K_{PD} > 0$) and $\Delta\Phi = \pi$ ($K_{PD} < 0$), $I_{VI,avg}$ equals to zero [Fig. 5(a) and (b)]. Yet, the alignments between I_{UP} and I_{DN} are different. If the PLL initially starts at $\Delta\Phi = \pi$, the PLL will enter the positive feedback loop, being unstable. Thus, $\Delta\Phi$ should accumulate and eventually will approach zero upon locking.

D. VCO AND FREQUENCY DIVISION CHAIN

Fig. 6(a) shows the mm-wave multi-LC-tank VCO similar to [12] driving the 1st divider-by-4 (DIV4) [15]–[20] in the division chain without extra buffer. The use of dynamic latch [Fig. 6(b)] also aids in improving power efficiency. To ensure the coverage of the overall tuning range of the VCO, a wider locking range (LR) of the 1st divider is desired via tuning V_T to have the combination of multiple sub-bands (e.g., 3 sensitivity curves). Differing from this small-swing LR of ~10% in [15], we effectively introduce a large-output-swing VCO to equivalently obtain a wider LR of the middle sensitivity curve [Fig. 6(c)] even without tuning the voltage bias (V_T), provided by an off-chip low-dropout (LDO) regulator. It covers the >15% tuning range of the VCO. Note that, in our design, the VCO outputs large swing intrinsically. It means that the larger injection amplitude of the DIV4 is enhanced for improving the injection efficiency, and further obtaining the large LR. To verify the robustness of the DIV4, its sensitivity characteristics under the key process corners are conducted. By properly tuning V_T, its sensitivity curves in Fig. 6(d) cover the lock range of the PLL.

To generate the constant quarter-period pulse as the intrinsic reference pulse, we proposed the true-single-phase-clock (TSPC) quadrature divider-by-2 (QDIV2) as exhibited in Fig. 7(a). The QDIV2 is composed of a high-level sensed TSPC latch and a low-level sensed TSPC

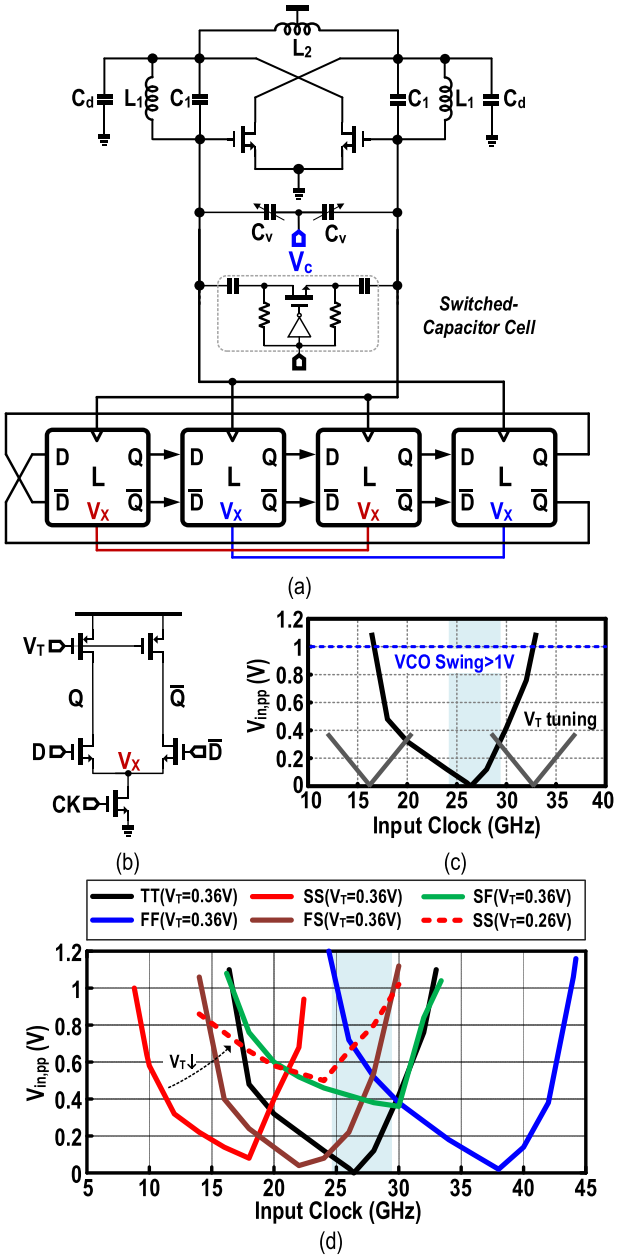


FIGURE 6. Schematic of (a) mm-wave VCO plus 1st DIV4, (b) latch, (c) latch's simulated sensitivity curve, and (d) simulated sensitivity curve under different process corners.

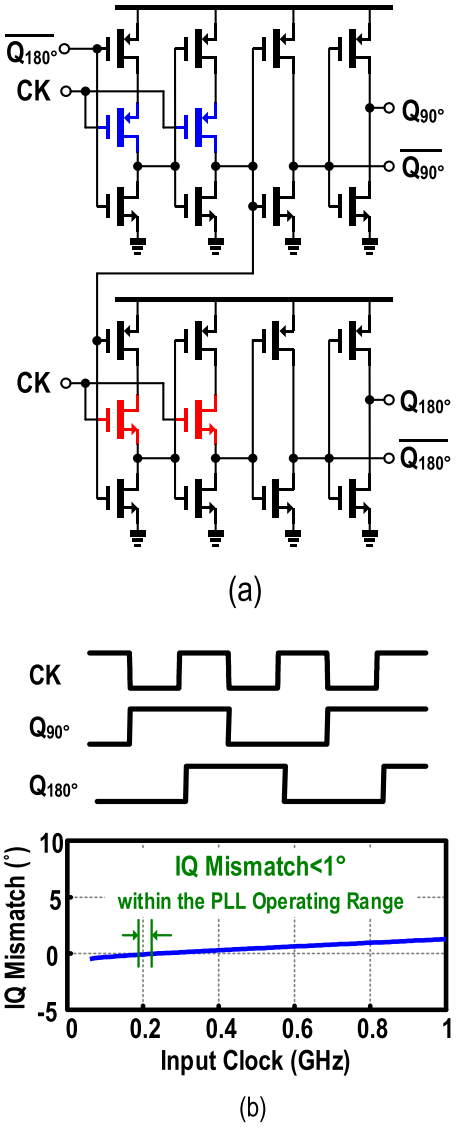


FIGURE 7. (a) Schematic of QDIV2 and (b) its timing diagram and IQ mismatch.

latch. Thus, a master-slave topology is formed by inputting a true single-phase clock from the single-ended TSPC-based divider-by-32. The simulated I/Q mismatch is <1° within the PLL operating range [Fig. 7(b)].

E. CALCULATION PROCEDURE OF THE LOOP PARAMETERS

To construct a stable dual-loop PLL, we summarize the calculation procedure [Fig. 8(a)] of the loop parameters in the dual-loop PLL as follows: 1) determine the main-loop (i.e., PLL) parameters, including phase margin (PM_{PLL}), loop bandwidth (BW), $I_{VI,PD}$, K_{vco}, and division ratio (N) based on the design specification; 2) calculate the LPF parameters (C_1, C_2, C_3, R_2, R_3) according to the above main-loop parameters; 3) preset initial current ($I_{VI,FD}$) of the $(VIC)_{FD}$. For example, its current is four times greater than that ($I_{VI,PD}$) of the $(VIC)_{PD}$; 4) compute phase margin of the frequency-locked loop (PM_{FLL}). As shown in Fig. 8(b), we define the PM_{FLL} of 35° as the minimum stable value of the FLL. Once PM_{FLL} <35°, $I_{VI,FD}$ will be reduced until PM_{FLL} >35°. After plenty of circuit simulations, both the main loop and the FLL are absolutely stable.

F. SIMULATED SETTLING BEHAVIOR

First, we summarize an intuitive insight into the closed-loop dynamic behavior. Recalling the loop parameters in Fig. 8(a), it's shown that the strong and weak loops [Fig. 9(a)] correct the frequency and phase errors, respectively. As observed in Fig. 9(b), during the settling process, the FLL will be

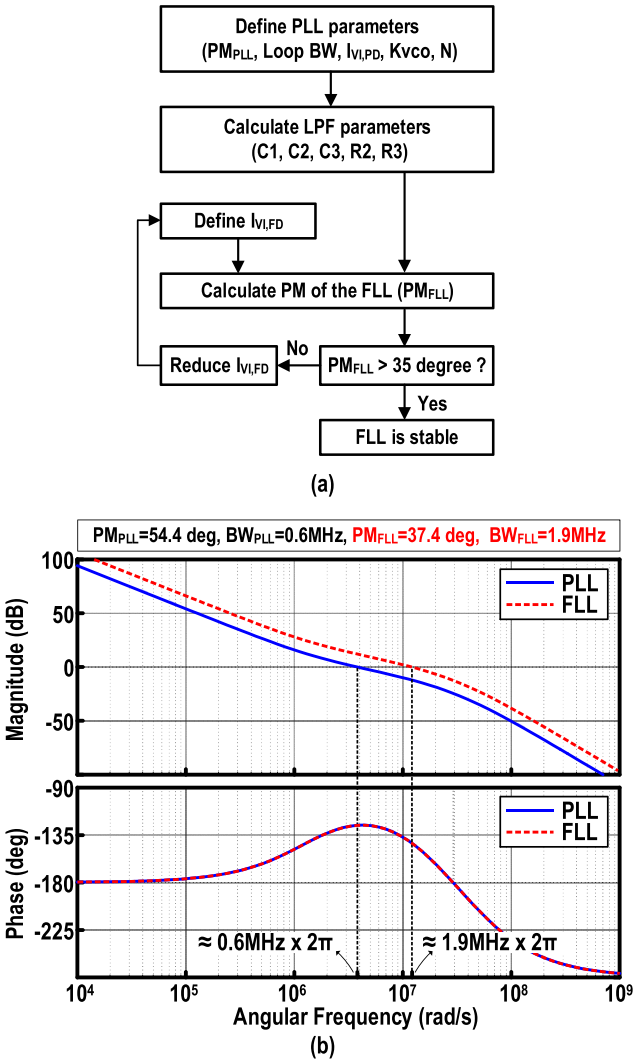


FIGURE 8. (a) Calculation procedure of the loop parameters in our dual-loop PLL. (b) Bode plots for the PLL and FLL of our dual-loop PLL.

turned on intermittently before the frequency is locked, which depends on the amount of the frequency error. Fig. 9(c) shows the zoomed-in settling behavior of our PLL. At this interval, the negative K_{pd}-related phenomena can be found as a special case. Fig. 9(d)-(f) plot the corresponding transient waveforms of the PLL operating at different instantaneous phase errors. When the PLL works around $\Delta\Phi = -\pi$, its settling behavior stays the *Region A* [Fig. 9(c)]. Correspondingly, negative K_{pd} can be observed in the open-loop phase-detection characteristics of the PD, as shown in Fig. 10. It implies that the PD + $(VIC)_{PD}$ operates in the weak positive feedback loop. Yet, the overall PLL is absolutely dominated by the strong negative feedback loop with FD + $(VIC)_{FD}$. Thus, the $(VIC)_{FD}$ sinks current from the LPF, and V_C decreases. After a period, the phase error is reduced from $-\pi$ to $-\pi/2$, approaching *Region B* [Fig. 9(c)]. The FLL will be powered off and $(VIC)_{PD}$ continues to sink current from the LPF. The reduction of V_C become very slow. After crossing $\Delta\Phi = -\pi/2$ (Fig. 10), the positive K_{pd} makes the phase-locking loop enter into the negative feedback loop for accumulating the instantaneous phase error under large frequency error. Eventually, the overall PLL will be locked at $\Delta\Phi = 0$ (Fig. 10) and the FLL has been automatically turned off.

Next, we brief the open-loop phase-detection curves (Fig. 10). The conventional tri-state PFD has an infinite frequency capture range along with its positive and linear gain. Yet, after the frequency is locked, it cannot be automatically turned off. Since the dead-zone (DZ) creator [14] is inserted after the tri-state PFD, it can automatically turn off the FLL when the frequency is locked. The issue of the DZ-based tri-state PFD is that its K_{PD} keeps constant zero and losing the loop dynamic capture behavior. Thus, when the DZ-based tri-state PFD is turned on, the CP behind it injects (or sinks) constant current to (or from) the LPF. As a result, the entire PLL takes more time to realize the frequency lock. Differently, our proposed FD keeps the loop dynamic as the classic tri-state PFD and can be automatically turned off when the frequency is locked. Therefore, our FD saves a lot of time to achieve the frequency lock.

Although the FD's settling behavior in both our proposed design and [21] varies as approaching the locking point, the PLL's settling behavior is far different. In our design, there is less cycle slip before entering the lock-state. As shown in Fig. 11, the simulated settling behaviors of the PLL with different reference frequencies are as follows. It indicates that our FD can switch alternatively even if the REF frequency (F_{REF}) is at a high frequency of 16 × 103 MHz. Fig. 11(a) and (b) show that the PLL locks faster when the FLL is turned on because the $(VIC)_{FD}$ provides more current and achieves a larger loop bandwidth. In addition, since the initial frequency error is amplified by N times when F_{REF} is increased by N times, the FLL needs more time to correct the frequency error before the FLL locks. According to Eq. (3), the starting frequency of V_{FD} will increase by N times simultaneously.

Interestingly, the GHz-reference frequency can be used as an input for the second stage of a cascaded PLL [22]. Especially in the ultra-scaled CMOS technology, it's very challenging to achieve low phase noise of the high-frequency VCO. Thus, a solution to implement a low-integrated-jitter PLL is to cascade a low-frequency ultra-low-noise PLL and a GHz-F_{REF} high-frequency PLL. The traditional PFD+CP can operate at MHz-to-GHz reference frequency, especially in the ultra-scaled CMOS technology. Yet, the designer must cope with the dead-zone issue in order to balance the multi-dimensional optimization. Differently, our PD and $(VIC)_{PD}$ are merged together and controlled by a quarter-period REF pulse, which is generated by the instinct I/Q output of the last stage of the divider chain. In addition, our PD and FD functions are based on the minimum number of transistors.

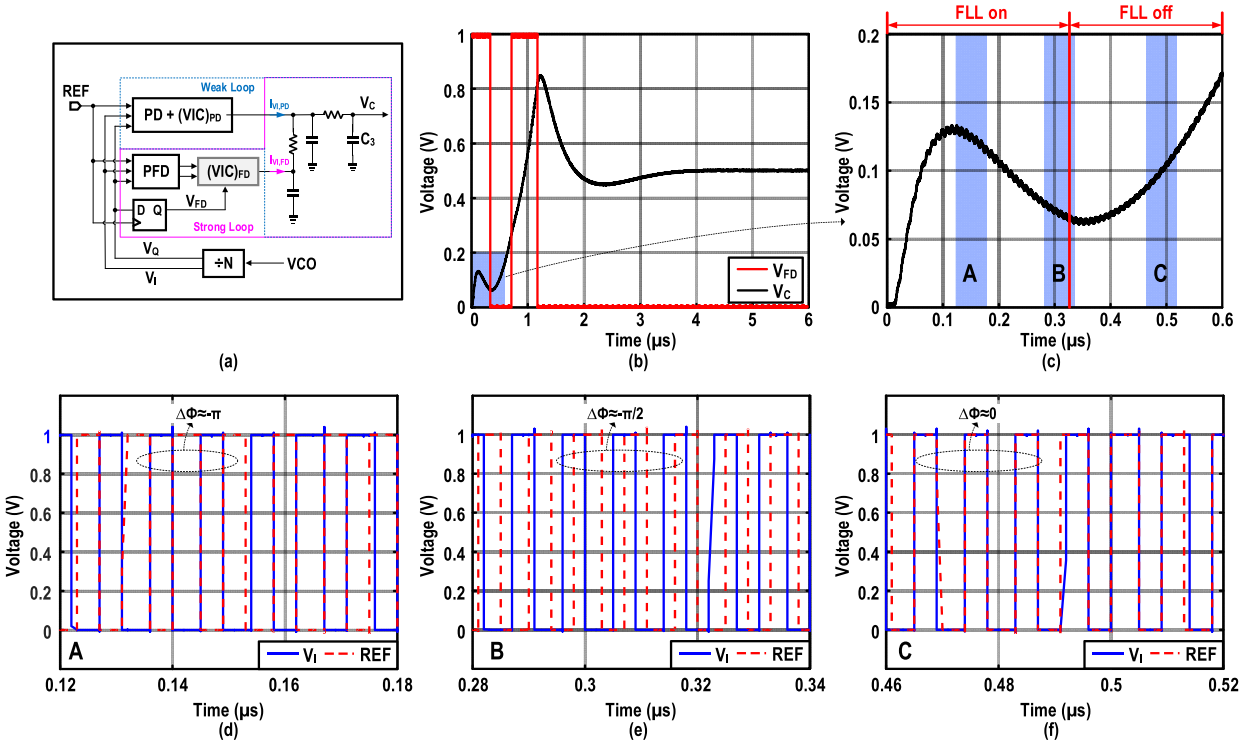


FIGURE 9. (a) Illustration of the strong FLL and weak phase-locking loop. (b) Settling behavior of our PLL. (c) Zoomed-in settling behavior of (b), associated with *Region A*, *B* and *C*. (d)-(f) Relationship between V_I and REF at *Region A*, *B* and *C*.

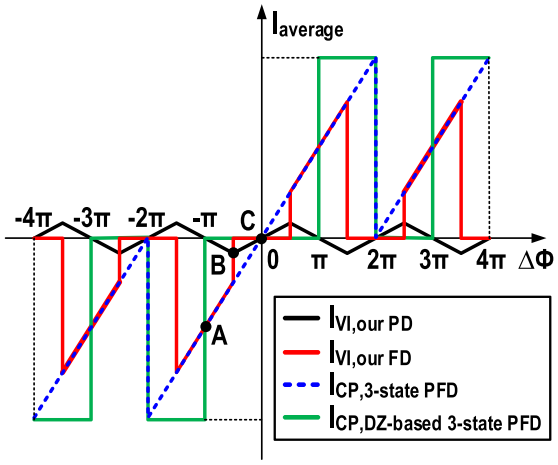


FIGURE 10. Simulated open-loop phase-detection curves.

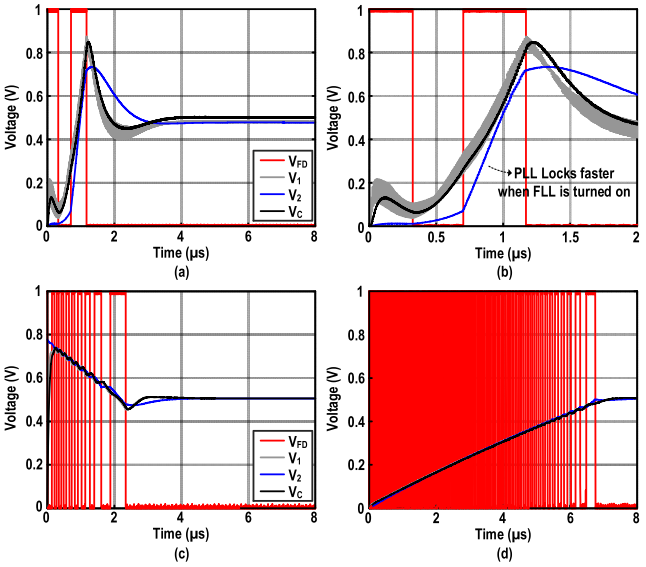


FIGURE 11. Settling behaviors under different reference frequencies: (a) 103 MHz., (b) 103 MHz (zoomed-in), (c) 8 × 103 MHz and (d) 16 × 103 MHz.

III. MEASUREMENT RESULTS

Fig. 12 depicts the chip micrograph of the mm-wave dual-loop PLL fabricated in 65-nm CMOS technology, with an active area of 0.26-mm^2 including all LF passives. At a 1-V supply, the PLL dissipates in a total of 10.64 mW with 0.28 mW consumed by the PD/FD + VIC. The VCO draws 6.5 mW under 0.55-V supply and the frequency division chains consume 3.86 mW. The power consumption of the reference buffer is 0.24 mW with a 1-V supply voltage. We use an external 103-MHz crystal oscillator to generate the REF input with the output tested via a divider-by-4 circuit to simplify the test setup.

Fig. 13 outlines the measured phase noise at 26.4 GHz. Consider the divider chain in our design with a large divide ratio, the in-band phase noise is mainly dominated by the loop components, while the high-pass-filtered VCO noise

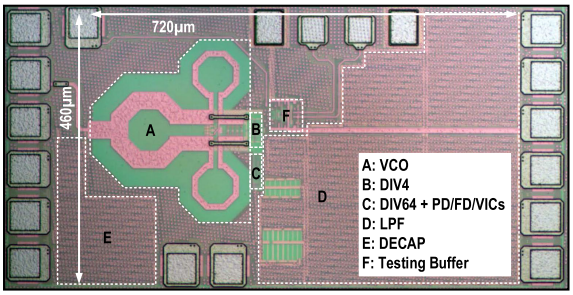


FIGURE 12. Chip micrograph of the fabricated mm-wave dual-loop PLL.

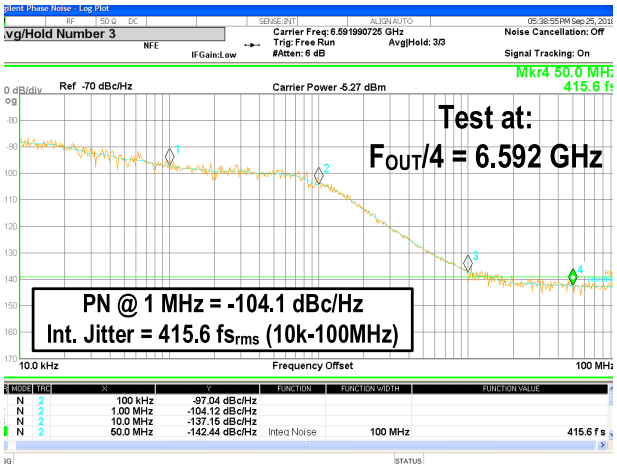


FIGURE 13. Measured phase noise of the output signal with a frequency of 6.592 GHz after a divider-by-4.

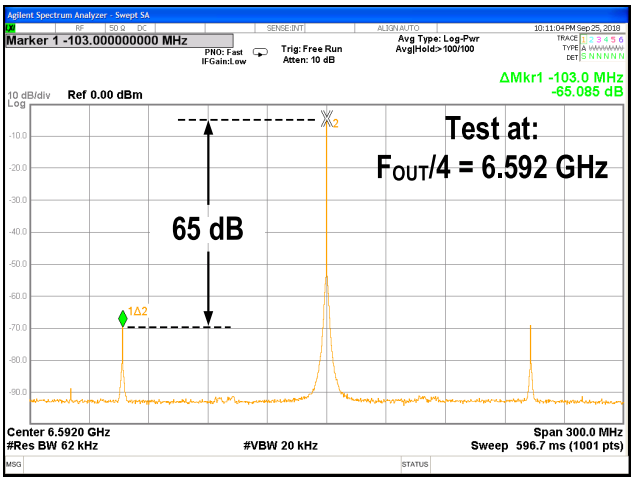


FIGURE 14. Measured REF spur of the output signal with a frequency of 6.592 GHz after a divider-by-4.

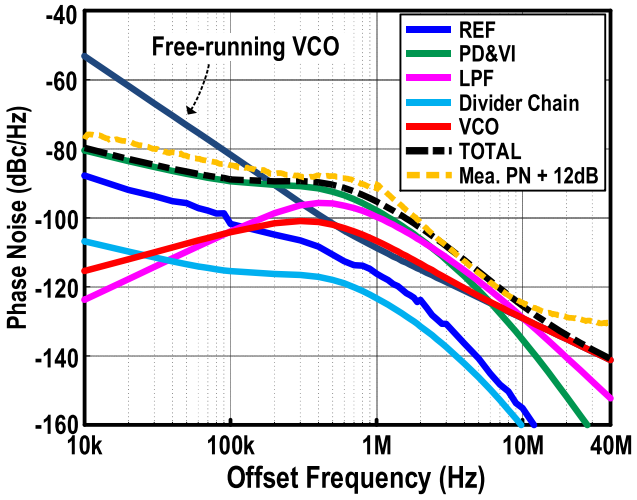


FIGURE 15. The measured and estimated phase noise contributions for the different components of our PLL.

rules the out-of-band phase noise. In addition, the current mismatch in the $(\text{VIC})_{\text{PD}}$ incurs significant voltage ripple on V_C. To optimize the PLL overall performances, a smaller loop bandwidth (≈0.6 MHz) is employed, which not only helps to suppress the in-band phase and balances the integrated jitter, but also significantly reduces the reference spur. The integrated jitter achieves 415.6 fs_{rms} from 10 kHz to 100 MHz, its variation is <30 fs_{rms} among the 5 chips.

Fig. 14 shows the measured REF spur level of −53 dBc at 103-MHz offset and its variation is <4 dB among the 5 chips. Herein, the reference spur is mainly induced by the current mismatch of the $(\text{VIC})_{\text{PD}}$. Moreover, the larger K_{VCO} (≈800 MHz/V) in this design magnifies the impacts of its current mismatch on the reference spur. We use a 3rd-order LPF with small loop bandwidth (≈0.6 MHz) to improve the reference spur while penalizing the active area in Fig. 12. Particularly, since our PD and the PD structure of [9] are based on the logic relationship, both achieve excellent linearity. The non-ideality to be illustrated here is the current mismatch, which causes the voltage ripple. The reference spur can be improved by introducing the calibration of the current-mismatch reduction like the counterpart in the conventional charge pump. To alleviate the reference spur, an isolated master-slave phase detector [24] is realized to output the dc voltage and the VIC converts dc voltage to dc current.

Fig. 15 plots the measured phase noise and estimated contributions for the different components of the entire PLL. We can observe that the in-band phase noise is dominated by the AND-based PD + $(\text{VIC})_{\text{PD}}$.

Fig. 16 shows the jitter-power performance among the recent 25+ GHz PLL. Table 1 compares our performance with the state-of-the-art [1]–[6] and [23], [24], where the proposed PLL exhibits a more competitive jitter-power performance at low power and low complexity, thereby an improved figure-of-merit (FoM) of −237.4 dB is along with a low reference spur level of −53 dBc. In our design, a smaller loop bandwidth (≈0.6 MHz) is employed to optimize the overall performance. That is, this helps us to suppress the in-band phase noise and reducing the reference spur. Compared with the sub-sampling PLL topology [24], our PLL is based on

TABLE 1. Performance summary and benchmark with state-of-the-art.

	This Work	ISSCC'16 [1]	JSSC'15 [2]	ISSCC'15 [3]	ESSCIRC'15 [4]	JSSC'14 [5]	ISSCC'11 [6]	RFIC'17 [23]	ISSCC'19 [24]
CMOS (nm)	65	65	40	SOI 32	65	SOI 32	45	BiCMOS 250	65
Type / VCO Topology	Integer-N / LC	Integer-N / LC	Integer-N / LC	Fractional / LC	Fractional / LC	Integer-N / LC	Integer-N / LC	Integer-N / LC	Integer-N / LC
Reference (MHz)	103	N/A	390	104.5	40	194	48	50	103
Output Frequency (GHz)	26.368 [b]	3.5 [c]	25	22.25	27.7	14 [f]	23.33	40	26.368
Frequency Range (GHz)	24.6-29.2 (17.1%)	25.3-30.4 (18%)	21.4-25.1 (15.9%)	13.1-28 (72.5%[6])	27.5-29.6 (7.4%)	23.8-30.2 (23.7%)	21.7-27.6 (24.9%)	37.2-40 (7.3%)	25.4-29.5 (14.9%)
PN @ 1-MHz (dBc/Hz)	-92.1[b]	-115.8 [d]	-102	-82.2	-96 [d]	-91.8	-95	-100.7	-112.8[b]
Integrated Jitter (fs)	415.6	183	392	320	510	199	306.2	103.8	71
FoM_j [a] (dB)	-237.4	-235.5	-230	-235	-231	-239.1	-234.3	-234.6	-252.9
Reference Spur (dBc)	-53 [b]	N/A	N/A	-68	-80	N/A	-50	-73	-63
Supply (V)	0.55/1.0	1	1	1	1	1	0.9/1.1/1.8	3.3	0.55/1
Power (mW)	**10.64**	87	64	31	33	31	40	323	10.2
Power Eff. (mW/GHz)	**0.40**	3.11	2.56	1.40	1.19	1.11	1.89	8.08	0.39
Die Area (mm^2)	0.26	N/A	0.1	0.24	1.2 [e]	0.02	0.14	0.45	0.24

[a] $FOM_j = 10\log_{10}((Jitter/1s)^2 x(Power/1mW))$. [b] Restored from the measured output after divider-by-4. [c] After divider-by-8. [d] Extracted from phase noise plot. [e] Full chip. [f] After divider-by-2.

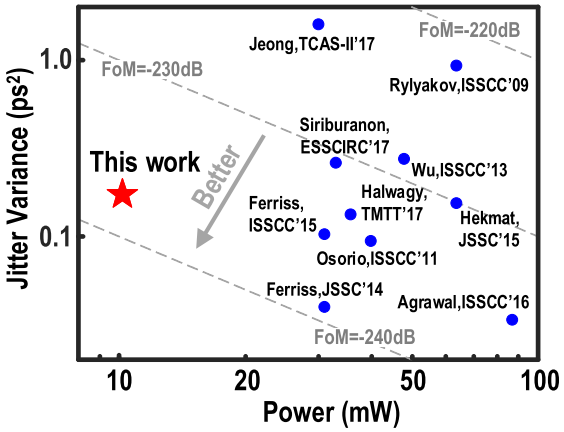


FIGURE 16. Jitter-power FoM comparison among recent 25+ GHz PLLs.

the explicit division chain, indicating that it still shows the advantages in terms of stability and robustness.

IV. CONCLUSION

This paper reported an mm-wave dual-loop type-II PLL with low power and a simpler dynamic frequency detector (FD) and a phase detector (PD) to enhance the operating speed up to GHz. It scores a measured jitter of 415.6 fs_{rms}, with a reference spur of −53 dBc and a total power of 10.64 mW. The achieved jitter-power FoM compares favorably with the prior art.

ACKNOWLEDGMENT

R. P. Martins was on leave from the Instituto Superior Técnico, Universidade de Lisboa, 1049-001 Lisboa, Portugal.

REFERENCES

[1] A. Agrawal and A. Natarajan, "A scalable 28 GHz coupled-PLL in 65nm CMOS with single-wire synchronization for large-scale 5G mm-wave arrays," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2016, pp. 38–39.

[2] M. Hekmat, F. Aryanfar, J. Wei, V. Gadde, and R. Navid, "A 25 GHz fast-lock digital LC PLL with multiphase output using a magnetically-coupled loop of oscillators," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 490–502, Feb. 2015.

[3] M. Ferriss, B. Sadhu, A. Rylyakov, H. Ainspan, and D. Friedman, "A 13.1-to-28 GHz fractional-N PLL in 32 nm SOI CMOS with a ΔΣ noise-cancellation scheme," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[4] T. Siriburanon, H. Liu, K. Nakata, W. Deng, J. H. Son, and D. Y. Lee, "28-GHz fractional-N frequency synthesizer with reference and frequency doublers for 5G cellular," in *Proc. IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 76–79.

[5] M. Ferriss, A. Rylyakov, J. A. Tierno, H. Ainspan, and D. J. Friedman, "A 28 GHz hybrid PLL in 32 nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1027–1035, Apr. 2014.

[6] J. F. Osorio, C. S. Vaucher, B. Huff, E. van der Heijden, and A. de Graauw, "A 21.7-to-27.8 GHz 2.6-degrees-rms 40 mW frequency synthesizer in 45 nm CMOS for mm-wave communication applications," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2011, pp. 278–280.

[7] W.-H. Wu, X. Bai, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz spurious-free all-digital fractional-N PLL in 65 nm CMOS," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2013, pp. 352–353.

[8] A. Rylyakov, J. Tierno, H. Ainspan, J.-O. Plouchart, J. Bulzacchelli, Z. T. Deniz, and D. Friedman, "Bang-bang digital PLLs at 11 and 20 GHz with sub-200 fs integrated jitter for high-speed serial communication applications," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2009, pp. 94–95.

[9] J. Lee, "High-speed circuit designs for transmitters in broadband data links," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1004–1015, May 2006.

[10] G. Sun, Y. Li, W. Jin, and L. Bu, "A nonlinear three-phase phase-locked loop based on linear active disturbance rejection controller," *IEEE Access*, vol. 5, pp. 21548–21556, Oct. 2017.

[11] H. Ko, W. Bae, G.-S. Jeong, and D.-K. Jeong "Reference spur reduction techniques for a phase-locked loop," *IEEE Access*, vol. 7, pp. 38035–38043, Mar. 2019.

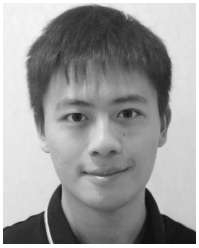
[12] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.083-mm^2 25.2-to-29.5 GHz multi-LC-tank class-F_{234} VCO with a 189.6-dBc/Hz FOM," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 86–89, Apr. 2018.
[13] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate linear phase detector," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 761–768, May 2001.
[14] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A low noise sub-sampling PLL in which divider noise is eliminated and PD/CP noise is not multiplied by N2," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec. 2009.
[15] A. Ghilioni, U. Decanis, E. Monaco, A. Mazzanti, and F. Svelto, "A 6.5 mW inductorless CMOS frequency divider-by-4 operating up to 70 GHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Tech. Dig.*, Feb. 2011, pp. 282–284.
[16] A. Ghilioni, U. Decanis, A. Mazzanti, and F. Svelto, "A 4.8 mW inductorless CMOS frequency divider-by-4 with more than 60% fractional bandwidth up to 70 GHz," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Sep. 2012, pp. 1–4.
[17] A. Ghilioni, A. Mazzanti, and F. Svelto, "Analysis and design of mm-wave frequency dividers based on dynamic latches with load modulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1842–1850, Aug. 2013.
[18] M. Vigilante and P. Reynaert, "A 25-102 GHz 2.81-5.64 mW tunable divide-by-4 in 28 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2015, pp. 1–4.
[19] Y. Chen, Z. Yang, X. Zhao, Y. Huang, P.-I. Mak, and R. P. Martins, "A 6.5×7 μm^2 0.98-to-1.5 mW non-self-oscillation-mode frequency divider-by-2 achieving a single-band untuned locking range of 166.6% (4 to 44 GHz)," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 4, pp. 86–89, Apr. 2019.
[20] A. I. Hussein and J. Paramesh, "Design and self-calibration techniques for inductor-less millimeter-wave frequency dividers," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1521–1541, Jun. 2017.
[21] R. C. H. van de Beek, C. S. Vaucher, D. M. W. Leenaerts, E. A. M. Klumperink, and B. Nauta, "A 2.5-10-GHz clock multiplier unit with 0.22-ps RMS jitter in standard 0.18-m CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1862–1872, Nov. 2004.
[22] J. Kim, H. Yoon, Y. Lim, Y. Lee, Y. Cho, T. Seong, and J. Choi, "A 76fsrms Jitter and −40 dBc integrated-phase-noise 28-to-31 GHz frequency synthesizer based on digital sub-sampling PLL using optimally spaced voltage comparators and background loop-gain optimization," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2019, pp. 258–260.
[23] Y. Chen, L. Praamsma, N. Ivanisevic, and D. M. W. Leenaerts, "A 40 GHz PLL with −92.5 dBc/Hz in-band phase noise and 104 fs-RMS-jitter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 31–32.
[24] Z. Yang, Y. Chen, S. Yang, P.-I. Mak, and R. P. Martins, "A 25.4-to-29.5 GHz 10.2 mW isolated sub-sampling PLL achieving −252.9 dB jitter-power FoM and −63 dBc reference spur," in *IEEE Int. Solid-State Circuits (ISSCC) Conf. Dig. Tech. Papers*, Feb. 2019, pp. 270–272.

ZUNSONG YANG received the B.E. degree in microelectronics from Qingdao University, Qingdao, China, in 2014, and the M.S. degree in electronics and communications engineering from the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS), Beijing, China, in 2017. He is currently pursuing the Ph.D. degree with the University of Macau (UM), Macao, China.

His current research interest includes high-speed IC circuits.

YONG CHEN (Member, IEEE) received the B.Eng. degree in electronic and information engineering from the Communication University of China (CUC), Beijing, China, in 2005, and the Ph.D. in engineering degree in microelectronics and solid-state electronics from the Institute of Microelectronics of Chinese Academy of Sciences (IMECAS), Beijing, in 2010.

He is currently an Assistant Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI (AMSV), University of Macau, Macao, China. His research interests include integrated circuit designs involving analog/mixed-signal/RF/mm-wave/wireline. Dr. Chen was a member of Technical Program Committee of APCCAS, in 2019. He was a co-recipient of the Best Paper Award at the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), in 2019. His team reported two chip inventions at the 2019 IEEE International Solid-State Circuits Conference—ISSCC (Chip Olympics): mm-wave PLL 2019 and VCO 2019. He has been the Vice-Chair of IEEE Macau CAS Chapter, since 2019, and a conference local organization committee of ASSCC in 2019. He has been an Associate Editor of the IEEE Transactions on Very Large Scale Integration Systems (TVLSI), since 2019; and an Associate Editor of IEEE Access, since 2019.



SHIHENG YANG (Student Member, IEEE) received the B.Sc. degree in electrical and electronics engineering from the University of Macau (UM), Macao, China, in 2014, where he is currently pursuing the Ph.D. degree in electronic and computer engineering.

His research interests include analog/mixed IC designs and RF circuits specializing in the PLL. He received the SJM and Frank Wong Foundation Scholarships for the outstanding academic achievement. He was the Founding Chairman of the Faculty of Science and Technology Postgraduate Students' with University of Macau. He also serves as a Reviewer for the IEEE Journal of Solid-State Circuits and the IEEE Transactions on Circuits and Systems I and II.

PUI-IN MAK (Fellow, IEEE) received the Ph.D. degree from the University of Macau (UM), Macao, China, in 2006.

He is currently a Full Professor with the UM Faculty of Science and Technology—ECE, and an Associate Director (Research) with the UM State Key Laboratory of Analog and Mixed-Signal VLSI. His research interests are on analog and radio-frequency (RF) circuits and systems for wireless and multidisciplinary innovations.

Prof. Mak has been elected Overseas Expert of the Chinese Academy of Sciences, since 2018; a Fellow of the U.K. Institution of Engineering and Technology (IET) for contributions to engineering research, education and services, since 2018; and a Fellow of the IEEE for contributions to radio-frequency and analog circuits, since 2019. He serves/served as the Chair of Distinguished Lecturer Program, since 2018; and a member of Board-of-Governor, from 2009 to 2011 of the IEEE Circuits and Systems Society (CASS). He was the Distinguished Lecturer of both IEEE Circuits and Systems Society, from 2014 to 2015, and IEEE Solid-State Circuits Society, from 2017 to 2018. He was the TPC Vice Chair of ASP-DAC, in 2016. His involvements with IEEE are an Editorial Board Member of IEEE Press, from 2014 to 2016; a member of Board-of-Governors of IEEE Circuits and Systems Society, from 2009 to 2011; a Senior Editor of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems, from 2014 to 2015; an Associate Editor of the IEEE Transactions on Circuits and Systems—I, from 2010 to 2011 and from 2014 to 2015, the IEEE Transactions on Circuits and Systems—II, from 2010 to 2013, the IEEE Journal of Solid-State Circuits since 2018, and the IEEE Solid-State Circuits Letters, since 2018.

RUI P. MARTINS (Fellow, IEEE) was born in April 1957. He received the bachelor's, master's, Ph.D., and Habilitation degrees in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He was a Full Professor in electrical engineering and computers from the Department of Electrical and Computer Engineering, Instituto Superior Técnico (IST), TU of Lisbon. He has been with the Department of Electrical and Computer Engineering (DECE) / IST, TU of Lisbon, since October 1980. In FST, he was the Dean of the Faculty, from 1994 to 1997. He has also been Vice-Rector of the University of Macau, since 1997. Since 1992, he has also been on leave from IST, TU of Lisbon (now University of Lisbon since 2013). He has also been a Chair Professor with the University of Macau (UM), Macao, China, since August 2013. He is currently with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM). From September 2008, after the reform of the UM Charter, he was nominated after open international recruitment, and reappointed, in 2013, as the Vice-Rector (Research), until August 2018. Within the scope of his teaching and research activities, he has taught 21 bachelor and master courses and, in UM, has supervised (or co-supervised) 40 theses, 19 Ph.D. and 21 Masters. He has coauthored six books and nine book chapters; 18 Patents, USA, in 2016, and Taiwan; 377 articles, in 111 scientific journals and in 266 conference proceedings; and other 60 academic works, in a total of 470 publications. He was a Co-Founder of Chipidea Microelectronics (Macao) (now Synopsys), in 2001 and 2002, and created in 2003 the Analog and Mixed-Signal VLSI Research Laboratory of UM, elevated in January 2011 to State Key Laboratory of China (the 1st in Engineering in Macao), being its Founding Director. He was a recipient of two government decorations: the Medal of Professional Merit from Macao Government (Portuguese Administration), in 1999, and the Honorary Title of Value from Macao SAR Government (Chinese Administration), in 2001. In July 2010 was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences (in Lisbon), being the only Portuguese Academician living in Asia. He was Founding Chairman of both IEEE Macau Section, from 2003 to 2005, and IEEE Macau Joint-Chapter on Circuits and Systems (CAS) / Communications (COM), from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of 2008 IEEE Asia-Pacific Conference on CAS—APCCAS'2008. He was Vice-President for Region ten (Asia, Australia, and the Pacific) of IEEE CASS, from 2009 to 2011. Since then, he was the Vice-President (World) Regional Activities and Membership of IEEE CASS from 2012 to 2013, and an Associate Editor of the IEEE TRANSACTIONS ON CAS—II: Express Briefs from 2010 to 2013, nominated Best Associate Editor of T-CAS II from 2012 to 2013. Plus, he was a member of the IEEE CASS Fellow Evaluation Committee in 2013 and 2014, and CAS Society representative in the Nominating Committee, for the election, in 2014, of the Division I (CASS/EDS/SSCS)—Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC'2016. He was a Nominations Committee Member in 2016. He is also the Chair of the IEEE Fellow Evaluation Committee (class of 2018), both of IEEE CASS.