A 10.6-mW 26.4-GHz Dual-Loop Type-II Phase-Locked Loop Using Dynamic Frequency Detector and Phase Detector

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ABSTRACT This paper reports a millimeter (mm)-wave type-II dual-loop phase-locked loop (PLL) with low-power and low-complexity design for improving jitter-power performance and power efficiency. Unlike the typical type-II single-loop PLL using a tri-state phase-frequency detector (PFD) plus a charge pump (CP) that has several limits in high-speed operation, our proposed PLL features a dual-loop scheme to enhance its performance and operating speed at low power. Specifically, we propose a dynamic frequency detector (FD) and a phase detector (PD) in conjunction with voltage-to-current converters (VICs) to avoid the typical current-mode-logic (CML) circuitry for static power reduction. Prototyped in 65-nm CMOS process, the entire PLL dissipates 10.6 mW, of which the dynamic FD and PD merely consume 0.28 mW. The integrated jitter is 415.6 fs_{rms} (10 kHz to 100 MHz) and the reference spur level is $-53$ dBc at a 26.4-GHz output.

INDEX TERMS CMOS, dual loop, phase-locked loop (PLL), frequency detector (FD), phase detector (PD), figure-of-merit (FoM), millimeter (mm)-wave, voltage-to-current converter (VIC), voltage-controlled oscillator (VCO), divider-by-4, dynamic latch.

I. INTRODUCTION

The continuous growth of data communications has pushed the operation speed of both wireline and wireless systems into the tens-of-GHz range (per lane or element). Their clock generation has to fulfill stringent jitter specifications in order to underpin dense data modulation schemes [1]–[11], where the phase-locked loop (PLL) remains as one of the most power-hungry building blocks. To achieve a better jitter-power performance, the development of millimeter (mm)-wave PLLs with low power and simpler hardware is of growing interest. The typical single-loop type-II PLL with a typical tri-state phase-frequency detector (PFD) has the benefits of design robustness and wide acquisition range when compared with its type-I counterpart. However, the deadzone issue of the tri-state PFD can create a bottleneck in the operating speed when it drives the charge pump (CP). Prior work [9] reported the dual-loop type-II PLL using several power-hungry CML-based sub-blocks, such as divider-by-2, frequency detector (FD) and phase detector (PD). This paper presents the design of a dual-loop type-II PLL emphasizing on its dynamic FD and PD. Together with a high-performance multi-LC-tank VCO [12] and a low-power frequency divider chain, our PLL prototyped in 65-nm CMOS achieves an overall performance that compares favorably with the state-of-the-art.

Section II introduces our PLL and details its specific circuits, calculation of loop parameters and settling behavior. Section III summarizes the measurement results, and Section IV draws the conclusions.
II. PROPOSED DUAL-LOOP PLL ARCHITECTURE

A. OUR PLL ARCHITECTURE

Compared with the typical tri-state PFD-based single-loop PLL, the dual-loop PLL separately performs the frequency and phase detection, and aids reduction of power and phase noise while preserving a wide acquisition range.

Fig. 1 depicts the proposed dual-loop PLL decomposing the typical tri-state PFD into an FD with the (VIC)FD for frequency detection and a merged PD + (VIC)PD for phase detection. Together, they eliminate the dead-zone (DZ) issue and overcome the speed limits of the typical tri-state PFD. Compared to [9], the main differences are the design topology of FD. Herein, a D-flip-flop (DFF)-based tri-state PFD is utilized to correct frequency error and automatically turned off the (VIC)FD when the frequency is locked. Two detection loops are combined by a 3rd-order lowpass filter (LPF) to suppress the voltage ripple on the control side of the voltage-controlled oscillator (VCO). All LPF passives are on-chip. The output current of the PD injected into the LPF achieves fast phase-locking, while the FD will produce the polarity of the frequency error, namely, the VCO frequency greater or less than the locking frequency, and injects the current of (VIC)FD into C1 for voltage integration, thus minimizing the frequency error in frequency locking. In the case of our dual-loop PLL design, we first optimize the loop parameters based on the phase-detection loop. And then the calculation method will be discussed later in Section II-E. The locking time may increase due to the settling process dominated by the frequency-detection loop. By properly setting the small current ratio (< 4 ×) between (V/I)FD and (V/I)PD, we can fully eliminate the instability risk. To reduce the entire PLL’s power and enhance jitter performance, the VCO design is critical which is based on a multi-LC-tank topology using the 2nd- to 4th harmonic resonances to shape the impulse-sensitivity-function and reduce its RMS value [12]. Subsequently, a frequency divider chain has a total modulus of 256, corresponding to an mm-wave output frequency of 26.368 GHz with a 103-MHz external reference (REF) input. Note that the last divider-by-2 will provide the quadrature outputs, VQ and VI, to create the quarter-period pulse. They compare with the REF signal (VREF) to modulate the pulse duration of the injection current for both phase and frequency detection loops.

The typical XOR-based FD and PD [9], [13] are based on the current-mode logic (CML) with small input/output swings to convert the phase and frequency error into the current. Their static biases regrettably penalize the total power consumption. Also, the CML topology suffers from the tail-current mismatch, inducing static phase error and jitter deterioration. However, extra voltage-bias circuitry is involved. To remedy it and save the static power, we propose the dynamic FD and PD enabling significant power reduction under a high-frequency REF input.

B. PROPOSED FD

Fig. 2(a) presents our proposed FD that detects the frequency error with a DFF-based tri-state PFD, which can secure a large acquisition range. Another DFF sampling VQ by VREF generates an indication signal (VFD) to turn on/off the subsequent (VIC)FD. If the two frequencies of VREF and V1 are unequal, VFD will be a pulse signal with two states: GND and VDD, to switch the (VIC)FD periodically. Fig. 2(b) shows the proposed (VIC)FD of the FD. When VFD is in the GND state, the tail current source (M1) turns off, while M2 and M3 work in the deep-triode or cutoff region, (VIC)FD is disabled, indicating that the impact of the FD on the entire PLL is blocked. Inversely, when VFD is in the VDD state (VIC)FD will be activated.
Similarly, if the VCO is fast, the period of $V_{FD}$ will be,

$$T_{FD} = \frac{1}{f_{DIV} - f_{REF}}$$  \hspace{1cm} (3)$$

Therefore, $(VIC)_{FD}$ will be turned on/off with a period of $T_{FD}$.

Our FD also has the function of the phase-detection once the VCO output frequency is locked. Fig. 3(b) illustrates its phase-identification characteristic, indicating that the phase error ($\Delta \Phi$) determines the state of $V_{FD}$. Compared to the tri-state PFD with a dead-zone of $\pm \pi$ range [14] for the phase detection, Fig. 3(c) shows the simulated phase-detection curve of our FD with a dead-zone of $\pm \pi/2$ range. Our FD can reduce the phase error to a smaller value before turning off, which helps the PLL locking faster. When the phase error, $|\pi| > \Delta \Phi > |\pi/2|$, $V_{FD}$ will be in the VDD state to enable $(VIC)_{FD}$ and integrate the VCO output frequency, thus reducing the phase difference. The $(VIC)_{FD}$ has turned off automatically when $\Delta \Phi < |\pi/2|$, which no longer contributes to the power consumption and noise. Then, the activation of the PD only happens for phase locking. For the simulated phase [Fig. 3(c)] and frequency [Fig. 3(d)] detection characteristic, within $|\pi| < |\pi/2|$, the current injection is zero to disable the FD. As $|\pi| > |\pi/2|$ and $f_{DIV} \neq f_{REF}$, the current of $(VIC)_{FD}$ injects hundreds of microamperes to aid fast frequency locking. Fig. 3(e) shows the simulated frequency-detection curves under different corners at 103-MHz REF. Additionally, we plot the simulated frequency-detection curve at 1-GHz REF, indicating that our FD is able to operate at a higher frequency.

**C. PROPOSED AND-BASED PD**

Fig. 4(a) presents our AND-based PD, which is similar to the $(VIC)_{FD}$ of the FD. Interestingly, the PD and its VIC are merged to reduce the number of transistors, thereby improving the power and operating speed. The overall PD + $(VIC)_{PD}$ contains only ten transistors that draw sub-1 mW in our design.

The up-current ($I_{UP}$) is determined by the pulses generated by the fixed phase error between $V_I$ and $V_Q$, leading to a constant $I_{UP}$ with a quarter-period REF pulse. The down-current ($I_{DN}$) is crucial to correct the phase error between $V_{REF}$ and $V_Q$, resulting in the pulses whose widths are proportional to the phase error. Their behavior can be expressed as,

$$\overline{V_I + V_Q} = I_{UP} = V_I \cdot V_Q$$

$$\overline{V_Q + V_{REF}} = I_{DN} = V_Q \cdot V_{REF}$$  \hspace{1cm} (4)$$

where the above equations exhibit the equivalent behavior between the implementation in [9] and our solution. The left-sided term shows the PD operation using the power-hungry CML-based XOR gate [9], furthermore, its function is determined by an extra voltage bias. Based on De Morgan’s laws, our AND-based PD represents the same operations at the right-sided term. Once the PLL is locked, the UP/DN current in our PD maintains within a quarter power.
FIGURE 4. (a) Proposed AND-based PD + (VIC)PD. (b) Its timing diagram. (c) Simulated phase-detection curves at 103-MHz and 1-GHz REF inputs. (d) Simulated phase-detection curves under different corners at 103-MHz REF period of REF. Compared to the CML-based PD that consumes static power, our PD reduces power consumption by four times.

Fig. 4(b) illustrates the timing diagrams of the proposed PD for leading and lagging conditions. When the VCO lags (i.e., $\Delta\Phi = \Phi_{REF} - \Phi_{DIV} > 0$), the rising edge of $V_I$ lags behind $V_{REF}$, the overlapping area between $V_Q$ and $V_{REF}$ for generating $I_{DN}$ is < $1/4$ cycle, pushing (VIC)PD to inject the current ($I_{UP} - I_{DN} > 0$) into the LF to raise the VCO frequency and minimize the phase error. When the VCO leads (i.e., $\Delta\Phi < 0$), vice versa, the rising edge of $V_I$ leads $V_{REF}$, the overlapping area of $V_Q$ and $V_{REF}$ for generating $I_{DN}$ is > $1/4$ cycle, pushing (VIC)PD to draw more current ($I_{UP} - I_{DN} < 0$) to decrease the VCO frequency for phase locking.

For the simulated phase-detection curves at 103-MHz and 1-GHz REF inputs [Fig. 4(c)] of our PD, as $\Delta\Phi < |\pi/2|$, the FD is disabled and the PD has a constant phase-detection gain ($K_{PD}$) of 0.4/2 $\pi$ mA/rad in the linear curve. The average output current ($I_{VI,avg}$) of the (VIC)PD reaches the maximum value $I_{VI,avg,max} = I_{UP(DN)}/4$ when $\Delta\Phi = |\pi/2|$. Since the PD will be enabled all the time, leading to $\Delta\Phi > |\pi/2|$, the PD will repeat the linear curve periodically. Since the injection current of the PD is four times smaller than that of the FD, it will not dominate the loop for locking. Fig. 4(d) shows the phase-detection curves under different process corners at 103-MHz REF input.

The PD aids the PD to only operate at $\Delta\Phi < |\pi/2|$, since the PD curve repeats periodically, when $\Delta\Phi = 0$ ($K_{PD} > 0$) and $\Delta\Phi = \pi$ ($K_{PD} < 0$), $I_{VI,avg}$ equals to zero [Fig. 5(a) and (b)]. Yet, the alignments between $I_{UP}$ and $I_{DN}$ are different. If the PLL initially starts at $\Delta\Phi = \pi$, the PLL will enter the positive feedback loop, being unstable. Thus, $\Delta\Phi$ should accumulate and eventually will approach zero upon locking.

D. VCO AND FREQUENCY DIVISION CHAIN

Fig. 6(a) shows the mm-wave multi-LC-tank VCO similar to [12] driving the 1st divider-by-4 (DIV4) [15]–[20] in the division chain without extra buffer. The use of dynamic latch [Fig. 6(b)] also aids in improving power efficiency. To ensure the coverage of the overall tuning range of the VCO, a wider locking range (LR) of the 1st divider is desired via tuning $V_T$ to have the combination of multiple sub-bands (e.g., 3 sensitivity curves). Differing from this small-swing LR of ∼10% in [15], we effectively introduce a large-output-swing VCO to equivalently obtain a wider LR of the middle sensitivity curve [Fig. 6(c)] even without tuning the voltage bias ($V_T$), provided by an off-chip low-dropout (LDO) regulator. It covers the >15% tuning range of the VCO. Note that, in our design, the VCO outputs large swing intrinsically. It means that the larger injection amplitude of the DIV4 is enhanced for improving the injection efficiency, and further obtaining the large LR. To verify the robustness of the DIV4, its sensitivity characteristics under the key process corners are conducted. By properly tuning $V_T$, its sensitivity curves in Fig. 6(d) cover the lock range of the PLL.

To generate the constant quarter-period pulse as the intrinsic reference pulse, we proposed the true-single-phase-clock (TSPC) quadrature divider-by-2 (QDIV2) as exhibited in Fig. 7(a). The QDIV2 is composed of a high-level sensed TSPC latch and a low-level sensed TSPC.
latch. Thus, a master-slave topology is formed by inputting a true single-phase clock from the single-ended TSPC-based divider-by-32. The simulated I/Q mismatch is $< 1^\circ$ within the PLL operating range [Fig. 7(b)].

**E. CALCULATION PROCEDURE OF THE LOOP PARAMETERS**

To construct a stable dual-loop PLL, we summarize the calculation procedure [Fig. 8(a)] of the loop parameters in the dual-loop PLL as follows: 1) determine the main-loop (i.e., PLL) parameters, including phase margin (PM\(_{PLL}\)), loop bandwidth (BW), \(I_{V_{L,PD}}\), \(K_{vco}\), and division ratio (N) based on the design specification; 2) calculate the LPF parameters (\(C_1, C_2, C_3, R_2, R_3\)) according to the above main-loop parameters; 3) preset initial current (\(I_{V_{L,FD}}\)) of the (VIC)\(_{FD}\). For example, its current is four times greater than that of the (VIC)\(_{PD}\); 4) compute phase margin of the frequency-locked loop (PM\(_{FLL}\)). As shown in Fig. 8(b), we define the PM\(_{FLL}\) of 35\(^\circ\) as the minimum stable value of the FLL. Once PM\(_{FLL}\) $< 35^\circ$, \(I_{V_{L,FD}}\) will be reduced until PM\(_{FLL}\) $> 35^\circ$. After plenty of circuit simulations, both the main loop and the FLL are absolutely stable.

**F. SIMULATED SETTLING BEHAVIOR**

First, we summarize an intuitive insight into the closed-loop dynamic behavior. Recalling the loop parameters in Fig. 8(a), it’s shown that the strong and weak loops [Fig. 9(a)] correct the frequency and phase errors, respectively. As observed in Fig. 9(b), during the settling process, the FLL will be
FIGURE 8. (a) Calculation procedure of the loop parameters in our dual-loop PLL. (b) Bode plots for the PLL and FLL of our dual-loop PLL.

turned on intermittently before the frequency is locked, which depends on the amount of the frequency error. Fig. 9(c) shows the zoomed-in settling behavior of our PLL. At this interval, the negative $K_{pd}$-related phenomena can be found as a special case. Fig. 9(d)-(f) plot the corresponding transient waveforms of the PLL operating at different instantaneous phase errors. When the PLL works around $\Delta \Phi = -\pi$, its settling behavior stays the Region A [Fig. 9(c)]. Correspondingly, negative $K_{pd}$ can be observed in the open-loop phase-detection characteristics of the PD, as shown in Fig. 10. It implies that the PD + (VIC)PD operates in the weak positive feedback loop. Yet, the overall PLL is absolutely dominated by the strong negative feedback loop with FD + (VIC)FD. Thus, the (VIC)FD sinks current from the LPF, and $V_C$ decreases. After a period, the phase error is reduced from $-\pi$ to $-\pi/2$, approaching Region B [Fig. 9(c)]. The FLL will be powered off and (VIC)PD continues to sink current from the LPF. The reduction of $V_C$ becomes very slow.

After crossing $\Delta \Phi = -\pi/2$ (Fig. 10), the positive $K_{pd}$ makes the phase-locking loop enter into the negative feedback loop for accumulating the instantaneous phase error under large frequency error. Eventually, the overall PLL will be locked at $\Delta \Phi = 0$ (Fig. 10) and the FLL has been automatically turned off.

Next, we brief the open-loop phase-detection curves (Fig. 10). The conventional tri-state PFD has an infinite frequency capture range along with its positive and linear gain. Yet, after the frequency is locked, it cannot be automatically turned off. Since the dead-zone (DZ) creator [14] is inserted after the tri-state PFD, it can automatically turn off the FLL when the frequency is locked. The issue of the DZ-based tri-state PFD is that its $K_{pd}$ keeps constant zero and losing the loop dynamic capture behavior. Thus, when the DZ-based tri-state PFD is turned on, the CP behind it injects (or sinks) constant current to (or from) the LPF. As a result, the entire PLL takes more time to realize the frequency lock. Differently, our proposed FD keeps the loop dynamic as the classic tri-state PFD and can be automatically turned off when the frequency is locked. Therefore, our FD saves a lot of time to achieve the frequency lock.

Although the FD’s settling behavior in both our proposed design and [21] varies as approaching the locking point, the PLL’s settling behavior is far different. In our design, there is less cycle slip before entering the lock-state. As shown in Fig. 11, the simulated settling behaviors of the PLL with different reference frequencies are as follows. It indicates that our FD can switch alternatively even if the REF frequency ($F_{REF}$) is at a high frequency of $16 \times 10^3$ MHz. Fig. 11(a) and (b) show that the PLL locks faster when the FLL is turned on because the (VIC)FD provides more current and achieves a larger loop bandwidth. In addition, since the initial frequency error is amplified by N times when $F_{REF}$ is increased by N times, the FLL needs more time to correct the frequency error before the FLL locks. According to Eq. (3), the starting frequency of $V_{FD}$ will increase by N times simultaneously.

Interestingly, the GHz-reference frequency can be used as an input for the second stage of a cascaded PLL [22]. Especially in the ultra-scaled CMOS technology, it’s very challenging to achieve low phase noise of the high-frequency VCO. Thus, a solution to implement a low-integrated-jitter PLL is to cascade a low-frequency ultra-low-noise PLL and a GHz-$F_{REF}$ high-frequency PLL. The traditional PFD+CP can operate at MHz-to-GHz reference frequency, especially in the ultra-scaled CMOS technology. Yet, the designer must cope with the dead-zone issue in order to balance the multi-dimensional optimization. Differently, our PD and (VIC)FD are merged together and controlled by a quarter-period REF pulse, which is generated by the instinct I/Q output of the last stage of the divider chain. In addition, our PD and FD functions are based on the minimum number of transistors.
III. MEASUREMENT RESULTS

Fig. 12 depicts the chip micrograph of the mm-wave dual-loop PLL fabricated in 65-nm CMOS technology, with an active area of 0.26-mm$^2$ including all LF passives. At a 1-V supply, the PLL dissipates in a total of 10.64 mW with 0.28 mW consumed by the PD/FD + VIC. The VCO draws 6.5 mW under 0.55-V supply and the frequency division chains consume 3.86 mW. The power consumption of the reference buffer is 0.24 mW with a 1-V supply voltage. We use an external 103-MHz crystal oscillator to generate the REF input with the output tested via a divider-by-4 circuit to simplify the test setup.

Fig. 13 outlines the measured phase noise at 26.4 GHz. Consider the divider chain in our design with a large divide ratio, the in-band phase noise is mainly dominated by the loop components, while the high-pass-filtered VCO noise
rules the out-of-band phase noise. In addition, the current mismatch in the (VIC)PD incurs significant voltage ripple on $V_C$. To optimize the PLL overall performances, a smaller loop bandwidth ($\approx 0.6$ MHz) is employed, which not only helps to suppress the in-band phase and balances the integrated jitter, but also significantly reduces the reference spur. The integrated jitter achieves 415.6 fs$_{\text{rms}}$ from 10 kHz to 100 MHz, its variation is <30 fs$_{\text{rms}}$ among the 5 chips.

Fig. 14 shows the measured REF spur level of $-53$ dBc at 103-MHz offset and its variation is <4 dB among the 5 chips. Herein, the reference spur is mainly induced by the current mismatch of the (VIC)PD. Moreover, the larger $K_{\text{VCO}}$ ($\approx 800$ MHz/V) in this design magnifies the impacts of its current mismatch on the reference spur. We use a 3rd-order LPF with small loop bandwidth ($\approx 0.6$ MHz) to improve the reference spur while penalizing the active area in Fig. 12. Particularly, since our PD and the PD structure of [9] are based on the logic relationship, both achieve excellent linearity. The non-ideality to be illustrated here is the current mismatch, which causes the voltage ripple. The reference spur can be improved by introducing the calibration of the current-mismatch reduction like the counterpart in the conventional charge pump. To alleviate the reference spur, an isolated master-slave phase detector [24] is realized to output the dc voltage and the VIC converts dc voltage to dc current.

Fig. 15 plots the measured phase noise and estimated contributions for the different components of the entire PLL. We can observe that the in-band phase noise is dominated by the AND-based PD + (VIC)PD.

Fig. 16 shows the jitter-power performance among the recent 25+ GHz PLL. Table 1 compares our performance with the state-of-the-art [1]–[6] and [23], [24], where the proposed PLL exhibits a more competitive jitter-power performance at low power and low complexity, thereby an improved figure-of-merit (FoM) of $-237.4$ dB is along with a low reference spur level of $-53$ dBc. In our design, a smaller loop bandwidth ($\approx 0.6$ MHz) is employed to optimize the overall performance. That is, this helps us to suppress the in-band phase noise and reducing the reference spur. Compared with the sub-sampling PLL topology [24], our PLL is based on
the explicit division chain, indicating that it still shows the advantages in terms of stability and robustness.

IV. CONCLUSION
This paper reported an mm-wave dual-loop type-II PLL with low power and a simpler dynamic frequency detector (FD) and a phase detector (PD) to enhance the operating speed up to GHz. It scores a measured jitter of 415.6 fs rms, with a reference spur of −53 dBc and a total power of 10.64 mW. The achieved jitter-power FoM compares favorably with the prior art.

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REFERENCES


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