A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC

Yan Song, *Member, IEEE*, Chi-Hang Chan, *Member, IEEE*, Yan Zhu, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— This article presents a successive approximation register (SAR)-assisted noise-shaping (NS) pipeline architecture which breaks the speed bottleneck of the existing SAR or SAR-assisted-type NS analog-to-digital converters (ADCs). Rather than only for residue amplification and pipeline operation, the multiplying digital-to-analog converter (MDAC) is also reused as unity buffer and analog adder to realize the NS with error feedback (EF) structure in this design. While incorporating the proposed alternative loading capacitor (ALC) technique, an ideal first-order noise transfer function (NTF) is realized without additional feedback phase and only with a small analog circuit overhead. Unlike other NS SAR ADCs that involved amplification, the inter-stage gain attenuates the noise from the second-stage comparator, thus leading to both high speed and resolution. Fabricated in a 65-nm CMOS process, the prototype achieves a signal-to-noise-and-distortion ratio (SNDR) of 77.1 dB over 12.5-MHz bandwidth (BW) with only over-sampling ratio (OSR) of 8. Under a 1.2-V supply voltage, the ADC consumes 4.5 mW and exhibits a Scherier figure of merit (FoM) of 171.5 dB.**

***Index Terms*— Alternative loading capacitor (ALC), analog-to-digital converter (ADC), multiplying digital-to-analog converter (MDAC) reusing, noise shaping (NS), successive approximation register (SAR)-assisted pipeline.**

I. Introduction

THE Internet-of-Things (IoT) and wireless communication systems in the forthcoming technological generation require energy-efficient analog-to-digital converters (ADCs) with high dynamic range (DR), while driven from the user end, the ADC's bandwidth (BW) has to be in more than tens of megahertz [1], [2] to support large enough data throughput. The conventional successive approximation register (SAR) architecture is well known for its outstanding power efficiency, but its speed and resolution are greatly confined by the serial conversion scheme as well as the thermal noise from the comparator and DAC mismatches [3], respectively. To relax the comparator design, the noise-shaping (NS) architecture can be hybrid within an SAR structure as first reported in [3]. It adopts an operation-transconductance-amplifier (OTA)-based active finite impulse response (FIR)-infinite impulse response (IIR) loop filter to achieve a first-order NS on both quantization and comparator noise in the SAR ADC. Nevertheless, in order to maintain a good NS efficiency and short integration time, the OTA needs to be with high gain and BW, thus leading to a power-hungry design. In [4] and [5], the proposed circuit removes the OTA by replacing the active filter in [3] with a passive switched-capacitor (SC) loop filter. Although it consumes no static power, the NS efficiency is degraded due to the signal attenuation during the passive charge sharing. Following works improve the NS efficiency and realize a high-order NS, but they still suffer from multiple input pairs of comparators leading to extra noise contribution, therefore deteriorating the NS improvement in the overall ADC signal-to-noise ratio (SNR). In [6] and [7], the dynamic amplifier is used to balance the performance between power and NS efficiency. The gain provided by the amplifier before the loop filter also suppresses the kT/C noise from the SC filters. However, the dynamic amplifier greatly suffers from process–voltage–temperature (PVT) variations that require gain calibration for a stable performance increasing the design complexity. The SAR + voltage-controlled-oscillator (VCO) hybrid structure [8] is another option to improve the resolution of the SAR ADC under low power consumption. The highly digitalized VCO is scaling friendly with the intrinsic first-order NS, while it is necessary to calibrate the tuning gain over PVT variation.

Although these designs show a promising energy efficiency to achieve high resolution, their BW is under 5 MHz for a signal-to-noise-and-distortion ratio (SNDR) $>$ 70 dB. This is mainly due to their low-speed NS procedure, where the whole SAR conversion should be completed before the residue voltage to be processed for NS. Thus, the SAR conversion halts during the residue integration. There are also prior NS SAR ADCs achieving wide BW [3], [9], but they are only targeting low-accuracy applications. It is also worth noting that in such a range of specifications, a Nyquist ADC without NS or over-sampling already demonstrates a better efficiency [10], [11]. This implies that further research should be pursued to extend both the resolution and BW while maintaining the excellent power efficiency.

In this article, the NS technique is applied in the SAR-assisted pipeline ADC where the multiplying digital-

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Y. Song, C.-H. Chan, and Y. Zhu are with the State Key Laboratory of Analog and Mixed Signal VLSI, Institute of Microelectronics, Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao 999078, China (e-mail: yansong@ieee.org; ivorchan@ieee.org).

R. P. Martins is with the State Key Laboratory of Analog and Mixed Signal VLSI, Institute of Microelectronics, Department of Electrical and Computer Engineering, Faculty of Science and Technology, University of Macau, Macao 999078, China, on leave from the Instituto Superior Técnico, Universidade de Lisbon, 649-004 Lisbon, Portugal.

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to-analog converter (MDAC) is not only adopted for residue amplification but also configured as a residue adder to realize error feedback (EF) NS in the second-stage SAR ADC. The proposed alternative loading capacitor (ALC) technique ensures a unity-gain feedback for the second-stage residue voltage, resulting in a standard first-order noise transfer function (NTF) without extra active circuits, additional residue feedback, and integration phase. Incorporated with the pipeline operation, the proposed SAR-assisted NS pipeline architecture achieves higher speed over the prior single-channel NS SAR ADCs [3]–[9]. Besides, since the residue summation is accomplished by the MDAC in our EF structure, additional comparator input pair as in the feed-forward (FF) structure [3]–[6] can be avoided. Moreover, the comparator noise is further suppressed through the inter-stage gain in the pipeline architecture, and thus, the ADC can reach a high SNR with a low over-sampling ratio (OSR). The ADC prototype fabricated in 65-nm CMOS with a 1.2-V supply voltage secures 77.1-dB SNDR operating at 200 MS/s with only OSR of 8. The proposed NS architecture with an energy-efficient MDAC and accuracy-relaxed comparator consumes only 4.5 mW of power, yielding a Schreier figure of merits (FoMs) of 171.5 dB over a 12.5-MHz BW.

The organization of this article is as follows. Section II discusses the resolution and speed constraints of prior NS SAR ADCs. Section III introduces the concept of the SAR-assisted NS pipeline architecture. Section IV presents the reusing of the MDAC and ALC techniques associated with MDAC design considerations. Section V details the overall architecture and circuit implementation. Finally, we report the measured results and conclude this article in Sections VI and VII, respectively.

II. NS Efficiency and Speed Constraints in SAR Hybrid NS Architecture With Amplifier

In prior arts, there are several hybrid ADCs that combine SAR with NS while involving amplification for the residue voltage. Such amplification leads to various effects on the overall ADC transfer function. In Section II, we will discuss their speed constraints and how their NTFs are affected by the gain of the amplifier.

A. Feed-Forward Architecture With Amplifier

Fig. 1(a) shows the block diagram of the NS SAR ADC with FF configuration assisted by an amplifier [3], [6]. Basically, it consists of an SAR ADC, an amplifier, and a loop filter. After the SAR conversion, the final residual voltage (V_{res}) is inherently ready at the DAC, which is then further sampled and passed through the loop filter to realize the desired transfer function. An additional input pair in the comparator receives the filtered residual voltage that is quantized together with the input signal in the next conversion cycle. Through the above-mentioned operations, the ADC's output (D_{out}) can be derived as

$$D_{\text{out}}(z) = V_{\text{in}} + \frac{D(z)}{D(z) + G \cdot N(z)} \cdot E_Q(z) \tag{1}$$

where E_Q is the quantization error, G is the gain of the amplifier, and $N(z)$ and $D(z)$ are the numerator and denominator in the transfer function of the loop filter ($H(z)$), respectively. In the FF NS SAR ADCs without the amplifier [4], [5], the residue transmission loss due to the passive charge-sharing results in the pole of the NTF moving toward "1" ($\alpha_i < 1$) and degrades the NS ability. In [3], the OTA-based integrator in the loop filter, where the amplifier is used, prevents the signal loss during the integration process. Since the zero (κ_j) of the NTF mainly affects the noise attenuation ability at low frequency, the active integrator keeps zero close to 1 to maintain a good NS efficiency. However, it imposes a high-gain and large BW OTA for high-speed operation, while in [6], a dynamic amplifier is utilized to provide a gain of G [see Fig.1(a)] to optimize the pole of the NTF for more in-band noise attenuation through the enlarged out-of-band gain.

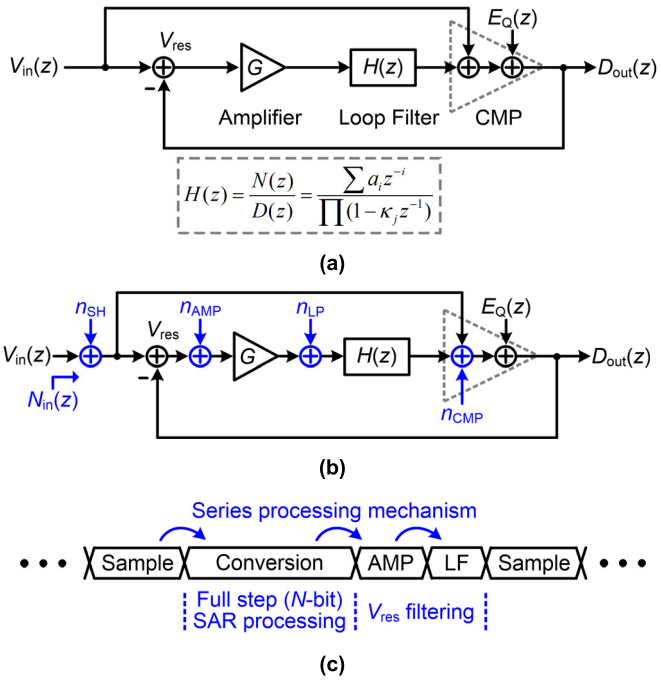


Fig. 1. (a) Block diagram, (b) noise source, and (c) timing sequence of the NS SAR ADC using the FF structure with amplifier.

The complete input-referred noise expression of the FF NS SAR ADC with amplifier can be written as (2) based on Fig. 1(b)

$$N_{\text{in}} = n_{\text{SH}} + \frac{G \cdot N(z)}{D(z) + G \cdot N(z)} \cdot n_{\text{AMP}} + \frac{1}{D(z) + G \cdot N(z)} \cdot n_{\text{LP}} + \text{NTF}_Q \cdot (n_{\text{CMP}} + E_Q) \tag{2}$$

where NTF_Q represents the NTF of $E_Q(z)$ in (1). It can be clearly deducted from (2) that the comparator noise (n_{CMP}) as well as the quantization error (E_Q) are shaped. However, the amplifier's thermal noise (n_{AMP}) and the loop filter's noise (n_{LF}) are not suppressed in the band of interest, which eventually causes either a large capacitive load or a large power consumption in the amplifier or the loop filter.

Fig. 1(c) shows the timing sequence of the NS SAR ADC with the FF architecture. Based on a series processing mechanism where the integration follows the SAR conversion,

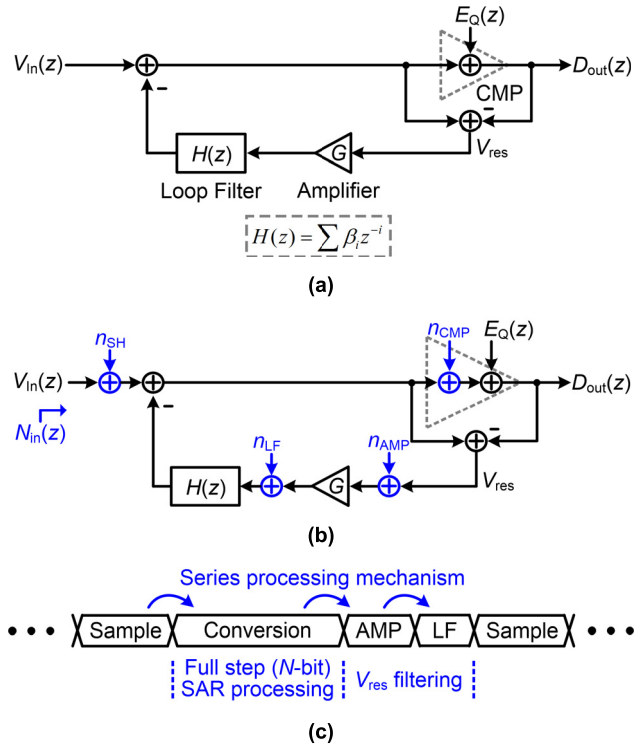


Fig. 2. (a) Block diagram, (b) noise source, and (c) timing sequence of the NS SAR ADC using error-feedback structure with amplifier.

the next sample only can be conducted after the completion of the whole SAR conversion and integration. Since N conversion cycles are needed for an N-bit SAR ADC quantization and the SAR ADC cannot release the result during the integration in [3] or amplification in [6], this setup greatly limits the speed of the ADC, especially with large N for high resolution.

B. Error Feedback Architecture With Amplifier

The EF architecture, shown in Fig. 2(a), is another commonly adopted structure for implementing SAR hybrid NS [7], [12]. It also comprises the basic SAR ADC, an amplifier, and a loop filter. After the SAR conversion, the full resolution residue is buffered to the loop filter through the amplifier with a gain of G. Different from the FF NS structure, the filtered residual voltage is added to the input signal during the next sampling period [12], and the summed voltage is subsequently quantized by the SAR ADC in the following conversion phase. The output of the ADC (D_{out}) will become

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \left[1 - G \cdot \sum \beta_i z^{-i}\right] \cdot E_Q(z). \quad (3)$$

In the EF architecture, the loop filter is implemented with the combination of several delay cells, where the zeros of the NTF are related to their coefficients. Due to the passive charge sharing in the SC loop filter, the zeros are smaller than 1, resulting in a poor NS effect at low frequency. Similar to the FF architecture, the amplifier here provides gain to compensate the signal loss from the loop filter and pushes the zeroes close to the unit circle. Besides, without the extra summation pair

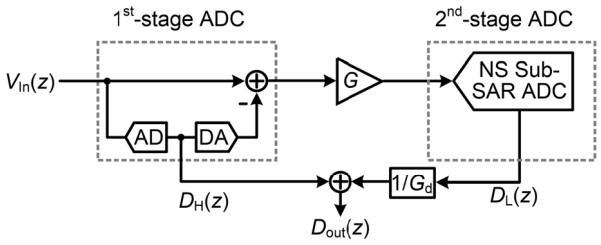


Fig. 3. Concept of the SAR-assisted NS pipeline structure.

in the comparator for FF structure that originated additional noise, the overall noise performance is also improved [7]. In [7], a further enhancement is obtained by introducing optimized zeros through the specific operation of the loop filter together with the amplifier, resulting in a notch in the NTF. Nevertheless, the location of the notch depends on G requiring gain calibration to ensure the accuracy of G and NTF.

Fig. 2(b) shows the noise source of the EF NS architecture. The input-referred transfer function of the major noise sources can be determined as

$$N_{\text{in}} = n_{\text{SH}} + \left(G \sum \beta_i z^{-i}\right) \cdot n_{\text{AMP}} + \left(\sum \beta_i z^{-i}\right) \cdot n_{\text{LF}} + \text{NTF}_Q \cdot (n_{\text{CMP}} + E_Q) \quad (4)$$

where NTF_Q represents the NTF of E_Q in (3). Generally, similar to the previously described FF architecture, the noise from the comparator also cannot be relaxed by the gain of the amplifier; besides, the amplifier has no effect on suppressing the noise from the loop filter.

The NS SAR ADC with the EF architecture is also based on a series working scheme, as shown in Fig. 2(c), which shares a similar limitation to the FF scheme in terms of speed. Although in [7], the residue is fed back to the DAC in the middle of the SAR conversion, which saves the time for residue feedback, the residue extraction and filtering process are necessary before the next ADC sampling.

III. Proposed SAR-Assisted NS Pipeline Architecture

As discussed in Section II, it can be concluded that there are two common issues on the prior NS SAR arts with amplifier: 1) the gain of the amplifier cannot relax the comparator noise that limits the achievable resolution, especially in an FF NS structure with an additional input pair in the comparator and 2) the full resolution conversion and integration/amplification conducted in series that limits the overall speed. To mitigate these constraints, the pipeline concept can be introduced in the NS SAR ADC, and Fig. 3 shows its block diagram. It consists of an SAR ADC in the first stage, which quantizes the coarse most significant bits (MSBs), and a pipelined NS SAR ADC in the second stage. The pipeline operation enabled by the inter-stage amplification releases the first-stage ADC to the next sampling, while the second-stage ADC determines the rest least significant bits (LSBs) conversion for complete residue extraction and filtering. This operation breaks the speed bottleneck in the existing NS SAR ADCs. In addition, the inter-stage amplification provides gain (G) to relax the

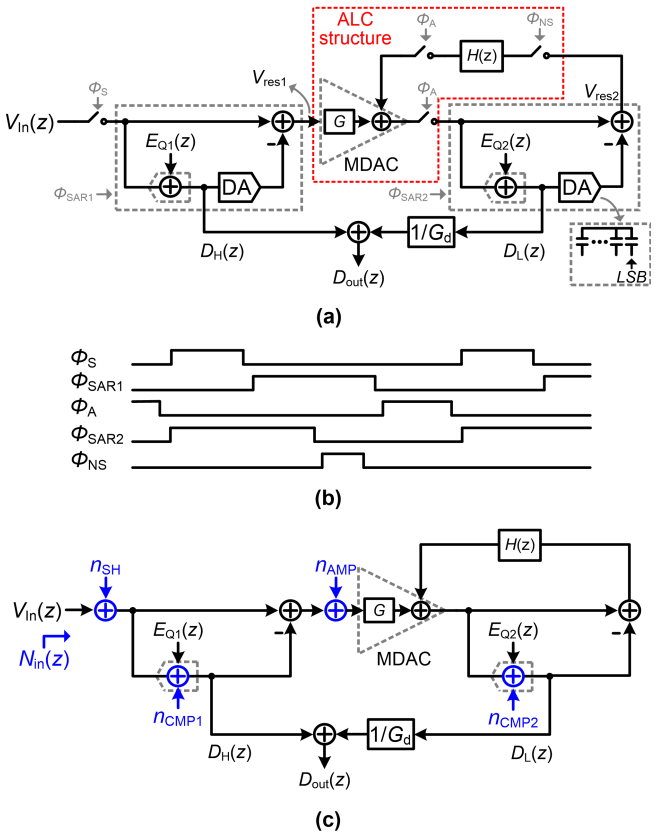


Fig. 4. (a) Block diagram, (b) timing sequence, and (c) noise source of the proposed SAR-assisted NS pipeline ADC architecture.

noise and matching requirement of the second-stage sub-ADC. Consequently, such amplification can enhance both speed and resolution from the previous NS SAR designs.

In the second stage, the NS SAR ADC can be implemented either by an FF or an EF architecture, as introduced in Section II. While the FF structure needs an extra amplifier for a good NS efficiency, the EF structure also requires an additional analog adder to sum the signal. Fortunately, in a conventional SAR-assisted pipeline architecture [10], [13], such adder is inherently available in the MDAC, which provides a convenient way to realize the EF architecture with a small hardware overhead. In this design, we reuse the residue amplifier as the analog adder to build the EF NS SAR ADC in the second stage, thus obtaining an NS pipeline structure through a small modification of the conventional SAR-assisted pipeline structure.

Fig. 4(a) shows the block diagram of the SAR-assisted NS pipeline architecture with the EF structure through the MDAC, where E_{Q1} and E_{Q2} are the quantization errors generated in the first- and second-stage SAR ADCs, respectively, and G_d is the attenuation factor for gain compensation in the digital domain. In Fig. 4(a), a feedback path containing a residue sampler (S/H), a buffer, and a loop-filter ($H(z)$) is necessary to realize the NS mechanism. Fig. 4(b) shows the timing sequence. The input signal is first sampled and quantized by the SAR ADC as the conventional operation in the SAR-assisted pipeline ADC. The second stage generates the full-resolution residue voltage (V_{res2}) by feeding back the LSB code to the capacitive digital to analog converter (CDAC) after the completion of the conversion. Then, $H(z)$ samples and filters V_{res2} and transferred to the MDAC for residue summation during the amplification phase (Φ_A). The second-stage ADC samples the summed voltage that is further quantized in the following conversion phase. The transfer function based on this design concept can be derived as

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \left(1 - \frac{G}{G_d}\right) \cdot E_{Q1}(z) + (1 - H(z)) \cdot \frac{E_{Q2}(z)}{G_d}. \tag{5}$$

It can be deducted that the quantization error from the first-stage ADC does not exist at the final ADC output, if G_d equals to G. Meanwhile, we introduce 1-bit overlapping to ensure that the conversion error from the first stage can be corrected. Eventually, the overall quantization error of the ADC only remains in the second stage that exhibits an NTF of $1 - H(z)$. Moreover, as the proposed architecture separates the SAR ADC into two stages, where the residue voltage only feeds back to the second-stage ADC, it enables the NS mechanism working in the pipeline operation. It is worth noting that there is an SAR-assisted VCO (0–1 MASH) architecture in the literature [8]; however, its first-stage SAR cannot be released during the second-stage conversion, thus posing the same speed limitation from [3], [6], and [7].

Fig. 4(c) shows the major noise sources of the proposed ADC architecture. When $G_d = G$, the input-referred NTF of the major noise sources will become

$$N_{\text{in}} = n_{\text{SH}} + n_{\text{AMP}} + (1 - H(z)) \cdot \frac{1}{G}(E_{Q2}(z) + n_{\text{CMP2}}(z)) \tag{6}$$

where n_{CMP1} and n_{CMP2} are the comparator's noises from the first-and second-stage SAR ADC, respectively. Through the proposed configuration of the SAR-assisted pipeline ADC, the second-stage quantization and comparator noise can be effectively shaped by $1 - H(z)$. Therefore, a smaller number of bits and a noisier comparator can be used in the second stage to save power when comparing it with the conventional SAR-assisted pipeline architecture. Besides, the number of unit capacitors can also be reduced in the second-stage DAC leading potentially to area saving. On the other hand, our architecture faces the same limitations as the existing NS SAR [3], [6], [7] and conventional SAR-assisted pipeline ADCs [10], [13]–15], where the noise from the amplifier cannot be shaped. However, this design takes a further step to fully utilize the amplification for additional NS (comparing to SAR-assisted pipeline) or pipelining (comparing to NS SAR). The proposed architecture shows a great potential for high resolution or BW targets under a good power efficiency. Furthermore, similar to the conventional pipeline ADC, the mismatch error from the first-stage DAC affects the linearity of the ADC. Although the second-stage DAC mismatch error cannot be shaped, it is suppressed by the inter-stage gain G. Thus, the second-stage DAC mismatch error just has a small influence on the overall ADC's linearity.

In this design, not only the NS efficiency is guaranteed through the amplifier, reused in conventional pipeline ADC,

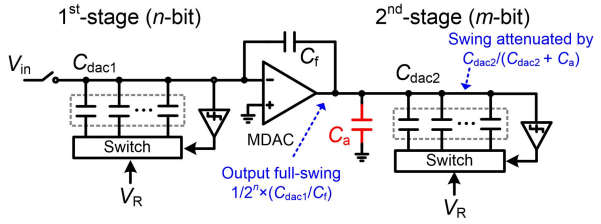


Fig. 5. Reference matching with attenuation capacitor in conventional SAR-assisted pipeline structure.

but also the speed is enhanced by the amplifier through pipeline operation. The closed-loop OTA structure exhibits high-gain stability without a calibration engine unlike its open-loop counterpart [7], thus avoiding extra power consumption from the calibration logic.

IV. Proposed ALC Technique for First-Order NS

In order to realize a standard first-order NS in the second stage, where $H(z) = z^{-1}$ in (5), the full-swing residual voltage in the second-stage ADC should be extracted and fed back to the input for residue summation with unit gain, as shown in Fig. 4. However, this additional feedback process needs extra active circuits and phase, which increases the design complexity and limits the speed. To avoid these drawbacks, we propose a solution that merges the residue feedback with the signal FF path. The basic circuit realizing the proposed solution is the SAR-assisted pipeline structure with attenuation capacitor in the second stage for reference matching [14], [15], as shown in Fig. 5. Usually, the inter-stage gain (C_{dac1}/C_f) is designed smaller than the full gain (2^n) for ensuring the linearity of the MDAC. The capacitor of C_a is added in parallel with C_{dac2} to attenuate the reference voltage in the second stage, where the output swings of the second-stage DAC and the MDAC match, and thus, the full-swing reference voltage can be used in both SAR ADCs for design simplicity. Considering the 1-bit overlapping between the two stages, the product of C_{dac1}/C_f and $(C_{\text{dac2}}+C_a)/C_{\text{dac2}}$ should be 2^{n-1} for reference matching. In our design, we utilize the inherent circuit of the MDAC, C_f, and C_a to realize the first-order NS with the ALC technique at high speed.

A. Proposed Alternative Loading Capacitor Technique

We propose the ALC technique utilizing combined charge-transferring and flip-around MDAC structure to realize the first-order NS, with its operation detail described next. Starting from Fig. 6(a), the first-stage ADC performs sampling and conversion of the current input. Meanwhile, the second-stage ADC converts the sample of the summed residue voltage, where the attenuation capacitor (C_{f2}) connects with C_{dac2} in parallel. After conversions, their corresponding residual voltages [$V_{\text{res1}}(n)$ and $V_{\text{res2}}(n-1)$] are generated on the top plate of C_{dac1} and C_{f2}, respectively. In the following amplification phase, as shown in Fig. 6(b), C_{f2} is configured as the feedback capacitor with the top and bottom plates connected to the output and input of the OTA, respectively. Meanwhile, C_{f1}, which is the feedback capacitor of the MDAC in the previous

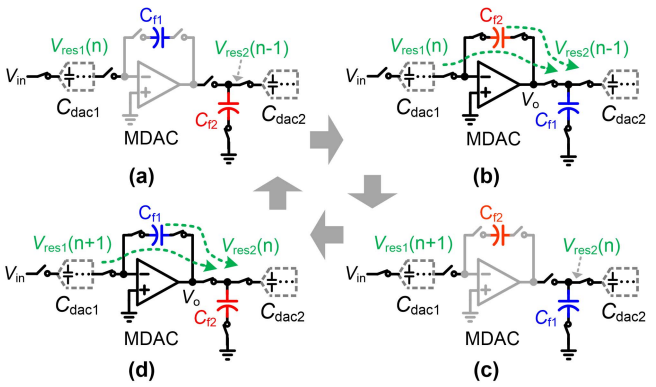


Fig. 6. Circuit operation of the proposed ALC technique.

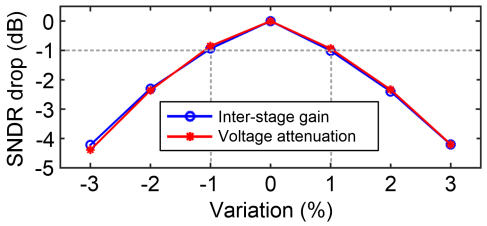


Fig. 7. Simulated SNDR drop due to inter-stage gain [$C_{\text{dac1}}/C_{f1}(C_{f2})$] and second-stage voltage attenuation ratio [$C_{\text{dac2}}/(C_{f2}(C_{f1})+ C_{\text{dac2}})$] variation in the ALC structure.

amplification phase, is configured and connected in parallel with C_{dac2} as the loading capacitor of the OTA. With such setup, $V_{\text{res2}}(n-1)$ is transferred to the second stage and added to V_o based on the flip-around MDAC structure. Simultaneously, the charge-transferring MDAC structure also amplifies $V_{\text{res1}}(n)$ with an inter-stage gain of C_{dac1}/C_{f2}. Consequently, the voltage summation of $V_{\text{res1}}(n)$ and $V_{\text{res2}}(n-1)$ is obtained at the output of the MDAC, which is expressed as

$$V_o(n) = \frac{C_{\text{dac1}}}{C_{f2}} \cdot V_{\text{res1}}(n) + V_{\text{res2}}(n-1). \tag{7}$$

The second-stage SAR ADC samples the summed voltage and quantizes it as normal SAR conversion. The following conversion process is similar to the one described earlier, but C_{f1} and C_{f2} are swapped. C_{f1} is parallelly connected with C_{dac2} during the second-stage conversion, as shown in Fig. 6(c), while C_{f1} and C_{f2} are configured as the feedback and loading capacitors in the following residue amplification process, respectively, as shown in Fig. 6(d).

As C_{dac2} performs the SAR conversion together with $C_{f1}(C_{f2})$ in the second stage, V_{res2} is inherently ready at the top plate of $C_{f1}(C_{f2})$ after the SAR conversion, thus avoiding the extra residue extraction procedure in conventional NS SAR ADC designs [3], [6], [7]. On the other hand, the ALC configures C_{f1} and C_{f2} alternatively as the feedback capacitor (for residue feedback and summation) and loading capacitor of the MDAC to realize NS in the second stage, where C_{f1} is set equal to C_{f2} for interleaving. In this way, the ALC technique realizes the flip-around MDAC structure for signal summation, which realizes the NS pipeline architecture without any additional active circuit. At the same time, it also implies speeding up the conversion due to the omitted residue extraction and

integrating procedures, which are the necessities in other NS SAR ADCs. According to our post-simulation results, the ALC improves the ADC's speed by 28%, while without ALC, V_{res2} should be sampled by extra S/H circuit and fed back to the MDAC before the amplification phase begins.

B. Capacitor Mismatch in the ALC Structure

A potential issue from the ALC technique is the mismatch of the capacitors, which alters the inter-stage gain and the reference attenuation ratio in the second stage. Consequently, it not only leads to a noise leakage and SNR drop of the ADC but the gain error can also cause harmonic distortions. It is because the inter-stage gain and the second-stage voltage attenuation ratio change from C_{dac1}/C_{f1} to C_{dac1}/C_{f2} and from $C_{\text{dac2}}/(C_{f2}+C_{\text{dac2}})$ to $C_{\text{dac2}}/(C_{f1}+C_{\text{dac2}})$ in each conversion cycle, respectively, where a signal-dependent error arises. The mismatches from the inter-stage gain and the voltage attenuation ratio lead to a similar effect on the ADC, since the overall stage gain of the pipeline structure is determined by the product of these two factors. To quantify the influence of the gain mismatch on both the noise and harmonic distortion, Fig. 7 shows the simulated SNDR drop versus the variation of the inter-stage gain and the voltage attenuation ratio. It shows that the SNDR has a similar degradation when the two factors have the same variation range. According to the simulation, the mismatches of the inter-stage gain and the voltage attenuation ratio are about 0.05% and 0.2%, respectively, in our design, which leads to a less than 1-dB SNDR degradation. Therefore, the capacitor mismatch is not a concern for the ALC. It is also worth noting that the unit gain for feeding back V_{res2} will not be affected by the capacitor mismatch, since its gain is not related to the capacitor ratio here.

C. MDAC Gain Accuracy Considerations

In practical implementations, the limited open-loop gain of the OTA affects the accuracy of the MDAC. While the voltage error arising in the inter-stage amplification causes noise leakage between the two pipelined stages, the non-ideal unit gain for V_{res2} also results in NTF degradation. Both the effects degrade the SNR of the ADC.

When we design the open-loop gain of the OTA to be A_o, the output voltage of the MDAC based on the circuit in Fig. 6 can be written as

$$V_o = -\frac{G}{1+\frac{1+G}{A_o}} \cdot V_{\text{res1}} + \frac{1}{1+\frac{1}{A_o}} \cdot V_{\text{res2}}. \tag{8}$$

The flip-around MDAC structure for V_{res2} amplification only consists of the OTA and $C_{f1}(C_{f2})$, which has no relation with the closed-loop gain. Thus, the V_{res2} part in (8) indicates the effect of a non-ideal residue feedback caused by the finite A_o, where the unit gain is decreased to $(1+A_o^{-1})^{-1}$. Consequently, the NTF will be altered to

$$\text{NTF} = 1 - \left(1+\frac{1}{A_o}\right)^{-1} \cdot z^{-1}. \tag{9}$$

According to (9), Fig. 8 shows the Bode diagrams of the NTF under different values of A_o. Fig. 9(a) shows the achieved SNR versus the required A_o with NTF degradation due to non-unity feedback, where a (6 + 5)-bit (1-bit redundancy) pipelined structure is adopted in our design under an OSR = 8. It can be noticed that the SNR stays above 83 dB even with a small A_o value, which indicates that the NTF degradation due to limited A_o is not a serious concern.

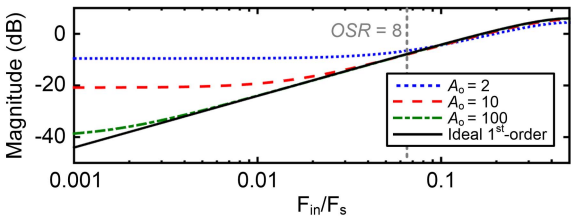


Fig. 8. Bode diagrams of the NTF under different values of A_o.

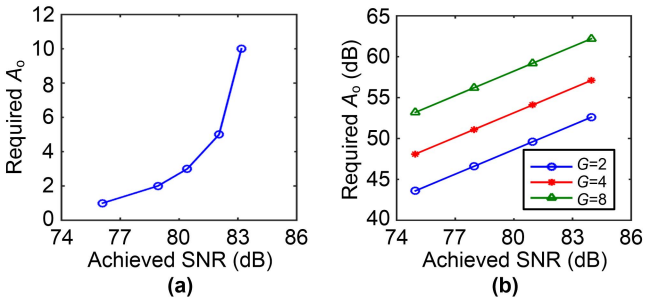


Fig. 9. Achieved SNR versus required A_o in the first-order NS pipeline architecture ($M = 6$ and OSR = 8) under (a) NTF degradation and (b) noise leakage.

It is also indicated by (8) that the non-ideal amplification of V_{res1} leads to noise leakage. This error cannot be noise-shaped, but it is still over-sampled. In order to ensure the resolution, the input-referred voltage error should be less than 1/2LSB referring to the full accuracy of the converter, which is represented by

$$\frac{1}{2^M} \cdot \left(1 - \frac{1}{1+\frac{1+G}{A_o}}\right) < \frac{1}{2} \cdot \frac{1}{2^{N-0.5\log_2 \text{OSR}}} \tag{10}$$

where M and N represent the resolutions of the first stage and the ADC with NS, respectively. It is indicated by (9) that the required A_o is increased with the overall resolution (N) of the ADC, which is similar to a conventional pipeline ADC. The SNR under non-ideal A_o can be calculated according to (10), as shown in Fig. 9(b), where its degradation for small A_o due to noise leakage can be observed. In addition, a larger G value leads to a larger gain error under the same A_o, meaning that the required A_o is proportional to G for the same SNR target. Specifically, with $G = 4$ in our design, A_o has to be larger than 55 dB.

V. Circuit Implementation and Design Consideration

A. Circuit Implementation

Fig. 10 shows the complete single-ended block diagram and the timing sequence of the proposed SAR-assisted first-order NS pipeline ADC, where a fully differential architecture is

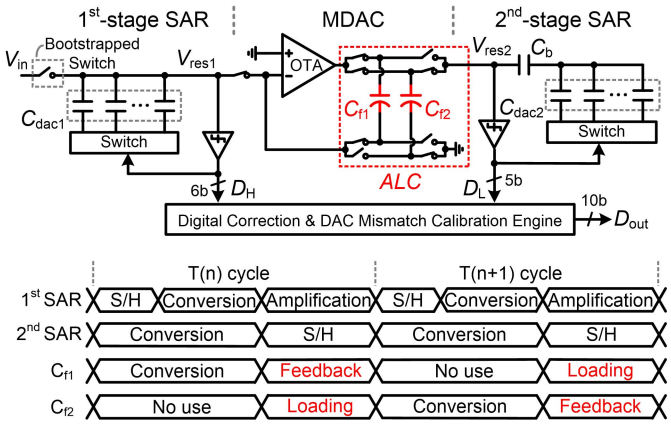


Fig. 10. Top-level schematic and timing sequence of the proposed SAR-assisted first-order NS pipeline ADC.

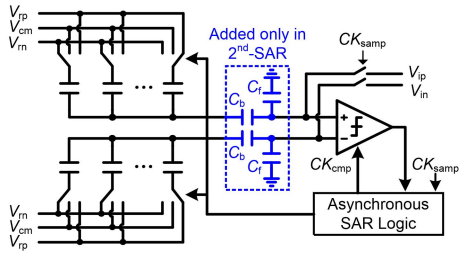


Fig. 11. Schematic of the sub-SAR ADC.

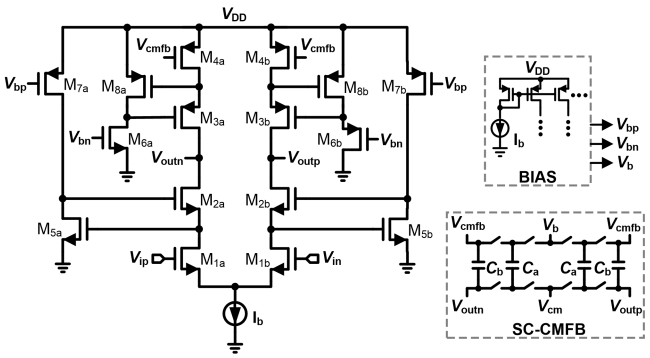


Fig. 12. Schematic of the OTA in the MDAC.

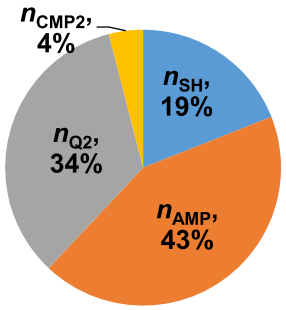


Fig. 13. Noise power breakdown.

implemented in the actual design. The architecture can be defined as a $(6 + 5)$-bit SAR-assisted pipeline ADC with 1-bit redundancy. Both SAR ADCs adopt the $V_{\rm cm}$-based switching scheme for a better linearity [16] due to its constant common-mode voltage, as shown in Fig. 11. The voltage attenuation capacitors (C_b and C_f) are only used in the second-stage ADC. The bootstrapped switch is used in the sampling circuit of the first-SAR ADC to suppress the sampling distortion. The double-tail-latch comparator [17] is adopted in both SAR ADCs. The asynchronous timing sequence is adopted in both the SAR ADCs to achieve high speed. The total capacitance of $C_{\rm dac1}$ and $C_{f1}(C_{f2})$ is 640 and 160 fF, respectively, resulting in an inter-stage gain (G) of 4. Originally, $C_{\rm dac2}$ should be 23 fF to achieve an attenuation factor of 1/8, resulting in a unit capacitance of 0.72 fF. However, such small unit capacitor can affect the linearity of the ADC. Consequently, a bridge capacitor C_b is added in the second stage, thus releasing the constraint of $C_{\rm dac2}$ which has its original size restricted by the ALC capacitors corresponding to the reference matching factor. The unit capacitance then can rise to 3 fF and C_b is set to 30 fF. The variation of C_b causes a similar effect as the reference matching error mentioned error. However, even 1% variation of C_b results in 0.7-dB SNDR drop in this design, whose effects on the performance degradation can be neglected.

Fig. 12 shows the schematic of the OTA in the MDAC. To obtain a large gain under a low supply voltage, the two-stage architecture is a good choice; however, its considerable power consumption degrades the overall efficiency of the ADC. Due to the reduced output swing of the MDAC, this design employs a single-stage cascode architecture with the gain further enhanced by gain-boosting circuits (M_5–M_8). The common-mode feedback reference ($V_{\rm cmfb}$) biases M_{4a} and M_{4b} to stabilize the common-mode voltage of the OTA's output. According to the simulation results, the achieved dc gain and gain bandwidth product (GBW) of the OTA are 61 dB and 3.3 GHz, respectively, where the design margin is left for parasitic effects and PVT variations. Since the design of the closed-loop MDAC structure exhibits adequate values of open-loop gain and GBW for the OTA, the MDAC reveals high stability and accuracy, which avoids any gain calibration.

B. Noise and Linearity Design Considerations

The major noise sources of the proposed ADC structure are shown in (6), including the quantization error (E_{Q2}), the sampling kT/C noise ($n_{\rm SH}$), the amplifier thermal noise ($n_{\rm AMP}$), and the second-stage comparator noise ($n_{\rm CMP2}$). With a target SNR around 78 dB, the quantization-limited SNR after NS and OSR of 8 is 84 dB. Moreover, $C_{\rm dac1} = 640$ fF can satisfy the requirement of the sampling kT/C noise, which is close to -86.5 dBFS with the contribution of the OSR. On the other hand, since the noise from the amplifier cannot be shaped in this design, we intentionally assign additional power to the OTA to suppress its noise to 3.6 nV^2. Benefitting from the proposed architecture, $n_{\rm CMP2}$ is both shaped by the first-order NTF and suppressed by the inter-stage gain. Therefore, it only contributes with a very small amount to the total noise power budget, as shown in Fig. 13.

Another concern about the design is the linearity, which is mainly affected by the capacitor mismatch of the

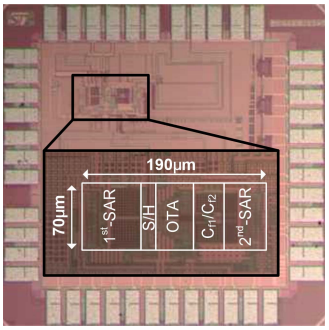


Fig. 14. Chip photograph.

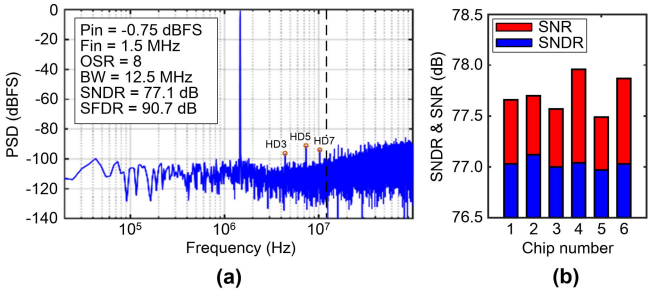


Fig. 15. (a) Measured ADC output spectrum and (b) measured results over six samples.

first-stage DAC. The mismatch error is calibrated in the foreground by estimating the actual DAC bit weight based on the least-mean-square (LMS) algorithm [19], [20]. This algorithm uses the error term between the output codes acquired with estimated bit weights and the standard codes without linearity error to update the estimated bit weights in the LMS iteration process. When the iteration finishes, the actual bit weights of the DAC capacitors are acquired and used to generate the calibrated output codes.

VI. Measurement Results

Fig. 14 shows the chip micro-photograph of the ADC prototype fabricated in 65-nm CMOS with an active area of 0.014 mm^2. The ADC has a BW that goes up to 12.5 MHz with 200 MS/s and OSR = 8. Fig. 15(a) shows the measured 32 768-point FFT spectrum with a 1.5-MHz, −0.75-dBFS sinusoidal input signal, with the prototype reaching the peak SNDR and a spurious-free DR (SFDR) of 77.1 dB and 90.7 dB, respectively. The remaining harmonics appear in the spectrum are mainly due to the limited calibration accuracy. We measured six samples with the same testing setup, leading to the results shown in Fig. 15(b), which confirms that they have a stable SNR and SNDR with only a small variation range of less than 1 dB. Under a supply voltage of 1.2 V, the ADC consumes 4.5 mW, where the first-stage SAR, second-stage SAR, MDAC, and clock generating block account for 13%, 7%, 73%, and 7% of the total power consumption. Although the MDAC with closed-loop amplification consumes a significant amount of power, it allows our design to avoid the inter-stage gain calibration. Due to the reutilization of the MDAC with high-energy efficiency, the ADC achieves an

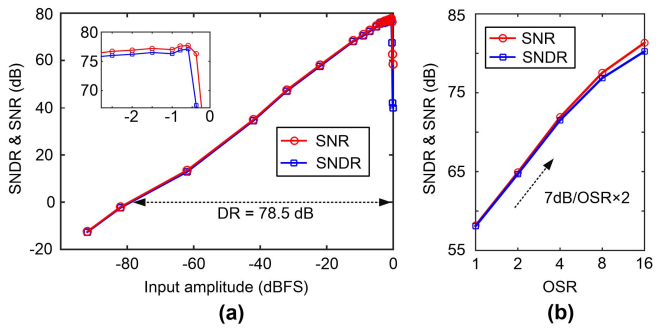


Fig. 16. Measured SNR and SNDR versus (a) input amplitude and (b) OSR.

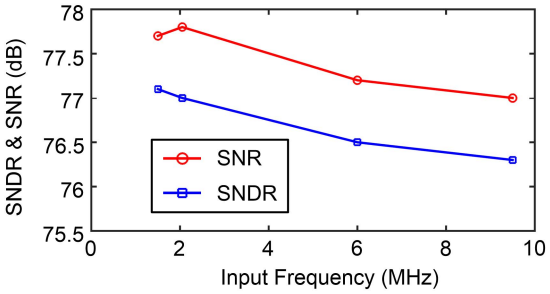


Fig. 17. Measured SNR and SNDR versus input frequency.

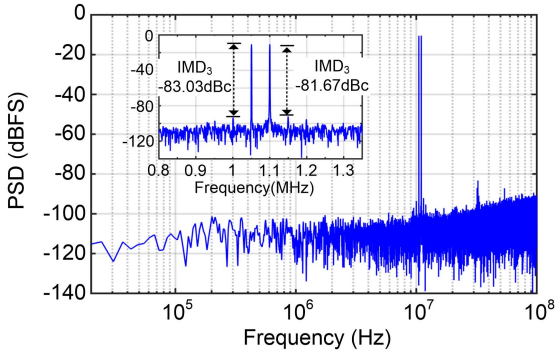


Fig. 18. Measured two-tone output spectrum.

FoMs of 171.5 dB. Fig. 16(a) shows the measured SNR and SNDR versus input amplitude, showing that the DR is 78.5 dB. Fig. 16(b) shows the measured SNR and SNDR versus OSR. Due to the noise floor, the SNR increases about 7 dB when the OSR doubles (with small OSRs), thus indicating a first-order NTF in our prototype. Fig. 17 shows the measured SNR and SNDR versus input frequency. The SNDR is above 76 dB when the input frequency increases. Fig. 18 shows the FFT spectrum of the two-tone test. The two tones are 10.5- and 11-MHz sine waves with −10-dBFS amplitude. They are close to the BW of the ADC. The measured IMD3 is −83.03 and −81.67 dBc, respectively.

Table I summarizes the performance of the ADC and compares it with the state of the arts. Our design achieves the highest BW among the single-channel NS SAR ADCs with an SNDR > 70 dB, demonstrating the effectiveness of the proposed SAR-assisted NS pipeline architecture on the enhancement of the ADC's speed at high resolution.

TABLE I
PERFORMANCE COMPARISON

Specifications	Fredenburg, JSSC'12 [3]	Liu, ISSCC'17 [6]	Li, JSSC'18 [7]	Lin, VLSI'16 [9]	Lin, ISSCC'19 [21]	Lim, JSSC'15 [10]	Gandara, ASSCC'17 [14]	This work
Architecture	NS SAR	NS SAR	NS SAR	PNS SAR	PNS SAR	SAR Pipeline	SAR Pipeline	NS Pipeline
Technology (nm)	65	28	40	14	14	65	130	**65**
Supply (V)	1.2	1	1.1	1	0.9	1.2	1.2	**1.2**
Fs (MS/s)	90	132	10	300	320	50	10	**200**
BW (MHz)	11	5	0.625	25	40	25	5	**12.5**
SNDR (dB)	62	79.7	79	69.1	66.6	70.9	67.3	**77.1**
Power (mW)	0.806	0.46	0.084	2.4	1.25	1.0	0.17	**4.5**
FoMs (dB)	163.0	180.1	178.0	169.0	171.7	174.9	172.0	**171.5**
Area (mm^2)	0.03	0.0049	0.024	0.0043	0.0021	0.054	0.14	**0.014**

VII. CONCLUSION

This article discussed in detail the speed and resolution constraints of prior NS SAR ADCs and presented a SAR-assisted NS pipeline hybrid architecture. The proposed NS pipeline structure enables a parallel working sequence and the ALC technique avoids extra residue feedback and integration phases, which enhances the conversion speed. The noise requirement in the comparator and loop filter are relaxed due to both the EF NS structure and the inter-stage gain from the MDAC. Measurement results demonstrate that the OTA-based MDAC is of high stability without gain calibration. The ADC prototype draws 4.5-mV power from a 1.2-V supply at a BW of 12.5 MHz and exhibits 77.1-dB SNDR with only OSR of 8.

REFERENCES

[1] C.-C. Liu, C.-H. Kuo, and Y.-Z. Lin, "A 10 bit 320 MS/s low-cost SAR ADC for IEEE 802.11ac applications in 20 nm CMOS," *IEEE J. SolidState Circuits*, vol. 50, no. 11, pp. 2645–2654, Nov. 2015.

[2] T. He, M. Ashburn, S. Ho, Y. Zhang, and G. Temes, "A 50 MHZ-BW continuous-time $\Delta\Sigma$ ADC with dynamic error correction achieving 79.8 dB SNDR and 95.2 dB SFDR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 230–232.

[3] J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

[4] Z. Chen, M. Miyahara, and A. Matsuzawa, "A 9.35-ENOB, 14.8 fJ/conv.-step fully-passive noise-shaping SAR ADC," in *Proc. Symp. VLSI Circuits*, Jun. 2015, pp. C64–C65.

[5] W. Guo, H. Zhuang, and N. Sun, "A 13 b-ENOB 173 dB-FoM 2^{nd}-order NS SAR ADC with passive integrators," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C236–C237.

[6] C.-C. Liu, and M.-C. Huang, "A 0.46 mW 5 MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 466–467.

[7] S. Li, B. Qiao, M. Gandara, D. Z. Pan, and N. Sun, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3484–3496, Dec. 2018.

[8] A. Sanyal and N. Sun, "A 18.5-fJ/step VCO-based 0–1 MASH $\Delta\Sigma$ ADC with digital background calibration," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. 1–2.

[9] Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, R.-X. Chu, and C.-H. Lu, "A 2.4-mW 25-MHz BW 300-MS/s passive noise shaping SAR ADC with noise quantizer technique in 14-nm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2016, pp. C234–C235.

[10] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2901–2911, Dec. 2015.

[11] T. Miki *et al.*, "A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC with SNR and SFDR enhancement techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1372–1381, Jun. 2015.

[12] K. S. Kim, J. Kim, and S. H. Cho, "nth-order multi-bit $\Sigma\Delta$ ADC using SAR quantiser," *Electron. Lett.*, vol. 46, no. 19, pp. 1315–1316, Sep. 2010.

[13] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[14] M. Gandara, P. Gulati, and N. Sun, "A 172 dB-FoM pipelined SAR ADC using a regenerative amplifier with self-timed gain control and mixed-signal background calibration," in *Proc. A-SSCC*, Nov. 2017, pp. 297–300.

[15] B. Vaz *et al.*, "A 13 b 4 GS/s digitally assisted dynamic 3-stage asynchronous pipelined-SAR ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 276–277.

[16] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

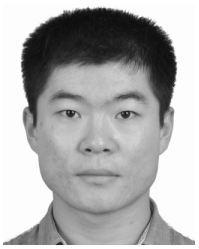
[17] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," in *Proc. IEEE A-SSCC*, Nov. 2008, pp. 269–272.

[18] J. Zhong, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "Thermal and reference noise analysis of time-interleaving SAR and partial-interleaving pipelined-SAR ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2196–2206, Sep. 2015.

[19] H. Garvik, C. Wulff, and T. Ytterdal, "An 11.0 bit ENOB, 9.8 fJ/conv.-step noise-shaping SAR ADC calibrated by least squares estimation," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr./May 2017, pp. 1–4.

[20] B. Catteau, P. Rombouts, J. Raman, and L. Weyten, "An on-line calibration technique for mismatch errors in high-speed DACs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 1873–1883, Aug. 2008.

[21] Y.-Z. Lin, C.-Y. Lin, S.-C. Tsou, C.-H. Tsai, and C.-H. Lu, "A 40 MHz-BW 320 MS/s passive noise-shaping SAR ADC with passive signal-residue summation in 14 nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 330–332.



Yan Song (M'18) received the B.Sc. and Ph.D. degrees in microelectronics from Xi'an Jiaotong University (XJTU), Xi'an, China, in 2011 and 2018, respectively.

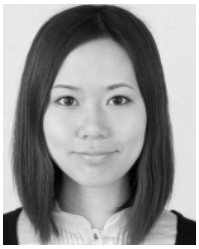
He is currently a Post-Doctoral Researcher with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China. His research interests include the successive approximation register (SAR) and SAR hybrid analog-to-digital converters (ADCs), offset and mismatch calibration techniques.

Dr. Song was a recipient of the XJTU Excellent Graduate Students Award in 2014 and the Lam Research Best Paper Award and the Best Paper Scholarship Award in 2017 from XJTU, and the 2018 Symposium on VLSI Circuit Student Travel Grant Award (STGA).

Chi-Hang Chan (S'12–M'15) was born in Macao, China, in 1985. He received the B.S. degree in electrical engineering from the University of Washington, Seattle, WA, USA, in 2008, and the M.S. and Ph.D. degrees from the University of Macau, Macao, in 2012 and 2015, respectively.

He was an Intern with Chipidea Microelectronics (Currently Synopsys), Macao, during his undergraduate studies. He is currently an Assistant Professor with the University of Macau. His research interests include Nyquist analog-to-digital converter (ADC) and mixed-signal circuits. His research mainly focuses on the comparator offset calibration, flash, and multi-bit successive approximation register (SAR) ADC.

Dr. Chan was a recipient of the Chipidea Microelectronics Prize and Macau Science and Technology Development Fund (FDCT) Postgraduates Award (Master Level) in 2012 and 2011, respectively, the Macau FDCT Award for Technological Invention (Second Class), the Macao Scientific and Technological Research and Development for Postgraduates Award (Ph.D. Level) in 2014 for outstanding Academic and Research achievements in Microelectronics, and the 2015 Solid-State-Circuit-Society (SSCS) Pre-Doctoral Achievement Award. He was a co-recipient of the 2011 ISSCC Silk Road Award and the Student Design Contest Award in A-SSCC 2011.



Yan Zhu (S'10–M'12–SM'19) received the B.Sc. degree in electrical engineering and automation from Shanghai University, Shanghai, China, in 2006, and the M.Sc. and Ph.D. degrees in electrical and electronics engineering from the University of Macau, Macao, China, in 2009 and 2011, respectively.

She is currently an Associate Professor with the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau. She has involved in more than 15 research projects for low-power and high-performance analog-to-digital converter (ADC). She has authored or coauthored more than 30 technical journals and conference articles in her field of interest. She holds four U.S. patents. Her research interests include low-power and wideband high-speed Nyquist A/D converters and digitally assisted data converter designs.

Dr. Zhu received the Chipidea Microelectronics Prize and Macao Scientific and Technological Research and Development for Postgraduates Award—Postgraduate Level in 2012 for Outstanding Academic and Research Achievements in Microelectronics and the Student Design Contest Award in A-SSCC 2011.

Rui P. Martins (M'88–SM'99–F'08) was born in April 1957. He received the bachelor's, master's, and Ph.D. degrees and the Habilitation degree (Full Professor) in electrical engineering and computer science from the Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), Universidade de Lisboa, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

Since October 1980, he has been with the Department of Electrical and Computer Engineering and the Instituto Superior Técnico, Universidade de Lisboa. Since 1992, he has been on leave from the Universidade de Lisboa and with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair Professor since August 2013. From 1994 to 1997, he was the Dean of the Faculty, FST, UM, where was the Vice-Rector (Research) from September 2008 to August 2018, has been a Vice-Rector since 1997, and has been the Vice-Rector (Global Affairs) since September 2018. In 2003, he created the Analog and Mixed-Signal VLSI Research Laboratory, UM. In January 2011, he elevated to the State Key Laboratory (SKLAB) of China (the first in Engineering in Macao), UM, where he was the Founding Director. From January 2009 to March 2019, he was the Founding Chair of UMTEC (UM company), supporting the incubation and creation in 2018 of *Digifluidic,* the first UM Spin-Off, whose CEO is an SKLAB Ph.D. graduate. He was also the Co-Founder of Synopsys-Macao, Macao, from 2001 to 2002. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and, in UM, has supervised (or cosupervised) 46 theses, Ph.D. (25), and masters (21). He has coauthored 7 books and 11 book chapters; 33 patents, USA (30) and Taiwan (3); 497 articles, in scientific journals (184) and in conference proceedings (313); and other 64 academic works, in a total of 612 publications.

Dr. Martins was a member of the IEEE CASS Fellow Evaluation Committee (2013, 2014, and 2018—Chair, and 2019). He was a recipient of the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He received two Macao Government decorations: the Medal of Professional Merit (Portuguese-1999) and the Honorary Title of Value (Chinese-2001). In July 2010, he was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia. He was the Founding Chair of the IEEE Macau Section from 2003 to 2005) and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair of the IEEE Asia–Pacific Conference on CAS (APCCAS 2008), the Vice-President (VP) Region 10 (Asia, Australia, and Pacific) from 2009 to 2011, and the VP-World Regional Activities and Membership of IEEE CASS from 2012 to 2013. He was the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014, and the IEEE CASS Nominations Committee from 2016 to 2017. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC 2016). He was the Vice President from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities (AULP). He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 2010 to2013. He was nominated as the Best Associate Editor from 2012 to 2013.