Uniform Quantization Theory-Based Linearity Calibration for Split Capacitive DAC in an SAR ADC

Jianwei Liu, Yan Zhu, Chi-Hang Chan, Sai-Weng Sin, Seng-Pan U, and Rui Paulo da Silva Martins

***Abstract*— This brief presents a uniform quantization theory (UQT)-based digital-to-analog converter (DAC) linearity calibration for a successive approximation register (SAR) analog-to-digital converter. According to the uniform quantization noise property, the nonlinearity due to the parasitics in an LSB array of the split-DAC structure is estimated and corrected in the digital domain. The calibration requires that the characteristic of the input signal must fulfill the prerogative of the quantization theory. The advantages lie in its low design complexity with no additional analog circuit modification. The proposed calibration is verified by both behavioral simulations and measured results in an SAR ADC. The measurements are based on a prototype implemented with large nonlinear split-DACs, which demonstrate that the UQT-based linearity calibration can effectively improve the Signal to Noise and Distortion (SNDR) from 56.9 to 63.3 dB at dc input with a sampling frequency of 120 MS/s.**

***Index Terms*— Background linearity calibration, split-digital-to-analog converter (DAC), successive approximation register (SAR) ADC, uniform quantization theory (UQT).**

I. Introduction

Successive approximation register (SAR) ADCs [1]–[7] become a rival to pipelined ADCs for moderate speed (10–100 MS/s) and medium- to high-resolution (10–14 bits) applications due to their simple architecture and highly digital-assisted operation, which benefits the most from CMOS technology downscaling. The SAR conversion relies on the digital-to-analog converter (DAC), comparator, and logic feedback to perform the binary-searched approximation. Since the SAR ADC does not require residue amplification, it offers superior power efficiency and achieves smaller die area, which is highly suitable for CMOS integration.

Binary-weighted [3], [5] and split [4], [6] capacitive arrays are two typical DAC structures widely used in SAR ADCs. The binary-weighted DAC achieves better conversion linearity, while its number of unit capacitors grows exponentially with the resolution that consumes a larger die area and increases the layout complexity, thus leading to larger routing parasitics. Consequently, the binary DAC is more commonly adopted in low-speed and high-resolution designs [3], [7]. For targeting high speed, the split-DAC can be employed [4], [6], as it can be built with much less number of unit capacitors than the binary-weighted, under the same total capacitance designed for kT/C noise, which originates less interconnection and overhead area. However, the split-DAC suffers from linearity degradation due to the mismatch series attenuation capacitor and top-plate parasitics in the LSB array.

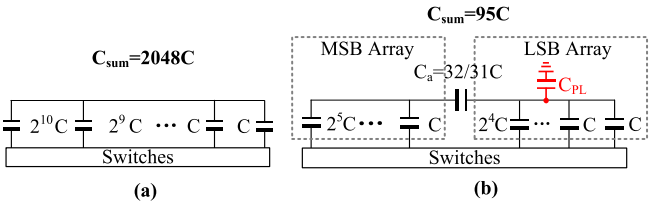

Fig. 1. (a) 11-bit binary-weighted DAC. (b) 11-bit (6 bit + 5 bit) split-DAC. C_{sum} should be equal to $95C + 32/31C$.

Recently, linearity calibration techniques [1], [2], [4] have been reported for the split-DAC, where the postprocessing of the errors are always performed in the digital domain drawing less design complexity. The perturbation-based calibration scheme uses a single-bit pseudorandom sequence injected to estimate the error [1], [2], but the additional signal injections increase the design complexity and trade the dynamic range for the calibration converging speed. The histogram-based calibration scheme [4] avoids additional signal injection, but it requires the input signal to be continuous at least in 64 codes at the detection range for the error estimation.

This brief proposes a digital calibration technique to correct the conversion nonlinearities due to the split-DAC in an SAR ADC. Based on the uniform quantization theory (UQT), the quantization process executed in the MSB and LSB subarrays is modeled as a coarse and fine quantizer, respectively, like a subranging ADC. The ratio mismatch between the MSB and the LSB array can be easily estimated according to the variance of the residue. The digital outputs are postprocessed according to the UQT calibration algorithm, which has no feedback loop to the ADC, thus relaxing the design effort. In addition, the calibration does not require any additional signal injection, as well as analog circuitries, and can be operated in the background. The calibration time is based on 1k data outputs, which is much less when compared with [1] and [2]. The proposed UQT calibration technique was verified in behavioral simulations and measured results of two 12-bit SAR ADCs containing different conversion nonlinearities.

II. Mismatch in Binary- and Split-DAC Array

The conversion nonlinearity in a binary-weighted DAC is mainly originated from the intrinsic capacitor mismatches, while for the split-DAC array, it is mainly caused by the top-plate parasitic capacitance in the LSB array that induces the mismatch in the attenuation ratio between the MSB and the LSB arrays [4]. Furthermore, with advanced switching [2], [6], only an 11-bit DAC is used for a 12-bit conversion, where the DAC capacitance is kT/C noise limited. Fig. 1 exhibits two types of DAC structures designed for 12-bit conversion, where the binary array contains a total of 2048 units,

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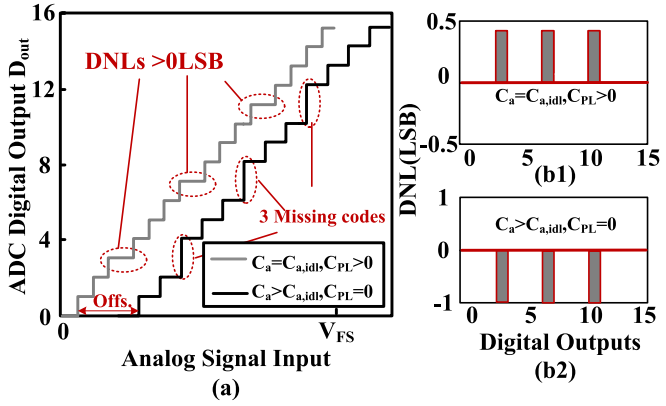

Fig. 2. (a) Output transfer characteristic of a 4-bit split-DAC. (b1) and (b2) Corresponding output code histogram of the 4-bit SAR ADC.

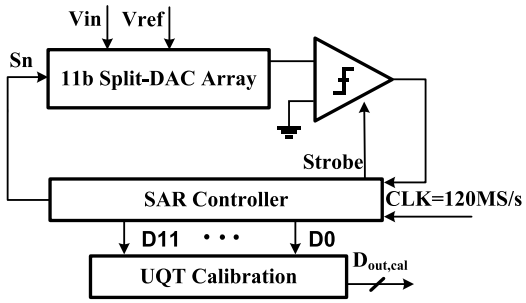

Fig. 3. Overall ADC architecture.

while the split array can be built with as few as 96 units. To satisfy 12-bit kT/C noise, the required total input capacitance is ~1.2 pF with 1.2 V_{p-p} full scale. Accordingly, the unit capacitance for the binary- and split-DAC is 0.6 and 19 fF, respectively. Since the unit capacitance in the split-DAC is increased by ~32 times, the unit element matching is improved by $\sqrt{32}$ times. However, it does not mean that the matching in the split-DAC is better, as the required unit capacitor matching ($\Delta C/C$) for binary- and split-DAC is 0.55% and 0.1%, respectively [8]. This $\sqrt{32}$ times improvement eventually cancels out, since the matching requirements of the unit in the bridge-DAC is also around $\sqrt{32}$ times more critical than the binary-DAC.

On the other hand, the linearity in the split-DAC is much worse, as the routing parasitic capacitance $C_{\rm PL}$ in the top-plate of the LSB array and the mismatch of the fractional value in the attenuating capacitor C_a cause a ratio mismatch between the LSB and MSB arrays. Fig. 2 shows the transfer characteristic of the 4-bit (2 bit + 2 bit) split-DAC with nonlinearities. If C_a is ideal and $C_{\rm PL}$ is larger than 0, the periodic gaps due to positive DNLs will occur. If C_a is larger than its ideal value and $C_{\rm PL}$ is 0, there will be periodically larger steps caused by missing codes at the DAC's output transfer curve. Ultimately, two cases lead to Differential nonlinearity (DNL) errors at the output of the ADC, as shown in Fig. 2(b1) and (b2).

III. Overall ADC Architecture

The proposed UQT calibration is adapted to a 12-bit SAR ADC architecture shown in Fig. 3. It consists of a split-DAC array, a comparator, an SAR controller, and a UQT calibration engine. The DAC array is used to sample the input signal and subtract the reference voltages with a binary-searched feedback. The comparator is a two-stage dynamic latch [9]. The SAR controller, including the bit register and switch drivers, performs $V_{\rm cm}$-based switching [6] for lower switching energy and better conversion linearity. In this split-DAC, a UQT calibration engine is implemented to fix the conversion nonlinearity in the digital domain, which is controlled

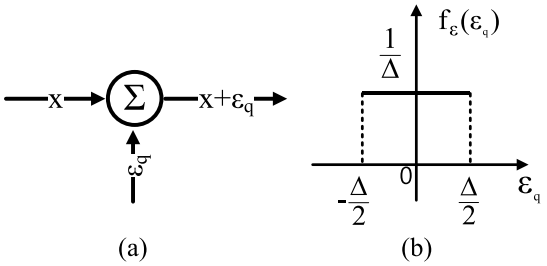

Fig. 4. (a) Model of quantizer. (b) Probability density function of quantization.

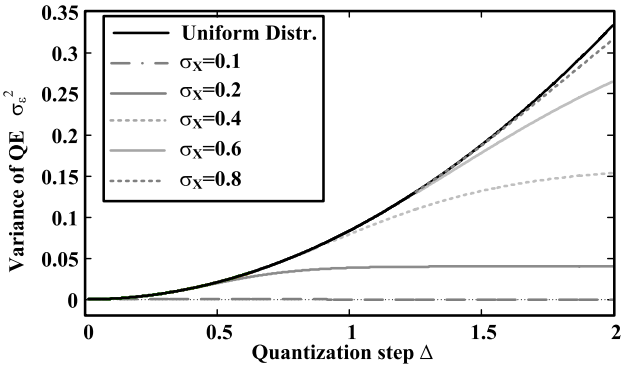

Fig. 5. Variance of the quantization error versus the quantization step over different values of σ_x of a Gaussian distributed analog input.

by the MATLAB running on a PC, with a controller that can easily be integrated in the Very-High-Speed Integrated Circuit Hardware Description Language. When the conversion is completed, the digital codes are employed in the calibration engine to estimate and correct the conversion error, where the calibration details are introduced next.

IV. Proposed UQT Calibration Scheme

A. Uniform Quantization Theory

The effect of uniform quantization is often modeled by an additive noise that is uniformly distributed and uncorrelated with the input signal [10], [11], as shown in Fig. 4. The input analog signal x is Gaussian distributed with variance σ_x^2, and ε_q is the quantization error, which has a variance σ_ε^2 of $\Delta^2/12$ (Δ is the minimum quantization step of the ADC). Important to note is the fact that this model does not always hold. A necessary and sufficient condition for quantization errors to be uniform and white is given in [10] and [11], and then, the variance of the quantization errors [11] is

$$\text{var}(\varepsilon_q) = \frac{\Delta^2}{12}\left[1 + \frac{12}{\pi^2}\sum_{k=1}^{\infty}\frac{1}{k^2}e^{-\frac{2(k\pi\sigma_x)^2}{\Delta^2}}\right]. \quad (1)$$

As the ratio σ_x/Δ increases, the quantization error becomes more uniformly distributed. This is true for many types of signal although (1) is drawn based on Gaussian distribution input. Fig. 5 shows the variance of the quantization error versus the quantization step, with different values of standard deviation σ_x of a Gaussian distribution input. The solid line shows the quantization error with uniform distribution. It can be deducted that the variance of the quantization error is closer to a uniform distribution when the quantization step is reduced. Consequently, a multibit quantizer is required to guarantee that the quantization errors are uniform and white under a Gaussian signal input with different variances. Moreover, if the variance of the input is large enough, and the quantization error is more likely to be uniformly distributed (the case of $\sigma_x = 0.8$ in Fig. 5).

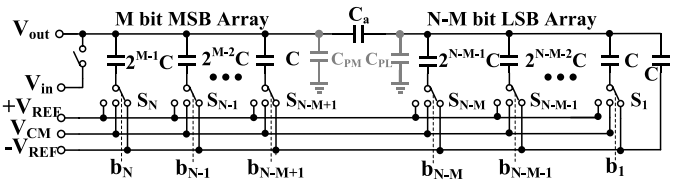

Fig. 6. N-bit split-DAC with M-bit MSB array and $N-M$ bit LSB array.

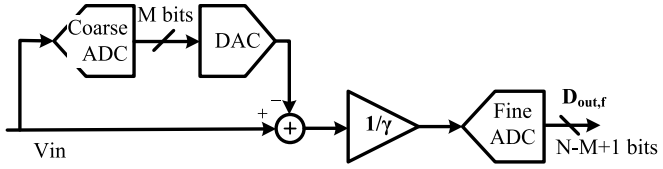

Fig. 7. Model of $N+1$ bits SAR ADC with split-DAC array.

B. Nonlinearity Analysis

The N bits split-array DAC with $V_{\rm cm}$-based switching [6] is shown in Fig. 6. The MSB and LSB arrays contain M bits and $(N-M)$ bits, respectively, which are separated by the attenuation capacitor C_a. $C_{\rm PM}$ and $C_{\rm PL}$ are the top-plate parasitic capacitors of the MSB and LSB arrays, respectively. After the conversion, the input signal $V_{\rm in}$ is reserved as a digital code, which can be expressed as

$$V_{\rm in} = \alpha \left[\sum_{i=N-M+1}^{N} 2^i b_i + \gamma \times \sum_{i=0}^{N-M} 2^i b_i \right] \tag{2}$$

where b_i is the ith bit of the digital code. The α causes an overall gain error that is not problematic for the linearity performance [8]. Therefore, it will be ignored in the following discussion. However, γ correlated with the LSBs is the only factor that causes the gain mismatch between the MSBs and the LSBs. The parameters α and γ depend on the fraction value of the attenuation capacitor and the DAC's top-plate parasitics, as depicted in (3) and (4), shown at the bottom of this page. Ideally, there is no top-plate parasitic capacitance and $C_a = (2^{N-M}/(2^{N-M}-1))C$, leading to $\gamma = 1$ and no error will be generated. While γ is not equal to 1 in practice due to existing parasitics $C_{\rm PM}$ and $C_{\rm PL}$ as well as the mismatch of the fractional value of C_a, the nonlinearities occur at the DAC output.

C. Proposed UQT Calibration

According to the above analysis from (2), the $N+1$ bits SAR ADC built with an N bits split-DAC can be modeled as a two-step subranging ADC, as shown in Fig. 7. The coarse M bit and the fine $(N-M+1)$ bits represent the number of bits in the MSB and LSB arrays, respectively. As a ratio mismatch of γ existing between two steps conversion, the output of the fine $(N-M+1)$ bits $D_{{\rm out},f}$ is considered as the digital residue of the coarse M-bit ADC output multiplied by a gain $1/\gamma$. Thus, the expected quantized residual of the coarse ADC ($D_{{\rm resi},c}$) is

$$D_{{\rm resi},c} = \gamma \times D_{{\rm out},f}. \tag{5}$$

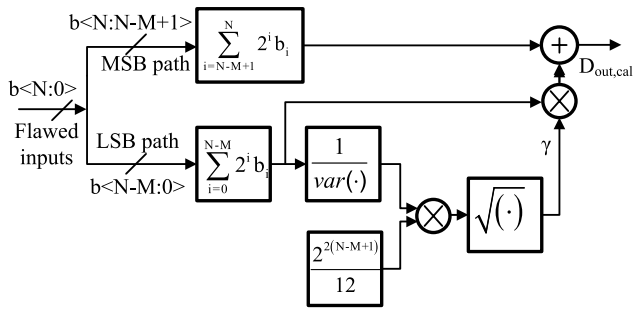

Fig. 8. Block diagram of the calibration based on UQT.

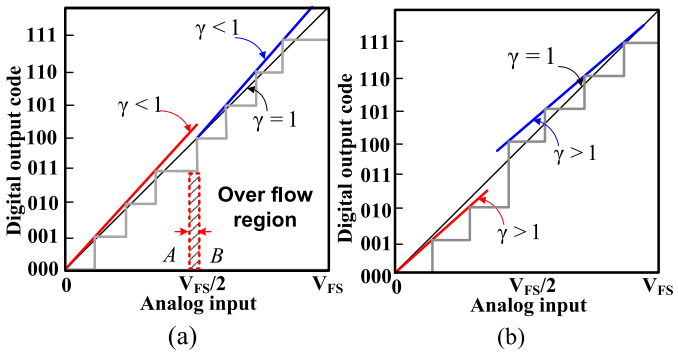

Fig. 9. Transfer curve of 3-bit ADC. (a) $\gamma < 1$. (b) $\gamma > 1$.

The variance of $D_{{\rm resi},c}$ should be approximated to the ideal quantization noise power $\Delta_c^2/12$ of the coarse ADC (Δ_c is $2^{N-M+1}\Delta$ approximately representing the quantization step of the coarse ADC). According to the UQT, the following equation can be obtained:

$$\frac{\Delta_c^2}{12} = {\rm var}[\Delta \cdot D_{{\rm resi},c}]. \tag{6}$$

From (5) and (6), the estimated gain γ can be derived as

$$\gamma = \sqrt{\frac{2^{2(N-M+1)}/12}{{\rm var}[D_{{\rm out},f}]}}. \tag{7}$$

The block diagram of the proposed calibration based on UQT is shown in Fig. 8. The attenuation capacitance C_a must be implemented larger than its ideal value to guarantee $\gamma > 1$. Otherwise, overflow will occur in the LSBs, which will affect the estimation of γ. In order to illustrate this, a transfer curve of a 3-bit ADC example with $M = 1$ is shown in Fig. 9. When $\gamma < 1$, the analog input from A to B would be on overflow. The analog inputs from A to B have the same digital output representation, which cannot be differentiated in the digital domain and causes positive DNL. When $\gamma > 1$, missing codes occur due to gain, but the output codes are uniformly distributed. Therefore, the calibration can identify the actual value of γ, and then compensate it in the digital domain.

D. Behavioral Simulation Verification

To verify the UQT calibration method, behavioral simulations were performed, which modeled the conversion nonlinearities in

$$\alpha = \frac{2^M C}{2^M C - C + C_{\rm PM} + \frac{C_a(C_{\rm PL}+2^{N-M}C)}{C_a+C_{\rm PL}+2^{N-M}C}} \tag{3}$$

$$\gamma = \frac{2^{N-M}C \cdot C_a \cdot \left(2^M C - C + C_{\rm PM} + \frac{C_a(C_{\rm PL}+2^{N-M}C)}{C_a+C_{\rm PL}+2^{N-M}C}\right)}{(C_a + C_{\rm PM} + 2^M C - C)(2^{N-M}C + C_{\rm PL}) + C_a(C_{\rm PM} + 2^M C - C)} \tag{4}$$

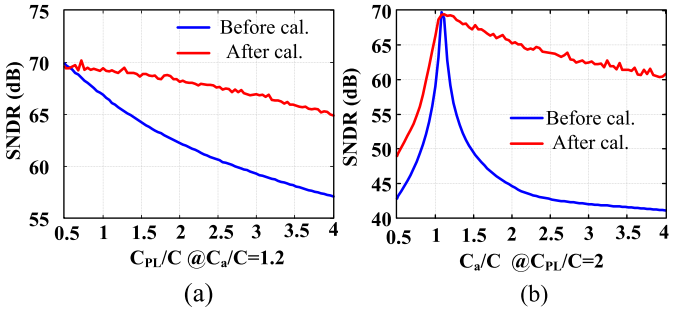

Fig. 10. Simulated SNDR of (a) C_{PL} and (b) C_a with and without the calibration block based on UQT.

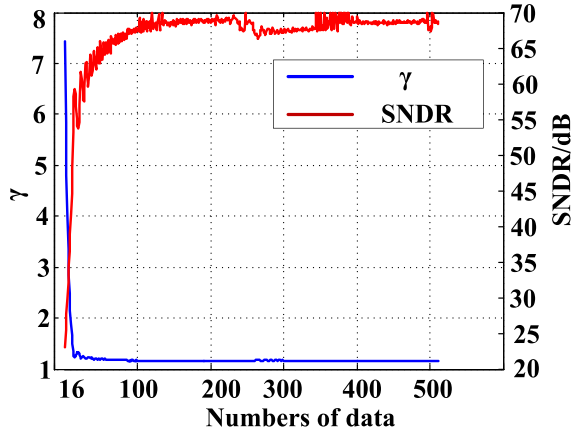

Fig. 11. Numbers of data versus the estimated value of γ and SNDR.

a 12-bit ADC. An 11-bit (6 bit + 5 bit) split-DAC has been used. The standard deviation of the unit capacitor and the comparator noise voltage is the Gaussian random variables with $\sigma_{(\Delta C/C)} = 0.1\%$ and 100 $\mu \mathrm{V_{rms}}$, respectively. In Fig. 10(a), the attenuation capacitor is set as $1.2C$ (16% larger than its ideal value), and the top-plate parasitic capacitance varies from $0.5C$ to $4C$. The SNDR plots from 100 times Monte Carlo simulations before and after calibration are exhibited in Fig. 10(a). The corresponding gain factor γ, which is estimated by the UQT calibration scheme, can compensate the nonlinearities caused by the variation of the parasitics C_{PL}. Similarly, the SNDR before and after calibration versus the attenuation capacitor C_a is shown in Fig. 10(b), where the parasitic C_{PL} is set as $2C$ (6% larger than the total LSB DAC). The calibration is effective once the C_a is larger than its ideal value, which implies $\gamma > 1$. Fig. 11 shows the convergence speed versus the SNDR of the UQT calibration method, where the ADC achieves near 70-dB SNDR based on 500 data outputs demonstrating the fast convergence of the proposed scheme.

E. Input Constraints of the Calibration Method

Since the proposed method utilized the quantization theory for calibration, it is important to make $D_{\mathrm{out},f}$ to be uniformly distributed in order to accurately estimate the internal gain of the split DAC. However, it will just imply a weaker sufficient condition which is also necessary for the quantization theorem, as shown in [11], and there it might be possible to have some cases where $D_{\mathrm{out},f}$ is not an uniform distribution. For instance, when the input signal is just 3.5% of the full swing (V_{FS}) for a sine wave input [Fig. 12(a)], $D_{\mathrm{out},f}$ is not an uniform distribution, as shown in Fig. 12(b). The estimated internal gain γ is 0.91 and the SNDR is only 53 dB after calibration, which is worse than the noncalibrated SNDR (57 dB), because the

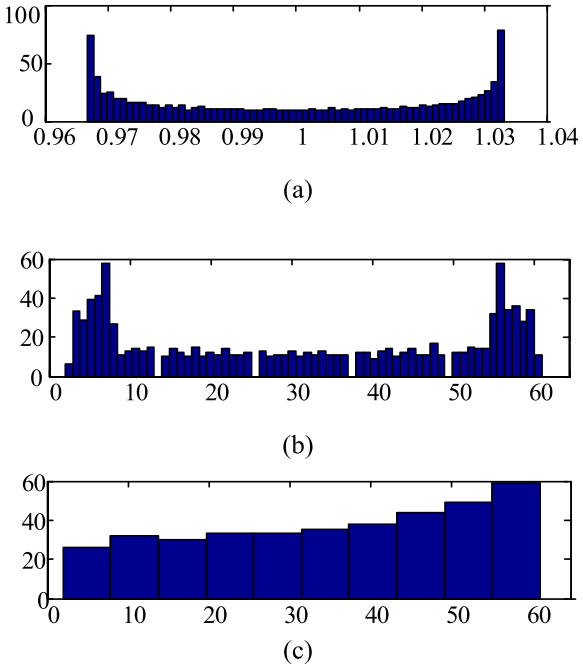

Fig. 12. Histograms of (a) input signal, (b) $D_{\mathrm{out},f}$, and (c) $D_{\mathrm{out},f}$ when the input is 3.5% of the full swing.

variance of the input signal is too small and $D_{\mathrm{out},f}$ is not uniformly distributed.

To improve the accuracy of the estimation, the algorithm can operate over a small input range instead of monitoring the whole V_{FS}. The histogram of $D_{\mathrm{out},f}$ at MSB = 100 000 is shown in Fig. 12(c), which is closer to a uniform distribution than that of Fig. 12(b). Then, the estimated gain γ is 1.06 and the SNDR is improved to 65.5 dB which is only 3 dB off from the ideal case.

The calibration efficiency of the algorithm becomes worse as the input swing drops less than 3.5% of V_{FS}. However, the main objective is to calibrate the internal gain of the DAC without extra signal injection and analog circuit modifications but with a relaxed signal requirement. Table I shows the comparison of different calibration methods. The major advancements of the proposed calibration method are: being able to work with a small swing, as well as not requiring a certain range of continuous input.

On the other hand, the calibration accuracy is also affected by the reference noise. We have added the reference noise in our MATLAB mode based on a similar scheme as in [12]. When the rms noise from the reference is <2.5 LSBs, the SNDR before and after calibration is 55 and 56 dB, respectively. While the SNDR with no DAC mismatch is also close to 56 dB. However, when the rms of the noise from the reference is >2.5 LSBs, the calibration becomes not effective (in this case). As the noise is already large enough to cover the error due to mismatch (in the current case, as the mismatch error causes the SNDR drop to 55 dB, but with >2.5 LSBs rms noise at the reference, the SNDR drops below 55 dB), the calibration is not able to improve the SNDR as the ADC's performance is limited by the reference noise.

V. Measurement Results

The proposed UQT calibration is verified in a 12-bit SAR ADC fabricated in a 1P7M 65-nm CMOS process with Metal-Oxide-Metal capacitors. The ADC is built with an 11-bit (6 bit + 5 bit) split-DAC containing different conversion nonlinearities. Fig. 13 shows the die photograph of the ADC, where the active area is 0.042 mm^2.

TABLE I
COMPARISON OF DIFFERENT CALIBRATION METHODS

12-bit SAR ADCs:	[1]	[2]	[4]	This work
Sampling Rate (MS/s)	45	50	120	120
SNDR (dB)	68.3	66.5	64.3	63.3
Power (mW)	2.8	3.3	3.2	3.2
FOM_{Walden} (fJ/conv-step)	36	45	28	28
Input signal limitation	No	Large input amplitude	Continuous at least in 64 codes at detection range	Amplitude= 3.5% of Full swing (SNDR drops 3dB)
Calibrated error type	LSB error	Internal gain error	Internal gain error	Internal gain error
Analog circuit modification	Yes	No	No	No
Signal injection	Yes	Yes	No	No

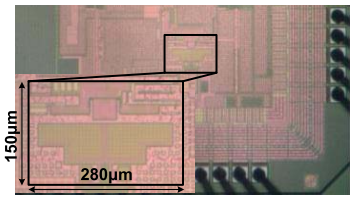

Fig. 13. Die chip photograph of the SAR ADC.

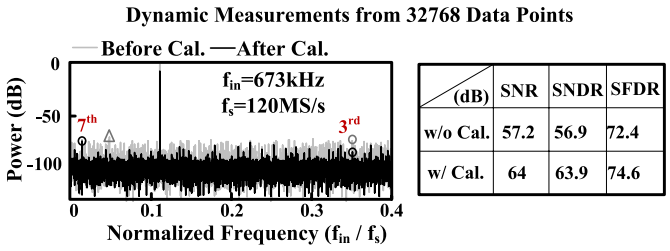

Fig. 14. Measured FFT of the digital output without and with calibration at low-frequency input (decimated by 25).

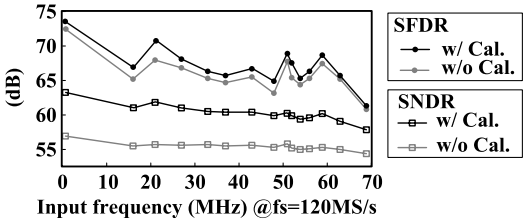

Fig. 15. Measured dynamic performance.

The analog power consumption is 0.8 mW and the digital power, including the SAR logic and the clock generator, is 2.4 mW. The total power consumption is 3.2 mW at 120 MS/s from 1.2 V supply. The digital outputs are postprocessed according to the UQT calibration algorithm. During the measurement, an input with $f_{\text{in}} = 673$ kHz and $V_{\text{FS}} = 2.4$ V is applied. The digital gate count of the calibration algorithm is ~4k and the estimated P&R area is 0.1 mm^2 with the operating power of 2.3 mW at 120 MS/s.

The SAR ADC implements a C_a of 27 fF guaranteeing a 30% correction range of parasitics. The SNDR from postlayout simulation results is 56 dB. Fig. 14 shows the measured fast Fourier transforms (FFTs) at 673 kHz with a conversion rate of 120 MS/s. Before calibration, the measured SNDR is 56.9 dB (close to the simulation). The ratio mismatch causes a brunch of spurs spreading among the whole spectrum, as well as the rise of the third harmonic that degrades the SNR and the SFDR to 57.2 and 72.4 dB, respectively.

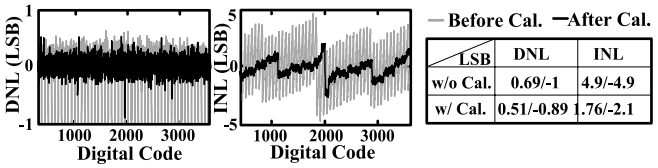

Fig. 16. Measured static performance of the SAR ADC without and with calibration.

Once the calibration is active, the spurs are removed. Therefore, the SNR and the SNDR are both improved by ~6.8 dB. Fig. 15 shows the measured dynamic performance. The SNDR and the SFDR at the Nyquist input are 60.2 and 68.7 dB, respectively.

The measured static performances with and without the UQT calibration are shown in Fig. 16. From the observation, before calibration, the DNL contains a large number of missing codes. When the calibration is active, the systematic comb-like pattern is removed, and both the DNL and the Integral nonlinearity are improved.

VI. CONCLUSION

This brief proposes a UQT-based calibration to correct the conversion nonlinearity due to the utilization of a split-DAC in SAR ADCs. The calibration is performed in the digital domain and can significantly improve both static and dynamic performances of the converter caused by internal gain in the split-DAC. Moreover, the scheme does not require extra signals injection or additional changes in the analog circuit. The solution is verified in a real chip design to demonstrate its calibration sensitivity and effectiveness over across-chip-variations and capacitor mismatches.

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