A CMOS Delta-Sigma PLL Transmitter with Efficient Modulation Bandwidth Calibration

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***Abstract*—A delta-sigma ($\Delta\Sigma$) phase locked loop (PLL) transmitter with an efficient modulation bandwidth calibration technique is proposed in this paper. With the proposed technique, the digital-analog mismatch between digital pre-emphasis filter and PLL is calibrated. The loop filter RC variation is tracked in the first place, and then the variation of the loop gain is calibrated by sensing the magnitude differences of the modulator between DC and ten times of the loop bandwidth. The proposed transmitter has been implemented in 0.18-μm CMOS technology for GSM/GPRS application. Measurement results show that the maximum RMS phase error of the proposed transmitter is 0.8°. In addition, the measured calibration accuracies for RC and loop gain variations are 0.5% and 0.8%, respectively. By reusing the PLL locking time, 18-μs calibration time is achieved. Moreover, most parts of the calibration circuitries can be shared with the receiver chain, reducing the circuit complexity overhead.**

***Index Terms*—Delta-sigma phase locked loop (PLL), modulation bandwidth calibration, transmitters.**

I. Introduction

TRANSMITTER topologies have been extensively reported these years, including direct up-conversion [1], offset phase-locked loop (PLL) [2], and delta-sigma ($\Delta\Sigma$) PLL. Among these, $\Delta\Sigma$ PLL topology [3]–[10] has been widely used due to its low noise, low power consumption and reduced complexity.

However, due to the low-pass characteristic of the PLL, the maximum achievable data rate of this transmitter is limited [3]. When the loop bandwidth is smaller than the modulation bandwidth, the modulation accuracy is deteriorated because of the signal spectrum shrinkage. To prevent this degradation, wideband PLL techniques have been adopted [11], [12]. Nevertheless, this strategy might not be suitable for some applications with stringent noise requirements. For example, for global system for mobile communication (GSM), the 400-kHz offset noise level requirement will be violated if the PLL's bandwidth is larger than 100 kHz [8]. Hence, with respect to a 270.83-kHz transmitted modulation bandwidth of GSM [13], compensation is needed to extend the modulation bandwidth beyond the PLL loop bandwidth without degrading the noise performance. Similar circumstances can be found in many other applications such as WiMAX/WLAN, Zigbee, Bluetooth, and WSN. In these applications, even when the modulation bandwidths are broaden to several MHz, the PLL bandwidths are typically restricted to be around 100 kHz [14]–[17].

There are two ways of extending the modulation bandwidth: two-point modulation and one-point $\Delta\Sigma$ modulation. Two-point modulation technique [4]–[6] circumvents the bandwidth limitation by splitting the modulated signal into two modulation paths: one from the voltage-controlled oscillator (VCO) and the other from the $\Delta\Sigma$ modulator. To prevent distortions, timing and gain matching between these two modulation paths are strictly required. Moreover, the dynamic range and linearity at the VCO control port is crucial for high modulation accuracy [6]. As such, the design difficulty of two-point modulation is increased.

As for one-point $\Delta\Sigma$ modulation, the low-pass characteristic of the PLL is compensated by cascading a digital pre-emphasis filter, whose transfer function is designed to be inverse to that of the PLL. However, under process, voltage, and temperature (PVT) variations, mismatch between the digital filter and the analog PLL will lead to degraded modulation accuracy. Hence, several techniques have been proposed to tackle this digital-analog mismatch [7]–[10].

In [7], a scalable charge pump current (I_{cp}) was employed to compensate the loop gain error. Based on an over-damped, second-order loop filter PLL structure approximation, the PLL bandwidth was proportional to the product of loop resistance, I_{cp} and VCO sensitivity (K_v) [18]. Once I_{cp} was set inversely proportional to the loop resistance, the loop gain error can be compensated by sensing the K_v error and setting the scalable I_{cp} accordingly. However, the application of this technique might be limited, as a third-order loop filter is normally required for more spurs and noise filtering at higher offset frequency [19].

Another technique for digital-analog mismatch calibration was reported in [8], where the loop gain error was detected by double-integrating the transient signal of PLL during a step response. For the loop filter RC variation, they were calibrated as a pseudo loop gain error. However, this pseudo approximation was difficult to ensure a flat modulation magnitude-frequency response within the modulation bandwidth, which leads to a large phase error. Moreover, a $\pm 2\%$ resolution of the scalable I_{cp} was required, increasing the design difficulty in a modern CMOS technology.

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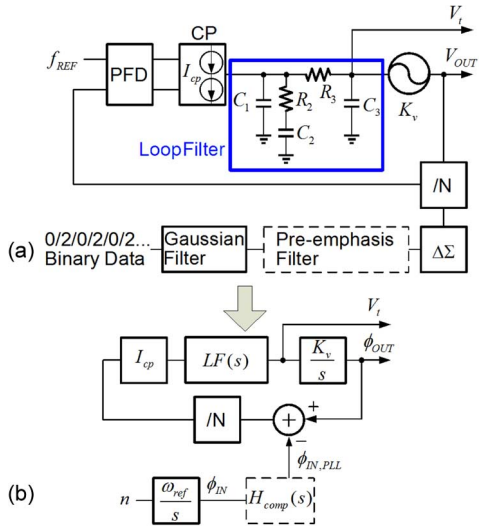

Fig. 1. (a) Block diagram of one-point ΔΣ PLL transmitter with a 3rd order loop filter. (b) Linear model of the ΔΣ PLL transmitter.

In [9], to detect the loop gain error, a 135.4-kHz calibration tone was applied to the GMSK modulator. As a result, a modulation index can be detected on VCO output. By comparing this index with its theoretical value from a look-up-table (LUT), a pre-distortion factor was generated for the compensation. Yet due to the low frequency calibration tone, a 43-μs calibration time was required for accurate index detection. This calibration time is too long for a frequency hopping system, where the stringent timing requirements make a short calibration time compulsory [13].

In view of the need to support a third-order loop filter, with short calibration time, high accuracy, and low circuit complexity, an efficient modulation bandwidth calibration technique for a ΔΣ PLL transmitter topology is proposed in this work. This calibration technique has been applied to a GSM/GPRS transmitter. Section II illustrates the theory of the proposed modulation bandwidth calibration technique. The circuit implementations of the ΔΣ PLL transmitter with the proposed calibration scheme are described in Section III. Section IV gives the discussion on calibration accuracy. Finally, Section V presents the measurement results and conclusion is drawn in Section VI.

II. Modulation Bandwidth Calibration Theory

A. Impact of Loop Gain and RC Variations on RMS Phase Error

Fig. 1(a) shows the block diagram of a one-point ΔΣ PLL transmitter, which consists of phase-frequency detector (PFD), charge pump (CP), loop filter, VCO and divide-by-N divider. The Gaussian-filtered data, modulated by the ΔΣ modulator, is used to control the division ratio of the divider. With this prototype, VCO outputs a GMSK modulated signal when receiving binary data.

The linear model of this one-point ΔΣ PLL transmitter is presented in Fig. 1(b). When a type-II, third-order loop filter is employed, the close-loop transfer function of the transmitter (from $\varphi_{IN,PLL}$ to φ_{OUT}) can be expressed as

$$H_o(s) = \frac{K(1+T_2 s)}{A_2 s^4 + A_1 s^3 + A_0 s^2 + K(1+T_2 s)} \tag{1}$$

where

$$\begin{aligned} A_2 &= C_1C_2C_3R_2R_3 \\ A_1 &= C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3 \\ A_0 &= C_1 + C_2 + C_3 \\ T_2 &= C_2R_2 \\ K &= \frac{I_{cp}K_v}{N} \end{aligned} \tag{2}$$

$A_2 - A_0$ and T_2 are loop-filter-related coefficients, I_{cp} is CP current, and K_v represents VCO sensitivity.

To compensate the low-pass characteristic of $H_o(s)$, the transmitted data needs to be pre-emphasized by a digital filter (shown as the dashed box in Fig. 1(a)). As discussed above, the transfer function of this filter is designed to be the inverse of $H_o(s)$. For more convenient analysis on the digital-analog mismatch, this discrete digital pre-emphasis filter is replaced by its equivalent continuous-time model. This equivalence proves to be valid when the sampling frequency is ten times beyond its bandwidth [9], [19]. The error caused by the Z-to-S approximation will be discussed in Section III-A. Hence, the transfer function of the pre-emphasis filter is given by

$$H_{comp}(s) = \frac{A_{2d}s^4 + A_{1d}s^3 + A_{0d}s^2 + K_d(1+T_{2d}s)}{K_d(1+T_{2d}s)} \tag{3}$$

where $A_{2d}, A_{1d}, A_{0d}, T_{2d}$, and K_d are loop coefficients with the subscript d denoting digital. Combining (1) and (3), the modulation transfer function can be expressed as

$$\begin{aligned} H(s) &= H_o(s)H_{comp}(s) \\ &= \frac{\left[A_{2d}s^4 + A_{1d}s^3 + A_{0d}s^2 + K_d(1+T_{2d}s)\right]\left[K(1+T_2 s)\right]}{\left[A_2 s^4 + A_1 s^3 + A_0 s^2 + K(1+T_2 s)\right]\left[K_d(1+T_{2d}s)\right]} \end{aligned} \tag{4}$$

(4) can be simplified by assuming that all the resistors are α times, and all the capacitors are β times of their nominal values. This assumption is valid since the relative accuracies of both resistors and capacitors can be kept in the order of 10^{-3} to 10^{-4} if their layout is well matched in modern CMOS technologies [20], [21]. In this work, to improve layout matching, unsilicided poly resistors are interdigitatedly implemented in the PLL loop filter. In addition, the cross-coupled metal-insulator-metal (MIM) capacitors are placed in close proximity to each other.

For further substantiation, Monte Carlo (MC) simulations with 500 samples are conducted. The simulated ratios between two of the equally sized resistors (with the same type as used in the loop filter) across random mismatch variations are shown in Fig. 2(a). With the mean value of 1, a 169-ppm standard deviation σ is achieved. The ratio variation of these resistors, which is regarded as their relative variation, is calculated to be approximately 0.05% for 3σ. Similarly, as shown in Fig. 2(b), for two capacitors with equal sizes, the simulated standard deviation of their ratio is 32 ppm and 3σ relative variation is calculated to be 0.01%. Since the RC relative accuracies are much higher than their absolute accuracies (typically with more than $\pm 10\%$ variations), (2) can be simplified as

$$\begin{aligned} A_2 &= \alpha^2\beta^3 A_{2n} \\ A_1 &= \alpha\beta^2 A_{1n} \\ A_0 &= \beta A_{0n} \\ T_2 &= \alpha\beta T_{2n} \end{aligned} \tag{5}$$

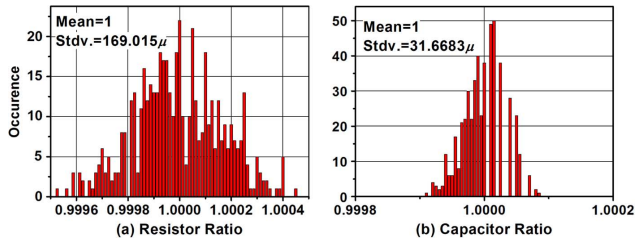

Fig. 2. Monte Carlo simulations on (a) resistor and (b) capacitor ratios.

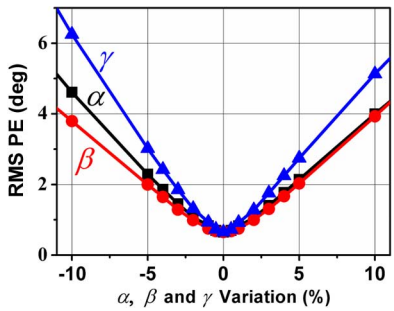

Fig. 3. Simulated RMS phase error (PE) φ_{RMS} under α, β, and γ variation.

The subscript n denotes the nominal values. In addition, K is assumed to be γ times of its nominal value, i.e.,

$$K = \gamma K_n \tag{6}$$

Substituting (5) and (6) into (4) yields

$$H(s) = \frac{\gamma K_n(1+\alpha\beta T_{2n}s)}{K_d(1+T_{2d}s)} \cdot \frac{A_{2d}s^4 + A_{1d}s^3 + A_{0d}s^2 + K_d(1+T_{2d}s)}{\alpha^2\beta^3 A_{2n}s^4 + \alpha\beta^2 A_{1n}s^3 + \beta A_{0n}s^2 + \gamma K_n(1+\alpha\beta T_{2n}s)} \tag{7}$$

As can be seen from (7), if there is no digital-analog mismatch (i.e., α, β, and γ are all equal to 1), $H(s)$ will be flat within the modulation bandwidth. However, under the scenario of α, β, or γ variations, $H(s)$ would deviate from evenness and thus increase the phase error. To verify this effect, the simulated RMS phase error versus α, β, and γ variations are shown in Fig. 3. It can be found that the γ variation causes the largest RMS phase error degradation. Besides, the variations of α and β, representing the RC absolute variations, also contribute a significant part to RMS phase error. Based on the GSM standard [13], the specified RMS phase error should be kept less than 1 degree [8]. As a result, not only γ, but also α and β variations should be calibrated.

Moreover, on the basis of (7), the validity of (5) can be further verified by evaluating the RMS phase error with the RC relative variations. The resistor relative accuracy α_1, with its variation ranging from -0.05% to 0.05% (acquired in the above MC simulation), is applied to R_2 and R_3 as:

$$R_1 = \alpha R_{1n},\ R_2 = \alpha_1 \alpha R_{2n} \tag{8}$$

where the subscript n still represents the nominal values. Then the simulated RMS phase errors under different absolute resistor variations (0, 5%, and 10%, respectively) are given in Fig. 4. It can be seen that the RMS phase error degradation due to the relative variation of the resistors is less than 0.05%.

Similarly, based on the simulated capacitor relative variation, the capacitor relative accuracy β_1 (between C_1 and C_2) and

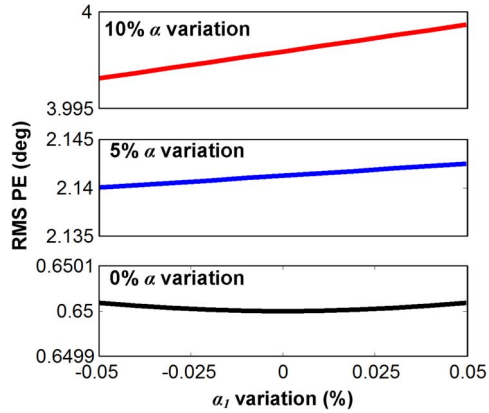

Fig. 4. Simulated RMS phase error with α_1 variation under α variations of 0, 5% and 10%, respectively.

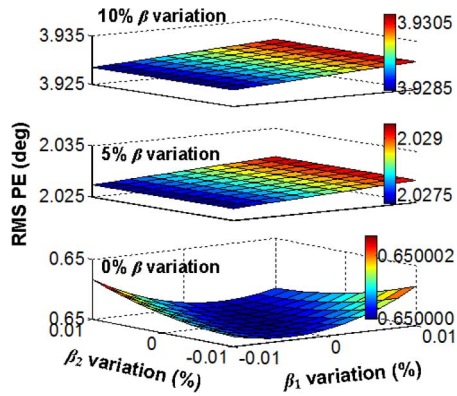

Fig. 5. Simulated RMS phase error with β_1, β_2 variations under β variations of 0, 5%, and 10%, respectively.

β_2 (between C_1 and C_3), with both variations from -0.01% to 0.01%, are applied to C_1, C_2, and C_3 as:

$$C_1 = \beta C_{1n},\ C_2 = \beta_1 \beta C_{2n},\ C_3 = \beta_2 \beta C_{3n} \tag{9}$$

The simulated RMS phase errors under different absolute capacitor variations ($\beta = 0$, 5% and 10%, respectively) are shown in Fig. 5, where the color-bars represent the range of the RMS phase error. It can be found that the RMS phase error degradation caused by capacitor relative variation is less than 0.02%.

Consequently, the calibration error caused by RC relative variations is negligible.

B. Proposed Modulation Bandwidth Calibration Technique

From (7), the RMS phase error caused by the digital-analog mismatch is theoretically eliminated if $H(j\omega) = 1(\omega \ll 2\pi \cdot f_{SYM})$. This only occurs when

$$\begin{aligned} A_{2d} &= (\alpha\beta)^2 A_{2n} \\ A_{1d} &= (\alpha\beta) A_{1n} \\ A_{0d} &= A_{0n} \\ T_{2d} &= (\alpha\beta) T_{2n} \end{aligned} \tag{10}$$

and

$$K_d = \frac{\gamma}{\beta K_n} \tag{11}$$

are met. As a result, to design the loop-filter-related coefficients $A_{2d} - A_{0d}$ and T_{2d} based on (10), the product of α and β should be found. In this work, it is achieved by using an RC tracking circuit. A replica RC value is tracked to model and obtain the

RC constant variation from its nominal value, and thus to find the value of $\alpha\beta$.

As finding γ/β and meeting (11), it is reached by measuring the differences of magnitude-frequency response between DC and high frequency as follows. With (10) achieved and K_d initially set to its nominal value K_n, (7) is rewritten as

$$H(s) = \frac{\gamma K_n(1+\alpha\beta T_{2n}s)}{K_n(1+\alpha\beta T_{2n}s)} \cdot \frac{\alpha^2\beta^2 A_{2n}s^4 + \alpha\beta A_{1n}s^3 + A_{0n}s^2 + K_n(1+\alpha\beta T_{2n}s)}{\beta(\alpha^2\beta^2 A_{2n}s^4 + \alpha\beta A_{1n}s^3 + A_{0n}s^2) + \gamma K_n(1+\alpha\beta T_{2n}s)} \quad (12)$$

As can be seen from (12), for a calibration frequency ω_c much higher than PLL's loop bandwidth ω_0, the s^4 terms dominate both nominator and denominator. On the other hand, for a DC signal, the s^0 terms dominate. Therefore, the value of γ/β can be approximated as

$$\frac{\gamma}{\beta} \approx \frac{|H(j\omega_c)|}{|H(j\omega_{dc})|}, \text{ if } \omega_c \gg \omega_0 \quad (13)$$

In this work, to obtain $|H(j\omega_c)|$ and $|H(j\omega_{dc})|$, a calibration pattern $A[sin(\omega_c t)+1]$ (both amplitude and DC equal to A) is inputted to the Gaussian filter (as n in Fig. 1(b)). The input phase is thus given by:

$$\phi_{IN} = A\omega_{ref}\int(\sin\omega_c t + 1)dt \quad (14)$$

The output phase, which is equal to $\varphi_{IN}|H(s)|$, is depicted as

$$\phi_{OUT} = A\omega_{ref}\int(|H(j\omega_c)|\sin\omega_c t + |H(j\omega_{dc})|)\,dt \quad (15)$$

Hence, the voltage shift ΔV_t observed on V_t is:

$$\begin{aligned}\Delta V_t &= \frac{1}{K_v}\cdot\frac{d\phi_{OUT}}{dt} \\ &= \frac{A\omega_{ref}}{K_v}(|H(j\omega_c)|\sin(\omega_c t) + |H(j\omega_{dc})|) \\ V_t\text{amplitude} &= \frac{A\omega_{ref}}{K_v}|H(j\omega_c)| \\ V_t\text{DC deviation} &= \frac{A\omega_{ref}}{K_v}|H(j\omega_{dc})| \end{aligned} \quad (16)$$

Therefore, based on (13) and (16), γ/β can be derived as:

$$\frac{\gamma}{\beta} \approx \frac{V_t\text{amplitude}}{V_t\text{DC deviation}}, \text{ if } \omega_c \gg \omega_0 \quad (17)$$

As a result, by detecting both V_t amplitudes (at ω_c) and DC deviation using a calibration ADC, the value of γ/β can be obtained. After that, the digital coefficient K_d is set to γ/β times of its nominal value to meet (11).

Comparing with the method used in [9], the proposed method avoids demodulating VCO output signal that works at high frequency. Furthermore, due to the value of γ/β is acquired by calculating the ratio of two magnitudes, LUT is not needed.

For the calibration frequency ω_c, it is determined under the considerations of high detecting accuracy with low power consumption in the calibration ADC. The higher the ω_c is, the more stringent resolution and power requirements are posed on the ADC. On the other hand, too low ω_c will cause inaccurate magnitude detection as (13) is no longer met.

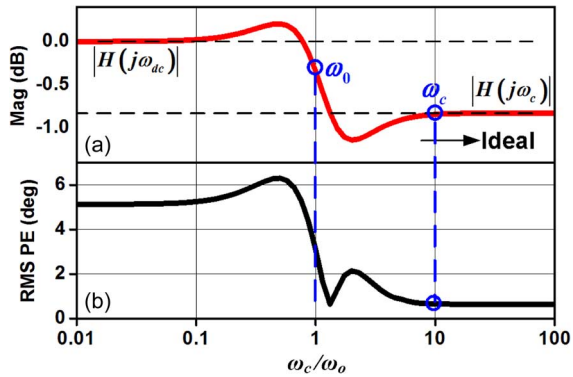

Fig. 6. Simulated (a) magnitude-frequency response of $H(s)$ and (b) RMS phase error (PE) with the ratio of ω_c/ω_o.

Fig. 6(a) shows the simulated frequency-magnitude plot of $H(s)$ with the digital-analog mismatch. Because of this mismatch, $|H(s)|$ experiences a fluctuation around the loop bandwidth ω_0, and then gradually turns flat when frequency goes beyond ten times of ω_0. As such, the minimum ω_c needs to be ten times of ω_0 to avoid amplitude detection error.

For further validation, the simulated RMS phase error versus the ratio of ω_c/ω_0 is given in Fig. 6(b). It can be found that the resulting RMS phase error reaches its lowest limit when ω_c/ω_0 approximately exceeds 10. As a consequence, ω_c is set to be 1 MHz in this work for $\omega_0 = 100$ kHz. The calibration error caused by this ω_c approximation will be discussed in Section IV.

C. Calibration Procedure

The proposed calibration procedure is divided into 3 stages, which was simulated with Simulink as shown in Fig. 7 and described as follows.

Stage 1: When calibration starts, a calibration binary data pattern of 0/2/0/2/0/2/$\cdots$(both amplitude and DC value to be 1 unit) at a frequency of ω_c is applied to the Gaussian filter (as in Fig. 1(a)). As such, a sine wave with a frequency of ω_c will be expected on V_t. In addition, due to the DC component of the input pattern, a DC deviation on V_t can be observed as well. Since PLL needs time to track the calibration data, the magnitude detection is not activated during this stage. However, the RC tracking is performed here and thus $\alpha\beta$ is found out to adjust respective coefficients as discussed in Section II-B. In the meanwhile, K_d is set to its nominal value K_n.

Stage 2: After PLL tracks the calibration data pattern stably, the waveform of V_t is measured by the calibration ADC. In ideal case, if the transfer function of the pre-emphasis filter $H_{comp}(s)$ matches the PLL transfer function $H_o(s)$, the measured amplitude of V_t should be equal to its DC deviation. Here, the DC value of the calibration data (V_{DC1}) is obtained by averaging out the V_t voltage over a number of periods. As for V_t amplitude, it is done by subtracting V_{DC1} from its peak value V_{peak}.

Stage 3: During this stage, the calibration data pattern is terminated. Without the calibration data pattern sent, PLL will lock to a carrier frequency for the coming transmission, and V_t will stabilize to the corresponding DC value (V_{DC2}). This DC value is also measured by the ADC, and thus the DC deviation can be calculated as $|V_{DC2} - V_{DC1}|$. Thereby, the value of γ/β is obtained based on (17) and K_d

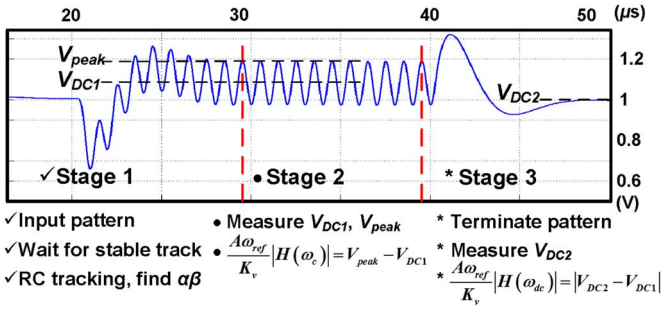

Fig. 7. Simulated V_t waveform during calibration.

is adjusted accordingly. After that, the calibration ends and the transmitter is ready for data transmission.

With these three stages, (10) and (11) are met and the limited modulation bandwidth can be compensated.

As for the calibration time, i) the transmission channel switching, ii) RC tracking, and iii) sending calibration data pattern are conducted simultaneously in Stage 1. For a GSM transmission slot with frequency hopping, PLL is required to relock to the coming carrier frequency before transmission begins. This relock time is re-used here to accommodate ii) RC tracking and iii) PLL tracking for the calibration data pattern. Therefore, the total calibration time is only contributed by the time consumed in Stages 2 and 3 where γ/β tracking is performed.

Considering the temperature variation, for most of the frequency hopping systems, a single transmission time slot (typically in the order of 10^{-3} s) is not long enough to generate sufficient heat and cause temperature variation of the chip. Thus, within one time slot, the temperature effect is negligible. For different slots, the temperature variation can be overcome by activating the proposed calibration before every transmission slot.

In brief, with both the RC variations and the loop gain error calibrated, the proposed technique can reduce phase error significantly. In addition, the calibration time is shortened by reusing the time of transmission channel switching. The design strategy of the calibration technique has been analyzed based on a type-II, third-order PLL.

III. Circuit Implementations

A. Transmitter Architecture

The simplified block diagram of the proposed ΔΣ PLL transmitter is shown in Fig. 8. Gaussian filtering and pre-emphasis reshaping are performed in the GMSK & Pre-emphasis Filter module. In this module, $G(t)$ represents the Gaussian filter, while $G''(t)$, $G'''(t)$ and $G''''(t)$ represent the second, third and fourth order derivatives of $G(t)$, respectively. The outputs of $G''(t)$, $G'''(t)$ and $G''''(t)$ are multiplied with digital coefficients A_{0d}, A_{1d}, and A_{2d}, and then they are summed up and further amplified by $1/K_d$. The result is then applied to a digital filter DF (corresponding to the $1 + T_2 s$ term in (1)) and added to the output of Gaussian filter $G(t)$. A_{0d}, A_{1d}, A_{2d}, T_{2d}, and K_d are designed in the same configurations as in (10) and (11).

The simulated magnitude-frequency response of the implemented digital pre-emphasis filter, together with its ideal S domain linear model $H_{comp}(s)$, is plotted in Fig. 9. It can be seen that these two transfer functions match each other well up to a

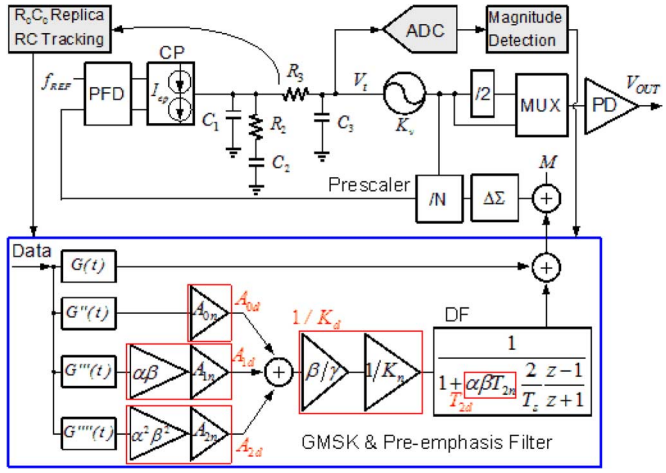

Fig. 8. Simplified block diagram of the proposed ΔΣ PLL transmitter.

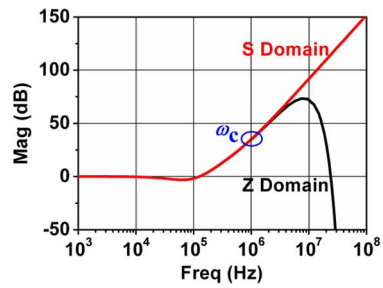

Fig. 9. Frequency response of pre-emphasis filter in Z domain and its linear model $H_{comp}(s)$ in S domain.

frequency higher than the calibration signal frequency ω_c. This validates the approximation of the pre-emphasis filter from Z to S domain in Section II-A.

The output of GMSK & Pre-emphasis Filter is added with the channel selection data M. The summed data is then fed to a second-order, multi-stage noise shaping (MASH 2-1) ΔΣ modulator, whose output is applied to a dual-modulus prescaler.

A single VCO is employed to cover frequency from 1648 MHz to 1910 MHz for GSM quad-bands. A divide-by-2 circuit is adopted to generate the low-band carrier. To select the transmission bands from the VCO and divider, a multiplexer is adopted. A power amplifier driver (PD) is implemented to drive the off-chip power amplifier (PA).

The calibration circuits consist of all the shaded blocks in Fig. 8 (calibration ADC, Magnitude Detection, and RC Tracking). These circuits are only activated in calibration. To reduce circuit complexity, the RC tracking circuit can be shared with cut-off frequency tuning circuit of low-pass filters in a full GSM transceiver implementation. In addition, the calibration ADC can reuse the down-conversion ADC. In this paper, only the calibration function of these two blocks is discussed.

B. VCO, PFD, and Charge Pump

The schematic of VCO is shown in Fig. 10(a). A symmetrically center-tapped inductor is employed, and the current source is replaced by a resistor (R_b) for low noise [22]. To further reduce the phase noise, K_v is decreased by dividing the VCO tuning range into several discrete sub-bands. These sub-bands are implemented with a switchable binary-weighted capacitor array, which is controlled by a 6-bit control word. This control word is obtained automatically with a coarse tuning algorithm

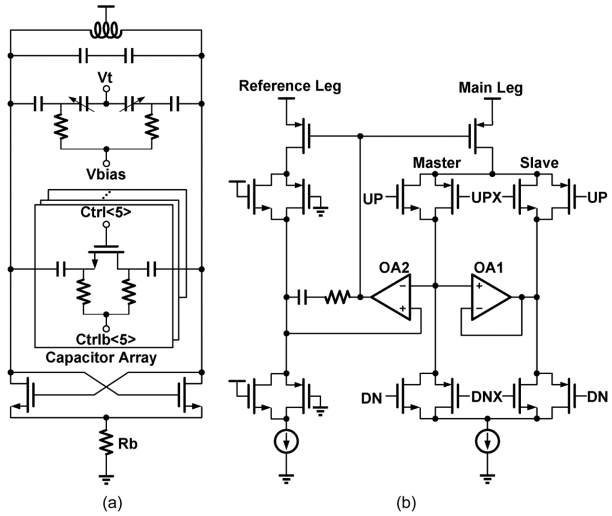

Fig. 10. Schematic of (a) the VCO and (b) the CP.

during the start-up period. Before every transmission, the corresponding control words are applied to the capacitor array for fast locking PLL to the desired channel.

Additionally, the schematic of the CP is shown in Fig. 10(b). The charge sharing effect is rejected by the rail-to-rail operational amplifier OA1. The spike noise is reduced by the master-slave CP prototype. OA2 and the reference leg are introduced to ensure that the up and down currents are matched over a wide range of output voltages.

C. Calibration ADC

To achieve high resolution and low power consumption with compatibility to the down-conversion ADC in the receiver, a 2-2 cascaded discrete-time $\Delta\Sigma$ ADC is implemented as shown in Fig. 11(a). The coefficients of the switch-capacitor integrator architecture are well defined owing to the good matching of capacitors. In addition, a single-bit quantizer is employed to improve the linearity. The simulated spectra of the ADC output are shown in Fig. 11(b). For a 150-kHz input (scenario in down-conversion), an ENOB of 13.37 bit is achieved whereas for a 1-MHz calibration signal, an ENOB of 10.47 bit is achieved. This resolution ensures the re-usability and γ/β tracking accuracy not to be degraded.

The calibration ADC is followed by a decimation filter for higher resolution. This decimation filter has an uneven frequency-magnitude response for ω_c and ω_{DC} (suppose the magnitude difference to be ΔA), which will introduce an extra detection error. To minimize this error, the detected γ/β needs to subtract ΔA before applying to the digital emphasis-filter. In this work, the theoretical value of ΔA is utilized in this subtraction. Due to the digital implementation of the decimation filter, ΔA remains constant to its theoretical value under PVT variations. Therefore, the uneven frequency response of the decimation filter will not degrade the calibration accuracy.

D. RC Tracking

The RC tracking circuit is designed to sense the $\alpha\beta$ value as depicted in Fig. 12(a). It consists of an integrator and a clock-driven hysteresis comparator (as shown in Fig. 12(b)). The replica R_0 and C_0 in the integrator are designed to match the resistors and capacitors in PLL's loop filter. The reference

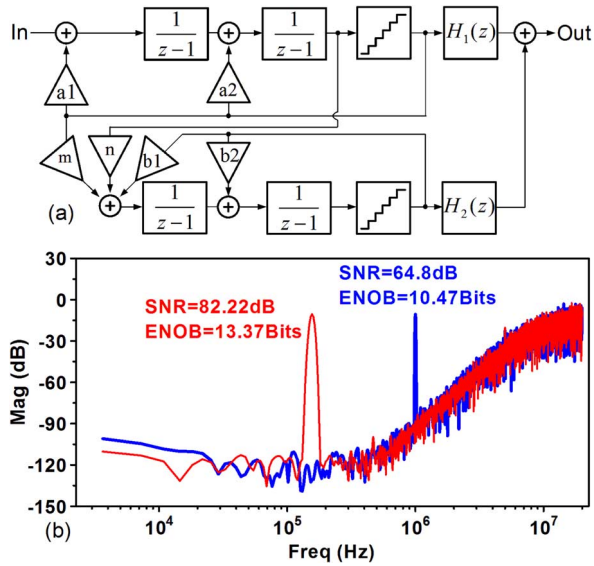

Fig. 11. (a) Architecture of the 2-2 cascaded $\Delta\Sigma$ ADC (b) Output spectra of the calibration ADC with a 150-kHz input and a 1-MHz input.

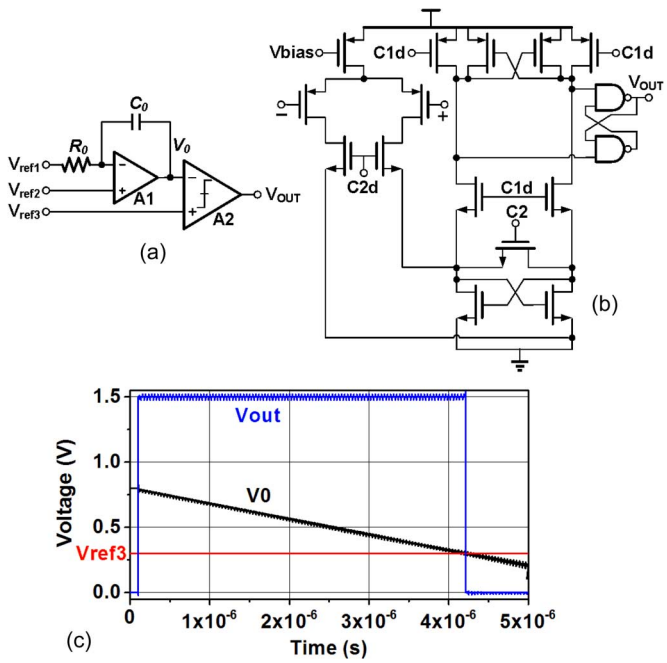

Fig. 12. Schematic of (a) RC tracking circuit and (b) comparator, and (c) simulated transient waveforms of the integrator and comparator outputs.

voltages V_{ref1}, V_{ref2}, and V_{ref3} are generated by a resistor ladder. The integrator output voltage V_0, initially set to $V_{\rm ref2}$ when RC tracking circuits enabled, is expressed as

$$V_{ref2} - V_0 = \frac{1}{C_0}\int_0^{T_0} \frac{V_{ref1} - V_{ref2}}{R_0} dt$$

$$T_0 = R_0 C_0 \frac{V_0 - V_{ref2}}{V_{ref2} - V_{ref1}} \tag{18}$$

where T_0 represents time for V_0 dropping from V_{ref2} to V_{ref3}. In this work, V_{ref1}, V_{ref2}, and V_{ref3} are designed to be 1.3 V, 0.8 V, and 0.3 V, respectively, making T_0 equal to R_0C_0.

The simulated transient waveforms of the RC tracking circuits are plotted in Fig. 12(c). When the tracking starts, V_0 begins to discharge from $V_{\rm ref2}$. The comparator output V_{out} is

sampled by a 104-MHz clock, and corresponding T_0 (and thus R_0C_0) is tracked by counting the number of sampling periods. Comparing with the nominal sampling periods, the coefficient $\alpha\beta$ can be obtained.

E. Magnitude Detection

Once the γ/β tracking is activated, the calibration ADC converts the signal on V_t into digital domain. This digitalized signal is then calculated in Magnitude Detection circuit to generate the amplitude and DC deviation as discussed in Section II-C. The ratio of the amplitude and DC deviation is fed back to the digital filter and adjust its coefficient K_d.

IV. Discussions on Calibration Accuracy

A. γ/β Tracking Accuracy

The ω_c approximation error and the finite ADC resolution contribute the most significant parts to the γ/β tracking inaccuracy.

For the ω_c approximation error, as discussed in the Section II-B, (13) is valid if ω_c is much higher than ω_0. However, a higher ω_c puts more stringent requirements on the calibration ADC. For a finite ω_c (ten times of ω_0 in this work), the deviation of $|H(j\omega_c)|$ from its ideal value $|H(j\omega_\infty)|$ will degrade the calibration accuracy. The ω_c approximation error is defined as

$$E = \left| \frac{H(j\omega_\infty) - H(j\omega_c)}{H(j\omega_\infty)} \right| \tag{19}$$

The simulated E with variations of the design parameters β and γ is depicted in Fig. 13. It can be observed that E is within 0.55% for β and γ varies up to $\pm 20\%$.

Another factor that affects the γ/β tracking accuracy is the finite ADC resolution. As depicted in Section II-D, the calibration ADC achieves 10.47-bit ENOB when sensing a 1-MHz calibration signal. Hence, the calibration error from ADC is calculated as $1/2^{10.47} \approx 0.1\%$.

Combing the inaccuracies arising from the ω_c approximation error and the finite ADC resolution, the total γ/β tracking error is within 0.56%.

B. RC Tracking Accuracy

The RC tracking accuracy is mainly limited by the input offset voltages of the amplifiers and quantization error as discussed below.

1) Two sources of the offset voltage. One is the input offset voltage of amplifier A1, and the other is that of the comparator A2. Assume the input offset voltage of A1 is $v_{\mathrm{ios},A1}$, resulting in a detecting error of $v_{ios,A1}/(V_{\mathrm{ref}2} - V_{\mathrm{ref}3})$. Similarly, the input offset voltage of A2 is assumed to be $v_{ios,A2}$ and it introduces an error of $v_{ios,A2}/(V_{\mathrm{ref}2} - V_{\mathrm{ref}3})$. Since both $v_{ios,A1}$ and $v_{ios,A2}$ are approximately less or equal to 2 mV, the total maximum input offset voltage is 2.8 mV, if $v_{ios,A1}$ and $v_{ios,A2}$ are not correlated with each other. For $V_{ref2} - V_{ref3} = 500$ mV in this work, the input offset voltage yields a total 0.56% error.
2) Quantization error due to the limited sampling frequency. To speed up the tracking, the nominal R_0C_0 is set to be around 4 μs. Therefore, when this RC constant is sampled by a 104-MHz clock, the RC tracking accuracy is approximately 0.24%.

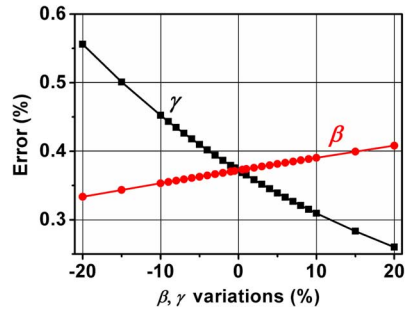

Fig. 13. Simulated ω_c approximation error due to β and γ variations.

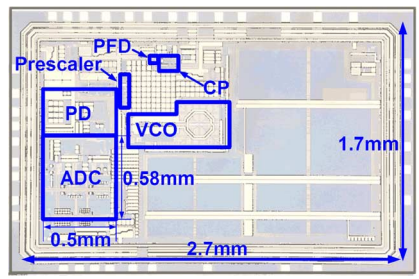

Fig. 14. Microphotograph of the transmitter with the calibration circuit.

TABLE I
Performance Summary of the ΔΣ PLL Transmitter

Bands	GSM850/GSM900 /DCS1800/PCS1900
400-kHz offset phase noise	−116 dBc/Hz
1-MHz offset phase noise	−129 dBc/Hz
3-MHz offset phase noise	−138 dBc/Hz
20-MHz offset noise level	−158 dBc/Hz
Reference Spur	−76.5 dBc
RMS jitter	0.918 ps
PE (unmodulated)	0.62° RMS
PE (without cal.)	2.05° RMS
Modulation spectrum 400-kHz	−64 dBc

In sum, the total RC tracking accuracy is estimated to be 0.61%, as the root mean square of the offset voltage and quantization error.

V. Measurement Results

The transmitter using the proposed modulation bandwidth calibration technique was implemented in a 0.18-μm CMOS process with one-poly silicon and six metal layers. The chip microphotograph is shown in Fig. 14. The total area of the chip is 4.59 mm^2 (2.7 mm $\times$ 1.7 mm). With a 3-dBm output power level of the power driver, the total current consumption of the transmitter is 32 mA at a supply of 1.8 V.

The uncalibrated $\Delta\Sigma$ PLL transmitter performances are measured and summarized in Table I. Fig. 15 depicts the output phase noise of the PLL at 1.88 GHz, where -116 dBc/Hz, -129 dBc/Hz, -138 dBc/Hz and -158 dBc/Hz were achieved at 400-kHz, 1-MHz, 3-MHz, and 20-MHz offsets, respectively. The measured RMS jitter was 0.918 ps (equivalent to 0.62° RMS phase error). In addition, a maximum -76.5-dBc reference spur was measured as in Fig. 16. The modulation spectrum at 1.88-GHz channel was presented in Fig. 17. With reference to the GSM mask, a 4-dB margin is achieved at the critical 400-kHz offset.

For the calibrated transmitter, the digital coefficients $\alpha\beta$ and γ/β in the pre-emphasis filter are automatically obtained with

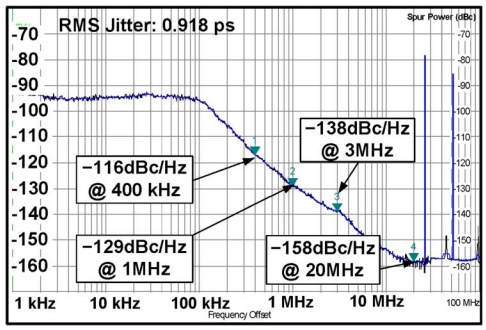

Fig. 15. Measured phase noise at 1.88-GHz channel.

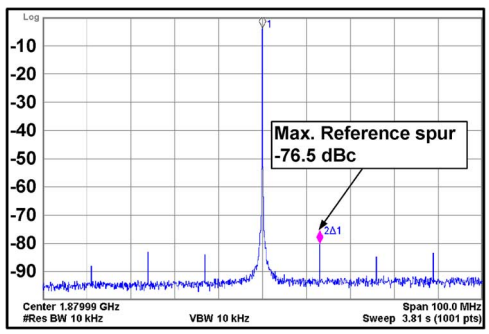

Fig. 16. Measured reference spur at 1.88-GHz channel.

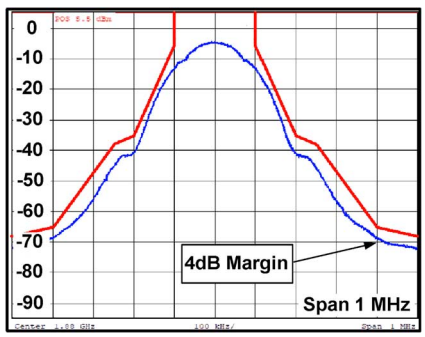

Fig. 17. Measured GSM modulation spectrum at 1.88-GHz channel.

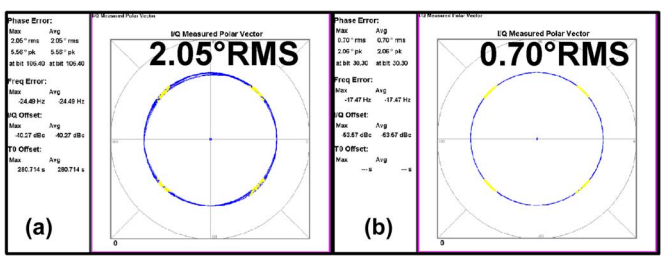

Fig. 18. Measured PE at 1.88-GHz channel (a) before, and (b) after calibration.

the proposed calibration technique. These coefficients are stored in registers and adopted in transmission slot.

In the phase error measurements, the minimum RMS phase error is reduced to 0.7° (Fig. 18(b)) from 2.05° (uncalibrated, Fig. 18(a)) with the proposed calibration technique. A 0.8° maximum RMS phase error was measured from 3 dies with continuous GSM uplink operations.

To further evaluate the effectiveness of the calibration, the modulation frequency-magnitude responses before and after calibration were summarized in Fig. 19. These responses were measured in the similar method as used in [23]. The calibration pattern, ranging from 1 kHz to 1 MHz, is applied to the modulation input. The measured uncalibrated gain shows a magnitude

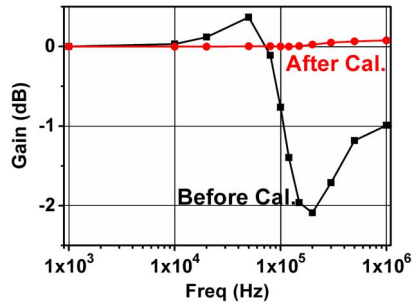

Fig. 19. Measured frequency responses before and after calibration.

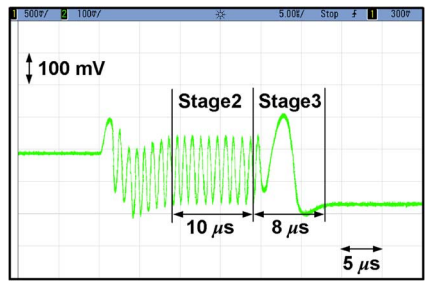

Fig. 20. Measured V_t transient response during calibration.

TABLE II
CALIBRATION ACCURACY

	$\alpha\beta$	γ/β
Auto Cal.	28,745	34,406
Optimized	28,890	34,130
Accuracy	0.5%	0.8%

drop within modulation bandwidth, while the calibrated gain is almost flat.

The measured calibration time is shown in Fig. 20. The transient waveform of V_t during calibration procedure was captured. From this graph, the overall calibration time was 18 μs, where 10 μs for Stage 2, and 8 μs for Stage 3.

To calculate the calibration accuracy, the digital coefficients $\alpha\beta$ and γ/β are manually adjusted to find out the smallest RMS phase error, independently. These manually found values are defined as the optimized values. These optimized values, together with the auto-calibrated ones applied in previous measurements, were read out from the Serial Peripheral Interface (SPI). The calibration accuracy is then defined as the deviation of the auto-calibrated values from the optimized values. Table II summarizes the measured optimized and auto-calibrated values, respectively. The calculated accuracy for $\alpha\beta$ tracking is 0.5% whilst 0.8% for γ/β tracking, which represents calibration accuracy for RC and loop gain, respectively.

A comparison with the state-of-the-art modulation bandwidth calibration techniques is presented in Table III. The proposed method is implemented in a type II, 3rd order PLL, which is more preferred in wireless communication system. Due to the calibrations on both loop gain error and RC variations, the transmitter with the proposed calibration technique achieves a comparable or better RMS phase error. Moreover, the calibration time is shortened to 18 μs by PLL locking time reusage. The calibration circuits, together with their areas and power consumptions, are also listed in this table. It can be found that with the assistance of the high-accuracy ADC, 0.5% RC calibration accuracy and 0.8% γ/β accuracy are achieved, respectively. Since the ADC and RC tracking circuits are

TABLE III
COMPARISON WITH STATE-OF-THE-ART MODULATION BANDWIDTH CALIBRATION TECHNIQUES

	Technology (μm)	Calibration Time (μs)	Accuracy	Maximum PE (^{o} RMS)	PLL Type /Order	Calibration Circuits	Area[d] (mm^2)	Power[d] (mA)
[7]	0.065	180	N.A.	1.55	I/2nd	ADC, *RC* calibration, Digital control	N.A.	N.A.
[8]	0.25	25	±2%	2	II/3rd	16-bit counter, 24-bit accumulator	0.4[c]	20
[9]	0.13	43	N.A.	3	I/2nd	Amp. Detector, Freq. discriminator, LUT	0.12[c]	N.A.
[10]	0.11	50	±1%	0.8	I/2nd	CP, BBPD, Adaptive gain accumulator	N.A.	N.A.
[24]	0.18	66	±10%	8.4	N.A.	CP, Calibration capacitor, ADC, Integrator	0.2[c]	0.3
This work	0.18	18	0.5%/0.8%[a]	0.8	II/3rd	ADC[b], *RC* tracking[b], Digital control	0.3	5

[a] For $\alpha\beta$ and $\gamma\beta$ accuracies, respectively.
[b] Shared with RX.
[c] Estimated from the chip photos.
[d] For calibration circuits only.

shared with RX in this work, the circuit complexity is not significantly increased.

VI. CONCLUSION

A $\Delta\Sigma$ PLL transmitter with an efficient modulation bandwidth calibration technique has been implemented in a 0.18-μm CMOS process for the GSM/GPRS application. The calibration technique uses $\alpha\beta$ tracking to calibrate the RC variations of the loop filter, and γ/β tracking to calibrate the variations of the loop gain. The measurement results have demonstrated that the transmitter with the proposed technique achieved a maximum RMS phase error of 0.8° within 18-μs calibration time. The measured respective calibration accuracy is 0.5% and 0.8%, for RC and γ/β tracking. With reference to the reported calibration techniques, the calibration technique in this work offers technical merits including 1) high accuracy, 2) shorter calibration time, and 3) lower circuit complexity.

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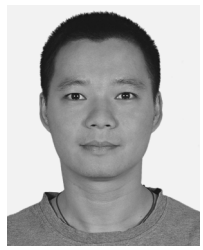

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