A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration

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***Abstract*— This article presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background timing-skew mismatch calibration. It divides a TI-SAR ADC into two split parts with the same overall sampling rate but different numbers of TI channels. Benefitting from the proposed split TI topology, the timing-skew calibration convergence speed is fast without any extra analog circuits. The input impedance of the overall TI-ADC remains unchanged, which is essential for the preceding driving stage in a high-speed application. We designed a prototype seven-/eight-way split TI-ADC implemented in 28-nm CMOS. After a digital background timing-skew calibration, it reaches a 54.2-dB signal-to-noise-and-distortion ratio (SNDR) and 67.1-dB spurious free dynamic range (SFDR) with a near Nyquist rate input signal and a 2.5-GHz effective resolution bandwidth (ERBW). Furthermore, the power consumption of ADC core (mismatch calibration off-chip) is 12.2-mW running at 1.6 GS/s, leading to a Walden figure-of-merit (FOM) of 18.2 fJ/conv.-step and a Schreier FOM of 162.4 dB, respectively.**

***Index Terms*— Analog-to-digital converter (ADC), digital background calibration, split ADC, time-interleaved (TI) ADC, timing-skew mismatch.**

I. Introduction

THE time-interleaved (TI) analog-to-digital converter (ADC) topology is a popular choice for wideband applications, such as ultra-wideband (UWB) communications, high-speed serial links, digital oscilloscopes, and software-defined radio [1]–[3]. A TI ADC architecture can increase the effective sampling rate of the overall converter by multiplexing several ADCs in parallel [4]. For an N-way TI ADC, the converter can achieve a sampling rate N times faster than a single channel.

However, this structure suffers from mismatches among the different sub-converters, including offset, gain, and timing skew [4]. Both offset and gain mismatches produce static errors, whose effects are ideally independent of the input frequency (input derivative or slope). Therefore, the offset and gain mismatches can be easily estimated by taking the average/rms of each sub-ADC output, followed by a correction in the digital domain directly [5], [24]. On the other hand, timing-skew mismatch generates a dynamic error, which increases with the input frequency, thus presenting a greater challenge, which is the calibration focus of this article.

A background calibration is more attractive than the foreground version because it can track supply and temperature variations during the normal operation. Numerous background timing mismatch calibration techniques have been developed for TI ADCs [1], [3]–[17]. Those previous works all estimate the timing skew in the digital domain and then correct the timing mismatch in analog by tuning the sampling clock's delay line [1], [2], [4], [7]–[13] or by subtracting the timing-skew error in digital directly [3], [5], [14]–[17]. References [3] and [14]–[16] presented fully digital background calibration techniques, but the additional channels required for the calibration add power or area overheads. Also, most importantly, the input impedance of the overall ADC is changing because of the reference channel, which is an obvious disadvantage for high-speed ADCs.

This article presents a split TIADC architecture with digital background timing mismatch calibration [18]. The proposed architecture allows the overall TI ADC to use a fast convergence timing mismatch calibration method without adding any analog circuits. Furthermore, the ADC input impedance remains constant with the proposed split architecture, and no spurs arise from impedance variations such as in the traditional reference-assisted architecture. To verify the proposed architecture, we implemented a prototype 1.6-GS/s seven-/eight-way split TI ADC in 28-nm

Manuscript received June 15, 2019; revised August 23, 2019; accepted September 26, 2019. Date of publication October 21, 2019; date of current version February 25, 2020. This article was approved by Guest Editor Qun Jane Gu. This work was funded by The Science and Technology Development Fund, Macau SAR [File no. MYRG2018-00204-AMSV & SKL-AMSV-2017-2019(DP)]. *(Corresponding author: Sai-Weng Sin.)*

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Digital Object Identifier 10.1109/JSSC.2019.2945298

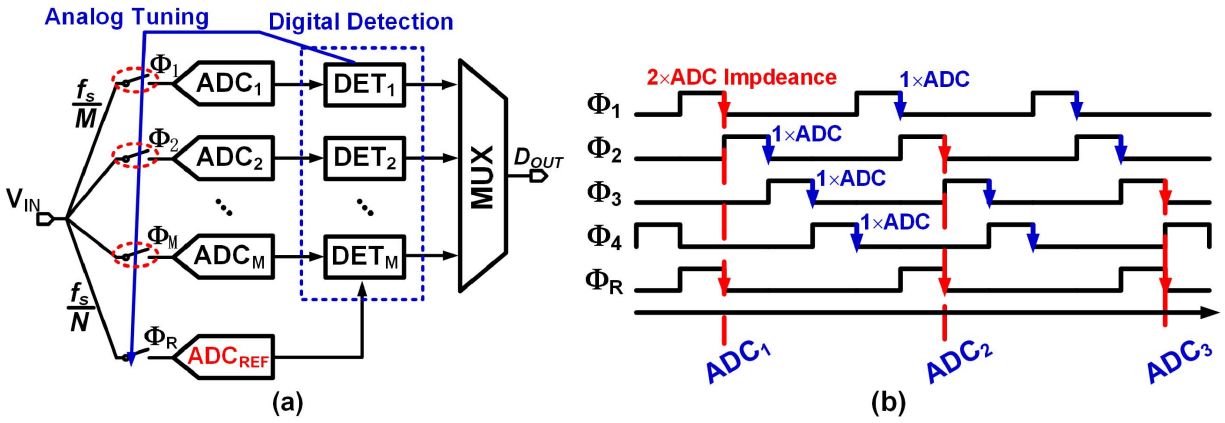

Fig. 1. (a) Block diagram of a TI ADC with a reference channel and (b) its clock phases.

CMOS. The ADC core (mismatch calibration off-chip) consumes 12.2 mW and achieves an signal-to-noise-and-distortion ratio (SNDR)/spurious free dynamic range (SFDR) of 54.2 dB/67.1 dB with a near Nyquist rate input, leading to a Walden figure-of-merit (FOM) of 18.2 fJ/conv.-step and a Schreier FOM of 162.4 dB, respectively.

This article is organized as follows. Section II presents the literature review of the TI ADCs with reference channel architectures. Section III describes the proposed split TI ADC topology. Section IV discusses the digital background timing -skew mismatch calibration based on the split TI ADC architecture. Section V presents the implementation details of the proposed seven-/eight-way split TI successive-approximation register (SAR) ADC. Section VI summarizes the silicon results and Section VII draws the conclusions.

II. Time-Interleaved ADC Calibrated With a Reference Channel

A. Architecture and Timing

The use of a reference channel is one of the effective ways to calibrate the timing mismatch in the background [6]–[8], [11], [13], [14], [16]. Fig. 1(a) shows an example of the block diagram of a TI ADC with a reference channel. It consists of M interleaved channels working at f_s/M and a reference channel operating at f_s/N, where f_s is the overall TI ADC sample rate, while M and N are mutual prime numbers.

Fig. 1(b) shows the timing diagram of an example of $M = 4$ and $N = 5$, illustrating the reference channel cycles through all the sub-ADCs. With an interleaving factor of 4, the reference channel is clocked with Φ_R which has a frequency of $f_s/5$, such that the first sampling edge of Φ_R coincides with the sampling edge of the first sub-ADC (Φ_1), the second sampling edges of Φ_R coincide with the one for the second sub-ADC (Φ_2), and so on for all four sub-ADCs. This allows the digital backend timing (DET) detection block to estimate the timing skew based on the difference [8], [13], [16] or the correlation function [7] between the output codes of the reference channel and each sub-ADC. Therefore, the digital backend DET block minimizes the difference or maximizes the correlation between each sub-ADC and the reference channel, by adjusting the clock delay lines [7], [8], [13] or correcting them in the digital domain [14], [16].

B. Challenges and Issues

There are two practical issues associated with the TI ADC with reference channel calibration. First, the additional reference converter will increase both power and hardware overhead. References [7] and [10] used a comparator/window detector to replace the reference ADC allowing the reduction of the power consumption, but implying the slowing down of the convergence speed [7] or the detection of the polarity allows only the analog tuning. Second, as shown in Fig. 1(b), the reference ADC changes the ADC input impedance periodically, and it will produce the extra spurs, which is a strong disadvantage for high-speed ADCs.

Fig. 2 shows the sampling for the four-way TI-ADC with a reference channel; it consists of a driver circuit to drive the sampling capacitance of TI-ADC, which consists of four-path sampling network of four-channel TI-ADC, and one path of reference ADC. We assume that each sampling network has the same sampling capacitance C and equalized turn-on resistance R_S of sampling switch. When the sampling switches turn-on, the driver's output signal has a sudden drop because of the driver's finite output resistance driving the sampling capacitance. The drop requires transient time to recover, which depends on the driver's output impedance, switch's ON-resistance, and the sampling capacitance, as shown in Fig. 2.

Because of the reference channel that is running at $f_s/5$, while each sub-channel of the TI-ADC is running at $f_s/4$, the reference channel will meet one of the TI-ADC channels (such as Φ_R with Φ_1) but not the remaining three TI-ADC sub-channels (Φ_{2-4}). As a result, the driver will see 2 × ADC input sampling networks in Φ_1 and 1 × ADC input sampling networks in Φ_{2-4}. This causes the sampling clock-dependent transient recovery if the driver is not fast enough to recover the transient (which is usually happening in high-speed ADCs). Therefore, it produces a dynamic error by sampling in every five clock cycles. Fig. 3 shows the output spectrum of a four-way 1.6-GS/s TI ADC with a 320-MS/s reference ADC that suffers from this phenomenon.

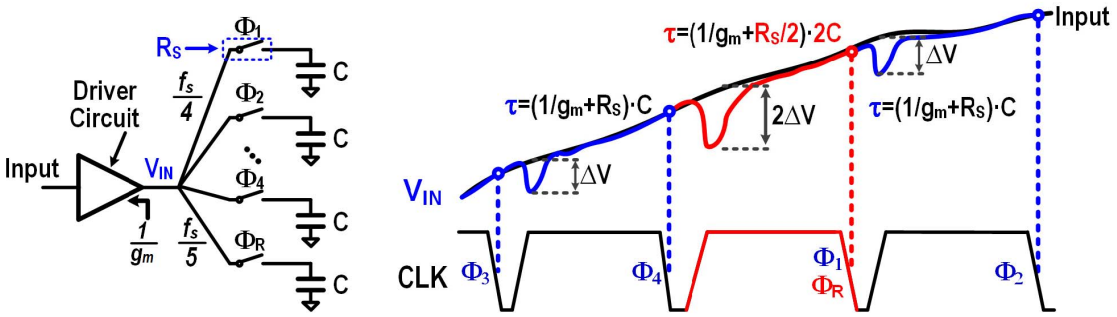

Fig. 2. Illustration showing the sampling of a four-way TI ADC with a reference channel.

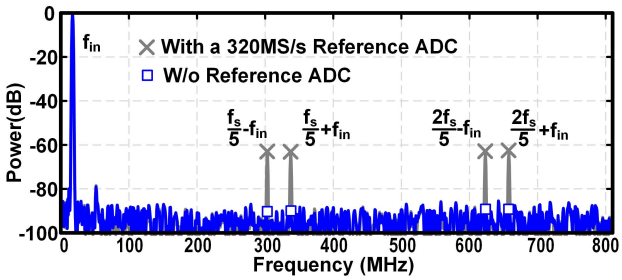

Fig. 3. Simulated output spectrum of a four-way 1.6-GS/s TI ADC with a 320-MS/s reference ADC.

Since this phenomenon is caused by the dynamic settling error, which depends on both the signal and the sampling clock phase, it is difficult to calibrate through the traditional calibration methods. To overcome these issues, we developed a split TI architecture as described next.

III. Split Time-Interleaved ADC

A. Proposed Split TI ADC Architecture

The concept of split TI ADC topology is to multiply the reference channel of the TI ADC in parallel to create another interleaved ADC. As shown in Fig. 4, a conventional TI ADC is split into two parts: A and B, with the same overall sampling rate but different interleaving numbers of channels M and N. Similar to the TI ADC with reference channel architecture, M and N must be mutual prime numbers to keep one of the sub-$\mathrm{ADC}_{\mathrm{A(or\ B)}}$ as the reference of $\mathrm{ADC}_{\mathrm{B(or\ A)}}$.

Fig. 5 shows an illustrative example of the three-/four-way split TI ADC with the proposed architecture; it consists of $4 \times \mathrm{ADC_A}$ working at $f_s/4$ and $3 \times \mathrm{ADC_B}$ working at $f_s/3$. Each of the $\mathrm{ADC_A}$ and the $\mathrm{ADC_B}$ samples the input signal V_{in} at the falling edge of its sampling clock (Φ_{A1}–Φ_{A4} and Φ_{B1}–Φ_{B3}). As the timing diagram shown in Fig. 5, the sample edge of $\mathrm{ADC_{A1-A4}}$ and $\mathrm{ADC_{B1-B3}}$ will meet each other after every 12 clock cycles, and it can serve as the implicit timing reference for mismatch calibration. It enables the background calibration based on the least mean square (LMS) algorithm, viewing the output of one channel of the $\mathrm{ADC_B}$ as the reference signal to calibrate the mismatch error of $\mathrm{ADC_A}$, while we also apply the same principle simultaneously to $\mathrm{ADC_B}$ to calibrate the mismatch error. Finally, it is worth to note that there are always two sub-converters (one in $\mathrm{ADC_A}$ and another in $\mathrm{ADC_B}$) sampling in every cycle simultaneously, imposing a constant ADC input impedance.

B. Implication for Power and Area

Like the traditional non-interleaved split ADCs [19], [20], the two split parts have the same SNR performance. Therefore, when we average the digital outputs of TI-$\mathrm{ADC_A}$ and TI-$\mathrm{ADC_B}$ to obtain the final output, as shown in Fig. 4, the final SNR performance will be improved by 3 dB. Thus, the requirements of SNR of each split part are halved.

Without the loss of generality, now, we discuss the implication of a split TI-SAR ADC for power and area. The accuracy of a high-speed SAR ADC [21], [22] is usually limited by the kT/C noise and comparator noise, which depends on the size of the sampling capacitor and comparators, respectively. With half of the SNR requirement of each part in the split TI-SAR ADC, the sizes of the sampling capacitor and comparator also become only half compared with traditional TI-SAR ADC. Therefore, the other blocks in the SAR ADC are also scaled down twice, such as the capacitor DAC buffers and the clock generators.

Global clock generation for interleaving channels is the other key point for the high-speed TI-ADC. For the split TI ADC, we also scale down the global clock buffer twice to maintain the total power and area unchanged. Thus, the jitter noise of each part of the split-TI ADC increases with a factor of $\sqrt{2}$. The SNR degradation caused by the jitter noise for the split TI-ADC with a sine wave input $[\mathrm{A} \cdot \sin(\omega_{\mathrm{in}} t)]$ can be expressed as

$$\mathrm{SNR_{jitter}} = 10 \cdot \log_{10} \frac{\left(2 \times \frac{\mathrm{A}}{\sqrt{2}}\right)^2}{\mathrm{A}^2 \cdot \omega_{\mathrm{in}}^2 \cdot \left[\delta_{\mathrm{A}}^2 + \delta_{\mathrm{B}}^2 + (2\delta_{\mathrm{ext}})^2\right]} \quad (1)$$

where $\delta_{\mathrm{A/B}}$ and δ_{ext} represent the rms value (in unit second) of the jitters from the internal TI-$\mathrm{ADC_{A/B}}$ or the external ADC clock, respectively. Note that (1) reflects the fact that the two main signals from parts A and B are correlated (identical in the ideal case), the effect of δ_{ext} to parts A and B is also correlated, while δ_{A}, δ_{B}, and δ_{ext} are mutual uncorrelated. Thus, we can write $\delta_{\mathrm{A}} = \delta_{\mathrm{B}} = \sqrt{2}\delta_{\mathrm{int}}$. Therefore, we can obtain

$$\mathrm{SNR_{jitter}} = 10 \cdot \log_{10} \frac{\left(\frac{\mathrm{A}}{\sqrt{2}}\right)^2}{\mathrm{A}^2 \cdot \omega_{\mathrm{in}}^2 \cdot \left(\delta_{\mathrm{int}}^2 + \delta_{\mathrm{ext}}^2\right)} \quad (2)$$

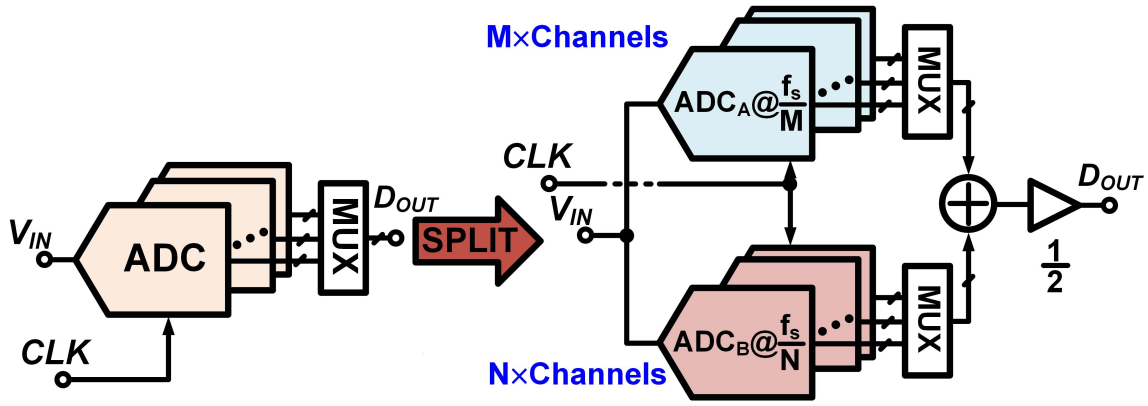

Fig. 4. Conceptual idea of split TI ADC.

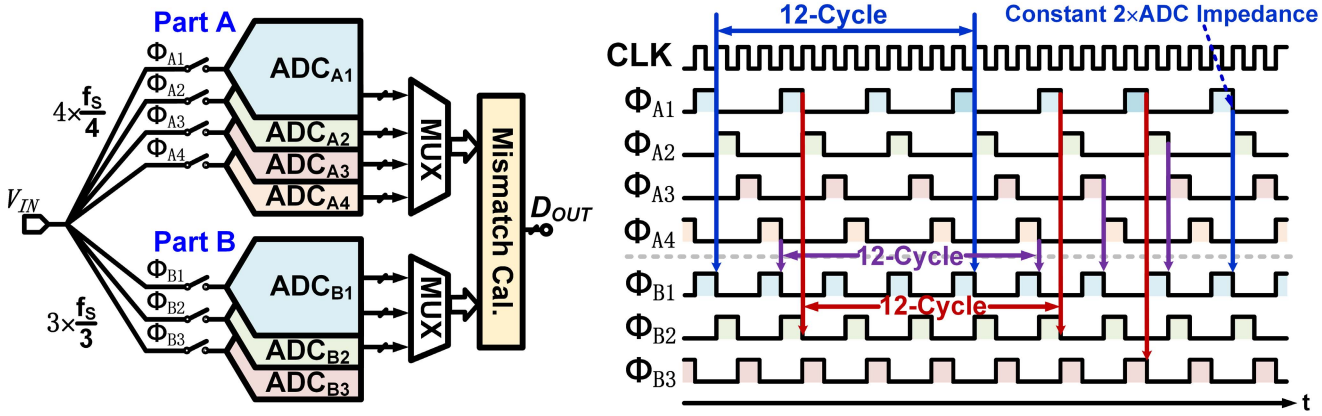

Fig. 5. Architecture and timing diagram of the proposed three-/four-way split TI ADC.

which also remains unchanged when compared with the conventional TI-ADC architecture.

On the other hand, the digital part, such as SAR control logic and digital logic circuits, cannot simply scale down, but it takes advantage of technology. In summary, there is no apparent power and area overhead compared with the conventional TI-SAR ADC.

IV. Digital Background Timing Mismatch Calibration

Based on the proposed split TI topology, a digital background timing-skew mismatch calibration algorithm will be explored in this section. To explain this method, we also use a three-/four-way TI ADC as an example.

A. Overview of Timing Mismatch Calibration

Fig. 6 shows the principles of the timing-skew calibration, it exhibits the $\mathrm{ADC_{B1}}$ (one of the unit converters of $\mathrm{ADC_B}$) as the reference to calibrate all the sub-channels in the $\mathrm{ADC_A}$ ($\mathrm{ADC_{A1-A4}}$). The goal of the calibration algorithm is to determine the timing skew of all interleaved channels of $\mathrm{ADC_A}$ that is equal to those of the reference channel $\mathrm{ADC_{B1}}$.

$D_{\mathrm{A,out,raw}}$ and $D_{\mathrm{B,out,raw}}$ represent the raw outputs without timing-skew correction from $\mathrm{ADC_A}$ and $\mathrm{ADC_B}$, and their data rate is $4 \times f_s/4$ and $3 \times f_s/3$, respectively. $\mathrm{ADC_{B1}}$ will meet each sub-channel of ADC_A ($\mathrm{ADC_{A1-A4}}$) every 12 cycles, as shown in Fig. 5. A multi-path switch works at $4 \times f_s/12$ to choose the output $D_{\mathrm{A,out}}$ that corresponds to the output of ADC_A after timing-skew correction. Therefore, the corrected data $D_{\mathrm{A,out}}$ can be written as

$$D_{\mathrm{A,out}} = \mathrm{D_{A,out,raw}} - \frac{dV_{\mathrm{in}}(t)}{dt} \cdot \Delta t \tag{3}$$

where $dV_{\mathrm{in}}(t)/dt$ is the derivative of the input and the Δt is the estimated timing skew of $\mathrm{ADC_A}$. In this article, we use a digital finite impulse response (FIR) differentiator to obtain $dV_{\mathrm{in}}(t)/dt$, as it will be discussed later. Then, it obtains the current conversion error e defined as the difference of the outputs between the unit converter of $\mathrm{ADC_A}$ ($D_{\mathrm{A,out}}$) and the corresponding one from $\mathrm{ADC_{B1}}$ ($D_{\mathrm{B1,out,raw}}$). The LMS search block updates the coefficient of mismatch factors effectively minimizing the difference e [8], [13]–[16]. Since Δt is not known in advance, it has to be estimated with the LMS algorithm by digital accumulators (Acc) with the update equation [14]

$$\Delta t^{(\mathrm{new})} = \Delta t^{(\mathrm{old})} + 2 \cdot \mu \cdot \frac{dV_{\mathrm{in}}(t)}{dt} \cdot e \tag{4}$$

where the step size μ controls the convergence speed and accuracy of the LMS search.

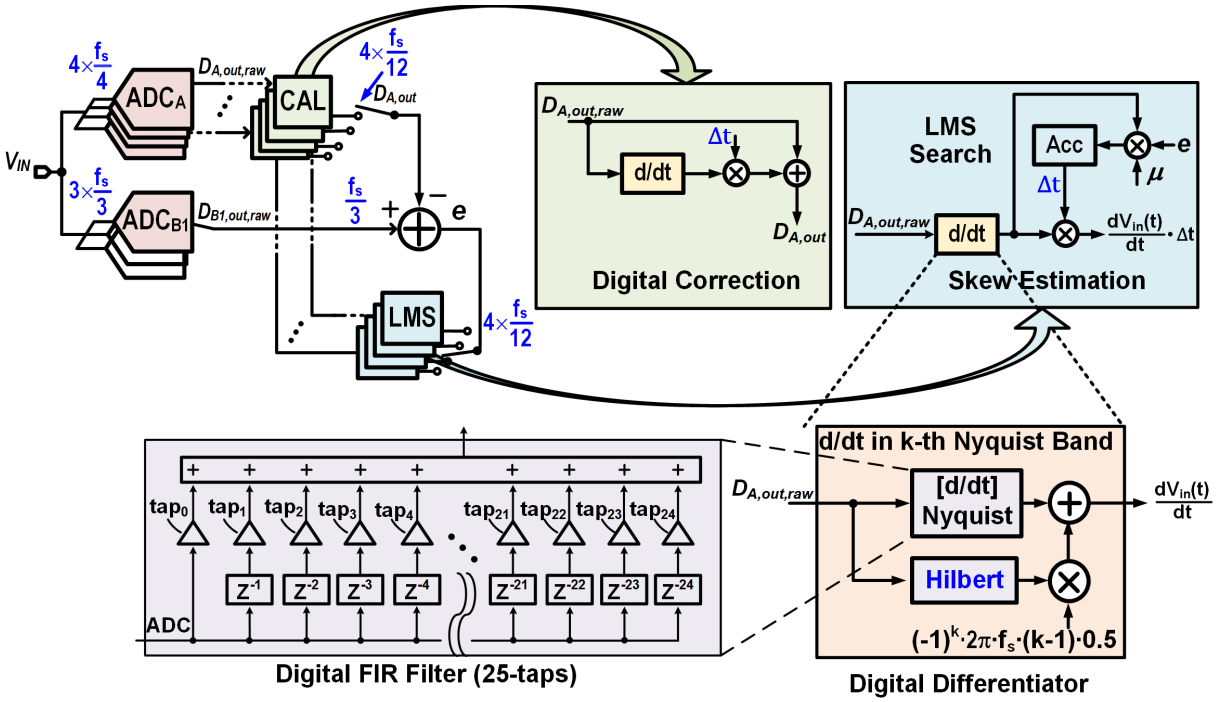

Fig. 6. Timing-skew mismatch calibration of a three-/four-way split TI ADC for part A.

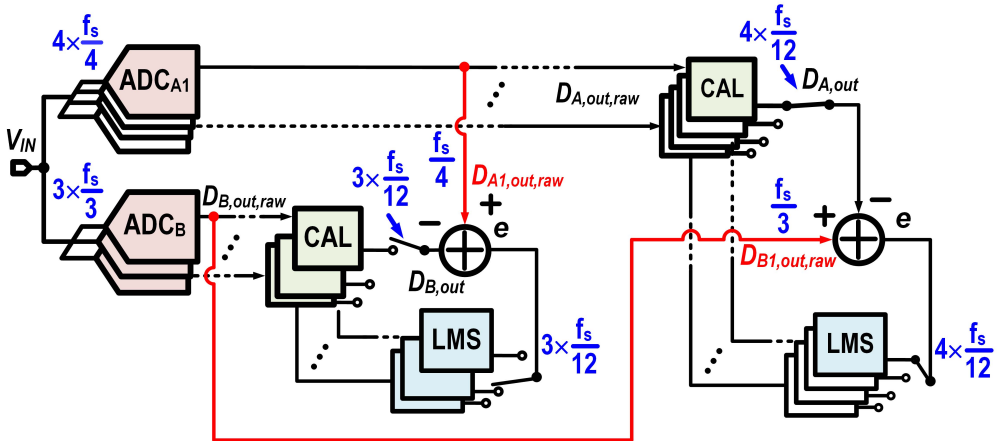

Fig. 7. Synchronous timing-skew mismatch calibration of a three-/four-way split TI ADC for parts A and B.

The mismatch calibration of ADC_B is similar to ADC_A, as shown in Fig. 7. We consider the sub-converters of the ADC_B as the reference to correct each converter of the ADC_A, with the factors "3" and "4" interchanged. Furthermore, we obtain the mismatch calibration of the ADC_A and the ADC_B synchronously and independently.

After the timing-skew calibration of Fig. 7, the sub-converters of ADC_A and ADC_B are both skew-free. However, there is a timing skew Δt_{AB} between ADC_A and ADC_B, as shown in Fig. 8. ADC_A and ADC_B are sampling the same time-instance input, instead of working in a TI manner. The final output of the split TI ADC $(y_A + y_B)/2$ represents the interpolated samples at $(t_A + t_B)/2$. Thus, the final values of the split TI ADC are also skew-free.

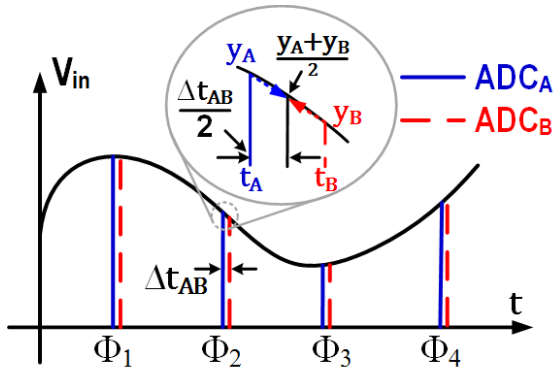

Fig. 8. Split TI ADC after timing mismatch calibration.

B. Implementation of the Derivative Filter

The performance of traditional digital correction methods is usually limited by the differentiator [5], [14], and they do not work well for input over Nyquist. For the differentiator, with the help of a Hilbert transform filter, we can compute the derivative of the input at about 90% (0.05–0.95) within

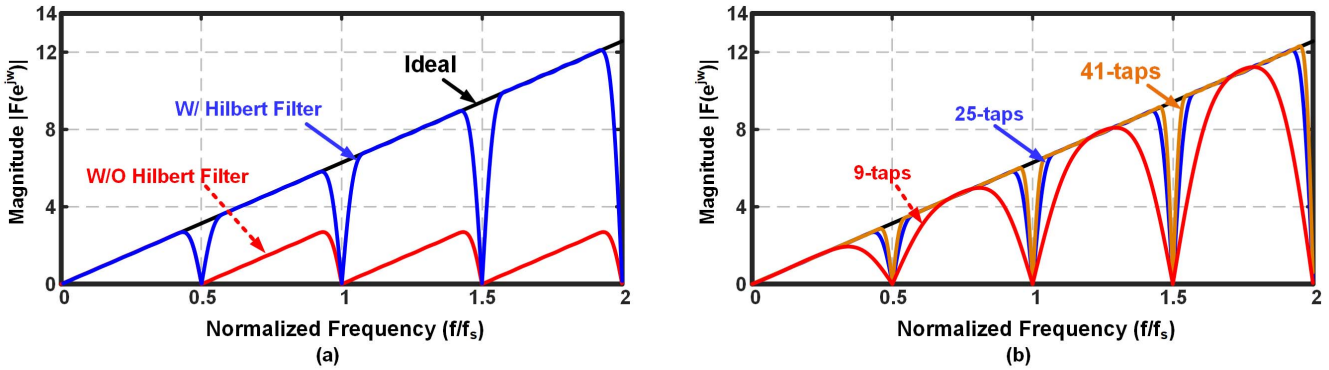

Fig. 9. Frequency responses of the derivative filter (a) without/with Hilbert transform filter (25 taps, with Hamming window) and (b) with Hilbert transform filter of the different number of taps.

any Nyquist band [17]. Now, let us analyze the details of the differentiator considerations. Without loss of generality, we can assume that the input is a sinusoidal signal as

$$x(t)|_{t=nT} = \sin(2\pi \cdot f_{\text{in,Nyq}} \cdot t)|_{t=nT} \tag{5}$$

where $f_{\text{in,Nyq}}$ is the input frequency in the first Nyquist band. Thus, the derivative of the signal is a product of cosine function with 2π of input frequency as

$$\text{x}'(t)|_{t=nT} = 2\pi \cdot f_{\text{in,Nyq}} \cdot \cos(2\pi \cdot f_{\text{in,Nyq}} \cdot nT). \tag{6}$$

We can use a conventional FIR differentiator to get the derivative. However, if we assume that the input frequency is over the first Nyquist band as

$$x(t)|_{t=nT} = \sin\{2\pi[f_{\text{in,Nyq}} + 0.5 \cdot (k-1) \cdot f_s]t\}|_{t=nT} \tag{7}$$

where k represents the input that is located in the kth Nyquist band. Then, the derivative of the input can be expressed as

$$\begin{aligned} x'(t)|_{t=nT} &= 2\pi \cdot f_{\text{in,Nyq}} \cdot \cos(2\pi \cdot f_{\text{in,Nyq}} \cdot nT) \\ &\quad + (-1)^k \cdot \pi \cdot (k-1) \cdot f_s \cdot \cos(2\pi \cdot f_{\text{in,Nyq}} \cdot nT). \end{aligned} \tag{8}$$

If we still use the conventional FIR differentiator, it only gets the first term of (8). To correct this error, we used a differentiator with the help of the Hilbert transform filter [17] here, as shown in Fig. 6. The Hilbert transform converts the sin into "−cos" to obtain $\cos(2\pi \cdot f_{\text{in,Nyq}} \cdot nT)$. Thus, we can supplement the missing part by adding the product of the output of the Hilbert filter and the scaling factor $(-1)^k \cdot \pi \cdot (k-1) \cdot f_s$; here, we need to know k ahead of time because the ADC cannot distinguish the signal in which Nyquist band. Fig. 9 shows the frequency response of the derivative filter with/without the Hilbert transform filter from dc to $2 \times f_s$.

A simple truncation of the number of coefficients to the specified number of taps, in both FIR differentiator and Hilbert Transform filter, does not lead to an optimal in-band accuracy in the frequency response. Truncation is equivalent to the multiplication of the filter coefficients by a rectangular window, which is known to have big sidelobes in the frequency domain. Hamming windows enable the lower sidelobes and give better performance in the band, as shown in Fig. 9. The coefficients of $(2K+1)$-tap conventional digital FIR differentiation filter [14] and Hilbert transform filter [17] with window function can be expressed as

$$\begin{cases} \text{tap}^D_{K-n} = (-1)^{n+1} \cdot \dfrac{1}{n} \cdot W_{K-n}, & 1 \le n \le K \\ \text{tap}^D_K = 0 \\ \text{tap}^D_{K+n} = -(-1)^{n+1} \cdot \dfrac{1}{n} \cdot W_{K+n}, & 1 \le n \le K \end{cases} \tag{9}$$

$$\begin{cases} \text{tap}^H_{K-n} = \dfrac{2}{\pi} \cdot \dfrac{1}{n} \cdot \sin\left(\dfrac{\pi \cdot n}{2}\right)^2 \cdot W_{K-n}, & 1 \le n \le K \\ \text{tap}^H_K = 0 \\ \text{tap}^H_{K+n} = -\dfrac{2}{\pi} \cdot \dfrac{1}{n} \cdot \sin\left(\dfrac{\pi \cdot n}{2}\right)^2 \cdot W_{K+n}, & 1 \le n \le K \end{cases} \tag{10}$$

where tap^D_m and tap^H_m represents the mth tap coefficient of differentiator and Hilbert transform filter, respectively, $W_{K\pm n}$ is the coefficient of $(K \pm n)$th taps of the window function, and when it is with the Hamming window that can be given by [14]

$$W^{\text{Hamming}}_{K\pm n} = 0.54 - 0.46\cos\left[2\pi\left(0.5 - \frac{n}{K}\right)\right], \quad 1 \le n \le K. \tag{11}$$

The digital FIR differentiator and Hilbert transform filter are the dominant hardware parts for the timing mismatch calibration because of the number of multipliers as well as FIR filter taps. From (9)–(11), we note that for a $(2K+1)$-tap FIR filter for digital differentiator or Hilbert transform filter, it holds for $\text{tap}_{K+n} = -\text{tap}_{K-n}, 1 \le n \le K$. Thus, the coefficients of these taps are antisymmetric, and we can use one multiplier to implement both tap_{K-n} and tap_{K+n}. Fig. 10 shows an efficient way to implement an example of a 25-tap digital derivative filter with only 12 multipliers. Therefore, the number of multipliers can be reduced by half.

As shown in Fig. 9, the frequency responses have an attenuation for the frequency near $n \times 0.5 f_s$, where $n = 1, 2, 3 \ldots$ The attenuation of the estimated derivative of input will not significantly affect the accuracy of the algorithm as long as it converges. Take (4) as an example, and if the estimation of $(dV_{\text{in}}(t)/dt)$ has an error of 20% (i.e., the derivative is $0.8\times$ of its ideal value), then the LMS will estimate the $\Delta t^{(\text{new})}$ that is $1.25\times$ larger than the actual timing skew in (4), and the final calibrated $D_{\text{A,out}}$ in (3) is still correct. However, the attenuation of the filter coefficients near $n \times 0.5 f_s$ makes the

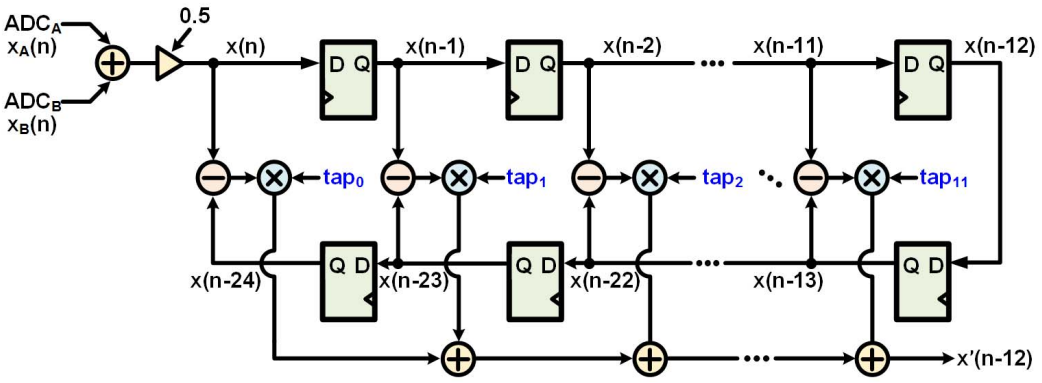

Fig. 10. Efficient 25-tap digital FIR filter implementation.

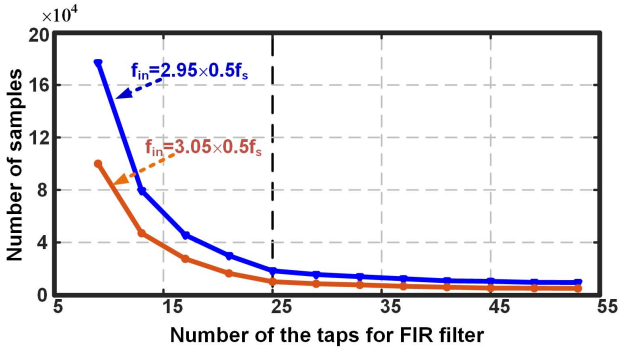

Fig. 11. Number of convergence samples versus the taps of FIR filter (three-/four-way split TI ADC).

convergence step size of LMS smaller than the normal one, as shown in (4). The term $2 \cdot \mu \cdot (dV_{\text{in}}(t)/dt) \cdot e$ is decreased by the attenuation of $(dV_{\text{in}}(t)/dt)$, and it will prolong the convergence or even cause non-convergence.

Naturally, as shown in Fig. 7(b), the frequency response of the digital FIR filter gets closer to the theoretical frequency response with the increasing number of taps. However, both area and power also increase linearly with the number of taps for the digital FIR filter. We target the effective bandwidth of ADC in the fourth Nyquist band, as well as in any Nyquist band below fourth band and it can work well about 90% (0.05–0.95) within the kth band. The worst case will appear at where the input frequency is near $3 \times 0.5 f_s$, as shown in Fig. 9. A behavior simulation for a split three-/four-way TI-ADC is shown in Fig. 11 to determine the number of convergence samples required by timing-skew calibration versus the different number of taps for two inputs of $2.95 \times 0.5 f_s$ and $3.05 \times 0.5 f_s$. The number of convergence samples increases with the reducing number of taps in digital FIR filters, and the tap number of around 25 is a good tradeoff between the convergence and the hardware overhead by digital mismatch calibration.

V. ADC Implementation

A. ADC Architecture

To verify the proposed split TI ADC architecture, we implemented a seven-/eight-way split TI-SAR ADC, as shown in Figs. 12 and 13. The channel mismatch, including offset, gain, and timing skew, calibrated in the digital domain off-chip, as shown in Fig. 12. It consists of an eight-way TI-SAR ADC$_A$ and a seven-way TI-SAR ADC$_B$ working at 200 and 228 MS/s, respectively. The ADC has the input impedance matching on-chip, as shown in Fig. 13 (blue line). To ensure the equal distance to the time-interleaving channels, we use an H-tree structure to route the input signals and clocks. Furthermore, we shielded the master clock CLK-1.6G with the ground to avoid interference through capacitive coupling with the input.

B. Phase Generator

The seven-/eight-way split-interleaved systems require both eight and seven clock phases, each having a 12.5% and 14.3% duty cycle, respectively. Fig. 14 shows the phase generator where a 1.6-GHz master clock, divided by eight-cycle or seven-cycle ring counters, generates the outputs Q_{A1}–Q_{A8} and Q_{B1}–Q_{B7} for ADC$_A$ and ADC$_B$, respectively. The ring counter is composed of D-Flip-Flops (DFF) connected to a shift register, being equivalent to a cascade of tens of gates, accumulating significant jitter. We use the master clock CLK-1.6G to retime Q_{A1}–Q_{A8} and Q_{B1}–Q_{B7} from the ring counters to get the low-jitter final sample clock $\Phi_{\text{A1–A8}}$ and $\Phi_{\text{B1–B7}}$.

As shown in Fig. 14, we use the master–slave DFF to build the ring counters. Therefore, it can obtain the output Q_n and M_n from the slave and master register of the nth DFF for the ring counter, respectively. Fig. 15 shows the retiming technique by a custom-implemented logic gate expressed as

$$\Phi_n = (\overline{CLK} + M_n) Q_n \tag{12}$$

where the rising edge of the final sample clock phase Φ_n depends on the rising edge of Q_n and the critical sampling falling edge of Φ_n is defined by the master clock CLK. Thus, it not only removes the jitter and timing skew produced by frequency-division circuits but also allows the use of the minimized size logic gate for those DFF components. From the post-layout transient-noise simulation, the total extracted jitter of each sampling edge ($\Phi_{\text{A1–A8}}$ and $\Phi_{\text{B1–B7}}$) is close to 70-fs rms, dominated by the global clock buffer, and the total power consumption of the phase generator is only 2.3 mW.

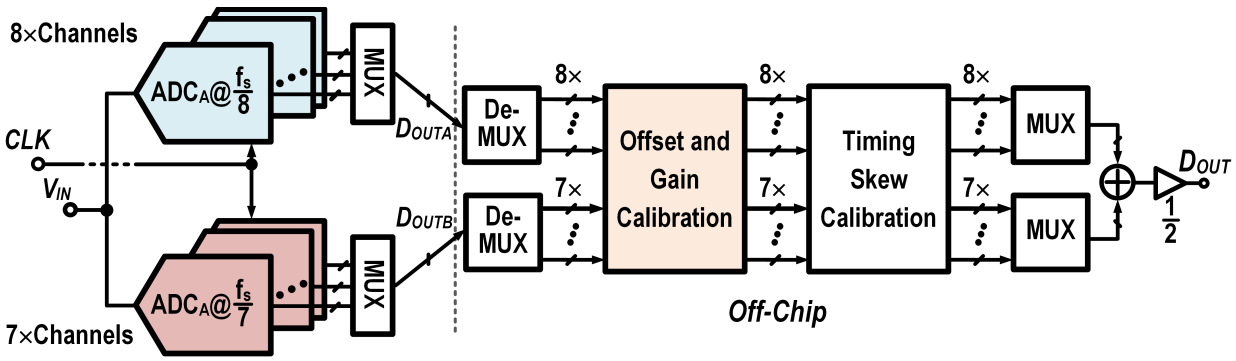

Fig. 12. ADC architecture.

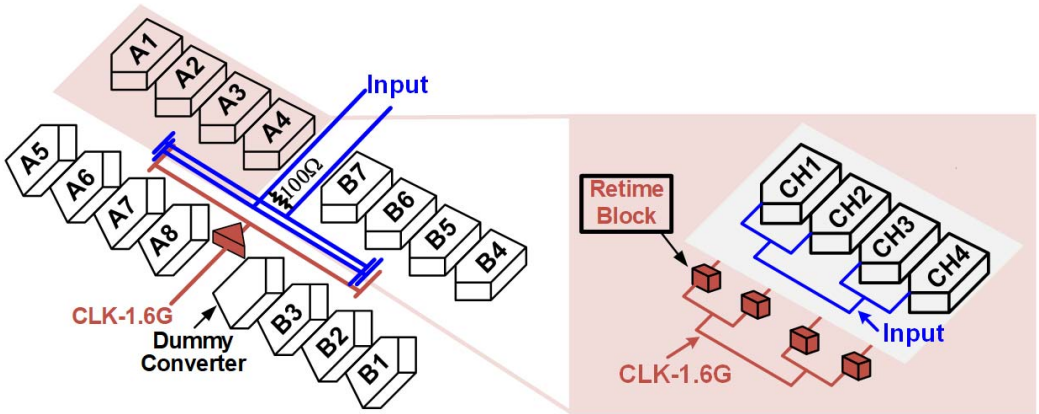

Fig. 13. Block diagram of seven-/eight-way split TI-SAR ADC.

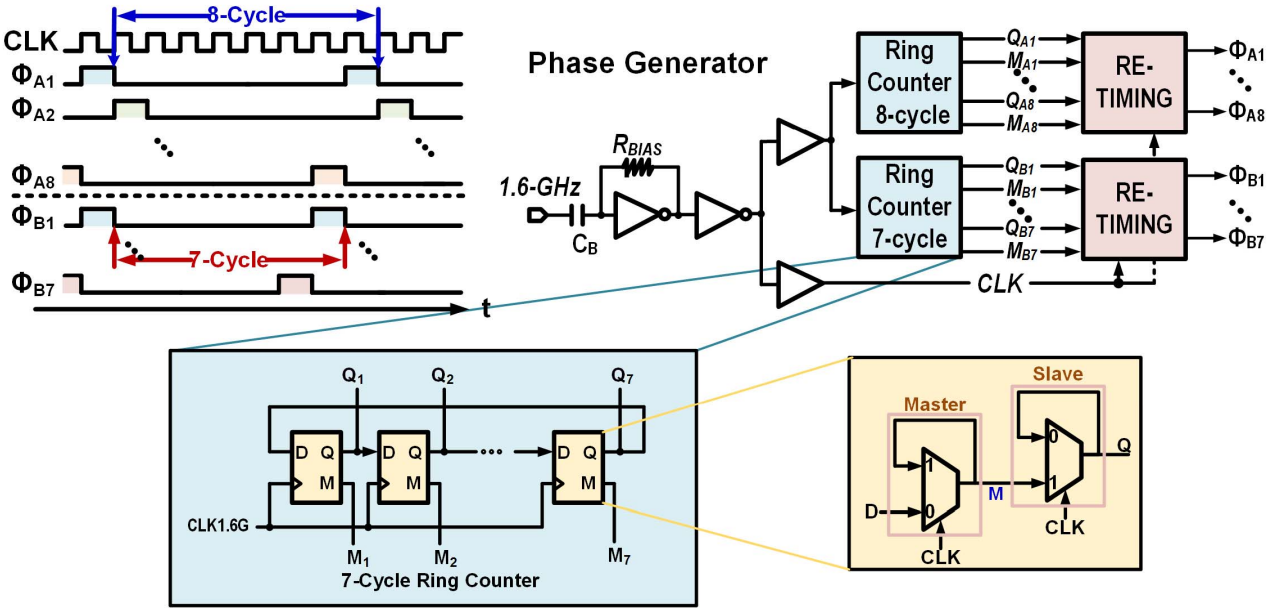

Fig. 14. Phase generation.

C. Single-Channel SAR ADC

The single-channel SAR ADC is similar to the architecture in [22]. Fig. 16 shows the architecture of the single-channel SAR ADC, which consists of a comparator, bootstrapped switches, DAC capacitor arrays, SAR control logic, and digital error correction (DEC) logic. Similar to the previous works [22], [23], the ADC sampled input signal on the top plates of capacitor arrays, and the first MSB can be determined by the polarity on the top plates. Therefore, the 10-bit ADC only needs 2^9 capacitor cells in each capacitor array. The bottom

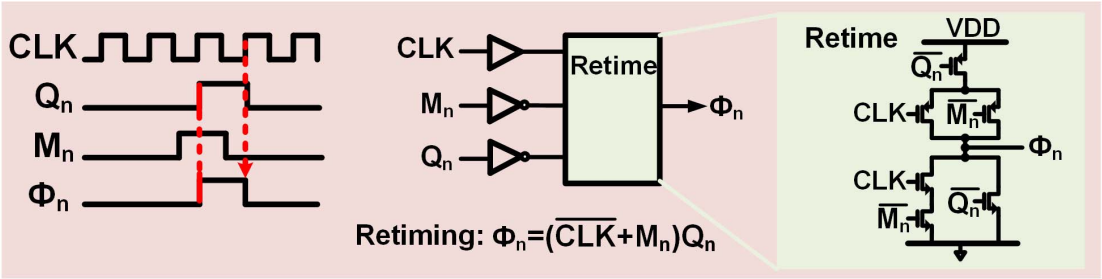

Fig. 15. Retiming logic.

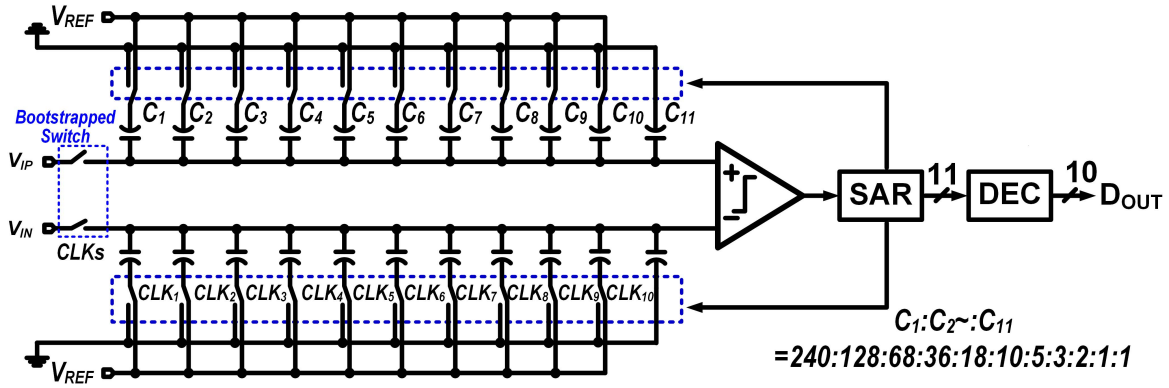

Fig. 16. Architecture and timing diagram of the single-channel SAR ADC.

plates of capacitors' cells are either connected to the reference voltage or ground. A CMOS inverter can perform the DAC switching with very simple control logic. The ADC adds one extra redundant bit cycles to alleviate the DAC settling problem. The 2^9 capacitor cells will be arranged into ten capacitor groups C_1–C_{10} with the binary-scaled recombination weighting method. It uses the custom-layout metal–oxide–metal capacitor with a unit capacitance of ~0.35 fF, and the total single-ended input capacitance is 180 fF. Also, an asynchronous control circuit [22], [23] is used to generate the necessary clock signal internally in each single channel. For each single-channel SAR ADC, it only needs one sampling clock (CLKs) from the global clock generation.

D. Impact of Sampling by Timing Skew

For the split TI-ADC, there are two ADCs sampling the input simultaneously. Due to the timing skew between two ADCs, the turn-off time of sampling switches is a bit different. As mentioned in [11], the bond-wire inductance makes the driving current cannot track well the sudden impedance change because of sampling switch turn-off sharply.

Now, we use the prototype seven-/eight-way split TI-ADC as an example to analyze this problem. Let us talk about how the sampling switch's turn-off for ADC_{Bi} $(i = 1, 2, \ldots 7)$ will impact the sampling of ADC_{A1}. Fig. 17 shows the input interface of ADC, where $R_M = 50\ \Omega$ is the resistance for input impedance matching on-chip, $C_{\mathrm{eq}} = 3$ pF is the equalized capacitance to the GND including the capacitance (2.5 pF) for ESD protection and parasitic of the PAD (500 fF), and

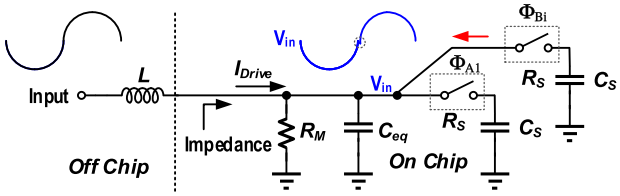

Fig. 17. Illustration showing the impact of input interface by sampling switch turn-off.

$C_s = 270$ fF is the sampling capacitance for each single-channel including the CADC (180 fF) and parasitic (90 fF).

Due to the shunt impedance ($\mathrm{R_M//C_{eq}}$) dominates the overall interface in both the low and high frequency, it absorbed the kickback fluctuation from the switches, and there is no obvious change of drive current I_{Drive}. Therefore, the sampling switch's turn-off for $\mathrm{ADC}_{Bi}(i = 1, 2, \ldots 7)$ event does not fluctuate the sampling of $\mathrm{ADC_{A1}}$ significantly.

E. Offset and Gain Calibration

The offset and gain mismatches are calibrated by averaging and variation functions as in [5] and [24]. First, the digital codes of $\mathrm{ADC_A}$ and $\mathrm{ADC_B}$ off-chip are divided into eight and seven channels by the demultiplexer (De-MUX). Then, the codes are averaged by the mean function in each channel, and the offset information is acquired [24]. Thus, the offset mismatch is removed in the digital domain with code subtraction. The gain error is obtained by moving average (MA) of absolute (ABS) values replacing the squaring operation to reduce the hardware overhead [5], as shown in Fig. 18, where

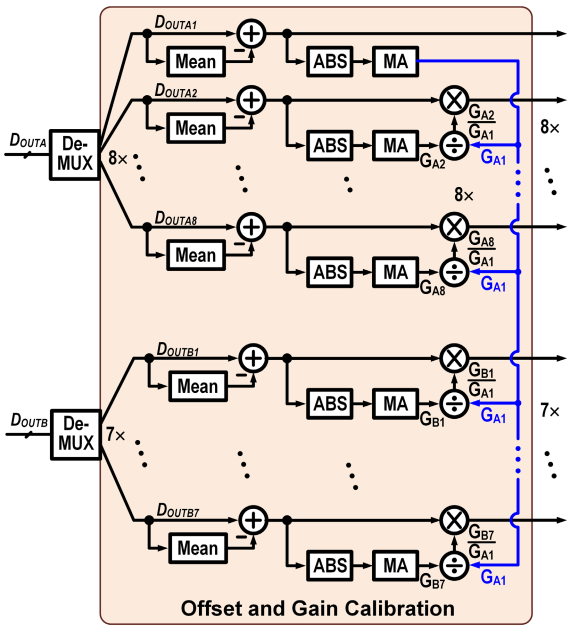

Fig. 18. Offset and gain calibration of seven-/eight-way split TI ADC.

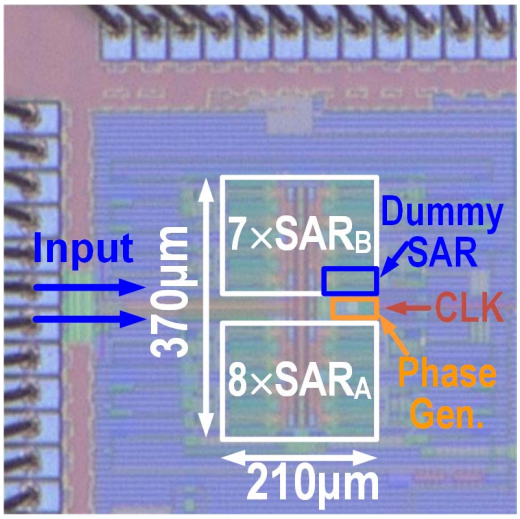

Fig. 19. Prototype ADC microphotograph.

G_{A1-A8} and G_{B1-B7} are the gain factors of ADC_{A1-A8} and ADC_{B1-B7}, respectively. Finally, the gain factors of all other channel ADC_{A2-A8} and ADC_{B1-B7} are normalized to ADC_{A1}.

VI. Experimental Results

The prototype seven-/eight-way split TI-SAR ADC, fabricated in 28-nm CMOS, occupies a core area of 370 × 210 μm^2, with the chip microphotograph shown in Fig. 19. The analog input and the clock are routed from the left and right to the center, then traveling to the 8 × ADC_A and 7 × ADC_B, respectively. We designed ADC_A and ADC_B with a similar layout except for some digital control logic circuits. We inserted a dummy SAR layout in the 7 × ADC_A to get a better matching regarding the boundary conditions, while most of this part (capacitor array of the dummy SAR) can connect as the decoupling capacitance, in order not to waste the dummy channel. The digital supply of the SAR logic and other digital control circuits is 0.8 V, while the analog supply of the clock generator, comparator, and DAC switches is 0.9 V in order to obtain sufficient linearity and low jitter of the input sampling. Besides, we also included the reference power in the analog part, because we use the analog supply directly as a reference. The total power consumption of the ADC core is 12.2 mW (S/H, comparator and DAC switches 51%, SAR logic and other digital control circuits 30%, and clock generator 19%). The gate counts for the digital background calibration are around 150k, which results in an estimated power consumption of 7.6 mW with a 0.8-V power supply and an area of 0.09 mm^2 in 28-nm CMOS. The total estimated power also includes the gain and offset calibration.

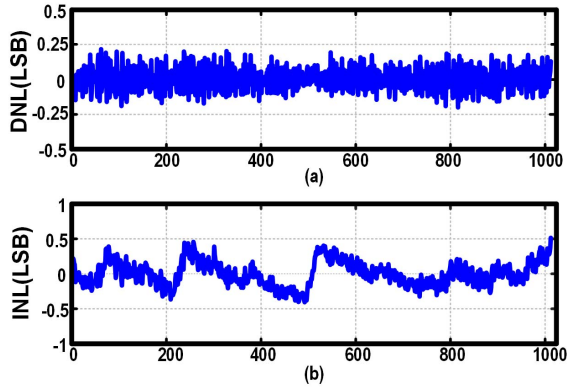

Fig. 20. Measured DNL and INL at a clock rate of 1.6 GS/s.

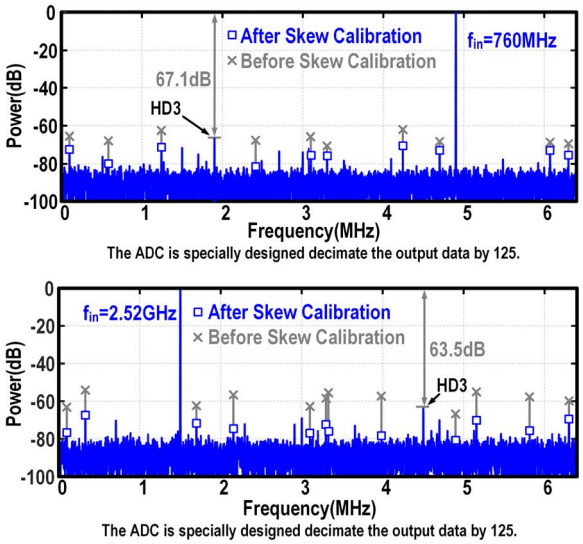

Fig. 21. Measured output spectrum with a sampling rate of 1.6 GS/s before and after skew calibration.

Fig. 20 shows the measured DNL and INL at 1.6 GS/s, indicating a maximum of 0.22 LSB for the former and 0.51 LSB for the latter. Fig. 21 shows the measured dynamic performance at 1.6 GS/s before and after timing mismatch calibration, indicating an SNDR/SFDR

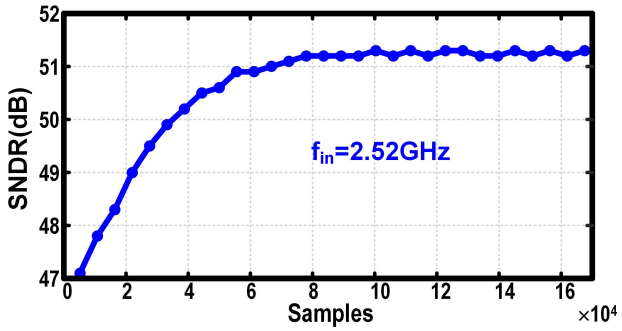

Fig. 22. Measured SNDR after skew calibration with an input of 2.52 GHz during convergence (seven-/eight-way split TI ADC).

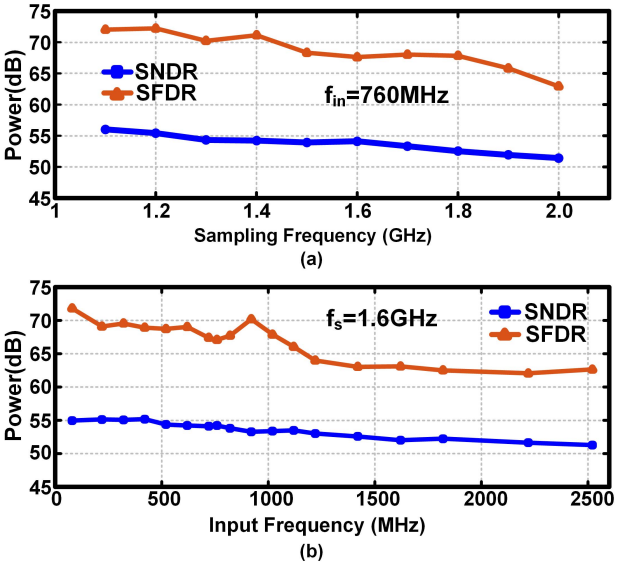

Fig. 23. Measured dynamic performance versus (a) sampling rate and (b) input frequency.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

	ISSCC-15 [25] H.-K. Hong	ISSCC-15 [26] B.-R.-S. Sung	JSSC-18 [3] C.-Y. Lin		VLSI-16 [13] Y.-C. Lien	VLSI-17 [12] Lei Luo	This Work	
Technology	45nm	45nm	40nm		16nm	16nm	28nm	
Architecture	TI-SAR	TI-FATI	TI-SAR		TI-SAR	TI-SAR	TI-SAR	
Resolution(bit)	10	10	10		10	10	10	
Speed(GS/s)	1.7	1.6	2.6		1.6	2.0	1.6	
Supply(V)	1.2	1.1	0.95		1.1	0.85/1.5	0.9/0.8	
Skew Correction	Analog	Analog	Digital		Analog	Analog	Digital	
SFDR@Nyq.(dB)	62.0	61.2	57.8		61	56	67.1	
SNDR@Nyq.(dB)	51.2	56.1	50.6		50.3	50.1	54.2	
SNDR@>Nyq.(dB)	NA	NA	NA		NA	NA	51.3@2.52GHz	
Power(mw)	15.4	17.3	18.4	39.2(1)	9.8	10.4	12.2	19.8(1)
Area(mm^2)	0.057	0.36	0.825	0.92(1)	0.023	0.014	0.078	0.168(1)
FOM@Nyq.(fJ/c.-s)	30.4	21	25.6	54.5(1)	19.2	19.9	18.2	29.5(1)
FOMS@Nyq.(dB)	158.6	162.8	159.1	155.8(1)	160.2	159.9	162.4	160.3(1)

(1)With estimated calibration power and area

of 54.2 dB/67.1 dB with a 760-MHz input signal and the SNDR/SFDR of 51.3 dB/63.5 dB at a 2.52-GHz input. Fig. 22 shows the measured SNDR with a 2.52-GHz input at 1.6 GS/s during the convergence of timing-skew calibration. The proposed calibration method improves the SNDR from 47 to 51.3 dB and converges within 80k samples.

Fig. 23(a) shows the dynamic performance versus sampling rate with a 760-MHz input signal. The SNDR exhibits a 3-dB variation from 0.7- to 2.5-GHz input frequency with a sampling rate of 1.6 GS/s [see Fig. 23(b)]. Table I shows the performance summary and a comparison with similar state-of-the-art TI-ADCs. The total power consumption with the estimated digital background mismatch calibration is 19.8 mW while reaching a Walden FOM of 29.5 fJ/conv.-step and a Schreier FOM of 160.3 dB at Nyquist.

VII. CONCLUSION

This article proposed a split TI ADC topology with digital background timing-skew calibration. The overall ADC consists of two parts: part A with eight TI channels and part B with seven channels. The errors between parts A and B are driven and minimized by the LMS adaptation engine. The use of a Hilbert transform filter extends the usable bandwidth of this article much beyond the first Nyquist band. Important advantages of this architecture are the constant ADC input impedance that does not cause extra spurs. Using the concept, a 1.6-GS/s seven-/eight-way split TI ADC achieves an SNDR of 54.2 dB and an SFDR of 67.1 dB at the Nyquist rate, simultaneously with an effective resolution bandwidth (ERBW) over 2.5 GHz.

ACKNOWLEDGMENT

The authors would like to thank their colleagues B. Wang, L. Qi, D. Jiang, S. Liu, W. Wang, and C. Fang from AMSV, University of Macau (UM), and W. Mo in Qualcomm, Shanghai, for technical supports and useful discussions.

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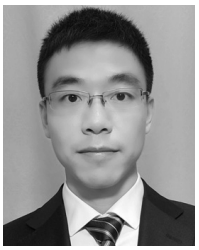

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Rui P. Martins (M'88–SM'99–F'08) was born in April 30, in 1957. He received the bachelor's, master's, and Ph.D. degrees and the Habilitation degree (Full Professor) in electrical engineering and computer science from the Department of Electrical and Computer Engineering (DECE), Instituto Superior Técnico (IST), Universidade de Lisboa, Lisbon, Portugal, in 1980, 1985, 1992, and 2001, respectively.

He has been with the Department of Electrical and Computer Engineering and the Instituto Superior Técnico, Universidade de Lisboa, since October 1980. Since 1992, he has been on leave from the Universidade de Lisboa and with the Department of Electrical and Computer Engineering, Faculty of Science and Technology (FST), University of Macau (UM), Macao, China, where he has been a Chair Professor since August 2013. In FST, he was the Dean of the Faculty, UM, from 1994 to 1997, where has been a Vice-Rector since 1997, was the Vice-Rector (Research) from September 2008 to August 2018, and has been the Vice-Rector (Global Affairs) since September 2018. In 2003, he founded the Analog and Mixed-Signal VLSI Research Laboratory, UM, elevated in January 2011 to the State Key Laboratory (SKLAB) of China (the first in Engineering in Macao), where he was the Founding Director. He was the Founding Chair of UMTEC (UM company) from January 2009 to March 2019, supporting the incubation and creation in 2018 of *Digifluidic,* the first UM Spin-Off, whose CEO is an SKLAB Ph.D. graduate. He was also the Co-Founder of Chipidea Microelectronics (currently Synopsys-Macao), Macao, from 2001 to 2002. Within the scope of his teaching and research activities, he has taught 21 bachelor's and master's courses and, in UM, has supervised (or cosupervised) 46 theses, Ph.D. (25) and masters (21). He has coauthored seven books and 11 book chapters; 33 patents, USA (30) and Taiwan (3); 497 articles, in scientific journals (184) and in conference proceedings (313); and other 64 academic works, in a total of 612 publications.

Dr. Martins was a recipient of the IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award in 2016. He received two Macao Government decorations: the Medal of Professional Merit (Portuguese-1999) and the Honorary Title of Value (Chinese-2001). In July 2010, he was elected, unanimously, as a Corresponding Member of the Lisbon Academy of Sciences, being the only Portuguese Academician living in Asia. He was the Founding Chair of the IEEE Macau Section from 2003 to 2005) and the IEEE Macau Joint-Chapter on Circuits And Systems (CAS)/Communications (COM) from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)], the General Chair of the IEEE Asia–Pacific Conference on CAS (APCCAS 2008) the Vice-President (VP) Region 10 (Asia, Australia, and Pacific) from 2009 to 2011, and the VP-World Regional Activities and Membership of IEEE CASS from 2012 to 2013. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS from 2010 to2013. He was nominated as the Best Associate Editor from 2012 to 2013. He was a member of the IEEE CASS Fellow Evaluation Committee (2013, 2014, and 2018—Chair, and 2019); the IEEE Nominating Committee of Division I Director (CASS/EDS/SSCS) in 2014, and the IEEE CASS Nominations Committee from 2016 to2017. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference (ASP-DAC 2016). He was the Vice President from 2005 to 2014 and the President from 2014 to 2017 of the Association of Portuguese Speaking Universities (AULP).