A 13-bit 8-kS/s Δ−Σ Readout IC Using ZCB Integrators With an Embedded Resistive Sensor Achieving 1.05-pJ/Conversion Step and a 65-dB PSRR

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***Abstract*— This paper reports on an energy-efficient Δ−Σ readout IC (ROIC) with a high power-supply-rejection ratio (PSRR). The static power consumption is minimized by applying a zero-crossing-based (ZCB) circuit to implement switched-capacitor (SC) integrators, while the resistive sensor is embedded inside the circuit to reuse the bias current. Oversampling Δ−Σ modulation also directly provides the digitized output, avoiding the need for a power-hungry instrumentation amplifier while preserving the linear settling behavior of the ZCB SC integrators. A dual-path bridge measurement aids in upholding PSRR of ROIC against bridge imbalance. Prototyped in 0.18-μm CMOS, the dual-path ROIC for the bridge measurement shows a nonlinearity of <400 ppm and an rms-noise-equivalent resolution of 13 bits at a conversion rate of 8 kS/s, corresponding to a figure of merit of 1.05-pJ/conversion step. The achieved noise-frequency-independent PSRR is 65 dB, and the supply and temperature sensitivities are 0.23%/V and 55 ppm/°C, respectively.**

***Index Terms*— CMOS, figure of merit (FoM), oversampling Δ−Σ modulation, power-supply rejection ratio (PSRR), readout IC (ROIC), resistive sensor, Wheatstone bridge, zero-crossing-based (ZCB) integrator.**

I. Introduction

TO ENABLE the smart sensing of environmental parameters in the Internet-of-Things (IoT) era, energy-efficient sensor readout ICs (ROICs) [1]–[8] are critical, and it is desirable for them to use the harvested energy to achieve the autonomous operation [6]–[8]. One key challenge is that the typical energy-harvesting units comprising a rectifier usually result in a scarcity of energy and large variations in the supply voltage. As a result, while miniaturized resistive sensors are broadly utilized for temperature, pressure, and humidity sensing, there is an essential need to develop an energy-efficient resistive ROIC that can provide high resolution and a high power-supply rejection ratio (PSRR).

A Wheatstone bridge can assist in enhancing PSRR of a resistive ROIC [9]–[15]. However, the related challenges are threefold.

1) Since the bridge resistance must be low (1–10 kΩ [14]), static power consumption cannot be avoided; for example, 42% of the total power consumption in [10] is due to the bridge.
2) To provide a stable voltage gain and linear settling behavior for a subsequent switched-capacitor (SC) analog-to-digital converter, a power-hungry instrumentation amplifier (IA) is necessary [10]–[13].
3) The achievable PSRR is sensitive to the balancing quality of the bridge elements; a 5% imbalance can penalize PSRR to ∼30 dB. Improving PSRR by adding a supply-voltage regulator with a bandgap is also undesirable because it is always power hungry and reduces the voltage headroom available for signal swings [15].

An alternative means of improving PSRR is to use a phase-locked loop-based force-balancing mechanism to keep the Wheatstone bridge in its balanced position [15]. However, the measured resolution achieved with this approach has been found to be limited to 10 bits due to the phase noise (jitter) of the voltage-controlled oscillator.

This paper details a Δ−Σ ROIC with energy-efficient zero-crossing-based (ZCB) SC integrators to prevent the need for any operational transconductance amplifier (OTA). Unlike the original ZCB SC integrator [16]–[19], our topology is tailored to embed the resistive sensor inside the Δ−Σ modulation loop while being compatible with both single-element-mode [20] and bridge-mode measurements. As such, the bias current of the resistive sensor is fully nullified, further improving the power efficiency of the proposed ROIC. Our dual-path bridge-mode measurement also aids upholding PSRR against bridge imbalance. Finally, since oversampling Δ−Σ modulation directly produces a digitized output, there is no need

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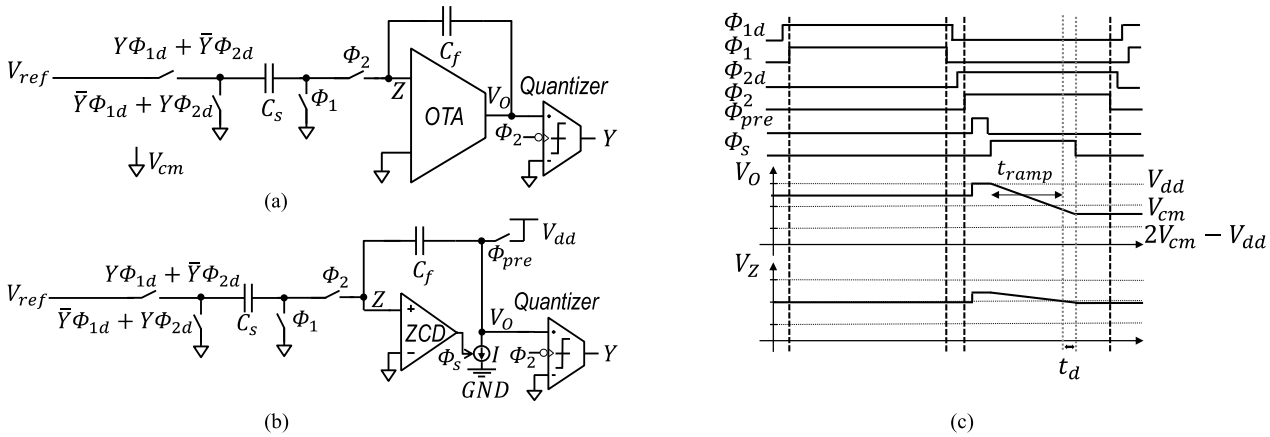


Fig. 1. SC integrator. (a) OTA-based, (b) ZCB, and (c) timing scheme and ramp-down settling behavior, where Φ_1, Φ_{1d}, Φ_2, and Φ_{2d} are the nonoverlapping clocks for the bottom-plate sampling and the clock frequency is F_s.

for a power-hungry IA, and the linear settling behavior of the ZCB integrators is preserved. With an extensive analysis on the circuit nonidealities, to be presented later, the performance of the resistive ROIC is mainly limited by the tradeoff between the power and noise (resolution). Furthermore, our resistive ROIC is compatible with its capacitive counterpart [21], and these two devices can be combined to realize a hardware-efficient generic ROIC for both capacitive and resistive sensors.

Following this introduction, Section II describes the proposed resistive ROIC and its operating principle. Section III details the circuit implementation and analyzes its circuit nonidealities. The measurement results are discussed in Section IV, and finally, conclusions are drawn in Section V.

II. Proposed Resistive ROIC

A. OTA-Based and ZCB SC Integrators

First, we consider the OTA-based SC integrator [Fig. 1(a)]. The charge on C_s that depends on the value of Y is transferred to the integration capacitor C_f every cycle. By some special arrangements for the switching scheme, when $Y = 1$ or 0, the charge should be $C_s(V_{\text{ref}} - V_{\text{cm}})$ or $C_s(V_{\text{cm}} - V_{\text{ref}})$, where V_{ref} and V_{cm} are the reference and common-mode voltages, respectively. Together with the quantizer, putting this integrator inside the oversampling Δ–Σ modulation loop keeps updating Y at the falling edge of Φ_2, forcing the average value of Q_z from C_s to approach zero [22] as given by

$$Q_z = (V_{\text{ref}} - V_{\text{cm}}) \cdot C_s \cdot N(1) + (V_{\text{cm}} - V_{\text{ref}}) \cdot C_s \cdot N(0) = 0 \tag{1}$$

where $N(1)$ and $N(0)$ are the number of 1s or 0s in the single-bit output stream Y, respectively, and $N = N(1) + N(0)$. The average value of Y is given by

$$Y_{\text{ave}} = \frac{N(1)}{N} = \frac{1}{2} \tag{2}$$

which can be obtained from the output of the decimation filter following the Δ–Σ modulator.

As a counterpart, we replace the OTA-based SC integrator with the ZCB one [21] as depicted in Fig. 1(b). To preset V_z above V_{cm}, V_o is first pulled to the supply voltage V_{dd} in a short preset phase Φ_{pre}. Next, current source I is switched ON for the integrator to settle [Fig. 1(c)]. The zero-crossing detector (ZCD) senses the virtual ground condition ($V_z = V_{\text{cm}}$) and turns off the current source, and induces a delay t_d. At this instant, the same virtual ground condition is obtained as in the OTA-based circuit. As a result, Y_{ave} (=1/2) becomes identical to that of its OTA-based counterpart.

B. Proposed Resistive ROIC—Single-Element Measurement

As Fig. 2(a) shows, the proposed resistive ROIC consists of several parts. The SC branch and the Δ–Σ modulator force the average value of Q_z from C_s to approach zero. In the Δ–Σ modulator, OTA-based SC integrators are replaced by ZCB SC integrators but with the new switching scheme. Moreover, current source I here is used not only to settle the output of the integrator but also to bias the embedded resistive sensor R_s (connected across the two square terminal points in the diagram), producing a voltage drop $V_{R_s} = I \cdot R_s$. The charge Q_z transferred to C_f from C_s should be $(V_{\text{ref}} - V_{\text{cm}} + V_{R_s}) \cdot C_s$ or $(V_{\text{cm}} - V_{\text{ref}} + V_{R_s}) \cdot C_s$ when $Y = 1$ or 0 [Fig. 2(b) and (c)], respectively. Thus, we have

$$[(V_{\text{ref}} - V_{\text{cm}} + V_{R_s}) \cdot Y + (V_{\text{cm}} - V_{\text{ref}} + V_{R_s}) \cdot (1 - Y)] \cdot \frac{C_s/C_f \cdot z^{-1}}{1 - z^{-1}} + E(z) = Y \tag{3}$$

where $E(z)$ is the quantization noise from the quantizer.

The signal transfer function is

$$\text{STF} = \frac{C_s/C_f \cdot z^{-1}}{1 + 2(C_s/C_f \cdot (V_{\text{cm}} - V_{\text{ref}}) - 1/2) \cdot z^{-1}}. \tag{4}$$

The noise transfer function is

$$\text{NTF} = \frac{1 - z^{-1}}{1 + 2(C_s/C_f(V_{\text{cm}} - V_{\text{ref}}) - 1/2)z^{-1}} \tag{5}$$

when $V_{\text{cm}} - V_{\text{ref}} = 1/2 \text{and} C_s/C_f = 1$, then $\text{STF} = z^{-1}$ and $\text{NTF} = 1 - z^{-1}$, which is attributed to the first-order noise shaping by the Δ–Σ modulation loop.

Therefore, without considering the noise, the average value of Y is given by

$$Y_{\text{ave}} = \frac{1}{2} + \frac{V_{R_s}}{2 \cdot (V_{\text{cm}} - V_{\text{ref}})}. \tag{6}$$

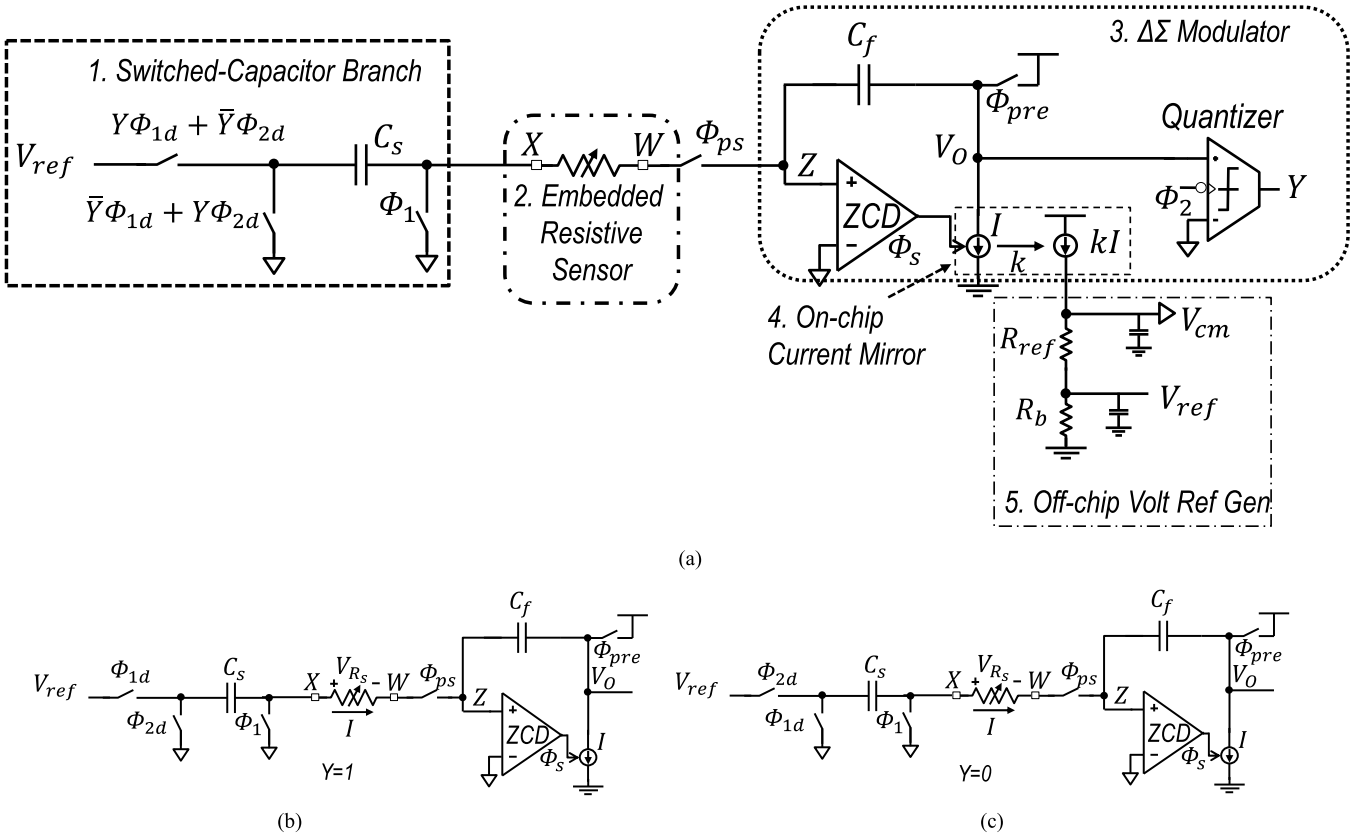


Fig. 2. Proposed resistive ROIC for the single-element measurement. (a) Switching scheme. The configurations of the first ZCD integrator of the Δ–Σ modulator when (b) $Y = 1$ and (c) $Y = 0$.

With the current mirror and the voltage reference generator, $V_{\rm cm} - V_{\rm ref} = k \cdot I \cdot R_{\rm ref}$; then

$$Y_{\rm ave} = \frac{1}{2} + \frac{R_s}{2 \cdot k \cdot R_{\rm ref}} \tag{7}$$

where k is the current mirror parameter and $R_{\rm ref}$ is the reference resistor with a constant value. This expression implies that the measured variation in $Y_{\rm ave}$ is the ratio of sensing resistance R_s to reference resistance $R_{\rm ref}$, which is independent of any voltage and current parameters, inherently enhancing PSRR and temperature sensitivity performance. The limited accuracy of $R_{\rm ref}$ and k will lead to the gain error of $Y_{\rm ave}$. The calibrations in the digital domain are entailed to reduce the gain error and improve the accuracy of the read-out circuit output. Because $0 < Y_{\rm ave} < 1$, design parameters k and $R_{\rm ref}$ must be selected in accordance with the nominal resistance R_o and the variation range ΔR_s, where $R_s = R_o + \Delta R_s$.

C. Proposed Resistive ROIC—Bridge-Mode Measurement

A conventional Wheatstone bridge with two resistive biasing branches is shown in Fig. 3(a), where $V_p - V_n = V_{p+} - V_{p-} - V_{n+} + V_{n-} = \Delta R_s / R_o \cdot V_{dd}$, which clearly depends on V_{dd}. To improve PSRR in the case of unbalanced bridge elements, the conventional bridge can be reconfigured as shown in Fig. 3(b). The two resistive branches are measured simultaneously in the single-element mode to obtain two digital outputs, $Y_{{\rm ave},p}$ and $Y_{{\rm ave},n}$, and we can take the difference of them as follows:

$$Y_{{\rm ave},p} - Y_{{\rm ave},n} = \frac{2}{k} \cdot \frac{\Delta R_s}{R_{\rm ref}}. \tag{8}$$

This expression shows that ΔR_s from the bridge can also be observed from the difference in the average outputs of the two measurements in the digital domain. This pseudodifferential implementation further improves PSRR and the supply and temperature sensitivities compared with the single-element measurement mode, as experimentally demonstrated in Section IV.

To roughly quantify the figure-of-merit (FoM) advantage of the proposed ROIC, we compare it with the conventional design presented in [13], which consists of a capacitively coupled IA (CCIA) followed by a continuous-time Δ–Σ modulator. Given the same speed of operation and the same supply voltage, the FoM differences between this work and [13] are mainly associated with the noise bandwidth, the noise power spectral density (PSD), and the static current consumption. To simplify the analysis, only the static power consumption of CCIA and bridge is considered for [13], whereas only the first stage of ZCD is considered for this paper. The power consumed by the dynamic SC charging current and the latch of ZCD is negligible. In addition, the power consumptions of the circuit that drives the initial sampling capacitance and the decimation filter are ignored.

1) Noise Bandwidth: Similar to the analysis in [23], the ratio of the CCIA noise bandwidth ($\rm NBW_{CCIA}$) to the ZCD noise

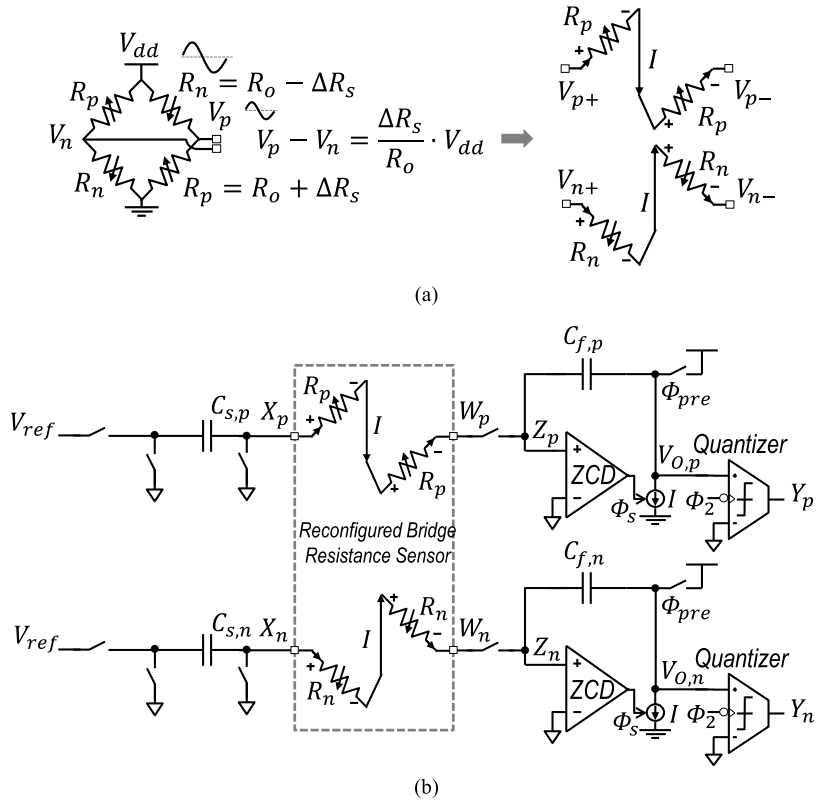


Fig. 3. Proposed resistive ROIC for the bridge measurement. (a) Bridge. (b) Configurations.

bandwidth (NBW_{ZCB}) in terms of the defined parameters is given by

$$\frac{\text{NBW}_{\text{CCIA}}}{\text{NBW}_{\text{ZCB}}} = \frac{\alpha \cdot m}{2} \tag{9}$$

where CCIA typically requires 10–15 (m) time constants to settle, depending on the resolution, and t_i can be made to be approximately 0.22 (α) of the half clock cycle. As a result, NBW_{CCIA} is $\sim$1.3$\times$ larger than NBW_{ZCB}.

2) Noise PSD: To ease the design tradeoffs and achieve a high gain, a two-stage Miller amplifier with a folded-cascode input stage is often employed [13], [24]. When the noise contributions of both the input and output stages of the amplifier are considered, there is an equivalent of eight devices contributing to the input-referred noise. By contrast, ZCD has only an equivalent of four devices contributing to the input-referred noise, resulting in an $\sim$2$\times$ lower input-referred PSD.

3) Static Current Consumption: For a two-stage Miller amplifier with a folded-cascode input stage as discussed above, there is an equivalent of six current branches for the input devices. Under the assumption of the same current for the input devices in ZCD, it has only an equivalent of two current branches and is active for only a duration of $T_s/4$ on average. The bridge in the traditional design consumes an equivalent of four extra current branches. This implies that the static current consumption of the design presented in this paper is $\sim$10$\times$ lower overall [considering the two resistive branch measurements shown in Fig. 3(b)]. As a result, our resistive ROIC can ideally achieve an FoM that is 13$\times$ better than that of the conventional design [13].

III. Circuit Implementation and Nonidealities

The resistive ROIC is based on a second-order oversampling $\Delta-\Sigma$ modulator. Its simplified schematic (for one path) is shown in Fig. 4. To realize the bilinear function of the second stage without feedback from Y [22], two identical capacitors $C_{i1,A}$ and $C_{i1,B}$ are used to sample the first-stage integration result in phases Φ_{2A} and Φ_{2B}, respectively, and perform the second-stage integration in phases Φ_{1A} and Φ_{1B}, respectively. Because of the first-stage noise shaping behavior, the mismatch between $C_{i1,A}$ and $C_{i1,B}$ is insignificant. The reference voltages V_{ref} and V_{cm} are generated by a voltage reference generator, as shown in Fig. 4, with off-chip R_{ref} and R_b and decoupling capacitors to suppress the noise induced in the supply and reference voltages [24]. To reduce the biasing current of the kI branch (e.g., microampere level), large resistance values of R_b and R_{ref} are needed (e.g., hundreds of kilohm levels). Then, the sampling behavior on C_s (e.g., picofarad level) is mainly attributed to the off-chip decoupling capacitor (e.g., microfarad level). As a result, the settling error on C_s should be tiny by the charging share between the decoupling capacitor and C_s and is signal independent on the variation range of R_s. The current sources are nMOS-based cascoded current sources with enable switches, as in [16], and these current sources were checked over a range of V_o for various design corners to ensure that the noise induced by the current source's finite output resistance is negligible, as described in (20). Moreover, the layout of the current sources in the two channels [see Fig. 3(b)] was treated with care to minimize the mismatch. The ON-resistance of the switch was designed to lie within the range of 100–300 Ω.

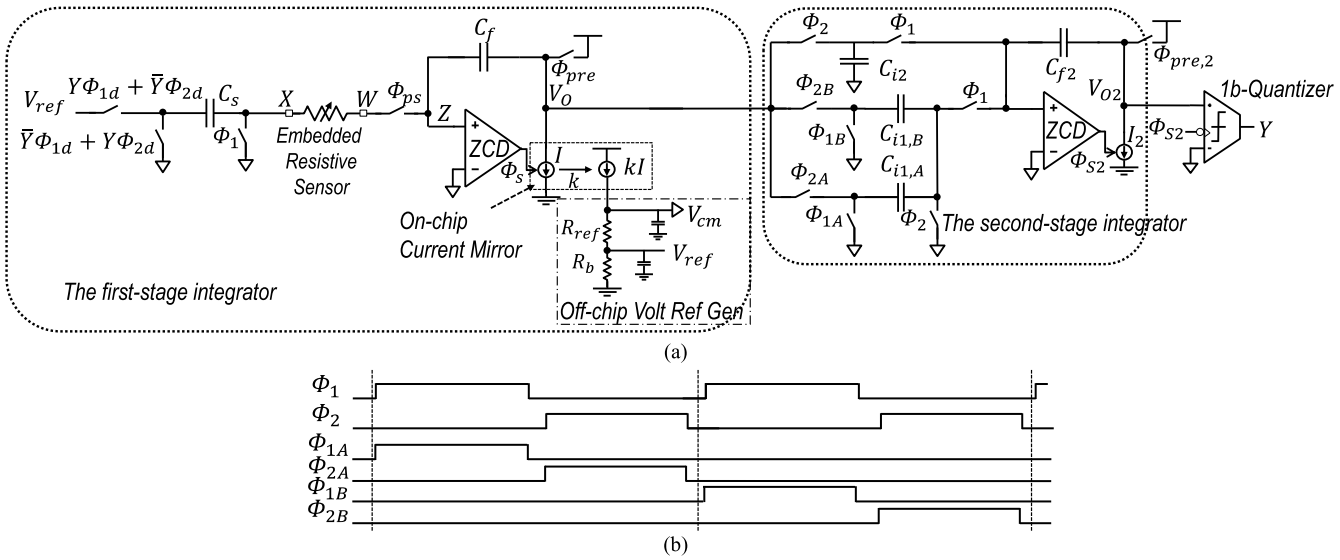


Fig. 4. Simplified circuit diagram for one path of ROIC. (a) Circuit. (b) Switching scheme.

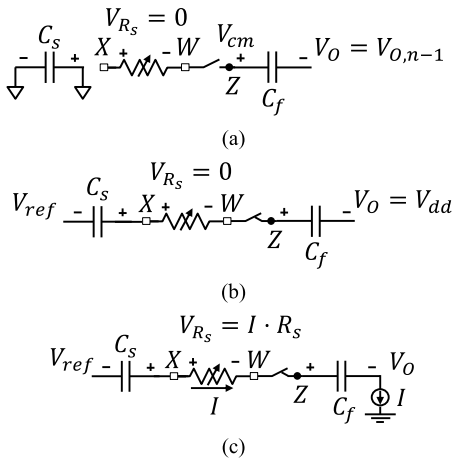


Fig. 5. Switching scheme with $Y = 0$. (a) Φ_1. (b) At the end of Φ_{pre}. (c) At the beginning of Φ_s.

ZCD is a differential-to-single-ended preamplifier followed by a dynamic threshold-detecting latch [17]. To mitigate the impact of $1/f$ noise, choppers are applied across the first preamplifier stage [25], [26]. The chopper frequency is $F_s/8$.

A. Presetting in the ZCB Integrator

To ensure proper settling behavior of the ZCB integrator, during the short preset phase Φ_{pre}, V_z must be preset above V_{cm} by shorting V_O–V_{dd}. However, there are two challenges. One is C_s, which is cleared in Φ_1, as shown in Fig. 5(a), and pulls down V_z by shorting to V_{ref} (under the assumption that $V_{\text{ref}} < V_{\text{cm}}$) in Φ_{pre}, as shown in Fig. 5(b). The other is the voltage drop V_{R_s} induced in R_s by I, which drops V_z down from V_X at the beginning of Φ_s, as shown in Fig. 5(c). By the conservation of the charge on the combination of nodes X and Z, V_z at the beginning of Φ_s must be higher than V_{cm}. Thus, the design parameters must satisfy

$$\frac{C_f}{C_s}(V_{dd} - V_{o,\max}) > (V_{\text{cm}} - V_{\text{ref}}) + \left(1 + \frac{C_f}{C_s}\right) \cdot V_{R_s} \quad (10)$$

where $V_{o,\max}$ can be determined through the behavioral-level simulation of the equivalent Δ−Σ modulator. Moreover, only the worst case with $Y = 0$ is considered. This is because when $V_{\text{ref}} < V_{\text{cm}}$, the switching scheme on C_s with $Y = 1$ will pull V_z up instead.

B. Energy and Noise Analyses

Similar to the energy analysis in [21], the energy of the first-stage integrator dominates. The main energy $\overline{E_{\text{ZCBC}}}$ in every cycle consists of two parts: the dynamic energy $\overline{E_{\text{dyn,cap}}}$ of the capacitors' charging and discharging behaviors in the first-stage integrator and the ZCD energy $\overline{E_{\text{ZCD}}}$.

With the switching scheme shown in Fig. 2(a), the dynamic energy $\overline{E_{\text{dyn,cap}}}$, which originates from various power sources (V_{DD}, V_{ref}, and V_{cm}), can be presented as follows:

$$\overline{E_{\text{dyn,cap}}} = \left((V_{\text{cm}} - V_{\text{ref}})^2 - V_{R_s}^2\right) \cdot C_s + V_{dd} \cdot (V_{dd} - V_{\text{cm}} - V_{R_s}) \cdot C_s \cdot C_f/(C_s + C_f). \quad (11)$$

The static energy of the preamplifier dominates $\overline{E_{\text{ZCD}}}$. Because its static current is turned on only when ZCD is active and is turned off after the detection of zero crossing, we can deduce that

$$\overline{E_{\text{ZCD}}} \approx V_{dd} \cdot I_{\text{amp}} \cdot \left(\frac{T_s}{4} + t_d\right) \quad (12)$$

where I_{amp} is the dc-biasing current of the preamplifier and $T_s = 1/F_s$ is the clock period.

Similar to the noise analysis in [21], the noise of the first stage dominates, and the two main thermal noise sources are the sensor and switch resistances and ZCD

$$N_{\text{ZCBC}} = N_{\frac{kT}{C}} + N_{\text{ZCD}} = \left(\frac{2kT}{C_s} + \frac{8kT \cdot \gamma}{g_m \cdot t_i}\right) \cdot \frac{1}{\text{OSR}} \quad (13)$$

where k is Boltzmann's constant, T is the temperature, γ is a noise parameter, g_m is the transconductance of the MOSFETs in the preamplifier, and t_i is the preamplifier integration time required for the preamplifier output to undergo

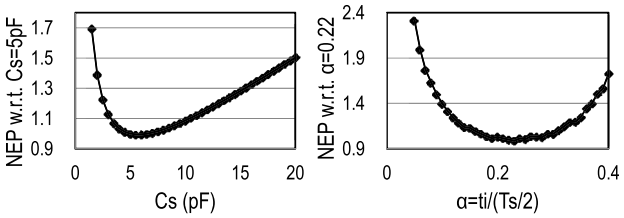


Fig. 6. Simulated NEP results with varying values of two parameters. (a) C_s. (b) α.

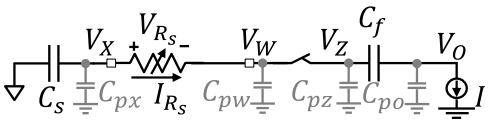


Fig. 7. Parasitic capacitance in Φ_s.

a transition $|\Delta V|$ from V_{dd} in the preset state (Φ_{pre}) to the latch threshold [23]. Because the latch delay is negligible, we find that $t_i \approx t_d$.

C. Design Tradeoffs

Based on the above analysis, the performance of the resistive ROIC should be subject to a tradeoff in terms of power and noise (resolution), which depends on two important design parameters, C_s and t_i. First, a larger C_s results in the lower noise, as seen from (13), but will cause more energy consumption according to (11). Second, lower noise can be obtained with a larger t_i according to (13), which means that a shorter ramping time t_{ramp} remains and a larger current source I is needed for complete settling. However, a larger I also yields a larger V_{R_s}, which in turn results in a larger V_{dd} to satisfy (10), so the required energy also increases.

The noise–energy product (NEP) of ROIC can be calculated from (10) to (13) as follows:

$$\text{NEP}_{\text{ZCBC}} = N_{\text{ZCBC}} \cdot (\overline{E_{\text{dyn,cap}}} + \overline{E_{\text{ZCD}}}). \tag{14}$$

To minimize NEP, simulations were performed to sweep different values of C_s and α ($t_i = \alpha T_s/2$). The results shown in Fig. 6 suggest that $C_s = 5$ pF and $\alpha = 0.22$ are the optimal parameters for the circuit implementation. Moreover, for the process variations on C_s and α, e.g., 10% absolute variation, the optimal NEP will not be damaged.

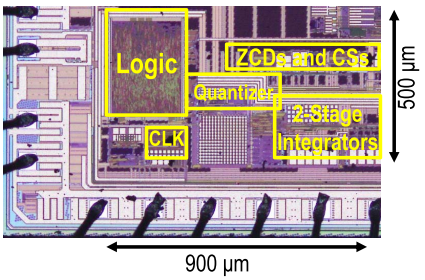
D. Circuit Nonidealities

Ideally, current source I will flow completely through R_s in Φ_s; i.e., $I_{R_s} = I$. However, some portion of I will be shunted by the parasitic capacitances C_{px}, C_{pw}, C_{pz}, and C_{po}, as shown in Fig. 7, resulting in $I_{R_s} \neq I$. Taking I_{R_s} and R_s as constant within an infinitesimal time interval dt, which approaches zero, we obtain

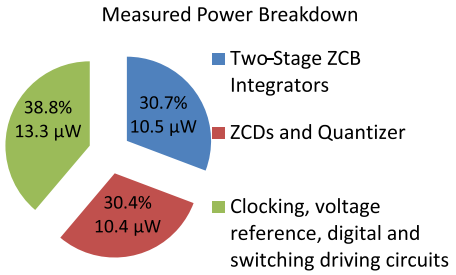
$$dV_X = dV_W = dV_Z. \tag{15}$$

The conservation of charge on the combination of nodes X, W, and Z can be expressed as follows:

$$dV_X \cdot (C_s + C_{px}) + dV_W \cdot C_{pw} + dV_Z \cdot C_{pz} + (dV_Z - dV_O) \cdot C_f = 0. \tag{16}$$



(a)



(b)

Fig. 8. (a) Photograph of the ROIC chip (one path) and (b) its power breakdown.

Considering I and I_{R_s}, respectively, we have

$$I \cdot dt = dV_O \cdot C_{po} + (dV_O - dV_Z) \cdot C_f \tag{17}$$

$$I_{R_s} \cdot dt = dV_X \cdot (C_s + C_{px}). \tag{18}$$

The I_{R_s}-to-I ratio can be obtained by combining (15)–(18)

$$\frac{I_{R_s}}{I} = \frac{C_s + C_{px}}{(C_s + C_{px} + C_{pw} + C_{pz}) \cdot (1 + C_{po}/C_f) + C_{po}}. \tag{19}$$

This expression shows that the I_{R_s}-to-I ratio is independent of sensing resistance R_s. Since C_s, C_f, and the parasitic capacitances are constant during the measurement, they will not cause the degradation in the linearity performance when R_s varies.

In practice, current source I will have a finite resistance, which will lead to a varying current ($I[n] = \overline{I} + \Delta I[n]$) in the nth cycle with different $V_o[n]$ values. Similar to the analysis in [21], the signal to the input-referred noise error power induced by this nonideality can be calculated as follows:

$$\text{SNR}_{CS} = 1/\frac{\Delta^2}{12 \cdot N} \tag{20}$$

where $\Delta = \max((\sum_{n=1}^{N} \Delta I[n]/\overline{I})/N) - \min((\sum_{n=1}^{N} \Delta I[n]/\overline{I})/N)$ and N denotes the oversampling ratio (OSR). Hence, (20) provides a design guideline for ensuring that the error induced by the current source's finite output resistance will be negligible.

Moreover, the finite ZCD delay t_d and the ZCD offset V_{off} can also cause the voltage overshoot on nodes O and Z [21]. This will induce an offset error in the ROIC output, which can be easily canceled out in the postdigital processing. For example, various R_s can be measured by ROIC, and with linear regression, the offset error for ROIC can be characterized and canceled easily.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	[29] TCASI 14	[15] JSSC 13	[10] TCASI 17	[9] VLSI 17	[13] ISSCC 17	[14] ISSCC 18	This work	
Technology	0.18 µm	0.13 µm	65 nm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	
Method	SAR	BBPLL	Switched-Capacitor	SCΔΣM	CCIA+CTΔΣM	Pulse+SAR ADC	ΔΣ+ ZCBC	
Resistive Meas. Mode	Single Element	Bridge	Bridge	Bridge	Bridge	Bridge	Single-Element	Bridge
Measured Range (Ω or %)	49.5 k~98 k	±10%	±1.875%	±0.889%	±0.2%	±1.889%	0.5 k~4.5 k	±5%
Speed (kS/s)	5.5	20	2	1	2	1	8	8
Meas. Error (%)	N/A	0.21	0.15	N/A	0.0028	N/A	0.025	0.04
Supply Voltage Variation (%/V)	0.65	2.33	N/A	N/A	N/A	6.8	1	0.23
PSRR (dB)	N/A	52	64	N/A	N/A	N/A	45	65
Temperature Dependence (ppm/℃)	58.6	56	N/A	N/A	8.9	N/A	216	55
SNR (dB)	48.1	64.4	55.6	59	95.5	49.2	80 [2]/1.2 [3]	78.8 [2]/1.2 [3]
Energy/Conv. include Bridge (nJ/Conv)	2.73	6.23	6.15	290	4870 [1]	2.5	4.39 [1,2] /0.19 [3]	7.5 [1,2] /0.26 [3]
FoMW [pJ/c-s]	13.1	4.59	12.5	398	100	10.6	0.54	1.05
FoMS (dB)	130.7	143.4	134.7	121.4	145.6	132.2	160.6	157
Percentage of Bridge Power in Total Power (%)	26	40.2	42.3	64.1	77.8	20	0	0
Decoupling Capacitor needed	On-chip	No need	No need	Off-chip/ 1 µF	N/A	On-chip/ 1.2 nF	Off-chip/ 0.1 µF	Off-chip/ 0.1 µF

1.The power of the digital decimation filter is not included.
2.The mean value of measured results for 10 chips.
3.The standard deviation of measured results for ten chips.
4.N/A means that the performance has not been reported in the paper.

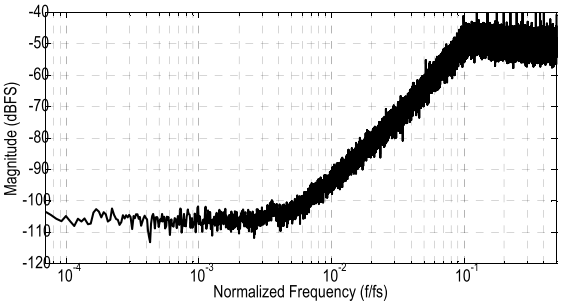


Fig. 9. Measured PSD of the ROIC output.

IV. MEASUREMENT RESULTS

Fig. 8(a) shows a photograph of the proposed ROIC chip (one path). The die area occupied by the design blocks for dual paths is ∼0.4 mm^2. Ten packaged chips were measured, and the mean values and standard deviations are included in Table I, which show that the performances of ten chips are found to be similar.

A. Single-Element Measurement

Fig. 9 shows the measured output PSD before off-chip decimation filtering. The noise shaping is attributed to the second-order Δ−Σ modulation, and the signal-to-noise ratio (SNR = 10 × log$_{10}$(Measured Fullscale Resistance Signal Power/Measured rms error power on Resistance)) is ∼80 dB with a conversion time of 128 μs, an OSR of 128, and an rms-noise-equivalent resolution, $R = (\text{SNR} - 1.76)/6.02$, of ∼13 bits. Power $\overline{P}$ is ∼34.3 μW, including the contribution from the off-chip voltage reference generator, and its breakdown is shown in Fig. 8(b). Fig. 8(b) shows that 30.7% of the power is consumed by the two-stage ZCB integrators. The power consumed in both ZCDs and quantizer is ∼30.4%, and the remaining power consumption is due to the clock, off-chip-voltage reference, digital logic, and switch-driving circuits.

To characterize the linearity of ROIC, an Accutrim 1242 21-turn trimmer (i.e., a variable resistor) [27] was measured at various resistance values ranging from 0.5 to 4.5 kΩ. Each resistance was measured first with a Keysight 34410A 6½-bit digital multimeter (R_{34410A}), which gives a nominal reading with a resistance measurement inaccuracy of <50 ppm [28] and then with our ROIC. The measured transfer characteristics are shown in Fig. 10(a), and the nonlinearity shown in Fig. 10(b) is defined as

$$\text{Nonlinearity}(\%) = \frac{R_{\text{ROIC}} - R_{34410\text{A}}}{R_{\text{full-scale}}} \times 100\% \qquad (21)$$

where $R_{\text{full-scale}}$ is the full-scale measurable resistance value. Similar to the definition in [10], the proposed ROIC was found to exhibit a good nonlinearity of <0.025% (i.e., 250 ppm). The measured rms-noise-equivalent resolutions are shown in Fig. 10(c). The resolutions are almost constant under various R_s, which verifies the noise analysis model by (13) that is independent of R_s. To verify the power analysis model by (11), the measured total power consumptions with resis-

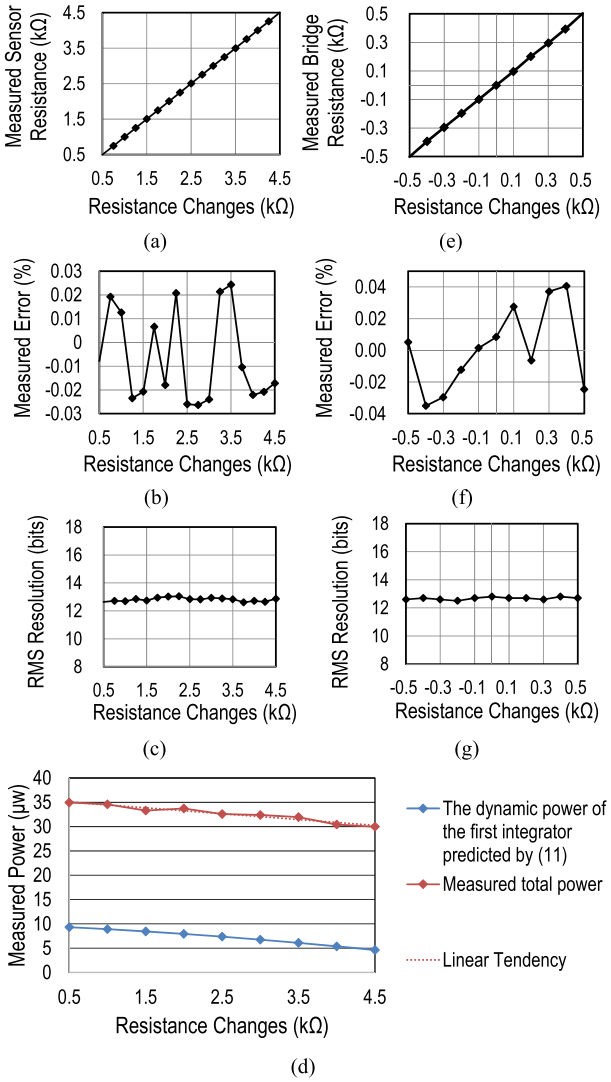


Fig. 10. Measured results with a varying single-element resistance for (a) transfer characteristics; (b) nonlinearity; (c) rms-noise-equivalent resolution; and (d) total power consumption. Measured results with a varying bridge resistance for (e) transfer characteristics; (f) nonlinearity; and (g) rms-noise-equivalent resolution.

tance changes have been shown in Fig. 10(d), which proves that the measured total power consumptions have the same tendency as the dynamic power of the first integrator predicted by (11).

B. Bridge Measurement

To investigate the behavior in the bridge mode, two Accutrim 1242 trimmers, whose values were varied in opposite directions to obtain differences ranging from -0.5 to 0.5 kΩ (the maximum variation $\Delta R/R$ for the emulated bridge was $\pm 5\%$), were measured with our ROIC using the bridge scheme shown in Fig. 3(b). Fig. 10(e) shows the measured transfer characteristics, and Fig. 10(f) shows a good nonlinearity of $<0.04\%$ (i.e., 400 ppm) in the bridge mode. The measured rms-noise-equivalent resolutions are also shown in Fig. 10(g). The total power consumption is $\sim 58.6\ \mu$W.

C. Supply Voltage Sensitivity

To analyze the performance as a function of the supply voltage, both static and dynamic measurements were performed.

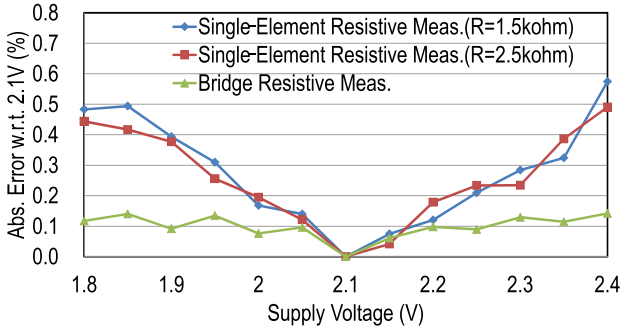


Fig. 11. Measured absolute errors under various supply voltages.

Static measurements were performed under various supply voltages, as shown in Fig. 11. For the single-element mode with $R_s = 1.5$ or 2.5 kΩ, a maximum absolute error of 0.6% with respect to the value at the 2.1-V supply was obtained under supply voltages ranging from 1.8 to 2.4 V, resulting in a sensitivity of 1%/V. By contrast, a maximum absolute error of 0.14% was obtained for the bridge mode, resulting in an improved sensitivity of 0.23%/V.

The dynamic measurements are shown in Fig. 12, where the measured digital output spectra are shown for both the single-element and bridge modes, with -10-dBFS 6-kHz sinusoid supply noise added to the 2.1-V dc supply. The noise was analyzed only for the in-band frequency spectrum since higher frequencies were digitally filtered out by the subsequent decimation filter. The supply noise amplitude was normalized to the full-scale reference of ROIC, which means that the gain of the power supply to the digital output was equal to PSRR [15]. Fig. 13 shows the plot of PSRR as a function of the frequency at a supply noise amplitude of -10 dBFS and as a function of the supply noise amplitude at a frequency of 1 kHz. The measured PSRR was improved by >20 dB (up to ~ 65 dB) in the proposed bridge mode, consistent with the results of the above static measurements.

D. Temperature Sensitivity

The temperature dependence of ROIC was measured with an Accutrim 1242 trimmer emulating the sensor. Thus, the measurement results include only the temperature dependence of the circuit itself, excluding any dependence on the resistive sensor [15]. In Fig. 14, the measured maximum absolute output error is plotted as a function of the temperature from -20 °C to 120 °C. For the single-element mode, a maximum absolute error of 3% with respect to 50 °C was measured over this 140 °C range. This error corresponds to ~ 216 ppm/°C and shows that ROIC is affected by temperature variations in the on-chip current source I. However, the error is improved to 55 ppm/°C in the bridge mode.

E. Performance Comparison

Table I summarizes the performance of the proposed ROIC and compares it with other state-of-the-art resistive ROICs. FoMs (FoM_W and FoM_S), which represent the normalized energy consumption with respect to SNR, are given by the

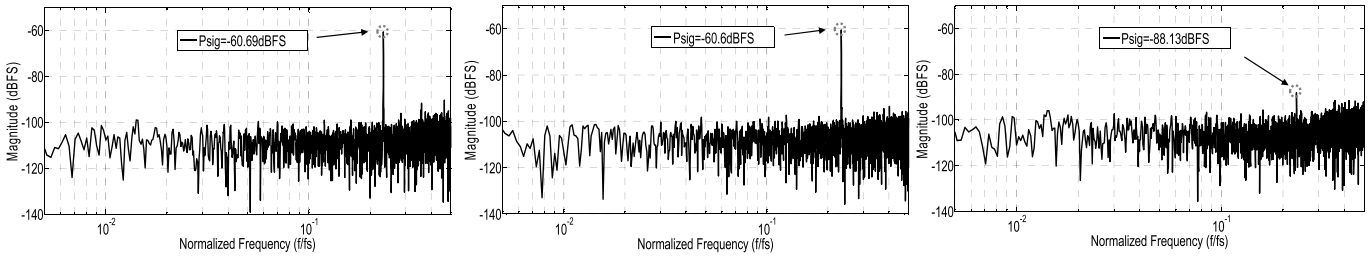


Fig. 12. Measured PSDs with −10-dBFS 6-kHz supply noise. (a) Single-element resistive measurement with $R_S = 1.5$ kΩ. (b) Single-element resistive measurement with $R_S = 2.5$ kΩ. (c) Bridge resistive measurement.

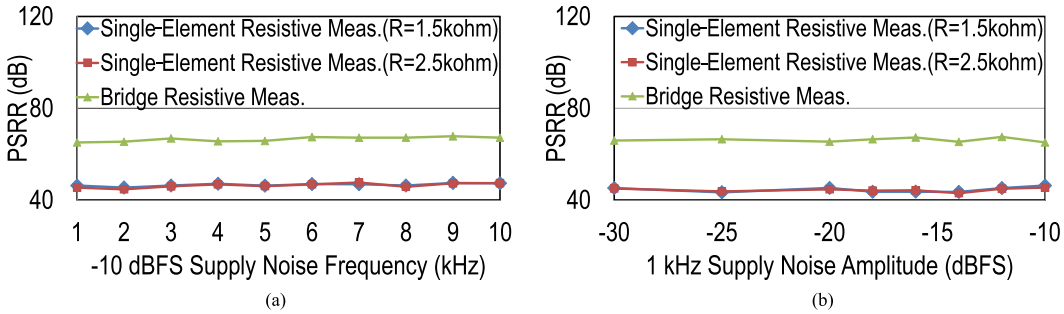


Fig. 13. PSRRs measured under (a) different supply noise frequencies and (b) different supply noise amplitudes.

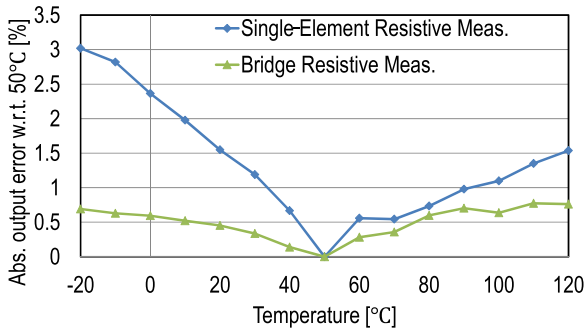


Fig. 14. Maximum absolute output errors at different temperatures. The error is expressed as a percentage of the entire output range with respect to the input–output curve at 50 °C.

following expressions [10], [14]:

$$\text{FoM}_W = \frac{E_{\text{CONV\_INC\_BRIDGE}}}{2^{(\text{SNR}-1.76)/6.02}} \tag{22}$$

$$\text{FoM}_S = \text{SNR(dB)} + 10\log\left(\frac{1}{2E_{\text{CONV\_INC\_BRIDGE}}}\right). \tag{23}$$

By reducing the bridge biasing power, which ranges from 20% to 77% of the total power in the conventional designs, the proposed ROIC achieves improved FoM, power-supply sensitivity, and PSRR performance. However, compared with the state-of-the-art Δ−Σ analog-to-digital converters, the proposed ROIC with the resistive sensor needs a larger C_s (5 pF) to get an optimal NEP, as shown in Fig. 6(a). As a result, it leads to relatively larger power and FOM.

V. Conclusion

This paper reports on an energy-efficient and high-PSRR Δ−Σ ROIC. It is based on dynamic ZCB SC integrators, into which the resistive sensor can be embedded to reuse the bias current. In addition, a pseudodifferential dual-path scheme for the bridge measurement is proposed to further protect PSRR against bridge imbalance. Oversampling Δ−Σ modulation directly produces a digitized output, avoiding the need for a power-hungry IA while preserving the linear settling behavior of the ZCB SC integrators. Prototyped in 0.18-μm CMOS, the proposed dual-path ROIC for the bridge measurement shows a nonlinearity of <400 ppm and an rms-noise-equivalent resolution of 13 bits at a conversion rate of 8 kS/s, corresponding to an FoM of 1.05 pJ/conversion step. The achieved noise-frequency-independent PSRR is 65 dB, and the supply and temperature sensitivities are 0.23%/V and 55 ppm/°C, respectively. These metrics together render the proposed device, a promising candidate for smart IoT sensing applications.

References

[1] H. Tang, Z. C. Sun, K. W. R. Chew, and L. Siek, "A 5.8 nW 9.1-ENOB 1-kS/s local asynchronous successive approximation register ADC for implantable medical device," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 10, pp. 2221–2225, Oct. 2014.

[2] X. Tang, W. T. Ng, and K.-P. Pun, "A resistor-based sub-1-V CMOS smart temperature sensor for VLSI thermal management," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 9, pp. 1651–1660, Sep. 2015.

[3] M. Zare and M. Maymandi-Nejad, "A fully digital front-end architecture for ECG acquisition system with 0.5 V supply," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 1, pp. 256–265, Jan. 2016.

[4] H. Bhamra, J. Lynch, M. Ward, and P. Irazoqui, "A noise-power-area optimized biosensing front end for wireless body sensor nodes and medical implantable devices," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 10, pp. 2917–2928, Oct. 2017.

[5] M. Taherzadeh-Sani, S. M. H. Hussaini, H. Rezaee-Dehsorkh, F. Nabki, and M. Sawan, "A 170-dBΩ CMOS TIA with 52-pA input-referred noise and 1-MHz bandwidth for very low current sensing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 5, pp. 1756–1766, May 2017.

[6] M. A. Ghanad, M. M. Green, and C. Dehollain, "A remotely powered implantable IC for recording mouse local temperature with ±0.09°C accuracy," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2013, pp. 93–96.

[7] M. A. Ghanad, C. Dehollain, and M. M. Green, "A 30 μW remotely-powered implant with time-based voltage regulation," in *Proc. ESSCIRC*, 2015, pp. 400–403.

[8] M. A. Ghanad, M. M. Green, and C. Dehollain, "A 30 μW remotely powered local temperature monitoring implantable system," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 54–63, Feb. 2017.

[9] R. Grezaud, L. Sibeud, F. Lepin, J. Willemin, J.-C. Riou, and B. Gomez, "A robust and versatile, −40°C to +180°C, 8Sps to 1kSps, multi power source wireless sensor system for aeronautic applications," *IEEE Symp. VLSI Circuits*, Jun. 2017, pp. C310–C311,

[10] K. C. Koay and P. K. Chan, "A low energy-noise 65 nm CMOS switched-capacitor resistive-bridge sensor interface," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 4, pp. 799–810, Apr. 2017.

[11] R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, "A 20-b ±40-mV range read-out IC with 50-nV offset and 0.04% gain error for bridge transducers," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152–2163, Sep. 2012.

[12] M. Maruyama, S. Taguchi, T. Yamanoue, and K. Iizuka, "An analog front-end for a multifunction sensor employing a weak-inversion biasing technique with 26 nVrms, 25 aCrms, and 19 fArms input-referred noise," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2252–2261, Oct. 2016.

[13] H. Jiang, K. A. A. Makinwa, and S. Nihtianov, "An energy-efficient 3.7nV/$\sqrt{}$Hz bridge-readout IC with a stable bridge offset compensation scheme," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 172–173.

[14] S. Oh *et al.*, "A 2.5 nJ duty-cycled bridge-to-digital converter integrated in a 13 mm^3 pressure-sensing system," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 328–330.

[15] J. Van Rethy, H. Danneels, V. De Smedt, W. Dehaene, and G. E. Gielen, "Supply-noise-resilient design of a BBPLL-based force-balanced wheatstone bridge interface in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2618–2627, Nov. 2013.

[16] L. Brooks and H.-S. Lee, "A zero-crossing-based 8-bit 200 MS/s pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2677–2687, Dec. 2007.

[17] L. Brooks and H.-S. Lee, "A 12b, 50 MS/s, fully differential zero-crossing based pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3329–3343, Dec. 2009.

[18] M. Chu, B. Kim, and B.-G. Lee, "A 10-bit 200-MS/s zero-crossing-based pipeline ADC in 0.13-μm CMOS technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2671–2675, Nov. 2015.

[19] Y.-H. Kim and S. H. Cho, "A 1-GS/s 9-bit zero-crossing-based pipeline ADC using a resistor as a current source," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 7, pp. 2570–2579, Jul. 2016.

[20] B. Li *et al.*, "A 480 fJ/conversion-step 13-bit resistive sensor readout IC with a 1%/V power supply sensitivity," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2018, pp. 1–5.

[21] B. Li, W. Wang, J. Liu, W.-J. Liu, Q. Yang, and W.-B. Ye, "A 1 pF-to-10 nF generic capacitance-to-digital converter using zero-crossing $\Delta\Sigma$ modulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 7, pp. 2169–2182, Jul. 2018.

[22] B. Li, L. Sun, C.-T. Ko, A. K.-Y. Wong, and K.-P. Pun, "A high-linearity capacitance-to-digital converter suppressing charge errors from bottom-plate switches," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 1928–1941, Jul. 2014.

[23] J. K. Fiorenza, T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2658–2668, Dec. 2006.

[24] R. R. Fernández, F. M. Hidalgo, B. Pérez-Verdú, J. M. R. Utrera, and Á. Rodríguez-Vázquez, *CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design*. Berlin, Germany: Springer, 2006.

[25] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.

[26] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[27] *AccutrimTM 1242 Datasheet*, Vishay, Malvern, PA, USA, 2018.

[28] *KeysightTM 34410A Datasheet*, Keysight Technol., Santa Rosa, CA, USA, 2018.

[29] A. Ghanad, M. Green, and C. Dehollain, "A 15 μW 5.5 kS/s resistive sensor readout circuit with 7.6 ENOB," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 12, pp. 3321–3329, Dec. 2014.

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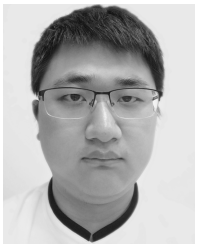

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