# Split-SAR ADCs: Improved Linearity With Power and Speed Optimization

Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, and Franco Maloberti

Abstract—This paper presents the linearity analysis of a successive approximation registers (SAR) analog-to-digital converters (ADC) with split DAC structure based on two switching methods: conventional charge-redistribution and  $V_{\rm cm}$ -based switching. The static linearity performance, namely the integral nonlinearity and differential nonlinearity, as well as the parasitic effects of the split DAC, are analyzed hereunder. In addition, a code-randomized calibration technique is proposed to correct the conversion nonlinearity in the conventional SAR ADC, which is verified by behavioral simulations, as well as measured results. Performances of both switching methods are demonstrated in 90 nm CMOS. Measurement results of power, speed, and linearity clearly show the benefits of using  $V_{\rm cm}$ -based switching.

*Index Terms*—Linearity analysis, linearity calibration, SAR ADCs, split DAC, V<sub>cm</sub>-based switching.

#### I. INTRODUCTION

**C** UCCESSIVE approximation registers (SAR) analog-to-digital converters (ADCs) [1]–[4], as an alternative to the pipelined ADCs [5]-[9] has become popular for battery-powered mobile applications, such as DVB-T, DVB-H and TDMB [10], [11] which require medium speed (10 MS/s-100 MS/s) and medium-resolution (8-10 b). SAR ADCs [2]–[4] achieve very low power consumption due to their simple architecture and operation. However, the SAR conversion relies basically on the performance of a capacitive DAC that subtracts the reference voltage from the input signal. The kT/C noise, capacitor mismatches, and parasitic of the split DAC [12] affect the conversion accuracy. As for medium resolution, the kT/C noise requirement is fulfilled with small capacitance, while other nonidealities like parasitic and nonlinearity, whose effect depends on the structure and the switching approach of the DAC, becomes significant.

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The binary-weighted capacitive DAC is widely used in SAR ADCs. However, the capacitance of the DAC array increases exponentially with the resolution, which imposes larger consumption of switching energy, area, and settling time. A valuable substitute is the split capacitive DAC, which has been recently reconsidered for medium resolution [13]–[18]. Its key limitation lies in the parasitic capacitors that destroy the desired binary ratio of the capacitive DAC array, thus degrading the conversion linearity. However, by using the metal-insulator-metal (MIM) capacitor or/and DAC mismatch calibrations [19]-[22], the split structure can become suitable for a medium-resolution target. On the other hand, the conversion linearity is also directly correlated with the switching sequences of the DAC array [12], [23], where the conventional charge-redistribution switching results in worse conversion linearity and more energy losses. A Vcm-based switching technique has been recently proposed [24], which achieves a significant switching energy saving when compared with set-and-down [3] and charge-recycling [25] switching approaches.

This paper analyzes the conversion nonlinearities, induced by supply noise, switching methods, and parasitic effects in SAR ADCs. The static nonlinearities based on the conventional and  $V_{\rm cm}$ -based [24] switching methods are theoretically analyzed, and the mathematical models are developed to verify the effectiveness of the  $V_{\rm cm}$ -based approach. Experimental results on a 90 nm CMOS 10 b 65 MS/s SAR ADC with conventional switching and a 10 b 100 MS/s SAR ADC with  $V_{\rm cm}$ -based switching demonstrate the performance benefits in terms of speed, power, and linearity by using  $V_{\rm cm}$ -based switching.

In addition, the internal node parasitic in the split DAC is also analyzed, as it degrades the conversion linearity. The above limitation can be fixed by a code-randomized digital calibration technique proposed here to improve the differential nonlinearity (DNL) and integral nonlinearity (INL).

Section II presents the overall SAR ADC architecture; Section III introduces the conventional and  $V_{cm}$ -based switching approaches. Section IV provides an analytical analysis of the static nonlinearity due to the capacitor mismatch and the parasitic effects in the two methods, and it also includes the behavioral simulations for confirmation of results. Finally, a DNL and INL calibration technique for parasitic nonlinearity in split DAC is proposed in section V. The measurement results of two integrated SAR ADCs and the conclusions are presented in Sections VI and VII, respectively.

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Fig. 1. Block diagram of the ADC architecture.

## II. OVERALL ADC ARCHITECTURE

Fig. 1 shows the architecture of the 10 b ADC. It is a conventional SAR ADC [24] consisting of a differential capacitive network a comparator and SA control logic. The SAR logic includes shift registers [26] and switch drivers which control the DAC operation by performing a binary-search algorithm during the conversion cycle. The capacitive DAC array is the basic structure of the SA ADC, which serves both to sample the input signal and subtract the reference. A reference-buffer-free technique [24] is used to improve the power dissipation and DAC settling. As the supplies  $V_{DD}$  and Gnd are used directly as reference voltages, the conversion sensitivity to supply variation is quantitatively analyzed in the Appendix.

# **III. SWITCHING METHODS**

When using the supplies as reference, the switching power is dynamic, which is correlated with the switching sequence Fig. 2(a) shows a conventional single-ended *n*-bit split [*k*-bit most significant bit (MSB) and *i*-bit LSB sub-array] DAC structure and its switching timing diagram. During the global sampling phase, the input signal  $V_{in}$  is stored in the entire capacitor array. The algorithmic conversion then begins by switching only the MSB capacitor to  $V_{DD}$  and the others to Gnd. Accordingly,  $V_{out}$  settles to  $-V_{in}$  and the comparator output Out\_{comp} in the first MSB decision will be

$$Out_{comp} = \begin{cases} 0 & V_{in} > 0 \\ 1 & V_{in} < 0. \end{cases}$$
(1)

The comparator output decides the switching logic of the MSB capacitor. If  $Out_{\text{comp}}$  is low  $S_{m,k}$  is switched back to Gnd If  $Out_{\text{comp}}$  is high, then  $S_{m,k}$  is kept to  $V_{DD}$ . For either decision, simultaneously, the  $S_{m,k-1}$  (the MSB/2) switches to  $V_{DD}$  for the next bit comparison. The above process will be repeated for n - 1 cycles.

The conventional charge-redistribution method is not very power effective [25], especially when discharging the MSB and charging the MSB/2 capacitor is required (bit decision back from "1" to "0") This is unnecessary in general, but it is required for that specific technique to operate properly. However, it would be beneficial if it can be avoided to save switching energy.

The  $V_{\rm cm}$ -based switching method proposed in [24] halves the array capacitance leading to around 90% energy saving when compared with the conventional one. Fig. 2(b) details the  $V_{\rm cm}$ -based switching algorithm. In the global sampling phase  $\Phi_1$ ,  $V_{\rm in}$  is stored in the capacitor array. During the conversion phase  $\Phi_2$ , all the capacitors' bottom-plates are switched to the  $V_{\rm cm}$  first, to give rise to the voltage  $-V_{\rm in}$  at the output. The sign of  $V_{\rm out}$  determines the MSB as the logic properly controls  $S_{\rm m,k-1}$ . If  $-V_{\rm in} < 0$ ,  $S_{\rm m,k-1}$  goes to Gnd while the other switches  $S_{\rm m,k-2}, ..., S_{\rm l,0}$  remain connected to  $V_{\rm cm}$ . If  $-V_{\rm in} > 0$ ,  $S_{\rm m,k-1}$  is switched to  $V_{\rm DD}$ . The cycle will be repeated for n - 2 times.

The  $V_{\rm cm}$ -based approach performs the MSB transition by connecting the differential arrays to  $V_{\rm cm}$ . The power dissipation is just derived from what is needed to drive the bottom-plate parasitic of the capacitive arrays, while in the conventional charge-redistribution where the necessary MSB "up" transition costs significant switching energy and settling time. Moreover, as the MSB capacitor is not required anymore, it can be removed from the *n*-bit DAC array. Therefore, the next n - 1 b estimation is done with an (n - 1) bit array instead of its *n*-bit counterpart, leading to half capacitance reduction with respect to the conventional method.

Using supplies as reference voltages prevents static power dissipation from reference buffers [3], [17], [24], although the conversion becomes very sensitive to the supply ripple due to the switching effect. For 10-b accuracy the supply variation needs to be suppressed within  $\pm 0.049\%$  of the full supply rail, or the supply ripple  $\pm 588 \ \mu V$  for a 1.2 V supply. The detailed analysis of conversion sensitivity to supply noise is presented in the Appendix. As the  $V_{\rm cm}$ -based switching charges 75% less capacitance, simultaneously, when compared with the conventional switching, it can effectively reduce the under-shoot of the supply or reference buffer (when used). The inductive ringing effect can be well suppressed by minimizing the bonding inductance, e.g., multiple bonding, through the addition of a damping resistor and an on-chip decoupling capacitor  $C_{decp}$ . On the other hand, to overcome this problem an effective approach might be the use of a SA searching algorithm like nonbinary conversion [27] that relaxes the settling accuracy requirement during large switch transients.

### **IV. LINEARITY ANALYSIS**

#### A. Effect of Switching Schemes on the Linearity

To analyze the conversion linearity of the conventional and the  $V_{cm}$ -based switching methods in a binary-weighted DAC (shown in Fig. 3) each of the capacitors is modeled as the sum of the nominal capacitance value and the error term

$$C_n = 2^{n-1}C + \delta_n \tag{2}$$

considering that all the errors are in the unit capacitors, whose values are independent-identically distributed Gaussian random variables, and have a variance of

$$E[\delta_n^2] = 2^{n-1}\sigma^2 \tag{3}$$



Fig. 2. Single-ended *n*-bit and (n - 1)-bit split capacitive DAC arrays with their switching timing diagrams (n = k + i). (a) Conventional switching. (b)  $V_{cm}$ -based switching.



Fig. 3. k-bit binary-weighted DAC.

and where  $\sigma$  is the standard deviation of the unit capacitor. The  $V_{\rm cm}$ -based method achieves half capacitance reduction when compared with the conventional one, while the switching linearity comparison between the two switching methods should be addressed in the same capacitive DAC, with the same value of capacitor mismatch as well as predictable gain errors caused by unbalanced array capacitance. Accordingly, to perform the  $V_{\rm cm}$ -based switching method in the *k*-bit DAC array of Fig. 3, both  $S_0$  and  $S_1$  are kept connected to  $V_{\rm cm}$ during bits cycling.

To calculate a given digital input X with its corresponding DAC output  $V_{out}$  (X), the array is considered initially

discharged ( $V_{in} = 0$ ). The analog output of the *k*-bit capacitive DAC with conventional switching can be calculated as

$$V_{\text{out}}(X) = \frac{\sum_{n=1}^{k} (2^{n-1}C + \delta_n) S_n + (C + \delta_0) S_0}{2^k C + \sum_{n=0}^{k} \delta_n} \cdot V_{\text{DD}}$$
(4)

where the DAC digital input  $X = [S_n...S_0]$ , with  $S_n$  equal to 1, 1/2 or 0 represents the DAC connecting  $V_{DD}$ , 1/2  $V_{DD}$ (i.e.,  $V_{cm}$ ) or Gnd for bit *n*. For a single channel SAR ADC, the comparator offset and linear gain error in the DAC are acceptable, thus closed form calculations of INL and DNL are specified with respect to a bestfit line. In the SAR conversion, the comparator offset appears as an offset error and does not cause nonlinearity, therefore, excluding the offset term, the INL and DNL are [28]

$$INL = \frac{V_{out}(X)/A - V_{idl}(X)}{ISB}$$
(5)

$$DNL = \frac{[V_{out}(X) - V_{out}(X-1)]/A - LSB}{LSB}$$
(6)

$$A = \frac{\sum_{X=0}^{2^{n-1}} V_{\text{out}}(X) \cdot V_{\text{idl}}(X)}{\sum_{X=0}^{2^{n-1}} V_{\text{idl}}^2(X)}$$
(7)

where A indicates the linear gain error of the DAC,  $V_{idl}(X)$  is the nominal value for the digital input X and LSB =  $1/2^k V_{DD}$ . From (7), it can be deduced that the linear gain error A is input X dependent, which implies that the gain error  $A_{\rm con}$  for conventional switching and  $A_{\rm CM}$  for  $V_{\rm cm}$ -based one are not equivalent. However,  $A_{\rm con}$  and  $A_{\rm CM}$  values are quite close as 1000-time Monte Carlo simulations running in a 10-b DAC, where unit capacitors are Gaussian random variables with standard deviation of  $\sigma (\Delta C/C = 1\%)$ , lead to variances of gain  $\delta_{\rm Acon} = \pm 41e-5$  and  $\delta_{\rm ACM} = \pm 4.2e-5$ . Hence, to simplify the analysis, it will be assumed that the prospective linear gain A and the  $\delta$  terms in the denominator of (4) will be neglected.

The INLs of the two switching methods represent the conversion error that combines together all the errors in each bit. Considering that in  $V_{\rm cm}$ -based switching, the transitions are  $V_{\rm cm}$  related (with capacitors connected to  $V_{\rm cm}$ ), it follows that the INLs of the two switching methods must be different. First, the worst INL in conventional switching happens at the MSB transition [23], where only the MSB is pre-charged to  $V_{\rm DD}$ , leaving other capacitors to Gnd. For the  $V_{\rm cm}$ -based switching MSB transition is performed by level shifting all capacitors to  $V_{\rm cm}$ , which is input independent and ideally always achieves an INL of 0 LSB in the middle. The worst INL of V<sub>cm</sub>-based switching happens at the step below the MSB transition, where the input digital code is X = [10...0]. The corresponding input digital code of conventional switching is X = [10...1] The DAC output  $V_{out}(X)$  and INL of the conventional method INLcon are calculated as

$$V_{\text{out}}(X) = \frac{2^{k-1}C + \delta_k + C + \delta_1}{2^k C} \cdot V_{\text{DD}}$$
(8)

$$INL_{con} = \frac{\delta_k + \delta_1}{2^k C} \cdot \frac{V_{DD}}{LSB} = \frac{\delta_k + \delta_1}{C}$$
(9)

with variance

$$E[\delta_{\text{INLcon}}^2] = \frac{(2^{k-1}+1)\sigma^2}{C^2}.$$
 (10)

The INL of the  $V_{cm}$ -based method INL<sub>CM</sub> and its variance  $E[\delta_{INL,CM}^2]$  can be similarly derived as follows:

$$INL_{CM} = \frac{\delta_k}{2^k C} \cdot \frac{V_{DD}}{LSB} = \frac{\delta_k}{C}$$
(11)

$$E[\delta_{\rm INL_{CM}}^2] = \frac{2^{\kappa - 1} \sigma^2}{C^2}.$$
 (12)

Comparing the results of (10) and (12) it proves that the conventional and  $V_{\rm cm}$ -based switching have similar INLs at the step below MSB transition. In reality,  $V_{\rm cm}$ -based switching is insensitive to the input common mode noise.

The maximum DNL for the conventional method is expected to occur at the step below the MSB transition. With X = [10...0] and (X - 1) = [01...1], the difference between the voltage errors can be calculated

as

$$V(X) - V(X - 1) = \frac{C + \delta_k - \sum_{n=1}^{k-1} \delta_k}{2^k C}$$
$$\cdot V_{\text{DD}} = \text{LSB} + \frac{\delta_k - \sum_{n=1}^{k-1} \delta_k}{C} \cdot \text{LSB} \quad (13)$$

thus, its DNL yields

$$DNL_{con} = \frac{\delta_k - \sum_{n=1}^{k-1} \delta_n}{C}$$
(14)

and with its variance

$$E[\delta_{\rm DNLcon}^2] = \frac{(2^k - 1)\sigma^2}{C^2}.$$
 (15)

In the  $V_{cm}$ -based switching the MSB "up" transition is replaced by an initial reset of all the capacitors to  $V_{cm}$  (with the middle digital input X equal to [1/2...1/2]). There exist two consecutive worst DNLs occurring at the steps above (X + 1) = [0, 1...1] and below (X - 1) = [1, 0...0] the MSB transition. One of the worst DNL<sub>CM</sub> with two digital inputsX = [1/2...1/2] and (X - 1) = [0, 1...1] is obtained similarly as

$$V(X) - V(X - 1) = \text{LSB} + \frac{1/2\sum_{n=0}^{k} \delta_n - \sum_{n=0}^{k-1} \delta_n}{C} \cdot \text{LSB}$$
(16)

$$DNL_{CM} = \frac{1/2\delta_k - 1/2\sum_{n=0}^{k-1}\delta_n}{C}$$
(17)

with variance

$$E[\delta_{\text{DNL}_{\text{CM}}}^2] = \frac{2^k \sigma^2}{4C^2}.$$
 (18)

Equations (15) and (18) show that the proposed method can achieve a DNL that is two times better in comparison to conventional switching. It can also be found that the error terms are decreased by half, which can be attributed to the cancellation of the terms  $\sum_{n=0}^{k-1} \delta_n$  in (16). In fact, this happens because the capacitors contributing to two-bit transitions are correlated, which are switched from  $V_{\rm cm}$  to  $V_{\rm DD}$ . In contrast, in the conventional method the capacitors connected to  $V_{\rm DD}$  in two-bit transitions are completely different, and the error terms in (13) are summed together instead of being cancelled.

# B. Effect of Parasitic Capacitors on Linearity of a Split DAC

The inherent linearity errors become worse when the split DAC array is used [12], [29]. The parasitic capacitance  $C_{PA}$  and  $C_{PB}$  in nodes A and B [shown in Fig. 2(a)] will deteriorate the desired voltage division ratio and degrade the conversion accuracy. The analog output  $V_{out}$  (X) of a split DAC with  $C_{PA}$  and  $C_{PB}$  taken into account can be calculated as shown in (19) at the bottom of the page, where  $C_{SL}$  and  $C_{SM}$  is the sum of the capacitance in LSB and MSB arrays,

$$= \frac{C_{a}\left(\sum_{n=1}^{i} 2^{n-1}CS_{l,n} + CS_{l,0} + \sum_{n=1}^{k} 2^{n-1}CS_{m,n}\right) + (C_{SL} + C_{PB})\sum_{n=1}^{k} 2^{n-1}CS_{m,n}}{C_{a}(C_{SL} + C_{SM} + C_{PA} + C_{PB}) + (C_{SL} + C_{PB})(C_{SM} + C_{PA})} \cdot V_{DD}$$

respectively. The parasitic capacitor  $C_{PB}$  in the numerator changes the value of second term. The  $C_{PA}$  and  $C_{PB}$  in the denominator cause a gain error which is irrelevant in the analysis. Subtracting the nominal value, the error term of the MSB/2 transition (X = [010...0]) in the conventional method is given by

$$V_{\rm err}(X)_{\rm con} = \frac{C_{\rm PB} 2^{k-2} C}{C_{\rm a}(C_{\rm SL} + C_{\rm SM}) + C_{\rm SL} C_{\rm SM}} \cdot V_{\rm DD}.$$
 (20)

Correspondingly, for the  $V_{cm}$ -based method, the error term at the MSB/2 transition (X = [0, 1/2...1/2]) is obtained as

$$V_{\rm err}(X)_{\rm CM} = \frac{C_{\rm PB}(2^{k-1}-1)C}{C_{\rm a}(C_{\rm SL}+C_{\rm SM})+C_{\rm SL}C_{\rm SM}} \cdot \frac{V_{\rm DD}}{2} = \frac{C_{\rm PB}(2^{k-2}-1/2)C}{C_{\rm a}(C_{\rm SL}+C_{\rm SM})+C_{\rm SL}C_{\rm SM}} \cdot V_{\rm DD}.$$
 (21)

From (20) and (21), it can be concluded that the  $V_{\rm cm}$ -based and the conventional switching have a similar INL.

$$V_{\rm err,con} = \frac{C_{\rm PB}C}{C_{\rm a}(C_{\rm SL} + C_{\rm SM}) + C_{\rm SL}C_{\rm SM}} \cdot V_{\rm DD} \qquad (22)$$

$$V_{\rm err,CM} = \frac{C_{\rm PB}C}{C_{\rm a}(C_{\rm SL} + C_{\rm SM}) + C_{\rm SL}C_{\rm SM}} \cdot \frac{V_{\rm DD}}{2}.$$
 (23)

As a consequence of (22) and (23),  $V_{\rm cm}$ -based switching reduces the DNL by half when compared with the conventional switching. This benefit can be explained by the switching nature of the  $V_{\rm cm}$ -based method, which divides half of the voltage contribution from the last bit of the MSB array, which is  $C_{\rm PB}$  related, to all the capacitors in the LSB array that are irrelevant to  $C_{\rm PB}$ . Table I summarizes the switching linearity of the two methods.

#### C. Behavioral Simulations

To verify the previous analysis, behavioral simulations were performed which modeled the conversion linearity of the conventional and  $V_{\rm cm}$ -based switching methods in a 10 b split DAC array with 5 b MSB and 5 b LSB arrays. The values of the unit capacitor are Gaussian random variables with a standard deviation of  $\sigma$  ( $\Delta C/C = 1\%$ ), and the parasitic capacitance is not considered. Fig. 4 illustrates the result of 1000-sample Monte Carlo runs, where the standard deviations of DNLs and INLs with respect to a best fit line are plotted versus the DAC input code at 10-b level. As expected, two methods have similarly large INLs, while  $V_{\rm cm}$ -based switching has lower INLs at the transitions where the input code is more relevant to  $V_{\rm cm}$ . This happens in the cases like the transitions

TABLE I Switching Linearity Comparison Between Conventional & VCM-Based Methods

	k-bit Binary DAC		(k+i)-bit Split DAC	
Switch Scheme	$E[\delta_{\scriptscriptstyle INL}^2]$	$E[\delta_{\scriptscriptstyle DNL}^2]$	$V_{err,INL}$	$V_{err,DNL}$
Conventional	$\frac{(2^{k-1}+1)\sigma^2}{C^2}$	$\frac{(2^k-1)\sigma^2}{C^2}$	$2^{k-2}T$	Т
V <sub>cm</sub> -based	$\frac{2^{k-1}\sigma^2}{C^2}$	$\frac{2^k \sigma^2}{4C^2}$	$(2^{k-2}-1/2)T$	$\frac{T}{2}$
$\sqrt{\frac{E[\delta_{con}^2]}{E[\delta_{CM}^2]}} \frac{V_{err,con}}{V_{err,CM}}$	≈1	≈ 2	≈1	2

Note: 
$$T = \frac{C_{PB}C}{C_a(C_{SL} + C_{SM}) + C_{SL}C_{SM}} \cdot V_{DD}$$



Fig. 4. Behavioral simulation comparing the DNL and INL of conventional and  $V_{\rm cm}$ -based 10-b SAR ADCs.

of MSB and MSB/2. The DNL plot shown in Fig. 4(b) confirms the presented analysis of  $V_{cm}$ -based switching that denotes two consecutive high DNLs at the middle. Their value is two times lower than its conventional counterpart.

The simulation estimates the effect of the parasitic capacitor in the split structure supposing 10% top-plate parasitic with matched capacitor. The DNLs and INLs results of conventional and  $V_{\rm cm}$ -based switching methods obtained by 100 000 points with sine wave input are shown in Fig. 5. The maximum DNLs and INLs of conventional and  $V_{\rm cm}$ -based switching are 2.9



Fig. 5. Behavioral simulation results of DNLs and INLs for 10-b SAR ADCs with  $C_{PB}$ . (a) Conventional switching. (b)  $V_{cm}$ -based switching.

LSB/1.5 LSB and 1.4 LSB/1.4 LSB, respectively. In Fig. 5, it can be found that the ratio mismatch between the MSB and LSB arrays, caused by  $C_{PB}$ , results in the large quantization errors, which happen periodically at the carry from LSB array to the MSB array. Consequently, the interval between two large quantization steps is  $2^5$ .  $V_{cm}$ -based method has two times better DNL than conventional while the INLs of the two methods are quite similar.

# V. DNL AND INL CALIBRATION TECHNIQUE

In practice, the conversion nonlinearity gets worse when the conventional switching is used. Since there is a large switching transient in its "down" transition, caused by switching two capacitors simultaneously, the large switching transient causes the excessive supply voltage undershoot as well as potentially exacerbates an overdrive condition of the preamplifier, which will finally result in a wrong decision on the comparator's output. In contrast,  $V_{\rm cm}$ -based switching prevents occurrence of such large switching transient. In every bit cycle, only one capacitor is switched to obtain a voltage value by successive approximation of the input voltage without wasting energy and settling time. Moreover, the mismatches of the attenuation capacitor, as well as, the routing parasitic capacitance in the internal node of the DAC, cause conversion nonlinearity.



From Fig. 5, it can be seen that the nonlinearity is a static conversion error, which happens periodically corresponding to the number of bits distributed in the LSB array. Therefore, the foreseeable static linearity errors can be potentially calibrated in the digital domain.

Ideally all the quantization levels of the *n*-bit ADC are uniformly spaced, but due to nonideal elements in the actual circuit implementation the code transition points in the transfer function will be moved shown in Fig. 6. To calibrate the linearity error, a code-randomized calibration is proposed, which provides a plausible digital post-processing to fix the large quantization errors. This is achieved by redistributing the steps with statistically equally over the step's  $\pm$  LSB range. The calibration algorithm is shown in Fig. 6. The digital outputs used to find the DNL and INL errors are compensated values, where the comparator offset and linear gain errors will not appear. First the calibration will determine whether the ADCs digital output needs to be corrected. For an n-bit ADC with the split DAC shown in Fig. 2(a) there are m  $(m = 2^n/2^i - 1)$  digital codes  $(D_{cal} = [D_1, D_2, ..., D_m]),$ where large quantization steps happen and they are subject





Fig. 7. Calibrated DNL and INL of SAR ADC with conventional switching.



Fig. 8. Die microphotograph of the SAR ADC with conventional switching.

to be calibrated. When the ADCs digital output  $D_n$  matches any of the digital code in  $D_{cal}$ , the random number generator will outcome a new digital output  $D_r$ . The randomized output  $D_r$  has one of the three possible values  $D_n$  and its two adjacent quantization levels  $D_{n-1}$  and  $D_{n+1}$ , which are equally spaced with an identical probability of 1/3. The randomized solution transfers the nonlinearity into increased average quantization noise power. Therefore, the large DNL and INL errors can be calibrated with signal-to-noise distortion ratio (SNDR) of the ADC dropping slightly. Verified by a behavior simulation of a 10 b level, the SNDR with and without code-randomized calibration is 56.2 and 55.6 dB, respectively (32768 samples are taken in a 10-b SAR ADC with 10% top-plate parasitic  $C_{PB}$ , while ADC is otherwise ideal).

The code-randomization calibration is used to calibrate the DNL errors shown in Fig. 5(a). For example, when the output digital code  $D_{31}$  is detected, the system will auto-generate a new digital output selected from the codes  $D_{30}$ ,  $D_{31}$ , and  $D_{32}$ . Fig. 7 exhibits the calibrated DNL and INL results, where the maximum DNLs and INLs of the conventional method are both improved from 2.9 LSB to 1.3 LSB and 1.5 LSB to 1.4 LSB, respectively.



Fig. 9. Die microphotograph of the SAR ADC with  $V_{cm}$ -based switching.



Fig. 10. FFTs of the digital outputs with input at 1.8 MHz. (a) Conventional SAR ADC sampled at 65 MS/s. (b)  $V_{\rm cm}$ -based SAR ADC sampled at 100 MS/s.

## VI. MEASUREMENT RESULTS

Two 1.2 V 10-b SAR ADCs were fabricated in 90 nm CMOS for conversion linearity comparison. The first chip is a 10-b 65 MS/s SAR ADC with conventional switching, while the second chip is a 10-b 100 MS/s SAR ADC with  $V_{\rm cm}$ -based switching. The die micrographs of the two ADCs are shown in Figs. 8 and 9. 10-b (conventional) and 9-b (the MSB capacitance is removed due to the advantages of  $V_{\rm cm}$ -based switching) split DAC arrays were implemented to verify switching efficiency. The unit capacitance of a MIM capacitor is 50 fF, and the value of the attenuation capacitor  $C_{\rm a}$  is 53.3 fF that is 16/15 unit. The  $C_{\rm s}$  capacitor shown in Figs. 8 and 9 is used to implement the reference-buffer-free technique [24] with a capacitance of 400 fF. On the other hand, MIM capacitors exhibit very low top-plate parasitic, estimated to be <5%. The active areas of the conventional and  $V_{\rm cm}$ -based ADC are 0.56 and 0.18 mm<sup>2</sup>, respectively.



Fig. 11. Measured INL and DNL of 10-b SAR ADC with conventional switching.



Fig. 12. Measured INL and DNL of 10-b SAR ADC with  $V_{\rm cm}$ -based switching.

Fig. 10 shows output spectrums of the two ADCs with the input frequency at 1.8 MHz. The conventional SAR ADC can achieve 8.6 b ENOB at a sampling rate of 65 MS/s. When the  $V_{\rm cm}$ -based approach is utilized, the ADC can achieve100 MS/s sampling rate and the ENOB is improved to 9.1 b.

The measured DNL and INL of the ADC with conventional and  $V_{\rm cm}$ -based switching are illustrated in Figs. 11 and 12, respectively. The experimental measurements verify the benefits of  $V_{\rm cm}$ -based switching approach that exhibits a lower DNL and INL when compared with the conventional one. By utilizing  $V_{\rm cm}$ -based switching, the maximum DNL and INL are improved from 3 to 0.79 LSB and from 2.8 to 0.86 LSB, respectively. The INL from Fig. 12 is s-like and is minimized in the middle, while in Fig. 11, it is quite large in both MSB and MSB/2 transitions. The advantage of  $V_{\rm cm}$ -based switching stems from the MSB decision's independence of the capacitor mismatch. This was discussed in Section IV-A.

Fig. 11 shows that the high spikes are not symmetrically distributed. This is mainly caused by the large switching transients leading to insufficient DAC settling and supply ripples. The effect of parasitic capacitors of a split DAC

TABLE II Summary of Performance

Switching Method	Conventional	V <sub>cm</sub> -Based				
Technology	90-nm CMOS	90-nm CMOS				
Resolution	10-b	10-b				
Sampling Rate	65-MS/s	100-MS/s				
Supply Voltage	1.2 V	1.2 V				
Full Scale Analog Input	1.2V <sub>PP</sub> differential	1.2V <sub>PP</sub> differential				
SNDR	54.7 dB	56.6 dB				
SFDR	66 dB	71 dB				
ENOB	8.8-b	9.1-b				
DNL	+ 3/-1 LSB	+ 0.79/- 0.27 LSB				
INL	+ 2.8/-1.6 LSB	+ 0.86/- 0.78 LSB				
DNL after Cal.	+ 0.9/-0.7 LSB	N/A				
INL after Cal.	+ 1/-1.1 LSB	N/A				
Power Consumption						
Sampling&DAC	1.7 mW	600\$\muW\$				
Comparator	3.3 mW	800\$\muW\$				
CLK Gen & SA Log	3.2 mW	1.6 mW				
Total Power	8.2 mW	3 mW				
$FOM = Power/2^{ENOB_{*fs}}$	280 fJ/conv-step	55 fJ/conv-step				



Fig. 13. Measured INL and DNL of 10-b SAR ADC with conventional switching after calibration.

is not a dominant factor in this design and the proposed digital calibration technique is applied to correct all the large nonlinearity codes. The calibrated DNL and INL results are presented in Fig. 13, where the large DNL and INL can be significantly reduced from 3 to 0.9 LSB and from 2.8 to 1.1 LSB, respectively. The SNDR drops by 0.5 dB upon the calibration. For the second SAR ADC, due to the advantages of  $V_{\rm cm}$ -based switching, no missing codes are presented implying that calibration is not necessary.

The measured performances of the two prototype SAR ADCs are summarized in Table II. The second

	[2] ISSCC'08	[3] VLSI'09	[6] ISSCC'08	[9] ISSCC'09	This paper [24] JSSC'10
Architecture	SAR	SAR	Pipelined	Pipelined	SAR
Technology (nm)	90	130	65	180	90
Resolution (bit)	9	10	10	10	10
Sampling rate (MS/s)	40	50	100	50	100
Supply voltage (V)	1	1.2	1.2	1.8	1.2
SNDR (dB)	53.3	52.8	59	58.2	56.6
ENOB (bit)	8.6	8.5	9.5	9.4	9.1
DNL (LSB)	+ 0.7/-0.45	+ 0.88/-1	+ 0.1/-0.1	N/A	+ 0.79/-0.27
INL (LSB)	+ 0.56/-0.65	+ 2.2/-2.09	+ 0.2/-0.2	+ 0.7/-0.8	+ 0.86/-0.78
Power (mW)	0.82	0.92	4.5	9.9	3
$FOM = Power/2^{ENOB_{*fs}}$ (fJ/conv-step)	54	52	62	300	55

TABLE III ISOTHERMAL SOLIDIFICATION REACTION RATE CONSTANTS ESTIMATED USING DSC DATA

design consumes 5.2 mW lower power than the first, of which 2.7 mW is the benefit from the  $V_{\rm cm}$ -based switching due to the reduction of switching power as well as the digital power from switching buffers. Another 2.5 mW of power reduction is due to the utilization of the dynamic comparator. Considering all the power benefits, the figure-of-merit (FoM) of the second design is improved from 280 fJ/conv-step to 55 fJ/conv-step. Table III benchmarks the prototype  $V_{\rm cm}$ -based SAR ADC (Fig. 9) with state-of-the-art ADCs. The design achieves competitive FoM for high-speed implementation.

# VII. CONCLUSION

Two 1.2 V 10-b SAR ADCs operating at tens of MS/s with conventional and  $V_{\rm cm}$ -based switching were presented. The linearity behaviors of the DACs switching and structure were analyzed and verified by both simulated and measured results. The  $V_{\rm cm}$ -based switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The proposed code-randomized calibration can eliminate the large DNL and INL errors in the conventional switching. Measured results demonstrated that both higher speed and lower power is achieved by using  $V_{\rm cm}$ -based switching.

## APPENDIX

## A. Sensitivity to Supply Noise

Using supply as a reference, removes not only the static power required in the resistive ladder and high-speed voltage buffer, but also their noise contribution. However, the package bonding inductor will generate switching noise with undesired ringing effect. In modern SoC design, the analog circuitry will be normally biased by a dedicated linear voltage regulator or LDO to isolate the large system digital noise. Commercial low-noise voltage regulator products achieve around several tens of  $\mu V$  RMS within a bandwidth of hundreds of KHz [30]. The proper placement of the decoupling capacitor can effectively attenuate the high-frequency noise. Therefore, the inductive switching noise due to the current transient of the DAC becomes the critical and dominating contribution for the total reference noise. Thus, it is necessary to analyze the reference safety margin to guarantee the expected conversion accuracy.

The differential DAC for conventional and  $V_{\rm cm}$ -based switching with the simplified power networks are shown in Fig. 14. In  $V_{\rm cm}$ -based switching after (n - 1) bit cycling, the DACs will finally settle to a value for LSBs decision. The differential DAC output is quite sensitive to supply variations, especially in the most critical case where the bottom plates of all the DAC capacitors (on the signal side) are connected to  $V_{\rm DD}$ . Since the operation is differential, considering one of the corresponding cases: all bits in  $V_{\rm op1}$  are "1" and all bits in  $V_{\rm on1}$  are "0," the differential output  $V_{\rm out}$  of the DACs can be represented as

$$V_{\text{out}} = V_{\text{opl}} - V_{\text{onl}}$$
  
=  $\left[\frac{2^{n-1} - 1}{2^{n-1}}(V_{\text{DD}} + \Delta V) + \frac{1}{2^{n-1}}V_{\text{cm}}\right] - \frac{1}{2^{n-1}}V_{\text{cm}}\right]$ (24)

where  $\Delta V$  is the variation of the supply. Equation (24) is independent of  $V_{\rm cm}$ , since the differential operation cancels the relative terms. Consequently, the voltage error  $V_{\rm err}$  is obtained as

$$V_{\rm err} = \frac{2^{n-1} - 1}{2^{n-1}} \Delta V \approx \Delta V.$$
<sup>(25)</sup>

It requires that the error term  $|\Delta V|$ due to the supply-noise needs to be suppressed within 1/4 LSB (LSB = 1/2  ${}^{n}V_{\text{FS}} = 1/2 {}^{n-1} V_{\text{DD}}$ ). Then, leading to

$$\frac{|\Delta V|}{V_{\rm DD}} < \frac{1}{2^{n+1}}.$$
 (26)

For 10-b accuracy, the supply variation needs to be suppressed within  $\pm$  0.049% of the full supply rail. It means that the supply ripple  $<\pm$  588  $\mu$ V for a 1.2 V supply. The supply ripple due to the switching effect is not problematic for a low speed SAR, since the DAC settling time is large enough. However, in high-speed designs, the request becomes



Fig. 14. Simplified supply network and differential DACs to perform  $V_{\rm cm}$ -based and conventional switching.



Fig. 15. Behavioral simulation of SNDR versus the supply noise in a 10-b SAR ADC (10-b split DAC is used with a unit capacitance of 50 fF).

quite stringent. The design of a 10-b SAR running at 100 MS/s involves an overall time, available to determine each bit, which is <1 ns, including the time for comparison, SR logic delay, and DAC settling. A behavioral simulation shows that the conversion sensitivity to supply variation of a 10-b 100 MS/s SAR ADC is within  $\pm$  600  $\mu$ V, as illustrated in Fig. 15. According to the switching sequences of the binary-searched algorithm, the most critical transition happens at the charging of the largest capacitor. Since the  $V_{\rm cm}$ -based switching charges 75% less capacitance, simultaneously, when compared with the conventional switching, it can effectively reduce the under-shoot of the supply or reference buffer (when used). The supply waveforms of conventional and  $V_{\rm cm}$ -based methods with a switching frequency of 1 GHz are illustrated in Fig. 16 (Conventional and the  $V_{\rm cm}$ -based switching are



Fig. 16. Supply waveform of performing the conventional and  $V_{\rm cm}$ -based switching in a 10 b SAR ADC with the unit capacitance of 50 fF.



Fig. 17. Simulated supply variations versus sweeping of  $C_P$  and supply inductance in a 10 b  $V_{cm}$ -based SAR ADC (9-b split DAC is used with a unit capacitance of 50 fF).

applied to a 10-b and 9-b split DAC with a unit capacitance of 50 fF).

The inductive ringing effect can be well suppressed by minimizing the bonding inductance, e.g., multiple bonding, adding damping resistor, and on-chip decoupling capacitor  $C_{\text{decp}}$ . Fig. 17 presents a plot of supply variation versus the sweeping of  $C_{decp}$  and bonding inductance in a 10 b  $V_{cm}$ -based SAR. It can be deduced that to achieve 10-b accuracy, with 2-5 nH bonding inductance, it would be necessary to have a decoupling capacitor with an approximate value of 500 pF, to suppress the switching reference noise. This value penalizes the die area, e.g., using typical pMOS as the decoupling capacitor with W  $\times$  L equal to 5  $\times$  5  $\mu$ m, the area for 500 pF would be close to 0.04 mm<sup>2</sup>. On the other hand, some SA searching algorithm like the nonbinary conversion [27] that relaxes the settling accuracy requirement during large switch transients would be the effective approach to overcome this problem.

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