A 0.016-mm^2 144-μW Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With >0.95-MHz GBW

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***Abstract*—A 0.016-mm^2 144-μW three-stage amplifier capable of driving 1-to-15-nF capacitive load (C_L) is described. It is optimized via combining *current-buffer Miller compensation and parasitic-pole cancellation* (via an active left-half-plane zero circuit) to extend the C_L drivability with small power and area. Fabricated in 0.35-μm CMOS, the minimum gain-bandwidth product (GBW), slew rate (SR) and phase margin measured over 1-to-15-nF C_L are 0.95 MHz, 0.22 V/μs and 52.3°, respectively. The results at 15-nF C_L correspond to 2.02x-improved small-signal $\mathrm{FOM_S}$ $(= \mathrm{GBW} \cdot \mathrm{C_L}/\mathrm{Power})$, and 1.44x-improved large-signal $\mathrm{FOM_L}$ $(= \mathrm{SR} \cdot \mathrm{C_L}/\mathrm{Power})$ with respect to prior art. The sizing and optimization are systematically guided by *Local Feedback Loop Analysis*. It is an insightful control-centric method allowing the pole-zero placements to be more analyzable and comparable at the system level.**

***Index Terms*—Active LHP zero, CMOS, current buffer, current buffer Miller compensation, frequency compensation, Miller compensation, pole-zero cancellation, three-stage amplifier.**

I. Introduction

HIGH-COLOR-DEPTH LCD drivers demand an extensive number of amplifiers to buffer the Gamma-corrected reference voltages, which have to be stabilized by nF-range capacitors to handle the glitch energy during the digital-to-analog conversion. To deal with such a large capacitive load (C_L), most commercial buffer amplifiers require an external resistor (e.g., $20\ \Omega$ for $\mathrm{C_L} = 10\ \mathrm{nF}$[1]) in series with the output for ringing reduction. This regrettably penalizes the cost, settling time and high-frequency gain droop.

Three-stage amplifiers are a suitable candidate for precision buffering for their speed, power and area efficiencies at low voltage [2]–[10]. Among the reported solutions, the one with damping factor control [2] has shown the highest C_L drivability up to 1 nF, but already consuming substantial power $(426\ \mu\mathrm{W})$ and area $(0.16\ \mathrm{mm}^2)$. Although recent works feature advanced gain-bandwidth product (GBW) and slew rate (SR), the C_L drivability has not been improved (e.g., 0.15 nF in [8], 0.8 nF in [9], and 0.5 nF in [10]). This paper describes a three-stage amplifier [11] managed to afford particularly large and wide range of C_L (1 to 15 nF) with optimized power $(144\ \mu\mathrm{W})$ and die size $(0.016\ \mathrm{mm}^2)$, being very suitable for compact LCD drivers [12] with different resolution targets.

Conventionally, design of frequency compensation using *Direct Circuit Analysis* hinges on the analysis of amplifier's open-loop transfer function, once a potential topology is conceived. Yet, the involvement cannot explicitly correlate the effects of each circuit element to the pole-zero composition of the transfer function. *Return Ratio Analysis* is another alternative that is particularly suitable for feedback circuits with unapparent feedforward and feedback networks [13]. However, when multiple feedback loops are present, different return ratio expressions for an identical loop may be generated, complicating the stability analysis. Also, at circuit level the well-established frequency compensation techniques based on the feedback model [14] cannot be applied. In this paper, a control-centric *Local Feedback Loop (LFL) Analysis* expanded from [14] is described, which enables effective analysis, comparison and design of three-stage amplifiers at the system level. Particularly, one crucial observation from this work is that the first non-dominant pole of an amplifier is determined by the unity-gain bandwidth (UGB) of the dominant LFL, which will be the key guiding the frequency compensation.

Guided by LFL analysis, an optimized scheme combining current-buffer Miller compensation (CBMC) and parasitic-pole cancellation is developed. Comparing the results with prior art in Fig. 1, the achieved small-signal $\mathrm{FoM_S}$ $(\mathrm{GBW} \cdot C_L/\mathrm{Power})$ and large-signal $\mathrm{FoM_L}$ $(\mathrm{SR} \cdot C_L/\mathrm{Power})$ are improved by at least 2.02x and 1.44x, respectively.

This paper is organized as follows. Section II compares LFL analysis with direct circuit analysis. In Section III, additional design insights that are not apparent from direct circuit analysis are revealed through LFL analysis on two recent works [8], [9] with their design tradeoffs outlined. The proposed three-stage amplifier is detailed in Section IV, and the experimental results are given in Section V. Section VI concludes the paper.

II. Direct Circuit Analysis Versus LFL Analysis

Emerging applications urge for improved frequency compensation to deal with the stringent resistive-load and capacitive-

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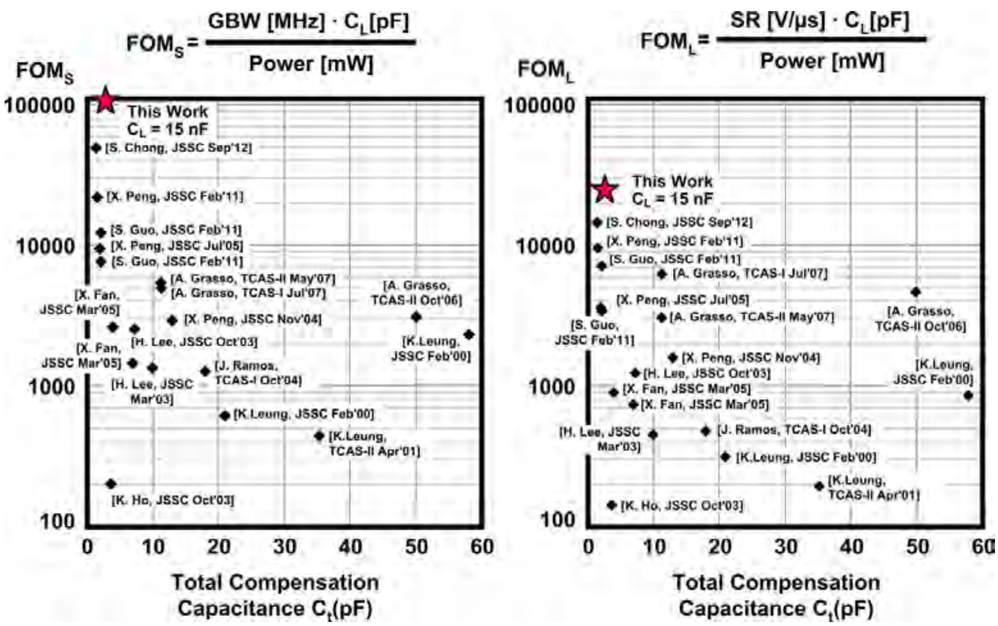

Fig. 1. Benchmark this work with the state-of-the-art in terms of $\mathrm{FOM_S}$ and $\mathrm{FOM_L}$.

load drivabilities with small power and area. This section introduces LFL analysis as a better option for the design of three-stage amplifiers, after describing the restrictions of direct circuit analysis.

A. Direct Circuit Analysis

Direct circuit analysis is a block-level verification-based design approach based on Kirchhoff's laws. After deducing the I/O transfer function of the amplifier, a full description of its small-signal dynamics is obtained [15]. Investigating the pole-zero composition and frequency response determines the merits and deficiencies of different frequency compensation schemes [16]. Each trial of a new potential scheme has to undergo the same steps, rendering the whole process more trial-and-error than systematic. Especially, repeating the calculation of high-order (e.g., ≥ 3) transfer function is tedious, while the gained insights are limited. This inefficiency is due to the fact that the correlation between the transfer function and circuit topology is weak in complicated frequency compensation. Although direct circuit analysis can determine the pole-zero position, it conveys little information on how to associate them with the circuit elements. Besides, direct circuit analysis is hard to differentiate certain schemes that are architecturally equivalent, but owning different transfer functions. A better analysis should be able to guide the pole-zero placements and eventually lead to the corresponding topology, but not the other way around as in direct circuit analysis.

B. Local Feedback Loop (LFL) Analysis

In most amplifiers internal feedback loops are always present, but are seldom treated from the viewpoint of classic feedback control [14]. LFL analysis considers the inner loop toward the outer loop one at a time, which is a common methodology in the design of multi-loop control systems [17]. The evaluation of the *LFL's transfer function* is easier than the *amplifier's transfer function* as a result of less number of elements involved. More importantly, the pole-zero composition of each LFL can be directly linked to its circuit topology. Pinpointing the pole or zero to the circuit elements becomes obvious, providing crucial insights which are not offered by direct circuit analysis.

Several key concepts of LFL analysis [18] are summarized as follows: 1) the LFL's unity-gain bandwidth (UGB) determines, up to which frequency, the feedback path of the LFL can still control the AC response; 2) the stability margins of the inner LFL reflects the high-frequency behavior of the next outer LFL; 3) the UGB of the upper-level LFL is mainly governed by the UGB of its inner LFL. Particularly, the UGB of the dominant LFL reveals which non-dominant pole limits the amplifier's GBW. A design example is given next to illustrate the above concepts.

C. Design Example

Fig. 2(a) shows a two-stage amplifier with standard Miller compensation. If direct circuit analysis is employed, the I/O transfer function can be established by solving two KCL equations (at the outputs of the 1st and 2nd stages), showing that the amplifier's GBW is limited by the $G_{\mathrm{mL}}/C_{\mathrm{L}}$-pole [19]. Alternatively, LFL analysis can be applied. The LFL is cut at the input of the 2nd stage. Calculating its transfer function $[T_{\mathrm{SMC}}(j\omega)]$ indicates that the LFL's UGB $(\omega_{\mathrm{u,SMC}})$ is $G_{\mathrm{mL}}/C_{\mathrm{L}}$, which is exactly the limiting pole obtained by direct circuit analysis. However, interpreting $G_{\mathrm{mL}}/C_{\mathrm{L}}$-pole as the LFL's UGB is certainly more important than only treating it as a limiting pole. Below $\omega_{\mathrm{u,SMC}}$, the magnitude of $T_{\mathrm{SMC}}(j\omega)$ is larger than unity and thus the amplifier's AC response is well controlled by the feedback path of the LFL. Beyond $\omega_{\mathrm{u,SMC}}$ the LFL gradually becomes inactive and the feedforward path takes over. Thus, the LFL's UGB should be the factor to be maximized when conceiving new frequency compensation. Note that the other unity-gain frequency $(g_{\mathrm{oL}}g_{\mathrm{o1}}/G_{\mathrm{mL}}C_{\mathrm{a}})$ can be ignored when

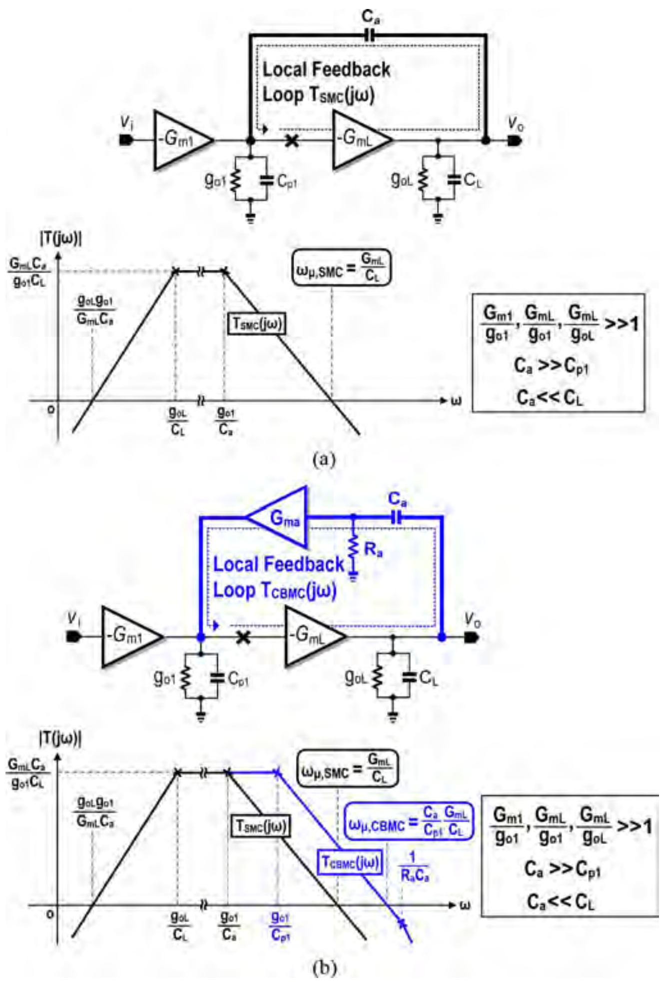

Fig. 2. Two-stage amplifier and its LFL magnitude response (a) Standard Miller compensation and (b) CBMC.

dealing with the GBW, since it affects only the low-frequency band of the amplifier.

CBMC can perform better frequency compensation than standard Miller compensation as shown in Fig. 2(b). Since there is no loading and voltage division effects, from C_a and C_{p1}, $\omega_{u,CBMC}$ surpasses $\omega_{u,SMC}$ by a factor of C_a/C_{p1} under the same power, area and C_L[20]. Specifically, as shown in Fig. 3(a), the same GBW as that of standard Miller compensation with identical C_L can be maintained by proportionally reducing G_{m1} and C_a. Although $\omega_{u,CBMC}$ is sacrificed, CBMC still shows better stability, power and area efficiencies than the standard Miller compensation counterpart, as evidenced in [20]. Alternatively, a smaller C_a can be selected to increase the GBW with smaller area, as shown in Fig. 3(b). As long as $\omega_{u,CBMC} > \omega_{u,SMC}$, the phase margin (PM) of CBMC is still higher than that of standard Miller compensation. Furthermore, $\omega_{u,CBMC}$ can be consciously reduced to exchange the C_L drivability, as illustrated in Fig. 3(c).

III. LFL Analysis on Recent Works

In this section, we apply LFL analysis to two recent works [8], [9] to examine their inner pole-zero composition and reveal

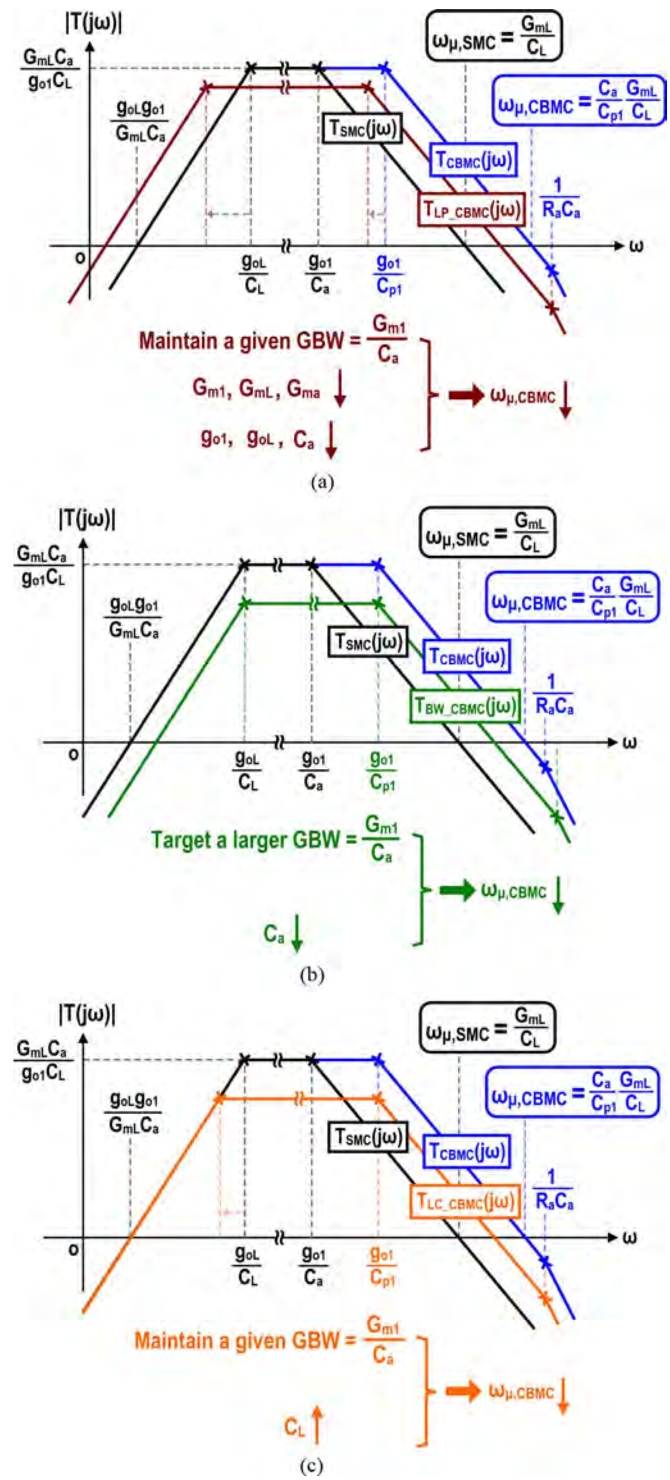

Fig. 3. Design flexibilities: (a) CBMC for low power and small area; (b) CBMC with large GBW and small area; (c) CBMC with high C_L drivability.

their pros and cons, which finally lead to the proposed solution to be described in Section IV.

A. Dual Active-Capacitive Feedback Compensation (DACFC) [9]

The Dual Active Capacitive-Feedback Compensation (DACFC) scheme is shown in Fig. 4(a). G_{m1}, G_{m2}, and G_{mL}

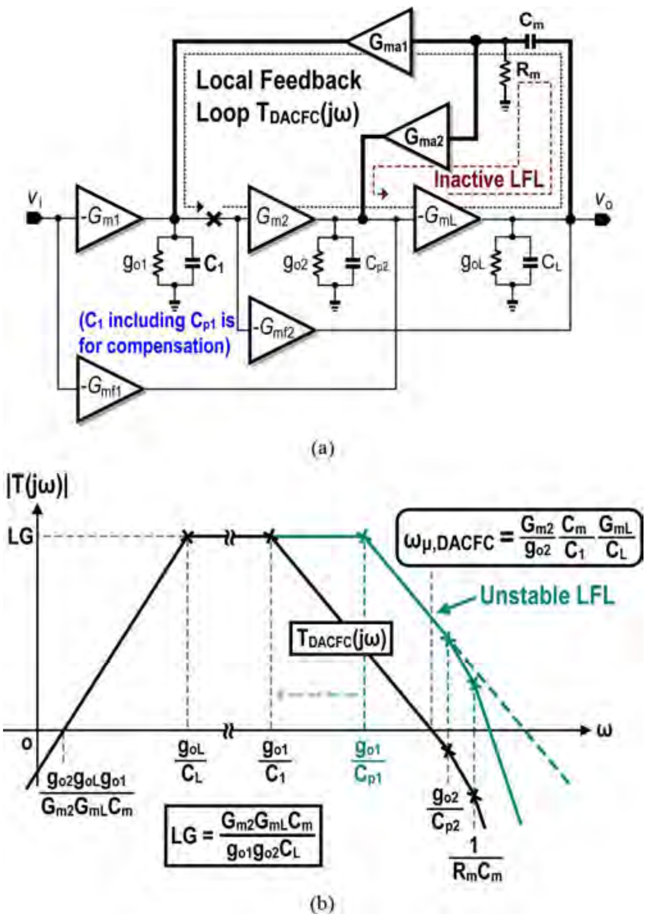

Fig. 4. (a) DACFC three-stage amplifier and its (b) LFL bode plot with and without C_1.

denote the three gain stages. The output conductance and lumped parasitic capacitance of each stage are $g_{\text{o1-2,L}}$ and $C_{\text{p1-3}}$, respectively. C_{p3} is embedded into C_{L}. G_{mf1} and G_{mf2} are two feedforward stages. The two LFLs are built around C_{m}, G_{ma1} and G_{ma2}.

LFL analysis can be first performed from the inner loop, which demonstrates that the inner LFL is almost inactive (inner LFL with G_{ma2} shows a loop gain < 1). Otherwise, the C_{L} drivability will be reduced to a level similar to that of a two-stage CBMC amplifier, due to the limitation from the inner LFL's UGB ($\omega_{\text{u,CBMC}} = C_{\text{m}}G_{\text{mL}}/C_{\text{p2}}C_{\text{L}}$). The key merit of DACFC is the outer LFL made up of CBMC, benefiting its UGB ($\omega_{\mu,\text{DACFC}}$). However, C_1 has to be added to ensure the stability of the outer LFL, offsetting the increment of $\omega_{\mu,\text{DACFC}}$ offered by CBMC. While this requirement is mathematically derived in [9], it can be explained via the outer LFL transfer function [$T_{\text{DACFC}}(\text{s})$] as

$$T_{DACFC}(s) \approx -\frac{sG_{m2}G_{mL}C_m\left(1+s\frac{G_{mf2}C_{p2}}{G_{mL}G_{m2}}\right)}{g_{o1}g_{o2}\left(1+s\frac{C_L}{g_{oL}}\right)\left(1+s\frac{C_1}{g_{o1}}\right)\left(1+s\frac{C_{p2}}{g_{o2}}\right)(1+sR_mC_m)}. \tag{1}$$

During the calculation of $T_{\text{DACFC}}(\text{s})$, three common assumptions are made: 1) DC gain of each stage is $\gg 1$; 2) $C_{\text{L}} \gg (C_{\text{m}}, C_1) \gg (C_{\text{p1}}, C_{\text{p2}})$ and 3) $G_{\text{ma1}} = 1/R_{\text{m}}$. The impact of the inner loop is negligible when C_{L} is sufficiently large. The outer LFL has four LHP poles: ($\omega_{\text{p1}} = g_{\text{o1}}/C_1$), ($\omega_{\text{p2}} = g_{\text{o2}}/C_{\text{p2}}$), ($\omega_{\text{p3}} = g_{\text{oL}}/C_{\text{L}}$) and ($\omega_{\text{p4}} = 1/R_{\text{m}}C_{\text{m}}$), and two LHP zeros. One zero ($\omega_{\text{z1}} = 0$) is at the origin. The other ($\omega_{\text{z2}} = G_{\text{mL}}G_{\text{m2}}/G_{\text{mf2}}C_{\text{p2}}$) is at a very high frequency being ignorable. $\omega_{\mu,\text{DACFC}}$ can be computed from (1) and given as

$$\omega_{\mu,DACFC} = \frac{G_{m2}}{g_{o2}}\frac{C_m}{C_1}\frac{G_{mL}}{C_L}. \tag{2}$$

The resultant LFL gain response is depicted in Fig. 4(b). If C_1 is not present, ω_{p1} will be placed at a much higher position ($g_{\text{o1}}/C_{\text{p1}}$), which will degrade substantially the LFL's PM as ω_{p2} cannot be shifted up. A worsen LFL's PM will result in a pair of complex conjugate poles with a small damping factor in the amplifier's transfer function, sacrificing the transient response [15]. Also, C_1 cannot be oversized as $\omega_{\mu,\text{DACFC}}$ will become smaller than the amplifier's GBW reducing the PM. Because of the lowered ω_{p1}, $\omega_{\mu,\text{DACFC}}$ decreases by a factor C_1/C_{p1} when compared with the ideal case (dashed line), and ultimately bounded by ω_{p2}. Pushing up ω_{p2} can only be achieved at the transistor level, e.g., reduce C_{p2} or increase g_{o2} via the gain reduction of G_{m2}[4]. Since the impact of increasing C_{L} is the same as C_1 [as seen from (2)], the C_{L} drivability of DACFC is constrained by the limited $\omega_{\mu,\text{DACFC}}$.

B. *Impedance Adapting Compensation (IAC) [8]*

The Impedance Adapting Compensation (IAC) scheme is shown in Fig. 5(a). Only one LFL is built by standard Miller compensation. Its key feature is a series network consisting of R_{a} and C_{a}, being attached at the 2nd stage's output. With similar assumptions as DACFC, as well as $g_{\text{o2}} \ll 1/R_{\text{a}}$ and $C_{\text{a}} \gg C_{\text{p2}}$, the LFL transfer function [$T_{\text{IAC}}(\text{s})$] is calculated as

$$T_{IAC}(s) \approx -\frac{sG_{m2}G_{mL}C_m(1+sR_aC_a)\left(1+s\frac{G_{mf}C_{p2}}{G_{mL}G_{m2}}\right)}{g_{o1}g_{o2}\left(1+s\frac{C_L}{g_{oL}}\right)\left(1+s\frac{C_m}{g_{o1}}\right)\left(1+s\frac{C_a}{g_{o2}}\right)(1+sR_aC_{p2})}. \tag{3}$$

There are four poles and three zeros in $T_{\text{IAC}}(\text{s})$. If the $g_{\text{o1}}/C_{\text{m}}$-pole is cancelled by the $1/R_{\text{a}}C_{\text{a}}$-zero and the effect of the high-frequency zero ($G_{\text{mL}}G_{\text{m2}}/G_{\text{mf}}C_{\text{p2}}$) is neglected, (3) can be simplified into

$$T_{IAC}(s) \approx -\frac{sG_{m2}G_{mL}C_m}{g_{o1}g_{o2}\left(1+s\frac{C_L}{g_{oL}}\right)\left(1+s\frac{C_a}{g_{o2}}\right)(1+sR_aC_{p2})}. \tag{4}$$

The magnitude response of $T_{\text{IAC}}(\text{s})$ is shown in Fig. 5(b). Also included for comparison are: 1) DACFC; 2) IAC without the series *RC* network (i.e., single Miller capacitor compensation in [4]), and 3) the case that the $g_{\text{o2}}/C_{\text{p2}}$-pole is eliminated. The series network not only generates a LHP zero ($1/R_{\text{a}}C_{\text{a}}$) to cancel the $g_{\text{o1}}/C_{\text{m}}$-pole, but also pushes the original $g_{\text{o2}}/C_{\text{p2}}$-pole to a lower position ($g_{\text{o2}}/C_{\text{a}}$) that increases the stability margin of the LFL. From (4), the LFL's UGB is given by

$$\omega_{\mu,IAC} = G_{m2}R_a\frac{G_{mL}}{C_L}, \tag{5}$$

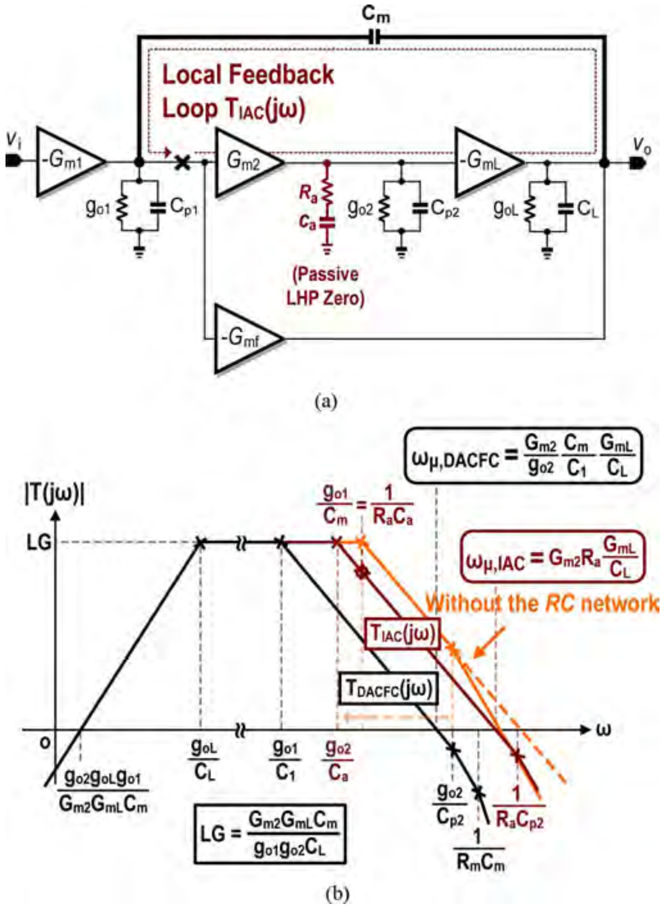

Fig. 5. (a) IAC three-stage amplifier and its (b) LFL bode plot. The DACFC's LFL and IAC's LFL without the series *RC* network are added for comparison.

which reveals that $\omega_{\mu,\text{IAC}}$ can be increased by selecting a large R_a. Although R_a cannot be oversized due to the third $1/R_\text{a}C_\text{p2}$-pole, it decouples the UGB boosting factor $(G_\text{m2}/g_\text{o2})$ and the limiting g_o2/C_p2-pole in DACFC, which allows $\omega_{\mu,\text{IAC}}$ surpassing $\omega_{\mu,\text{DACFC}}$ under the same design parameters. Besides, increasing R_a involves no power penalty. However, IAC still suffers from two key pitfalls: 1) since the LFL utilizes standard Miller compensation rather than CBMC, it decreases the LFL's UGB at the outset. Even using standard Miller compensation, owing to the introduction of the *RC* network, $\omega_{\mu,\text{IAC}}$ is significantly degraded in comparison with the scheme described by the dashed curve in Fig. 5(b); 2) when R_a is comparable to $1/g_\text{o2}$, it will destroy the LHP zero generation.

IV. Proposed Frequency-Compensation Scheme

Based on the analysis given in Section III, the proposed solution is intended to combine the benefit of CBMC in DACFC, while avoiding the bandwidth reduction originated from the *RC* network in IAC. As shown in Fig. 6(a), the outer LFL is built upon CBMC, whereas the parasitic g_o2/C_p2-pole is cancelled by a properly generated LHP zero for parasitic-pole cancellation. The proposed active LHP zero circuit for this parasitic-pole cancellation transforms the low-pass *RC* network into high-pass via negative feedback, offering the desired LHP zero without introducing unwanted low-frequency poles. G_mb2 offers V-to-I conversion for driving G_mL, as well as isolation between V_2 and V_3 nodes, imposing C_pb to be much smaller than C_p2 (i.e., shift up the parasitic pole). In this way, the problem of degraded $\omega_{\mu,\text{IAC}}$ owing to the passive LHP zero circuit can be solved.

A. LFL Transfer Function and Comparison

With similar assumptions in DACFC and IAC, the LFL transfer function of the proposed scheme can be obtained as shown in equation (6) at the bottom of the page. Comparing (6) with (1) and (4), two new poles $P_1(G_\text{mb1}/C_\text{z})$ and $P_2(1/R_\text{z}C_\text{pb})$ are introduced by the active LHP zero block. The LFL's UGB $\omega_{\mu,\text{Proposed}}$ is expressed by

$$\omega_{\mu,\text{Proposed}} = G_{m2}R_Z \frac{C_m}{C_{p1}} \frac{C_z}{C_{p2}} \frac{G_{mL}}{C_L}. \tag{7}$$

From (2), (5) and (7), $\omega_{\mu,\text{Proposed}} > \omega_{\mu,\text{DACFC}}$ and $\omega_{\mu,\text{IAC}}$ by one to two orders of magnitude is expected under the same conditions (e.g., transconductance, output conductance, parasitic, compensation and load capacitance). This extended $\omega_{\mu,\text{Proposed}}$ can be exchanged for a higher C_L drivability without power and area penalty. According to the magnitude responses given in Fig. 6(b), the non-dominant poles of the proposed amplifier can be discussed and compared with those of DACFC and IAC as follows.

P_1 is the main pole constraining $\omega_{\mu,\text{Proposed}}$. It should be located beyond the counterpart limiting poles: $(g_\text{o2}/C_\text{p2})$ in DACFC and $(1/R_\text{a}C_\text{p2})$ in IAC, when maximizing $\omega_{\mu,\text{Proposed}}$. Comparing with DACFC, the g_o2/C_p2-pole in our amplifier is cancelled with the active $1/R_\text{z}C_\text{z}$-zero, which is much lower than P_1 to maintain the high-pass characteristic. Comparing with IAC, P_1 is also much larger than its $1/R_\text{a}C_\text{p2}$-pole since a large $\omega_{\mu,\text{IAC}}$ necessitates a big R_a, penalizing the position of $1/R_\text{a}C_\text{p2}$-pole under a large C_L. For P_2, a very small C_pb makes it ignorable to $\omega_{\mu,\text{Proposed}}$, as it stays at a rather high frequency (5x to 10x of $\omega_{\mu,\text{Proposed}}$). Comparing with IAC, P_2 is also much higher than its limiting $1/R_\text{a}C_\text{p2}$-pole if $R_\text{z} = R_\text{a}$. Finally, $P_3(G_\text{ma}/C_\text{m})$ can be pushed sufficiently high too (e.g., 10x to 20x of $\omega_{\mu,\text{Proposed}}$) by employing a tailored wideband current buffer (to be discussed in Section IV-E). All these facts are verified by simulations next.

$$T_\text{Proposed}(s) \approx -\frac{sG_{m2}G_{mL}C_m}{g_{o2}g_{oL}\left(1+s\frac{C_L}{g_{oL}}\right)\left(1+s\frac{C_{p1}}{g_{o1}}\right)\left(1+s\frac{C_Z}{G_{mb1}}\right)(1+sR_ZC_{pb})\left(1+s\frac{C_m}{G_{ma}}\right)} \tag{6}$$

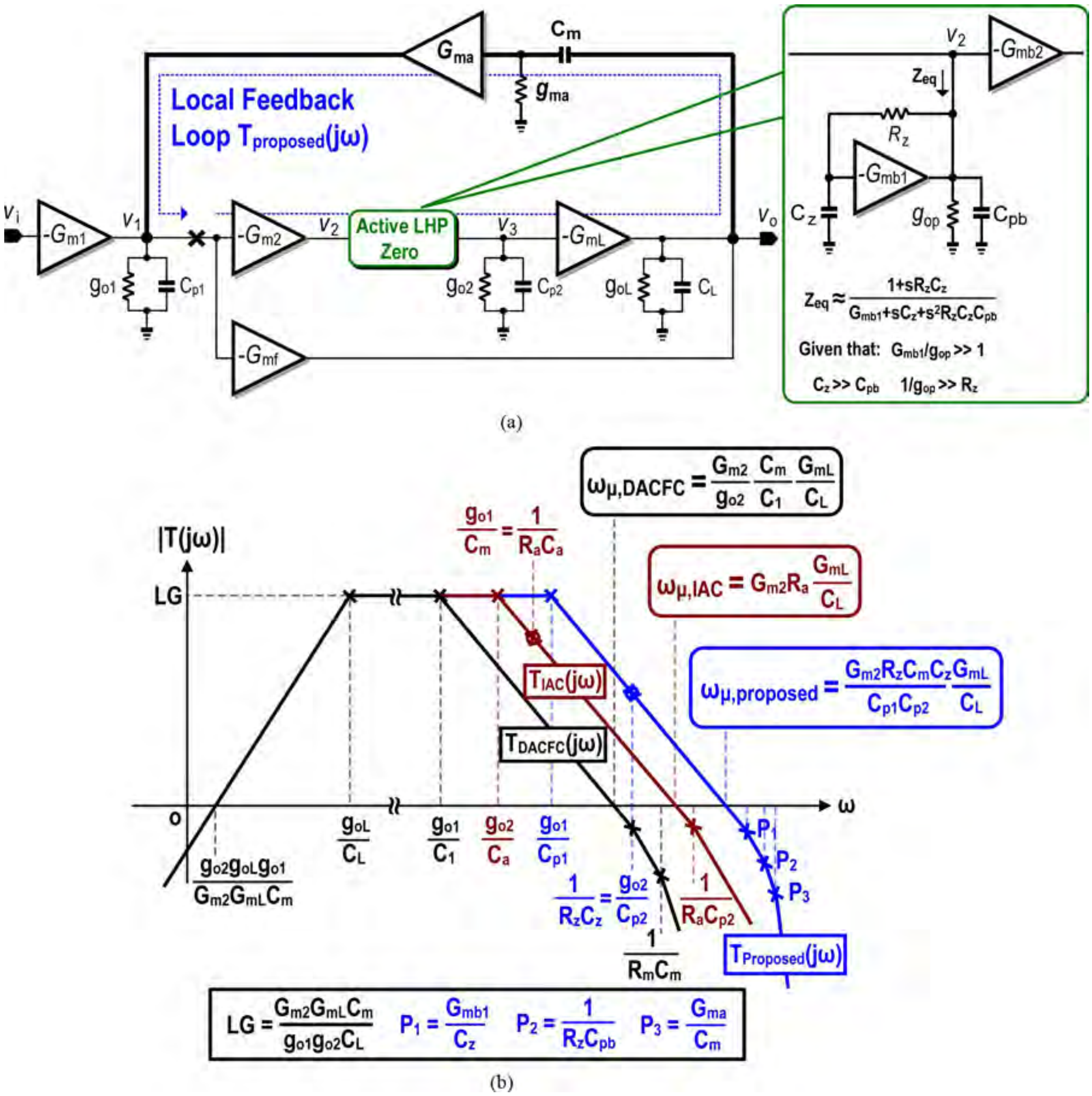

Fig. 6. (a) Proposed scheme using CBMC plus parasitic-pole cancellation, and its (b) LFL bode plot. The DACFC's LFL and IAC' s LFL are added for comparison.

TABLE I
BLOCK-LEVEL SIZING PARAMETERS OF IAC, DACFC, AND THE PROPOSED SCHEME

G_{m1} = 10 μS	G_{ma} = 500 μS	g_{o2} = 0.5 μS	C_{pb} = 0.01 pF	C_z = 0.8 pF
G_{m2} = 90 μS	G_{ma1} = 500 μS	g_{oL} = 6.67 μS	C_m = 1.2 pF	R_m = 2 kΩ
G_{mL} = 640 μS	G_{mb1} = 120 μS	g_{ob} = 0.5 μS	C_L = 10 nF	R_a = 1.5 MΩ
G_{mf} = 640 μS	G_{mb2} = 120 μS	C_{p1} = 0.4 pF	C_1 = 5 pF	R_z = 240 kΩ
G_{mf2} = 640 μS	g_{o1} = 0.13 μS	C_{p2} = 0.08 pF	C_a = 8 pF	

B. Block-Level Simulation Verification

Block-level simulations are employed to compare the performances between DACFC, IAC and the proposed schemes. The parameters are sized under the same power budget, $C_{\rm L}$ and LFL's PM, as summarized in Table I.

Unlike DACFC and IAC that require large-sized components ($C_1 = 5$ pF, $C_{\rm a} = 8$ pF and $R_{\rm a} = 1.5$ MΩ), they are manageably smaller ($C_{\rm z} = 0.8$ pF and $R_{\rm z} = 240$ kΩ) in the proposed scheme. Their LFLs' gain and phase responses are plotted in Fig. 7. With $< 8^\circ$ PM difference, $\omega_{\mu,\rm Proposed}$ exceeds $\omega_{\mu,\rm DACFC}$ and $\omega_{\mu,\rm IAC}$ by 14x and 10x, respectively. As mentioned earlier, $\omega_{\mu,\rm Proposed}$, $\omega_{\mu,\rm DACFC}$ and $\omega_{\mu,\rm IAC}$ are the limiting factors of their corresponding amplifier's GBW. Thus, comparing with DACFC and IAC, the proposed scheme should show higher $C_{\rm L}$ drivability under the same GBW or a larger GBW under the same $C_{\rm L}$.

C. Design Equations

For simplicity, the influences of P_2 and P_3 on the LFL are first ignored. Assuming that K is the ratio of P_1 to $\omega_{\mu,\rm Proposed}$, the LFL's PM can be approximately given by [21],

$$PM_{LFL} \approx 90^\circ - \arctan\frac{\omega_{\mu,\rm Proposed}}{P_1} = 90^\circ - \arctan\frac{1}{K}. \quad (8)$$

The amplifier's transfer function can be obtained with the aid of the signal-flow graph (SFG) and driving-point impedance

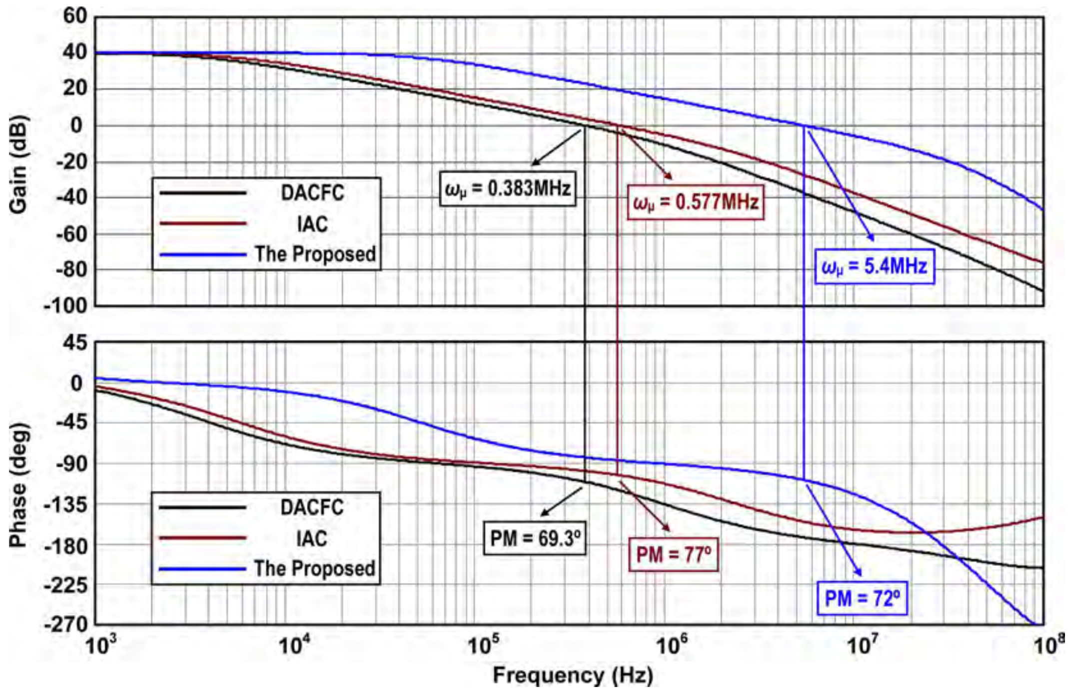

Fig. 7. Simulated LFL gain and phase responses of DACFC, IAC, and the proposed scheme.

(DPI) methodology [22] as given by equation (9) shown at the bottom of the page, where $A_{\rm f}$ is $(G_{\rm m2}G_{\rm mL}/G_{\rm mf}g_{\rm o2})$, $A_{\rm DC}$ is the DC gain $(G_{\rm m1}G_{\rm m2}G_{\rm mL}/g_{\rm o1}g_{\rm o2}g_{\rm oL})$, and $\omega_{\rm pd}$ is the dominant pole $(g_{\rm o1}g_{\rm o2}g_{\rm oL}/C_{\rm m}G_{\rm m2}G_{\rm mL})$. Hence, the GBW is $(G_{\rm m1}/C_{\rm m})$. The damping factor ζ and natural frequency $\omega_{\rm n}$ of the second-order polynomial in the denominator of (9) can be characterized by the LFL parameters $\omega_{\mu,{\rm Proposed}}$ and K, which are manifested as

$$\zeta = \frac{\sqrt{K}}{2} \tag{10}$$

$$\omega_n = \sqrt{K}\omega_{\mu,{\rm Proposed}}. \tag{11}$$

The exact relationship among GBW, ζ, and $\omega_{\rm n}$ can be determined by a proper set of coefficients for the denominator of the 3rd-order closed-loop transfer function, which is obtained by configuring the amplifier in unity-gain feedback (e.g., Butterworth coefficients). Alternatively, a more design-oriented approach is to link up the LFL parameters ($\omega_{\mu,{\rm Proposed}}$ and ${\rm PM_{LFL}}$) to those of the amplifier (GBW and PM) as given by

$$\begin{aligned} PM_{\rm Overall} &\approx 90^\circ - \arctan \frac{2\zeta\left(\frac{GBW}{\omega_n}\right)}{1-\left(\frac{GBW}{\omega_n}\right)^2} \\ &= 90^\circ - \arctan \\ &\quad\times \frac{\frac{GBW}{\omega_{\mu,{\rm Proposed}}}}{1-\frac{1}{\tan(PM_{LFL})}\left(\frac{GBW}{\omega_{\mu,{\rm Proposed}}}\right)^2}. \end{aligned} \tag{12}$$

With the given GBW, ${\rm PM_{LFL}}$ and ${\rm PM_{Overall}}$, it is possible to determine $\omega_{\mu,{\rm Proposed}}$ from (12). Other parameters should be optimized to achieve the desired GBW by pushing up other LFL non-dominant poles ($P_{1\text{-}3}$). Here, to achieve 76° ${\rm PM_{LFL}}$ and ${\rm PM_{Overall}}$, P_1 is located 4x higher than $\omega_{\mu,{\rm Proposed}}$ ($\zeta = 1$), and $\omega_{\mu,{\rm Proposed}}$ is set as 4x of the GBW. If $P_2(P_3)$ is 5x (10x) beyond $\omega_{\mu,{\rm Proposed}}$, $R_{\rm z}$ can be determined by the estimated

$$\begin{aligned} A_{\rm Proposed}(s) &\approx \frac{A_{DC}\left(1+\frac{s}{A_f\cdot P_1}+\frac{s^2}{A_f\cdot P_1\cdot P_2}\right)\left(1+\frac{s}{P_3}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{\mu,{\rm Proposed}}}+\frac{s^2}{\omega_{\mu,{\rm Proposed}}\cdot P_1}+\frac{s^3}{\omega_{\mu,{\rm Proposed}}\cdot P_1\cdot P_2}+\frac{s^4}{\omega_{\mu,{\rm Proposed}}\cdot P_1\cdot P_2\cdot P_3}\right)} \\ &\approx \frac{A_{DC}}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+2\zeta\left(\frac{s}{\omega_n}\right)+\left(\frac{s}{\omega_n}\right)^2\right)} \\ &= \frac{A_{DC}}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{\mu,{\rm Proposed}}}+\frac{s^2}{K\cdot\omega_{\mu,{\rm Proposed}}^2}\right)} \end{aligned} \tag{9}$$

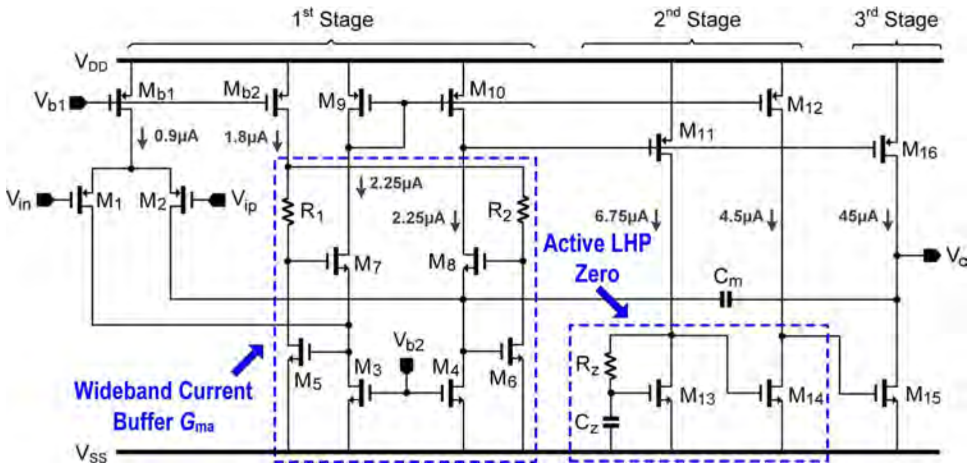

Fig. 8. Schematic of the proposed three-stage amplifier.

$C_{\rm pb}$. $G_{\rm ma}$ is set as 40x of $G_{\rm m1}$. Although this arrangement degrades $\rm PM_{LFL}$ by 17.1°, the impact on $\rm PM_{Overall}$ is only 4.3° as long as $\omega_{\mu,\rm Proposed}$ is 4x of the GBW. The optimization of $G_{\rm m2}$ and $G_{\rm mL}$ involves the power tradeoff between the 2nd and 3rd stages, and can be obtained by the estimated $C_{\rm p1}$ and $C_{\rm p2}$. Finally, $G_{\rm mf}$ should match $G_{\rm mL}$ for realizing a symmetric output stage.

D. Transient Response

The transient response includes the slewing and linear settling periods [23]. The SR of the proposed amplifier is mainly constrained by those of the first and final stages since the lumped parasitic capacitance $C_{\rm p2}$ is much smaller than $C_{\rm m}$ and $C_{\rm L}$. Like most three-stage amplifiers reported [2]–[10], the SR is not limited by the push-pull output stage if $C_{\rm L} < 5\ {\rm nF}$ (in the designed amplifier) as given by

$$SR \approx \frac{I_1}{C_m}, \tag{13}$$

where I_1 is the (dis)charging current for $C_{\rm m}$. If $C_{\rm L}$ is further increased, the SR of the output stage dominates as its dynamic current is not adequate to support fast slewing [21], which is in line with the measured SR data (Section V). Thus, the SR of the proposed amplifier can be expressed as

$$SR \approx \frac{I_{o,\max}}{C_L}, \tag{14}$$

where $I_{\rm o,max}$ denotes the maximum output current available to (dis)charge $C_{\rm L}$.

In parasitic-pole cancellation any component variations can lead to pole-zero mismatch. As a consequence, if the resulting doublet is located well below the unity-gain frequency of the amplifier, it will introduce a slow-settling component whose magnitude is proportional to the doublet frequency, and inversely proportional to the doublet spacing [23]. Since the parasitic-pole cancellation is applied within the LFL, the doublet spacing is roughly compressed by the LFL's loop gain at the doublet frequency [24], which is 20 dB for $C_{\rm L} = 10\ {\rm nF}$ and increases as $C_{\rm L}$ decreases in the designed amplifier. Hence, the impact of the parasitic-pole cancellation on the transient response is greatly suppressed.

After the impact of the doublet is ignored, the simplified 3rd-order transfer function (9) can help to analyze the linear settling behavior, which can be fully determined by the three open-loop parameters: GBW, ζ, and $\omega_{\rm n}$[25]. As the gain margin (GM) of the amplifier can be given by

$$GM_{\rm Overall} \approx 20\log\frac{2\zeta}{\left(\frac{GBW}{\omega_n}\right)}, \tag{15}$$

together with the $\rm PM_{overall}$ (12) and the GBW they set the pattern for the linear settling. Specifically, for a given ratio of GBW to $\omega_{\rm n}$ a large $\rm GM_{overall}$ implies a large ζ, thus introducing less ringing on the step response.

E. Circuit Implementation

Fig. 8 depicts the schematic of the proposed three-stage amplifier with the bias currents as shown. The 1st gain-stage $G_{\rm m1}(M_{1\text{-}10})$ is a folded cascode structure featuring a PMOS input differential pair $(M_{1\text{-}2})$. A wideband current buffer $G_{\rm ma}(M_{3\text{-}8}, R_{1\text{-}2})$ is embedded inside $G_{\rm m1}$. The active LHP zero circuit $(R_{\rm z}, C_{\rm z}, M_{13\text{-}14})$ is embodied in the 2nd gain stage $G_{\rm m2}(M_{11\text{-}14})$ to enhance the power efficiency. M_{13} and M_{14} realize $G_{\rm mb1}$ and $G_{\rm mb2}$, respectively. Connecting the gate of M_9 to that of M_{12} results in a push-pull 2nd stage enhancing the SR at the output of $G_{\rm m2}$ [26], and it also forms an undesired inverting current buffer (M_5, M_7, M_9, M_{12}). However, since the signal strength fed back from $V_{\rm o}$ to the source of M_7 is much smaller than that at the source of M_8 the impact of the inverting current buffer can be safely ignored. Besides, although the feedforward gain stage (M_1, M_9, M_{12}) can create a LHP zero, its location is far beyond the amplifier's GBW. The 3rd gain-stage $G_{\rm mL}(M_{15})$ is combined with another feedforward stage $G_{\rm mf}(M_{16})$ to form a push-pull structure. The optimization of $G_{\rm ma}$ and the active LHP zero are discussed as follows:

1) Wideband Current Buffer $G_{\rm ma}$: A very large $G_{\rm ma}$ is desired to push P_3 to a high frequency. The simple current buffer (M_8) in Fig. 9(a) will draw considerable power to achieve the required $G_{\rm ma}$. The regulated current buffer (M_6 and M_8) in Fig. 9(b) boosts $G_{\rm ma}$ by a factor of $(g_{\rm m6}r_{\rm o6}+1)$ as a result of the LFL formed by M_6, but it is hard to maintain a large $G_{\rm ma}$ at high frequencies due to the limited bandwidth of the

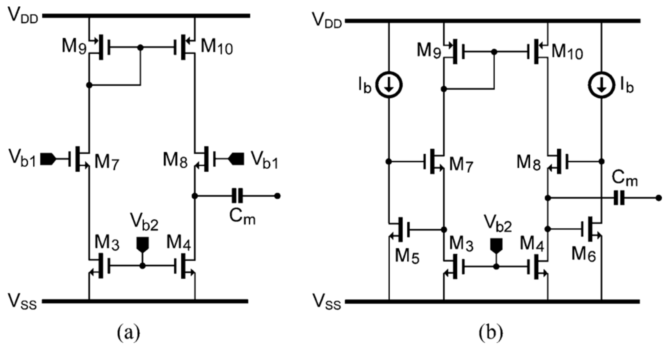

Fig. 9. Possible embedded current buffers for the PMOS folded cascode input stage. (a) Common gate. (b) Regulated.

LFL (i.e., the parasitic pole associated with the drain of M_6 is significant) [20]. The employed $G_{\rm ma}$ in Fig. 8 balances the tradeoff between $G_{\rm ma}$ and bandwidth [27]. The LFL ($M_{5\text{-}6}$ and $R_{1\text{-}2}$) can provide a better controlled LFL gain $(2g_{\rm m5}R_1 + 1)$ with moderately sized R_1, while pushing the parasitic pole beyond the LFL's UGB. The drain output impedance of M_8 is also boosted by the LFL gain.

2) Active LHP Zero Circuit: Locating P_2 to a high frequency requires the minimization of $C_{\rm pb}$ (a relatively large $R_{\rm z}$ is necessary to generate the $1/R_{\rm z}C_{\rm z}$-zero) and therefore the active LHP zero circuit should be as compact as possible. To accomplish this, both $G_{\rm mb1}(M_{13})$ and $G_{\rm mb2}(M_{14})$ are embodied in $G_{\rm m2}$ to avoid extra parasitic capacitance. A current mirror ratio of 2:3 is designed for M_{14}: M_{13} so as to minimize the parasitic capacitance induced by M_{14} while shifting up P_1. As mentioned before, for nF-range $C_{\rm L}$, the slew rate of the amplifier is dominated by the maximum charging or discharging current at the output stage $(M_{15\text{-}16})$. The output stage can attain certain resistive drivability (e.g., $25\ {\rm k}\Omega$ by a proper increment of its quiescent current (e.g., $+44\%$).

F. Performance Over PVT Variations

The effect of temperature and process variations on the amplifier's performance with $C_{\rm L} = 15\ {\rm nF}$ has been investigated via post-layout corner simulations. The results are summarized in Table II. At $27^\circ{\rm C}$, the GBW variation remains within 17.4% of its typical value while the phase and gain margins over various corners deviate about 3° and 1 dB, respectively. The corresponding deviations of the average SR and settling time, from their nominal values, are 39.5% and 30.4%, respectively, whereas the quiescent current $I_{\rm Q}$ changes less than 14% from its typical value. Roughly the same percentage of variations over the typical values is observed for $-40^\circ{\rm C}$ and $125^\circ{\rm C}$. On the other hand, 10% reduction of the supply voltage has no significant impact on the overall performance. The minimum supply voltage is limited by the proper operation of the current buffer, which is around 1.7 V.

V. EXPERIMENTAL RESULTS

The aim of this work is to maximize the $C_{\rm L}$ drivability while maintaining the power and area comparable with the recent works [8], [9]. The optimized circuit parameters and size of each device are given in Table III and IV, respectively. The prototype fabricated in 0.35-μm CMOS occupies 0.016-mm^2 die size (Fig. 10).

TABLE II
POST-LAYOUT SIMULATIONS OF THE PROPOSED AMPLIFIER AT $C_{\rm L} = 15\ {\rm nF}$ OVER PROCESS AND TEMPERATURE VARIATIONS

T = 27°C

Corner	TT	FF	SS	SNFP	FNSP
GBW (MHz)	0.92	1.08	0.78	1.04	0.82
PM (Degree)	52.5	50.3	55.6	50.6	55.2
GM (dB)	19.5	20.2	19.3	19.1	20.3
SR+/SR- (V/μs)	0.18/0.20	0.26/0.27	0.14/0.15	0.21/0.16	0.16/0.25
1% T_S+/T_S- (μs)	5.17/5.71	3.54/4.40	6.92/7.27	5.24/5.79	5.57/5.58
I_Q (μA)	69.2	78.6	63.2	78.0	63.7

T = -40°C

Corner	TT	FF	SS	SNFP	FNSP
GBW (MHz)	0.98	1.17	0.83	1.11	0.87
PM (Degree)	54.0	51.8	57.0	52.1	56.7
GM (dB)	20.7	21.2	20.6	20.4	21.3
SR+/SR- (V/μs)	0.18/0.26	0.26//0.36	0.14/0.20	0.21/0.22	0.16/0.33
1% T_S+/T_S- (μs)	5.89/4.92	4.07/3.80	7.08/6.81	4.38/4.86	6.33/4.81
I_Q (μA)	62.9	72.1	57.2	71.5	57.7

T = 125°C

Corner	TT	FF	SS	SNFP	FNSP
GBW (MHz)	0.82	0.94	0.70	0.92	0.72
PM (Degree)	52.3	50.4	55.5	50.7	55.0
GM (dB)	18.9	19.9	18.5	18.3	20.0
SR+/SR- (V/μs)	0.18/0.14	0.27/0.20	0.14/0.11	0.22/0.12	0.15/0.18
1% T_S+/T_S- (μs)	5.04/7.17	3.59/5.51	6.78/9.02	7.34/7.47	5.73/6.80
I_Q (μA)	78.0	89.2	71.7	87.1	73.6

TT = Typical; FF = fast NMOS/fast PMOS;
SS = slow NMOS/slow PMOS; FNSP = fast NMOS/slow PMOS.

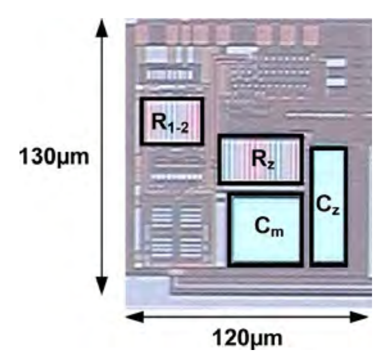

Fig. 10. Chip micrograph.

A. AC and Step Responses

The measured AC responses are plotted in Fig. 11. $C_{\rm L}$ can be as large as 15 nF with 18.1-dB gain and 52.3° phase margins, and as small as 1 nF with 9.8-dB gain and 83.2° phase margins. The extrapolated DC gain is $> 100\ {\rm dB}$. The GBW is 0.95 MHz at 15-nF $C_{\rm L}$. For the step responses (Fig. 12), the averaged SR and 1% setting time $(T_{\rm S})$ measured in unity-gain configuration are $0.22\ {\rm V}/\mu{\rm s}$ and $4.49\ \mu{\rm s}$, respectively. The overshoot appearing at 15-nF $C_{\rm L}$ is due to the SR limitation of the output stage [21].

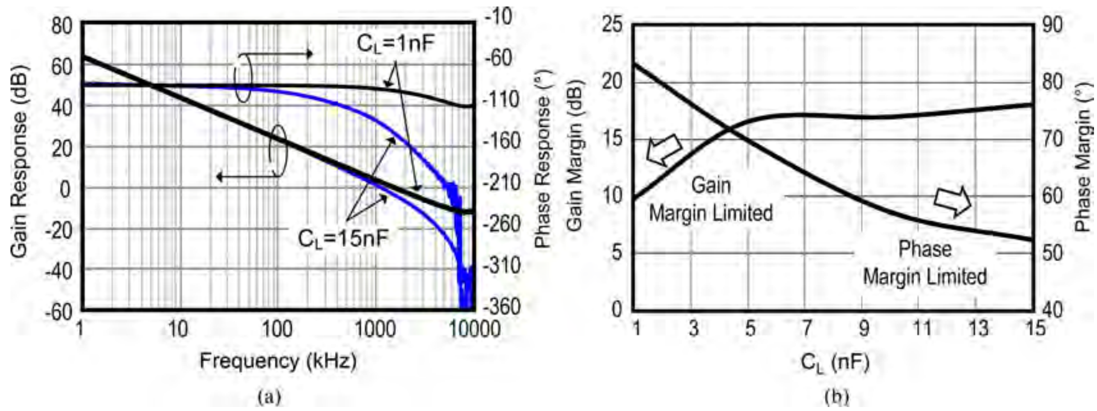

Fig. 11. (a) Measured AC responses at $C_{\mathrm{L}} = 1nF$ and 15 nF (b) Measured variation of gain and phase margins versus C_{L}.

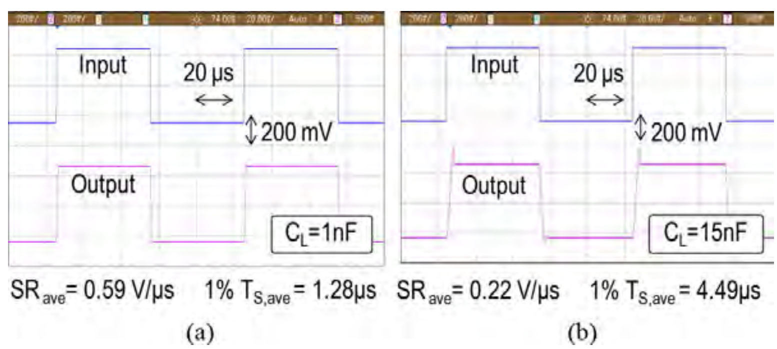

Fig. 12. Measured step responses at (a) $C_{\mathrm{L}} = 1$ nF and (b) $C_{\mathrm{L}} = 15$ nF.

TABLE III
CIRCUIT PARAMETERS FOR THE PROPOSED AMPLIFIER

G_{m1} = 11 μS	G_{mb1} = 96.4 μS	g_{m5} = 20.1 μS	C_L = 15 nF
G_{m2} = 93.8 μS	G_{mb2} = 64.2 μS	C_m = 1.424 pF	R_z = 239.9 kΩ
G_{mL} = 638.8 μS	g_{m8} = 46.8 μS	C_z = 1.219 pF	$R_{1,2}$ = 85.7 kΩ
G_{mf} = 629 μS	g_{mb8} = 9.6 μS		

TABLE IV
TRANSISTOR SIZES

Device	Size (μm/μm)	Device	Size (μm/μm)
M_1/M_2	12/2 (x8)	M_{13}	1.5/0.6 (x3)
M_3/M_4	4/2 (x3)	M_{14}	1.5/0.6 (x2)
M_5/M_6	1/0.35 (x3)	M_{15}	1.5/0.6 (x20)
M_7/M_8	1/0.35 (x4)	M_{16}	3/1(x40)
M_9/M_{10}	3/1 (x2)	M_{b1}	6/2
M_{11}	3/1 (x6)	M_{b1}	6/2 (x2)
M_{12}	3/1 (x4)		

B. Noise, PSRR and Unity-Gain Responses

Configured as a unity-gain feedback amplifier the measured output noise density spectrum [Fig. 13(a)] shows that the $1/f$ noise corner is close to 4 kHz and the white noise is $174\ \mathrm{nV}/\sqrt{}$Hz at 100 kHz, which is in good agreement with the simulated result. The discrepancy at low frequency $(< 30\ \mathrm{Hz})$ is due to the AC coupling capacitor $(100\ \mu\mathrm{F})$ in the test setup. From simulations $M_{3\text{-}4}$ and $M_{9\text{-}10}$ (Fig. 8) are the major contributors to the noise, with 52.6% and 32.4%, respectively, at 100 kHz. The PSRR is around 80 dB at 1 kHz [Fig. 13(b)]. The unity-gain magnitude responses at 1-nF and 15-nF C_{L} are shown in Fig. 13(c). The -3-dB bandwidth at 15-nF C_{L} is larger due to the existence of the complex poles.

C. Stability Versus C_{L} Variability

Although the measured gain (7.8 dB) and phase (79.5°) margins are not inferior when C_{L} is downsized to 0.5 nF, a small $(\sim\ 0.9\ \mathrm{mV_{pp}})$, long-lasting, high-frequency $(\sim\ 12\ \mathrm{MHz})$ ringing appears in the step response [Fig. 14(a)], which suggests that the closed-loop transfer function has a second-order polynomial with a very small damping factor and a high damping frequency. From an LFL analysis perspective this can be explained as follows: when C_{L} is significantly reduced, the damping factor in (9) decreases considerably, as well as the closed-loop damping factor. For a certain reduced value of C_{L} a long-lasting ringing occurs in the step response. The degradation on the LFL's PM and GM can capture the reduction in the damping factor from (9), since they are an indirect indicator of the ringing. When C_{L} is further downsized to 0.1 nF [Fig. 14(b)], the amplifier becomes unstable both internally (LFL) and externally (unity-gain feedback), owing to the RHP poles appearing in the amplifier's transfer function. This observation is consistent with the simulated gain and phase margins of $T_{\mathrm{proposed}}\ (j\omega)$ as shown in Fig. 14(c). Consequently, *the lower bound of* C_{L} *should be determined by the LFL stability, while the upper bound of* C_{L} *should be judged by the stability margins of the amplifier's transfer function*. This criterion cannot be drawn from conventional direct circuit analysis.

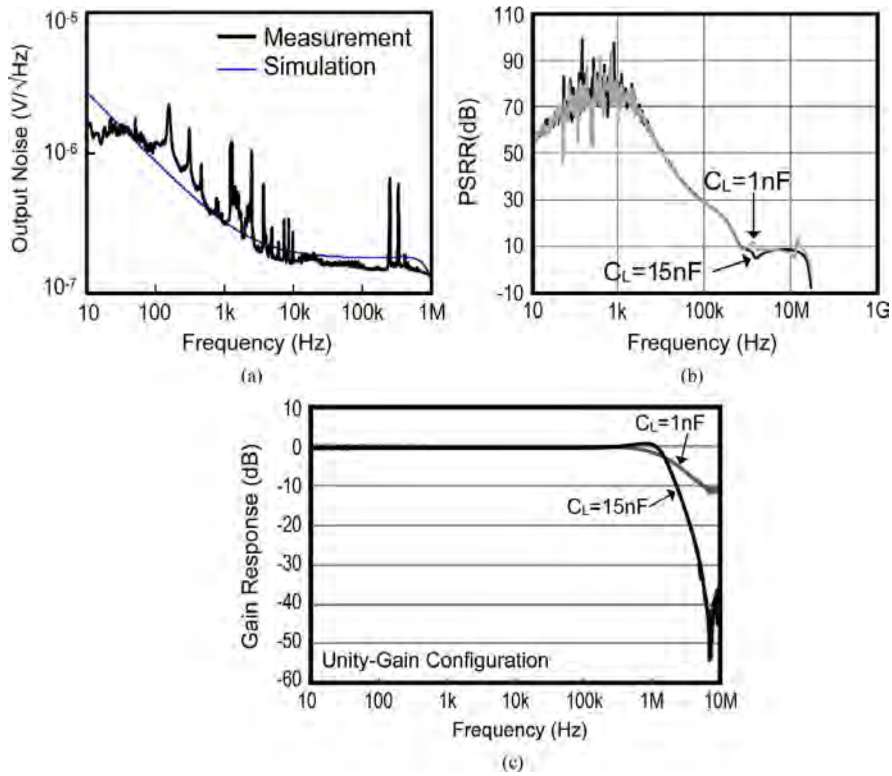

Fig. 13. Measured (a) Output noise density (b) PSRR and (c) Gain response in unity-gain feedback.

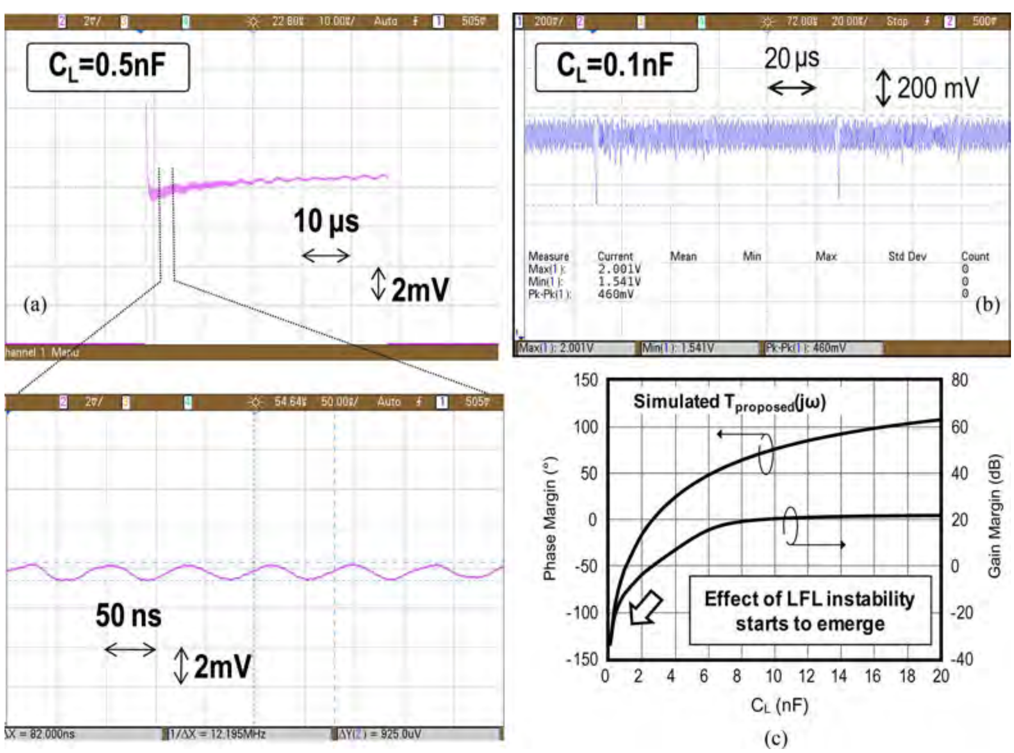

Fig. 14. (a) Measured step response at $C_{\mathrm{L}} = 0.5$ nF. A high-frequency small-amplitude is super-imposed on the step response, which is due to the reduced LFL stability (b) Unstable step response at $C_{\mathrm{L}} = 0.1$ nF (c) The simulated gain and phase margins of T_{proposed}.

D. Performance Benchmark and Robustness of Results

Table V summarizes the performance of one chip measured over different C_{L} and benchmarks with the three recent works. This work not only succeeds in extending the C_{L} drivability to 15 nF, but also shows improved $\mathrm{FOM_S}$ ($>$ 2.02x) and $\mathrm{FOM_L}$ (> 1.44x). The merits are held for supply-current FOM versions, i.e., $\mathrm{IFOM_S}$ (> 3.36x) and $\mathrm{IFOM_L}$, (> 2.4x). The

TABLE V
PERFORMANCE SUMMARY AND BENCHMARK

	[9] [S. Guo JSSC Feb'11]		[8] [X. Peng JSSC Feb'11]	[10] [C. Chong JSSC Sep'12]	This Work			
Load C_L (pF) [// R_L (k Ω)]	500 // 25	800 // 25	150	500	**1,000**	**5,000**	**10,000**	**15,000**
GBW (MHz)	4	3.6	4.4	2	1.37	1.24	1.06	0.95
Phase Margin (°)	70	58	57	52	83.2	69.8	57.2	52.3
Gain Margin (dB)	14*	16*	5*	8*	9.8	16.6	17.0	18.1
Average SR (V/µs)	2.2	1.7	1.8	0.65	0.59	0.50	0.30	0.22
Average 1% Ts (µs)	0.6	0.7	1.9	1.23	1.28	1.71	3.66	4.49
DC Gain (dB) (extrapolated)	>100		110	>100	>100			
Power (µW) @ V_{DD}	260 @ 2 V		30 @ 1.5 V	20.4 @ 1.2 V	144 @ 2 V			
Output Noise Density (nV/ √ Hz@10kHz)	N/A		N/A	N/A	172			
Total Capacitance C_t (pF)	2.2		1.6	1.15	2.6			
Chip Area (mm^2)	0.014		0.02	0.0088	0.016			
Technology	0.35µm CMOS		0.35µm CMOS	65nm CMOS	0.35µm CMOS			
FOM_S [(MHz · pF)/mW]	7,692	11,077	22,000	49,020	9,514	43,056	**73,611**	**98,958**
FOM_L [(V/µs · pF)/mW]	4,231	5,231	9,000	15,931	4,097	**17,361**	**20,833**	**22,917**
LC-FOM_S (MHz/mW)	3,497	5,035	13,750	42,626	3,659	16,560	28,311	38,061
LC-FOM_L [(V/µs)/mW]	1,923	2,378	5,625	13,853	1,576	6,677	8,013	8,814
$IFOM_S$ [(MHz · pF)/mA]	15,384	22,154	33,000	58,823	19,028	**86,112**	**147,722**	**197,916**
$IFOM_L$ [(V/µs · pF)/mA]	8,462	10,462	13,500	19,118	8,194	**34,722**	**41,666**	**45,834**

* denotes extracted values from plots

$$FOM_S = \frac{GBW \cdot C_L}{Power},\ FOM_L = \frac{SR \cdot C_L}{Power} \qquad LC\text{-}FOM_S = \frac{GBW}{Power} \cdot \frac{C_L}{C_t},\ LC\text{-}FOM_L = \frac{SR}{Power} \cdot \frac{C_L}{C_t} \qquad IFOM_S = \frac{GBW \cdot C_L}{I_{dd}},\ IFOM_L = \frac{SR \cdot C_L}{I_{dd}}$$

TABLE VI
MEASUREMENT RESULTS OVER 20 SAMPLES

20 chips, C_L=15nF	Mean	σ	$\frac{\sigma}{\text{Mean}}$ x 100%
GBW (MHz)	0.85	0.062	7.3%
Phase Margin (°)	53.2	2.64	5.0%
Gain Margin (dB)	19.96	1.42	7.1%
Average SR (V/µs)	0.21	0.014	6.7%
Average 1% Ts (µs)	4.77	0.21	4.4%
Power (µW)	140	14	10.0%
FOM_S [(MHz · pF)/mW]	89,290	10,888	12.2%
FOM_L [(V/µs · pF)/mW]	22,528	2,920	13.0%
LC-FOM_S (MHz/mW)	34,342	4,188	12.2%
LC-FOM_L [(V/µs)/mW]	8,661	1,123	13.0%
$IFOM_S$ [(MHz · pF)/mA]	178,580	21,776	12.2%
$IFOM_L$ [(V/µs · pF)/mA]	45,056	5,840	13.0%

robustness of the measured results over 20 samples has been confirmed. At 15-nF C_{L}, the standard deviation (σ) of each key performance parameter is $< 13\%$ of its mean (Table VI).

VI. CONCLUSIONS

The design and implementation of a power-efficient $(144\ \mu\mathrm{W})$ and compact $(0.016\ \mathrm{mm}^2)$ three-stage amplifier with large-and-wide C_{L} drivability (1 to 15 nF) have been presented. The employed LFL analysis is much more insightful than traditional direct circuit analysis in terms of topology selection, pole-zero placement, sizing of parameters and judging of C_{L} variability. The optimized frequency compensation scheme is CBMC plus parasitic-pole cancellation. Its transistor-level implementation is made particularly effective via a wideband current buffer and an active LHP zero circuit. The fabricated prototype exhibits advanced small-signal $\mathrm{FOM_S}\ (> 2.02\mathrm{x})$ and large-signal $\mathrm{FOM_L}\ (> 1.44\mathrm{x})$ with respect to the state-of-the-art. Robust results have been achieved over 20 available samples.

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