Missing-Code-Occurrence Probability Calibration Technique for DAC Nonlinearity With Supply and Reference Circuit Analysis in a SAR ADC

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***Abstract*— This paper reports a calibration scheme that can be used to correct the inter-stage gain error in two-stage analog-to-digital converters (ADCs). We measure the static nonlinearity at the raw ADC outputs and compensate it through a feedback path to adjust the gain in the analog domain, which avoids the dynamic range loss in the conventional pure digital calibrations. The proposed scheme detects the error via the missing-code-occurrence probability (MCOP), which is insensitive to the comparator offset and has better immunity to its noise. Besides the gain error, we discuss other DAC linearity issues, such as the implementations of the reference buffer and the low-dropout (LDO) regulator. To verify the MCOP calibration, we design a 12-bit successive-approximation-register ADC, employing the bridge-DAC, in 65-nm CMOS. We integrate the ADC operating at 100 MS/s with the MCOP calibration, the reference buffers, and the LDO. The measurement results demonstrate the linearity enhancement after the proposed calibration, where we improve the signal-to-noise-and-distortion ratio to 61.38 dB, leading to a FoM of 16.7 fJ/conversion step at the Nyquist input frequency.**

***Index Terms*— Gain error calibration, testing signal generation, SAR ADC, bridge DAC, *low-dropout* (LDO) regulator.**

I. Introduction

SAR ADCs [1]–[3] exhibit superior power efficiency, as the majority of its building blocks contain only digital elements, hence consuming mostly dynamic power and leading to simplicity in the implementation. The digital-like feature makes it more compatible with technology scaling, particularly, the conversion rate of the SAR ADC potentially increases with the advanced technology nodes. Typically, a SAR ADC comprises a capacitive DAC, a comparator and control logics, whose conversion accuracy is limited by the comparator thermal noise, the reference error from switching transient and the DAC mismatches. Targeting for more than 10-bit *effective-number-of-bit* (ENOB), a static or dynamic pre-amplifier [3], [4] is required to suppress the noise from the latch. Properly adding redundancy [5], [6] to relax the comparison accuracy in the leading bits is an effective approach to relieve the reference and DAC settling errors. Employing the binary-weighted DAC in high resolution (>12-bit) imposes that the capacitor matching rather than noise will dominate the performance, as the noise optimized design dictates the unit capacitance being too small to fulfill the required matching. The bridge-DAC [1], [3] is one of the prevalent structures that can circumvent this problem. By inserting an attenuation capacitor (C_a) between the *most significant bit* (MSB)- and the *least significant bit* (LSB)-array, the total capacitive units of the DAC can be significantly reduced. However, the mismatch of C_a and the inner node parasitics introduce a gain error between the reference voltages in the MSB- and the LSB-array. Such error characteristic is identical to the stage-gain-error in a sub-ranging ADC. Previous research has investigated such problems and tried to overcome them either in the analog [7]–[9] or the digital domain [10]–[16]. The analog domain calibrations [7]–[9] rely on the ADC itself to generate the residue that corresponds to the gain mismatch between two stages. By quantizing the residue, the gain error can be compensated accordingly, while the error measurement is sensitive to the comparator offset and noise. Suppressing them to a lower level usually implies increased analog circuit complexity and power. Motivated by the benefits of technology scaling, the digital assisted solution exhibits much better power efficiency in high speed implementations. Correlation-based calibrations [10]–[13] inject uncorrelated perturbation into the ADC and a mathematical algorithm like the *least-mean-square* (LMS) minimizes the error. The statistics-based calibrations [14], [15] detect the decision boundary gap to estimate the gain coefficient. Such digital-domain calibrations require less modifications of the ADC, while the estimation is based on accumulating a large amount of data, usually leading to a long converging time. Also, they face the same limitation, where the *dynamic range* (DR) is reduced after calibration.

Besides the inter-stage gain error, the conversion linearity is also limited by the reference error due to the switching transient. In practice, the analog circuitry, normally

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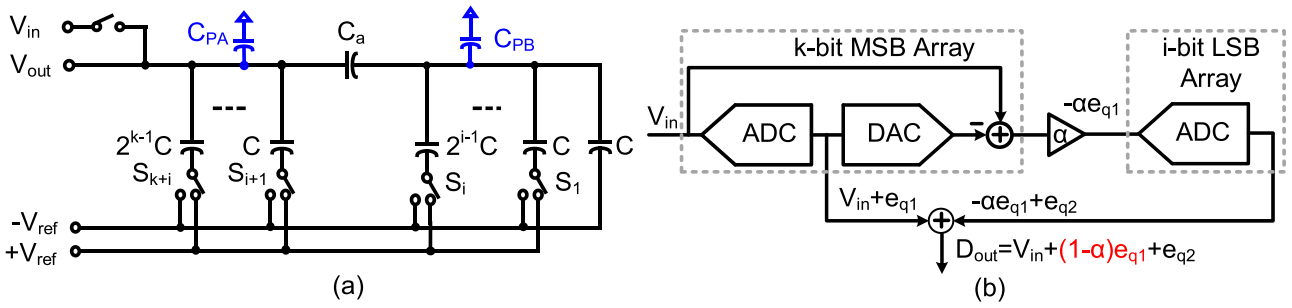

Fig. 1. (a) The n-bit bridge-structure DAC containing k-bit MSB- and i-bit LSB-array (k + i = n). (b) The nonlinearity introduced by the bridge DAC can be modeled as a stage-gain error in a two-stage ADC.

biased through a low noise reference voltage provided by the LDO [17], can isolate high frequency supply noise from the digital circuitries. On the other hand, the SAR conversion relies on the switched-capacitor DAC to subtract the input from the references, where the fast switching transient is desired for high speed. The DAC switching noise in the high speed SAR ADC is often in the GHz range with large voltage ripple due to its heavy load, which makes the LDO not be able to recover in time. In order to alleviate such noise and provide a fast recovery, reference buffers are required. The buffer provides a reference voltage for conversion and achieves *power-supply-rejection-ratio* (PSRR) to isolate the switching noise coupled to the LDO.

This paper reports a gain calibration applicable in either a SAR ADC using the bridge-DAC or other two-stage architectures. The gain error is sensed at the ADC outputs, and compensated through a feedback loop to the DAC to adjust the gain. The error measurement is based on the occurrence probability of the missing code at the ADC outputs, which has better immunity to the comparator's offset and noise. To detect the missing code a *test-signal generator* (TSG) [16] is implemented on-chip, which demonstrates a good robustness under process and temperature variations. Moreover, we discuss some practical issues when implementing the reference buffers and the LDO into the ADC and the error characteristic due to their design limitations. We performed the above-proposed techniques in a 12-bit, 100 MS/s SAR ADC utilizing a bridge-DAC in 65 nm CMOS. The ADC achieves an SNR of 61.99 dB at the Nyquist input frequency. The ADC core consumes 1.6 mW from a 1.2 V supply, which is equivalent to a FoM of 16.7 fJ/conv.-step.

II. Stage-Gain-Error Calibrations

A. Error Characteristic due to Inter-Stage Gain Mismatch

When the bridge DAC (Fig. 1(a)) structure is used in the SAR ADC the conversion can be modeled as a two-stage operation with a unity stage-gain, where the MSB- and the LSB-array resolve k- and i-bit, respectively. In this analysis we ignore the overall gain error caused by the parasitics C_{PA} and C_{PB} as that does not affect the overall linearity of the ADC. The output voltage V_{out} from the DAC can be simplified as [16],

$$V_{out} \approx \frac{1}{\delta}\left(\underbrace{\frac{2^iC+C_a+C_{PB}}{C_a}\sum_{j=1}^{k}2^{j-1}CS_{i+j}}_{\text{MSB Array}}+\underbrace{\sum_{j=1}^{i}2^{j-1}CS_j}_{\text{LSB Array}}\right)\cdot V_{ref}, \quad (1)$$

$$\delta = \left(2^i + 2^k - 1\right)C + 2^{i+k}C^2/C_a. \quad (2)$$

where C is the unit capacitor and S_j equal to 1 or 0 represents the digital output. From (1) it can be found that the parasitic C_{PB} and the mismatch of the attenuation capacitor C_a cause a gain error between two stages, i.e., the MSB- and the LSB-arrays. Assuming that the actual gain is α, and the k-bit residue e_{q1} is multiplied by α before passing to the LSB-array for fine i-bit quantization, if α deviates from the ideal value of 1, the final digital output contains a residue error ($(1-\alpha)e_{q1}$) as indicated in Fig. 1(b). We can obtain the relationship between the coefficient of the MSB array in (1) and α as,

$$\frac{2^iC + C_a + C_{PB}}{C_a} = \alpha\frac{2^iC + C_{a,id}}{C_{a,id}}, \quad (3)$$

where $C_{a,id}$ is the ideal value of the attenuation capacitor. Thus α can be derived as,

$$\alpha = 1 + \frac{\left(2^iC + C_{PB}\right)\cdot C_{a,id} - 2^iC\cdot C_a}{2^iC\cdot C_a + C_a\cdot C_{a,id}}. \quad (4)$$

Fig. 2(a1) and (a2) plot the residues after a k-bit quantizer in the 1st stage supposing that we apply a uniformly distributed input to an n-bit ADC using the bridge-DAC. If the numerator of (4) is larger than 0, implying $C_a < (1+C_{PB}/2^iC)C_{a,id}$ and accordingly $\alpha > 1$, the residue from the 1st stage (αe_{q1}) saturates the 2nd stage full-scale ($V_{FS,2}$). The outputs near the decision boundaries of the 1st stage are repeated creating peaks in Fig. 2(b1). Since k-bits are determined in the 1st stage, it results in 2^k intervals and the width of each segment is 2^i codes. The pattern is systematic, thereby the below discussion is based on one segment.

If C_a is adjusted to a value larger than $(1+ C_{PB}/2^iC)C_{a,id}$, leading to $\alpha < 1$, the residue from the 1st stage (Fig. 2(a2)) is smaller than the $V_{FS,2}$ resulting in the gaps at the boundaries

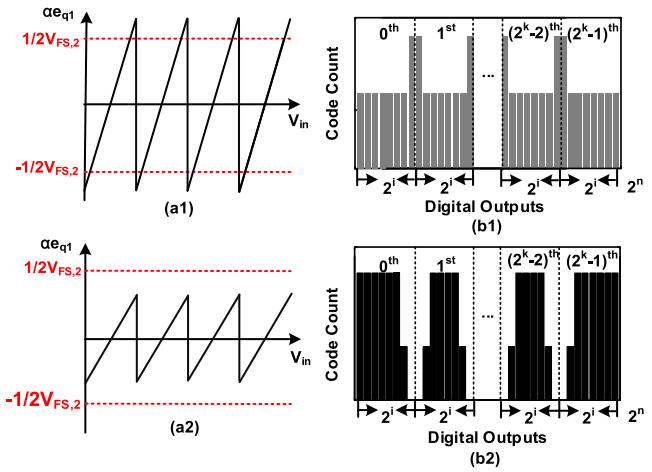

Fig. 2. (a1) Residue after k-bit quantizer in MSB array with $\alpha > 1$ (a2) with $\alpha < 1$; (b1) Output code histogram and corresponding code density with $\alpha > 1$ (b2) with $\alpha < 1$.

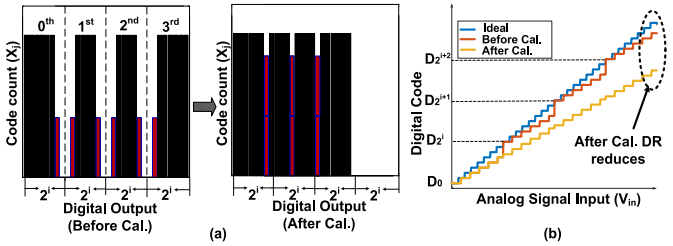

Fig. 3. (a) The code histogram and (b) transfer curve before and after digital gain compensation techniques.

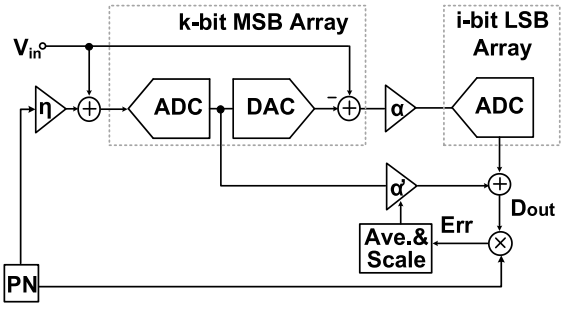

Fig. 4. Block diagram of correlation-based digital compensation technique.

of each segment as shown in Fig. 2(b2). The over-range errors ($\alpha > 1$) cannot be calibrated in the digital domain. Only the under-range errors ($\alpha < 1$) can be fixed in the digital domain [10]–[16], thereby to perform the digital calibrations C_a needs to be initially designed larger than its ideal value to ensure $\alpha < 1$.

B. Prior-Art Calibration Techniques

The digital domain calibrations estimate error and adjust the bit weight at the digital outputs, which involves no feedback to the analog circuitry and results in less calibration effort. The statistics-based calibrations [14], [15] measure the width of the error gap to estimate the gain coefficient β and apply it to the digital outputs as [15],

$$D_{cal,out} = \text{round}\left(\beta \cdot \sum_{j=1}^{k} 2^{i} \cdot 2^{j-1} B_{j+i} + \sum_{j=1}^{i} 2^{j-1} B_j\right), \quad (5)$$

where B_j is the ADC output and β is the gain coefficient. The 1st term $\cdot \sum_{j=1}^{k} 2^i 2^{j-1} B_{j+i}$ is the output from the MSB array. It defines the code width of each segment (the ideal width is 2^i codes) and the total number of segments (2^k segments in this case). As Fig. 2(b2) shows, when there is a gain error ($\alpha < 1$), the actual code width decreases, generating the gaps among each segment. The gain coefficient β multiplying the 1st term $\cdot \sum_{j=1}^{k} 2^i 2^{j-1} B_{j+i}$ adjusts the code width to fix the gaps. The gain coefficient β can be calculated as,

$$\beta = \frac{\sum_{j=1}^{2^i} X_{D,j}}{2^i}, \quad \begin{cases} \text{if} & X_j \geq 0.5\overline{X_j} \rightarrow X_{D,j} = 1 \\ \text{otherwise,} & X_{D,j} = X_j / \overline{X_j} \end{cases}$$

$$\overline{X_j} = \frac{1}{2^i} \sum_{j=1}^{2^i} X_j, \quad (6)$$

where $X_{D,j}$ is the code density of the j^{th} code, defined as the ratio of its code count (X_j) and the average $\bar{X}_j$. We set the determination threshold as half average ($0.5\bar{X}_j$). If X_j is larger than the threshold, implying that the output has no error, we set its code density as 1. Otherwise, it is determined as an error code, whose density calculated as $Xj/\bar{X}_j$ will be accumulated to the numerator of (6). Thus, the gain coefficient β is the ratio of the measured code width of one segment and its ideal value (2^i). By combining (5) and (6), we can obtain,

$$D_{cal,out} = \text{round}\left(\sum_{j=1}^{2^i} X_{D,j} \cdot \sum_{j=1}^{k} 2^{j-1} B_{j+i} + \sum_{j=1}^{i} 2^{j-1} B_j\right), \quad (7)$$

implying that the calibration is performed through the adjustment of the width of the segment from its ideal value of 2^i to the measured value of $\sum_{j=1}^{2^i} X_{D,j}$ as illustrated in Fig. 3(a). In practice, the gain estimation based on the code density requires a large computational effort and it has an input constraint. Obviously, the accuracy of the statistics-based scheme depends highly on the type of the input signal, and it may fail, if the input signal is non-uniformly distributed.

To remove the dependence to the input signal, correlation-based methods [10], [11] can be used to estimate the gain coefficient. Fig. 4 illustrates the block diagram of the calibration, where we inject a pseudo-random noise (PN) dithering, whose magnitude is scaled by a factor of η, to the input of the ADC. The PN sequence travels through the inter-stage gain block that contains the actual gain value α, then it is quantized by the back-end ADC. After we subtract the same PN-modulated estimation gain α', the digital output D_{out} needs to be correlated with the same PN sequence. Assuming that the PN sequence is sufficiently long, the residual error Err, which indicates the deviation between the actual gain α and the estimation gain α', can be extracted with the de-correlation signal term filtered out. Then, we utilize the iterative technique

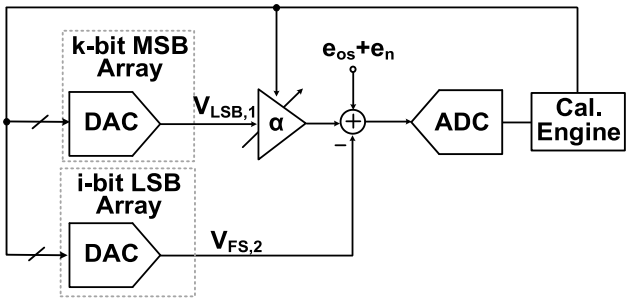

Fig. 5. Block diagram of analog-domain gain calibration technique.

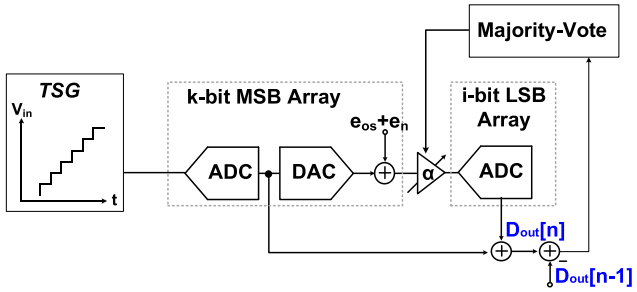

Fig. 6. Block diagram of the MCOP calibration technique.

to approach the estimation gain α' to the actual gain α. The PN-dithering calibration has two constraints. One is the measurement time limitation, as aforementioned we require a sufficiently long PN sequence to suppress the de-correlation signal term for high estimation accuracy. For n-bit resolution the measurement needs to be based on at least 2^{2n} outputs to guarantee sufficient calibration accuracy [18]. E.g. a 12-bit ADC operating at 100 MS/s takes nearly 0.17s (2^{24} samples). The other restriction is about the dither magnitude. Enlarging the magnitude of the PN dithering η helps to reduce the sensitivity to the measurement error from the de-correlated signal term, which is traded with the reduction of the DR due to PN injection.

According to the estimated gain α', the gain coefficient β can be represented as α'/ α_{id}, where α_{id} is the ideal gain. Finally the raw outputs are processed as (5). The behavioral simulation result shown in Fig. 3(b) exhibits the transfer characteristic of the ADC before and after the above digital calibrations [10]–[16]. The raw digital outputs contain the missing codes in each segment, which can be fixed after the calibration. However, the full-scale of the digital output is significantly reduced, sacrificing the DR of the ADC. It becomes even worse in [10]–[13], where extra DR is reserved for the PN sequence.

To eliminate the DR reduction in the above digital calibrations, the analog-domain gain-calibration schemes [7]–[9] were explored. The calibration concept is shown in Fig. 5, where the ADC senses the gain mismatch between two stages and adjusts it in the analog domain. Ideally, the LSB ($V_{LSB,1}$) in the 1st stage k-bit DAC should be equal to $V_{FS,2}$, if the unity- stage-gain is implemented ($\alpha = 1$). After quantizing the difference of those two voltages, a control signal is fed back to adjust the gain between two stages. For the bridge-DAC, the α adjustment can be achieved by trimming the value of C_{PB}, if the attenuation capacitor C_a is fixed, as according to (4), if $\alpha = 1$, the numerator of the 2nd term should be 0. C_{PB} can be trimmed by adding an extra controllable DAC at the top-plate of the LSB array. The difference between the two testing signals $V_{LSB,1}$ and $V_{FS,2}$ are generated through the DAC itself and estimated by the comparator implemented in the SAR ADC. The decision is passed to the calibration engine to adjust $V_{FS,2}$ accordingly. Then, the DAC is reset, and the mismatch is generated and sensed again. The operation repeats until the comparator output flips. As the calibration accuracy relies on the comparator it is sensitive to its offset (e_{os}) and noise (e_n). Usually, the offset in a single channel SAR ADC is not problematic, while in this case it needs to be suppressed to a value lower than ½LSB, increasing the design complexity and the power consumption.

III. Proposed MCOP Calibration

To avoid the calibration limitation discussed before we propose a *missing-code occurrence probability*(MCOP) calibration technique, which detects the error at the digital outputs while eliminating the calibration's high sensitivity to the comparator's offset [7]–[9], and adjusts the gain similarly in the analog domain. The MCOP calibration is an offline calibration and Fig. 6 shows its block diagram. Unlike [7], [8] the sense of the error relies on the DAC itself to generate the testing signal on-chip (a staircase) to the quantizer, and the gain adjustment is based on the detection of the missing codes at the quantizer's output. By initially designing C_a to be larger than its ideal value, the raw ADC outputs contain the missing-code at the boundaries of each segment. By sweeping the input with a slow ramp or staircase signal the missing codes can be easily detected in the digital domain. As the error is periodic, the testing signal is only required to cover a small range of 2^i codes, i.e. ~18.75mV in this work, which is easier to implement for obtaining the required accuracy. The calibration engine can easily sense the missing code by comparing the difference of two adjacent outputs $D_{out}[n-1]$ and $D_{out}[n]$. If their difference is larger than 2, it implies the occurrence of the missing codes. To suppress the noise, once the missing code is detected, the calibration engine and the TSG are reset and the searching operation is repeated V_N times. The final result is processed according to the majority-vote strategy [19] to determine whether there exist missing codes or not. The gain adjustment is performed similarly as [7], where an additional calibration DAC (Cal. DAC) is added at the top-plate of the LSB array and controlled by the feedback logic from the calibration engine.

The raw digital output of the nth sample can be represented as

$$D_{out}[n] = V_{in}[n] + (1-\alpha)e_{q1}[n] + e_{q2}[n] + e_{os}, \qquad (8)$$

where the offset term e_{os} can be canceled out during the subtraction of two digital outputs as the flowchart of Fig. 7 shows. Therefore, the offset calibration will not be necessary. To guarantee the calibration range the input is swept by 192 steps.

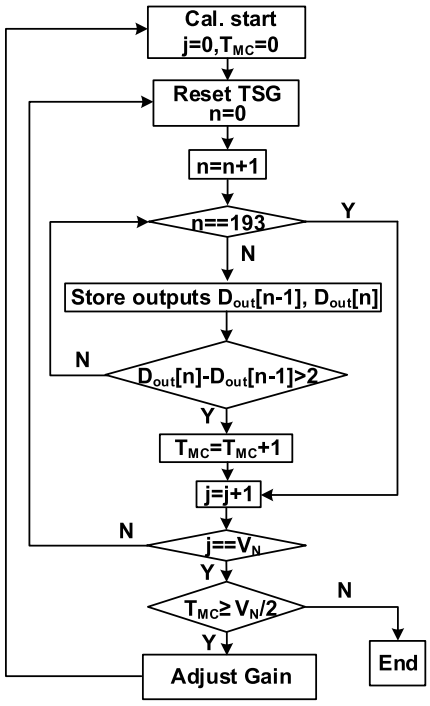

Fig. 7. The flowchart of the MCOP calibration.

The register (T_{MC}) records the times of the occurrence of the missing-code and the error probability threshold is set as 50%. If $T_{MC} \geq V_N/2$, indicating the occurrence of the missing code, $V_{FS,2}$ is adjusted through the tunable capacitive DAC. Then the testing signal will reset to the initial condition and the ADC starts a new search. The operation repeats until $T_{MC} < V_N/2$, implying that the $V_{FS,2}$ matches with the required accuracy.

To verify the effectiveness of the proposed calibration we performed behavioral simulations modeling the conversion nonlinearity in a 12-bit SAR ADC built with a (7b+4b) bridge-DAC. The values of the unit capacitors are Gaussian random variables with a standard deviation of σ_{cap} ($\Delta C/C$=0.1%), which satisfies the 12-bit matching requirement under a 1.2 V_{p-p} full-scale in an 11 bit DAC. Since the calibration relies on the SAR ADC itself to sense the error, its accuracy depends highly on the comparator noise. To achieve high calibration accuracy, a low comparator noise is necessary, which can be implemented by using the majority-vote scheme. According to [19] the effective comparator noise σ_e can be derived as,

$$\sigma_e = \frac{\sigma_{cmp}}{\sqrt{0.64V_N + 0.36}}, \tag{9}$$

where σ_{cmp} is one-sigma input-referred comparator noise and V_N is the number of votes. To achieve low σ_e we can either reduce σ_{cmp} or increase V_N. To see the reliance of the calibration accuracy under different V_N, we initially set a large comparator noise with σ_{cmp} of Δ in the behavioral simulation, where Δ is the LSB of the ADC, such comparator noise limits the SNDR to 64 dB. Fig. 8(a) plots the number of missing codes versus its detection probability under different voting times, where we include a capacitor mismatch of σ_{cap} ($\Delta C/C$) equal to 0.1%, reporting an average result of 100 *Monte-Carlo* (MC) simulations. We set the detection threshold to imply the occurrence of missing codes to 2 codes. We observe that the missing codes to be 100% detected when the outputs contain inherently more than 3 missing codes. When its number approaches the detection threshold, the comparator noise becomes dominant, increasing the voting times will help to suppress the detection error probability. On the other hand, the calibration accuracy also depends on the detection accuracy when there are no missing codes, implying the suspension of the gain adjustment. Fig. 8(b) plots the cases where the ADC has different inherent DNLs and their error probability under different voting times. We observe that there still exists a large probability of detecting the missing codes if the voting times are not sufficient. Through increasing V_N the error probability of the calibration can be significantly reduced. Moreover, setting the voting times of 8 or 32 does not imply much difference on improving the detection accuracy. Therefore, we designed the decision based on 8 votes, also verifiable through measurement, where we implemented different voting modes of 8, 32 and 128 times, with similar measured SNDRs after calibration.

IV. Circuit Implementation

A. Overall ADC Architecture

We implemented the proposed MCOP calibration technique in a 12-bit SAR ADC integrated with LDO and reference buffers operating at 100 MS/s. Fig. 9 shows the overall ADC architecture, which is composed of a bridge-DAC array, a comparator, a SAR controller, a TSG, a calibration engine, a reference buffer and a LDO. The SAR logic controls the DAC performing the binary-searched feedback to the input signal, where the V_{cm}-based switching [20] is used for better conversion linearity. Once the MCOP calibration is activated, the input signal is reconfigured to a staircase type signal generated by the TSG to search the missing-code. After the calibration, the ADC resumes its normal sampling. The LDO provides the supply to the analog building blocks like comparator, sampling network, reference buffers and TSG. Also, to isolate the switching noise from the other blocks we implemented the reference buffer with flipped voltage follower (FVF) topology [21], which achieves sufficiently low output impedance obtaining fast transient response. The design of the LDO is detailed in the subsection-D.

B. Proposed Testing Digital Generator

The TSG [16] is a simple dynamic current source implemented at the top-plate of the DAC as Fig. 10(a) shows. According to the control timing diagram illustrated in Fig. 10(b) the input signal is originally sampled at the bottom-plate of the DAC. When the signal Cal_En is set high, the calibration starts, which enables the ϕ_{C1} and resets the DAC at the 1st incoming sampling. The signal is quantized normally. In the subsequent sampling phases, the TSG is enabled by a clock ϕ_{C2} for a short duration that integrates constant charges in each sampling period generating a small voltage step V_{step} above the previous sampled value. The output of

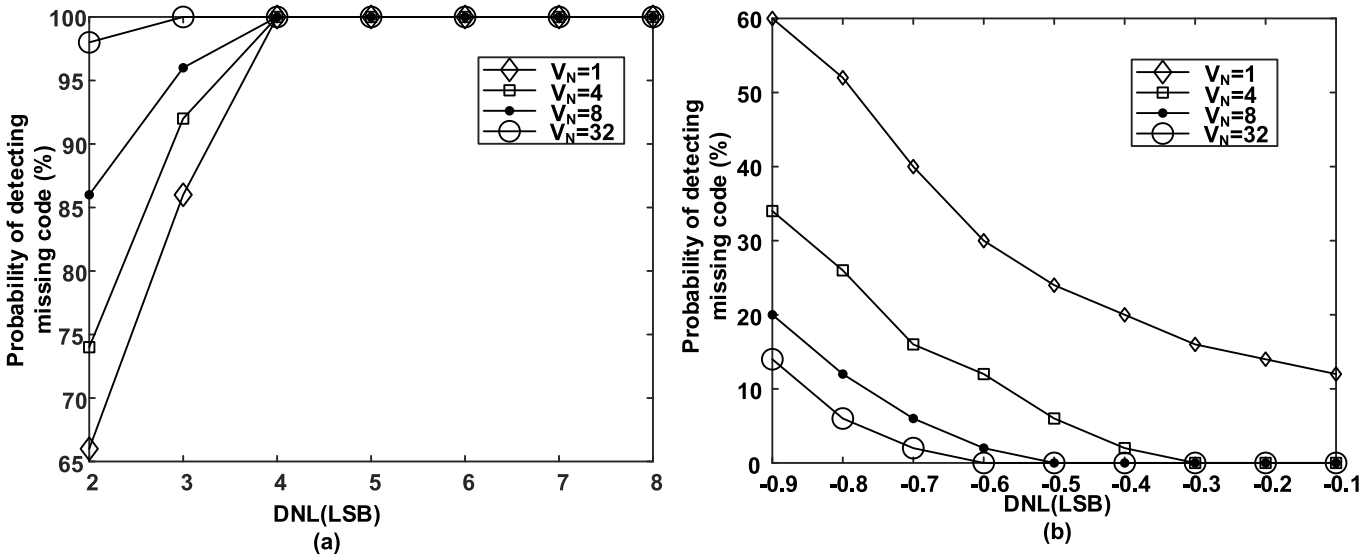

Fig. 8. (a) The missing code number v.s. the probability of detecting the missing-code with different vote times. (b) The negative DNL error caused by the DAC nonlinearity v.s. the probability of detecting the missing-code with different vote times.

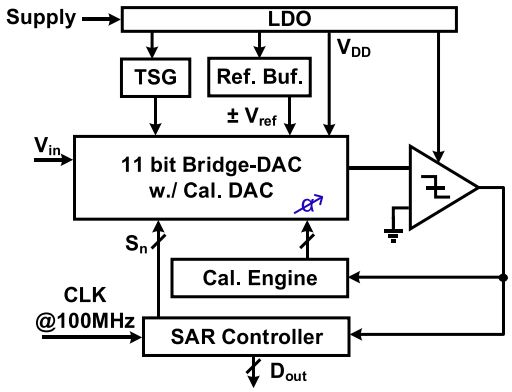

Fig. 9. The overall ADC architecture with LDO and buffer integrated.

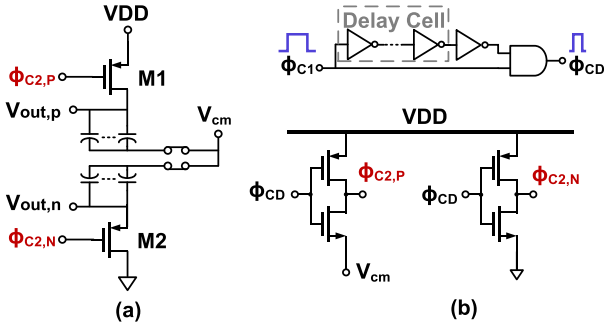

Fig. 11. (a) Current source; (b) Generation of the differential clocks.

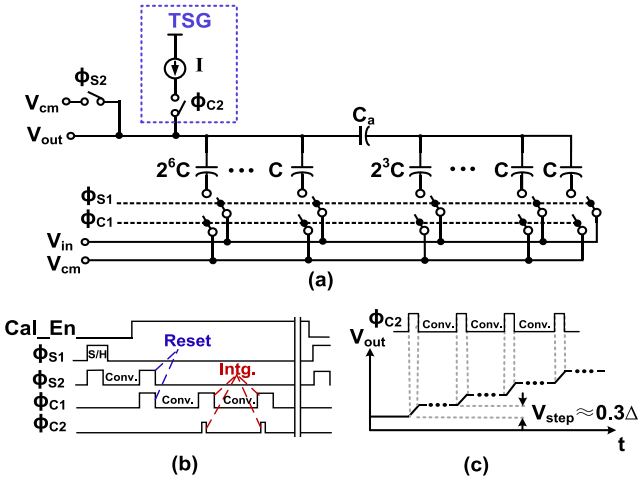

Fig. 10. (a) Architecture of the DAC and the TSG; (b) Timing diagram of the control clocks; (c) Top-plate voltage of the DAC array versus time.

the TSG forms a staircase type signal depicted in Fig. 10(c). According to the simulation results we designed the V_{step} as ~0.45 LSBs of 12-bit resolution under a full-scale of 1.6 V_{p-p} that is sufficiently small for sensing the missing codes. The V_{step} of the TSG is determined by the current source and the time for integration that can be vulnerable to PVT variations. The V_{step} variation can lead to either insufficient calibration range or inaccuracy in the detection of the missing codes. Fig. 11 shows the dynamic current source and its control signal generation circuits. We use the PMOS devices M1 and M2 with large channel lengths to obtain a small biasing current. When the calibration is enabled, both $V_{out,p}$ and $V_{out,n}$ are reset to V_{cm} first. During the charge integration phase, the biasing clock in the P side ($\phi_{C2,P}$) transits from VDD to V_{cm}, and the clock $\phi_{C2,N}$ in the N side transits from VDD to ground, thus the voltages of V_{cm} and ground are applied to the gate terminals of M1 and M2, respectively. The two PMOS devices act as current sources charging and discharging the DACs in the P- and the N- sides, respectively. Then, the enabled differential operation generates a small step difference of ~0.45 LSBs. The biasing clock is synchronous with ϕ_{C1}, and its pulse width (150 ps in TT corner) is determined by the delay cell built with the inverter chain. Fig. 11(b) shows the clock buffer circuitries of the TSGs, the lower supply potential for $\phi_{C2,P}$ is V_{cm} to

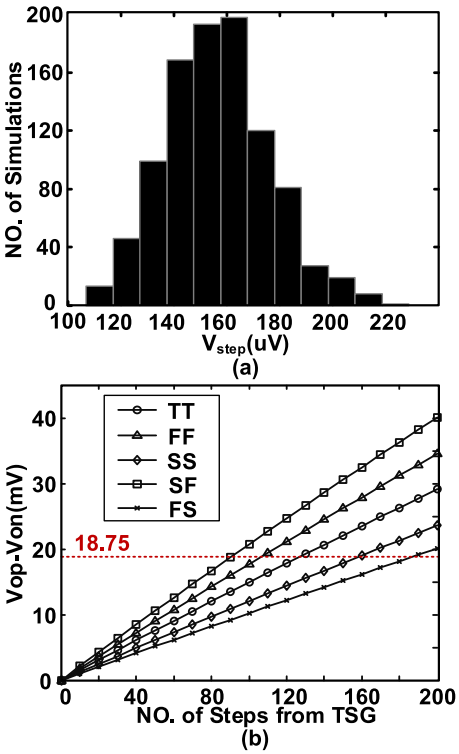

Fig. 12. (a) Histogram plot of V_{step} from 1000 times MC-Process simulations; (b) Number of steps from the TSG v.s. its corresponding output voltage obtained at the DAC top-plate.

properly bias the TSG in the P side. Considering that the pulse width of ϕ_{C2} and the biasing current may vary significantly under process, we simulated the TSG circuit under MC and process variation at 27°C. Fig. 12(a) plots the 1000 runs of the simulation results, where 3σ standard deviation of the step size is around 32% with a mean of 158 μV. It guarantees that the worst case step size approximates 0.45 LSBs for 12-bit accuracy, which is still smaller than the quantization noise satisfying the required accuracy for the MCOP scheme. Excluding the process variation, the V_{DS} of two PMOS current sources decreases as V_{step} increasing that reduces the biasing current as well. Fortunately, it only causes smaller V_{step} at the later calibration period leading to higher accuracy of the TSG. Since the LSB-array quantizes 5-bit, the range of the TSG covers at least 2^5 codes corresponding to 18.75 mV. Regarding to the V_{step} variations discussed above, we designed 192 running cycles for the TSG, which covers well the required range under a minimum V_{step}. Fig. 12(b) shows the output range of the TSG versus its number of steps under different corners, covering the required searching range of 18.75mV within 192 conversion cycles.

C. Design of the DAC Array With Cal. DAC

We implemented an 11-bit bridge-DAC with V_{cm}-based switching [20], where the attenuation capacitor C_a divides the capacitor array into the (7-bit) MSB- and the (4-bit) LSB-array. Fig. 13 shows the architecture of the 11-bit bridge-DAC with Cal. DAC. The unit capacitor is 5.68 fF resulting in the total sampling capacitance of 727 fF. The attenuator

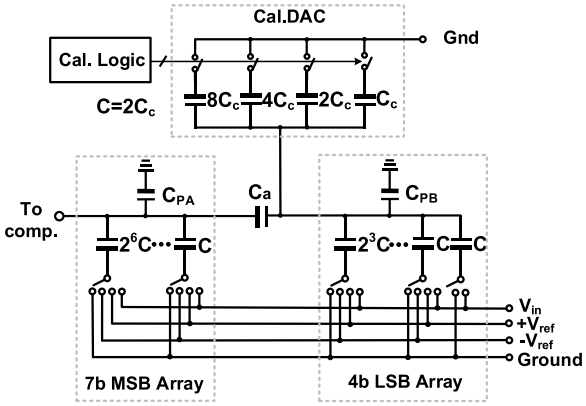

Fig. 13. 11-bit bridge-DAC with Cal. DAC.

C_a is set to be 9 fF, i.e., 1.48 times larger than its ideal value of 6.08 fF. It guarantees the raw ADC outputs contain missing-codes or negative DNLs, if the C_{PB} is less than 45 fF. For the target of 11-bit ENOB, the gain mismatch needs to be suppressed less than $\pm 3.125\%$. The binary-weighted Cal. DAC is added at the inner node of the DAC, whose unit capacitance (C_c) is set as half of the DAC corresponding to 2% of the gain adjustment for one step. According to the post-layout simulation, the outputs contain 6 missing-codes before calibration, implying C_{PB} of 17 fF. We designed the Cal. DAC with total 15 units covering $\pm 10\%$ variation of the parasitics.

D. Reference Buffer and LDO Designs

We use the FVF [21] as the reference buffer. This topology offers similar simplicity, low-voltage operation, and better current efficiency, when compared to the conventional source followers. The FVF employs shunt-shunt feedback where the output impedance is much smaller than the source follower with the same current consumption, thereby providing better driving capability during the DAC bit transition. Since large transient currents are delivered from the reference buffers during the switching transient, we put 1 pF decoupling capacitor at the buffer output for good phase margin ($\sim 71°$) to avoid overshoot. The p-type and n-type reference buffers are employed with output voltages of 1 V and 0.2 V, respectively. Since the reference calibration [22], [23] or redundancy is not implemented in this design, the reference buffers draw 3 mA static current from the LDO to drive the DAC. However, there still exist conversion errors due to insufficient settling accuracy of the DAC, where its code-dependent error characteristic will be discussed in the measurement section.

Since the frequency of switching noise from the digital circuit blocks and the clock generation block can be up to the GHz range, LDO regulators with wideband or full-spectrum power supply rejection (PSR) are vital for high resolution ADC designs. Fig. 14 depicts the schematic of the LDO, which adopts the dual-buffer cascode FVF topology [24]. The LDO is designed to have its dominant pole at the output node for wideband PSR and good transient response. The left part is the biasing generation circuit, where V_{set} is generated by diode-connected M16 from V_{mir} that is forced to track the

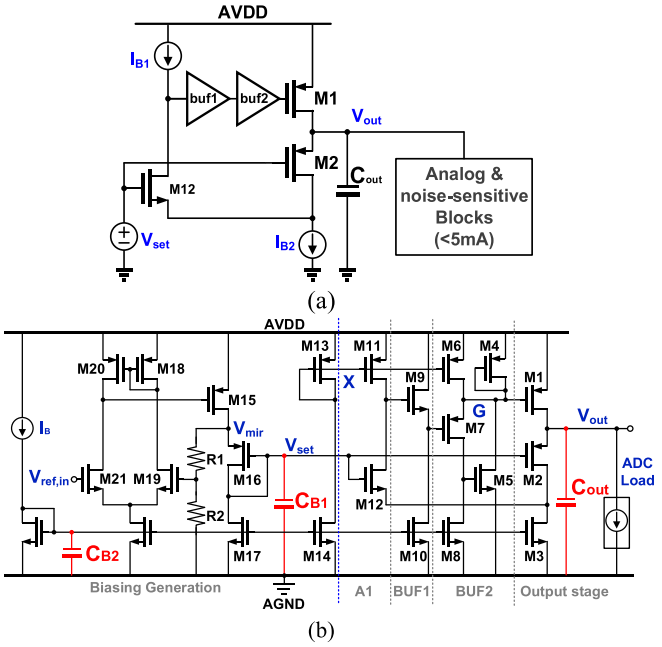

Fig. 14. LDO in this design: (a) Dual-buffer cascode FVF core and (b) Full transistor schematic of the LDO.

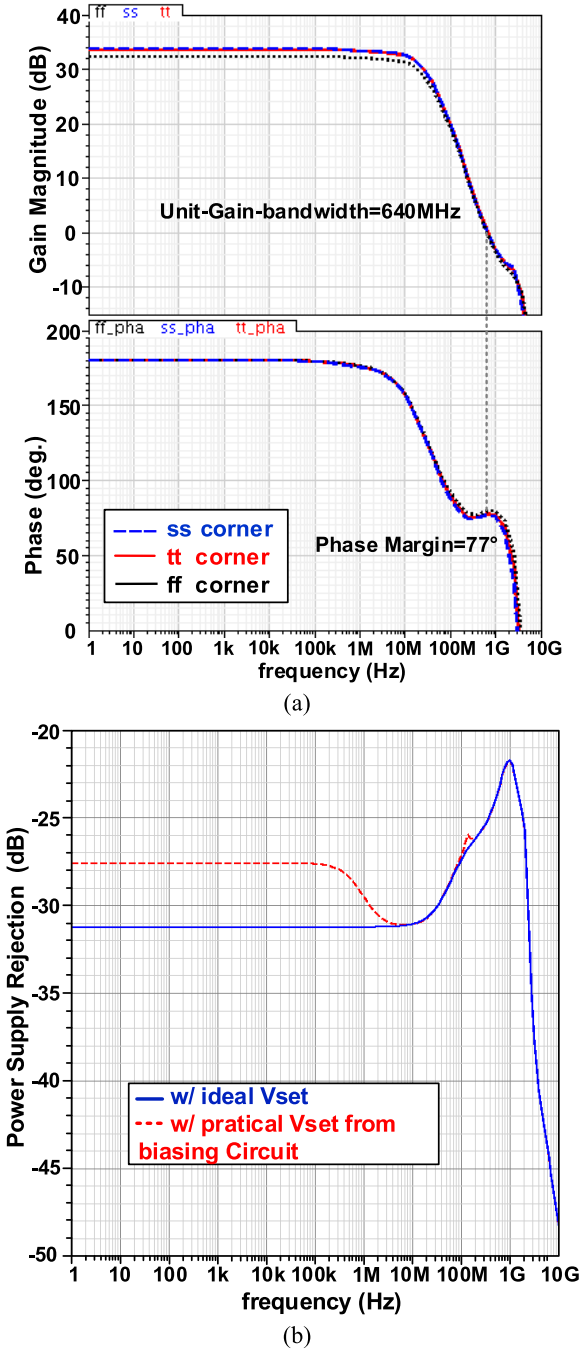

Fig. 15. Simulated AC response of the LDO: (a) Bode plots of the loop gain; (b) PSR.

external reference voltage $V_{ref,in}$ with the error amplifier (EA). In the right part, the cascode stage A1 provides a higher loop gain leading to higher unity-gain-bandwidth in the FVF stage. To achieve the output-pole-dominant LDO, two additional buffers are inserted between the cascode stage A1 and the power MOSFET, to split the low-frequency pole. The first buffer adopting source follower shifts down the DC operating point for more voltage headroom. To push the internal poles to higher frequencies, the second buffer introduces a super-source-follower (SSF) that provides low output impedance to drive the gate capacitance of the power MOSFET [25].

Multi-threshold-voltage (multi-V_{TH}) devices are used in this design. Using the low-threshold-voltage device for the power transistor M1 can significantly reduce its dimension and parasitic capacitance, thus making it easier to be driven by the SSF. Also, M2, M7, M9, M12 and M16 are using low-V_{TH} devices for high speed consideration. M5 which is the only one operates in the sub-threshold region is using high-V_{TH} device to set higher V_{DS} headroom for the current source M8. The other transistors are using standard-V_{TH} low power devices for lower leakage and higher DC gain.

The output of the LDO is designed to be 1.2 V with a dropout voltage of 200 mV. The input reference voltage is designed to be 1 V that can be shared by the reference buffers. The total power of the LDO including the biasing circuit is around 250 μA. A capacitor C_{out} of 190 pF is placed at the output of the LDO to guarantee its stability. We place a decoupling capacitor (C_{B1}) of 7.2 pF at the output node of the biasing generation circuit (V_{set}) to isolate the kickback noise from the load and reduce the thermal noise from the low-power biasing circuit in the left part. Since the biasing current I_B is generated off-chip, we place another bypass capacitor (C_{B2}) of 2 pF at the biasing current input node to reduce the off-chip noise. Both the gates of M2 and M12 are biased to V_{set} which can be considered as a virtual ground, because of the large capacitance of C_{B1}. To drive the ADC loads, the LDO should support the large transient current while keeping a good phase margin. Fig. 15 depicts the AC responses of the LDO with 10 mA load. The Bode plots at the TT, FF and SS corners are given in Fig. 15(a). The unity-gain-bandwidth of the buffered cascode FVF loop is 640 MHz with 77° phase margin. A left-half-plane zero appears on the Bode plots as a result of the signal feedforward coupling from node G to

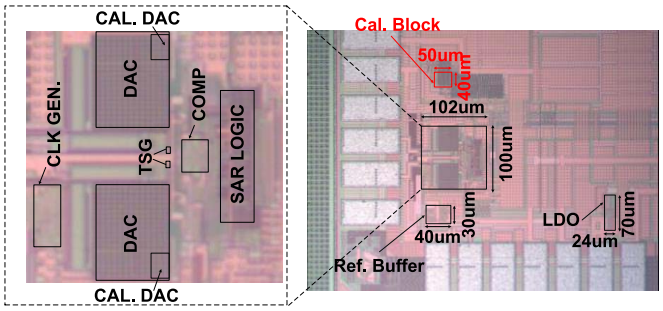

Fig. 16. Die microphotograph of the ADC.

node X. The PSR simulation of the LDO with 5 mA loading at TT corner are depicted at Fig. 15(b). Ideally, according to [26], the PSR is dominated by the open loop gain of the cascode FVF stage, as the blue dashed line shows. However, low-frequency PSR is degraded by the noise coupling from the output node of the biasing generation circuit (V_{set}), while C_{B1} can isolate the noise at high frequencies. The high frequency PSR is dominated by the filtering effect of C_{out}.

V. Measurement Results

Fig. 16 shows the die microphotograph of the proposed 12-bit SAR ADC with on-chip MCOP calibration, fabricated in 65 nm CMOS, with *Metal-Oxide-Metal* (MOM) capacitors. It occupies an active area of 0.015 mm^2 including the calibration. Fig. 17 shows the measured FFT at the low and the Nyquist inputs under a sampling rate of 100 MS/s. Before the calibration, spurs are widely spread over the spectrum, limiting the SNR to 59.9 dB due to the gain mismatch between the MSB- and LSB-array. After the calibration the spurs are removed and the SNR is improved to 64.9 dB. The SFDR is slightly improved by ≈1 dB, since the third harmonic caused by the DAC mismatches dominates over others. The SNDR drops by 2.7 dB at the Nyquist input frequency. Fig. 18 shows the measured dynamic performance before and after calibration where the SNDR remains above 60 dB up to a 60 MHz input frequency. Fig. 19 exhibits the measured static performance before and after the MCOP calibration. Since we implemented the reference buffer and the LDO on-chip the DAC settling errors dominate the DNL and INL under 12 bit measurement. Thus, to show better the effectiveness of the proposed calibration the static measurement in Fig. 19 is from 11 bit outputs. Before the calibration the missing codes appear periodically and have an interval of 2^4 codes. After the calibration is activated, the missing codes are all removed. The error pattern from a DNL measurement indicates the settling errors from both the MSBs and the LSBs, which will be discussed separately. The largest DNL errors highlighted in blue in Fig. 19 are caused by the large switching transient due to the transitions of the leading bits, implying insufficient DAC settling, reference ripples and finally results in the large DNL errors. It is expected that the DNL error is minimized in the middle, as we use the V_{cm}-based switching the MSB is determined directly by comparing two differential inputs which are reference-uncorrelated. On the other hand, the DNL

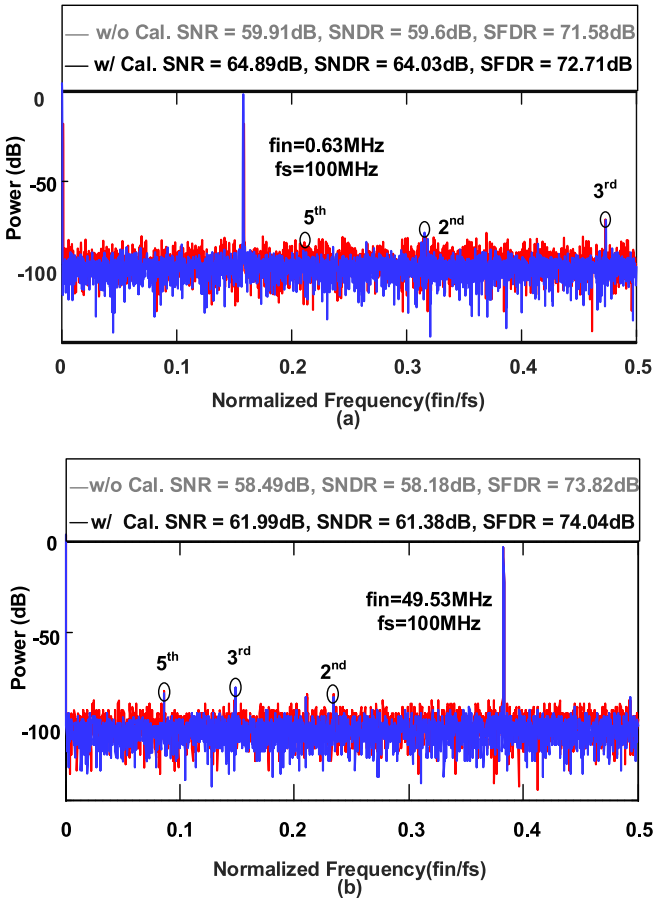

Fig. 17. Measured FFT of the digital output (decimated by 25) at (a) low-frequency input and (b) Nyquist input.

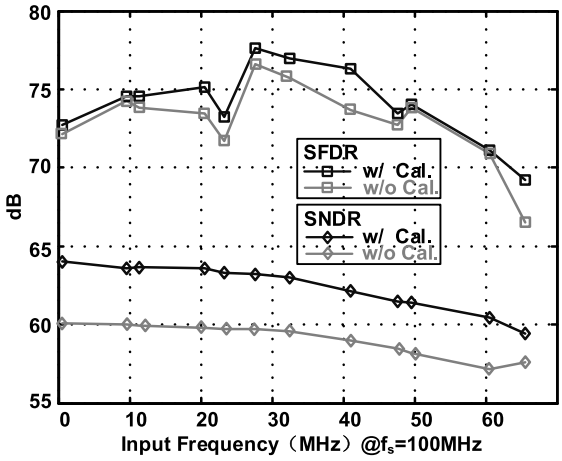

Fig. 18. Measured dynamic performance of the SAR ADC without and with calibration for different input frequencies.

exhibits an hourglass shape where the DNL errors are smaller in the mid-code region, and gradually get larger towards the two sides. This is caused by the settling error from LSBs. Though the transitions of LSBs cause much smaller reference ripples the error referred to the DAC output depends on the amount of the previous bits connecting to the same reference level. For example, in the mid-code region, the DAC has

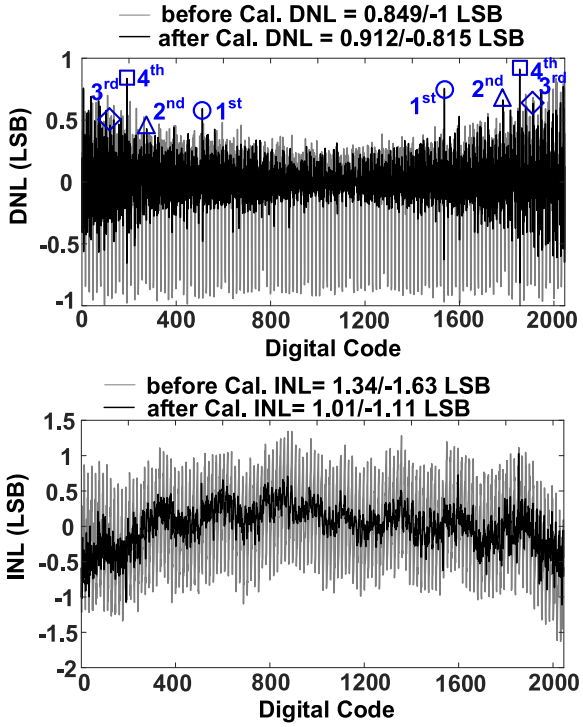

Fig. 19. Measured DNL and INL (a) before, and (b) after the stage-gain calibration.

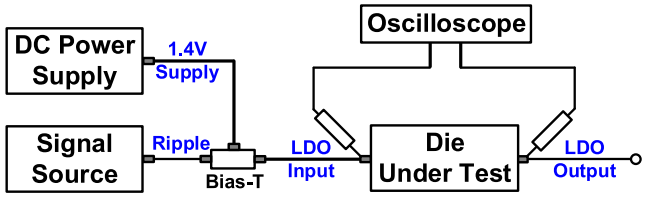

Fig. 20. Test setup for PSR measurement.

nearly an equivalent amount of bit-capacitors connecting to both reference levels, thus the reference errors referred to the DAC output can be cancelled out. However, in the code regions of the two sides, where the DAC has a majority of bit-capacitors connecting to either reference levels, the output-referred reference errors are accumulated, leading to a larger DAC output error. This, explains the reason why the error magnitude in the LSBs settling is code-dependent, which is related to the amount of previous bits connected to the different reference polarities.

We also measure the LDO and ADC performances with injected power supply noises. The test setup is depicted in Fig. 20. The measured transient waveform for the PSR calculation is shown in Fig. 21. Fig. 22(a) illustrates the summary of the measured results of the PSR of the LDO. At low frequencies, the measured PSR is better than -28 dB as the frequency goes up to 40 MHz, which matches well with the simulation result as Fig. 15(b) shows. The improvement of the PSR in the frequency range of several MHz is due to the low-pass filtering effect of the bypass capacitor C_{B1} placed at the output node of the biasing generation circuit (V_{set}).

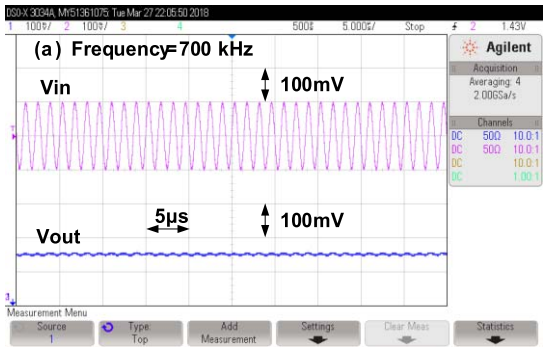

Fig. 21. Measured transient waveforms for PSR calculation at 700 kHz.

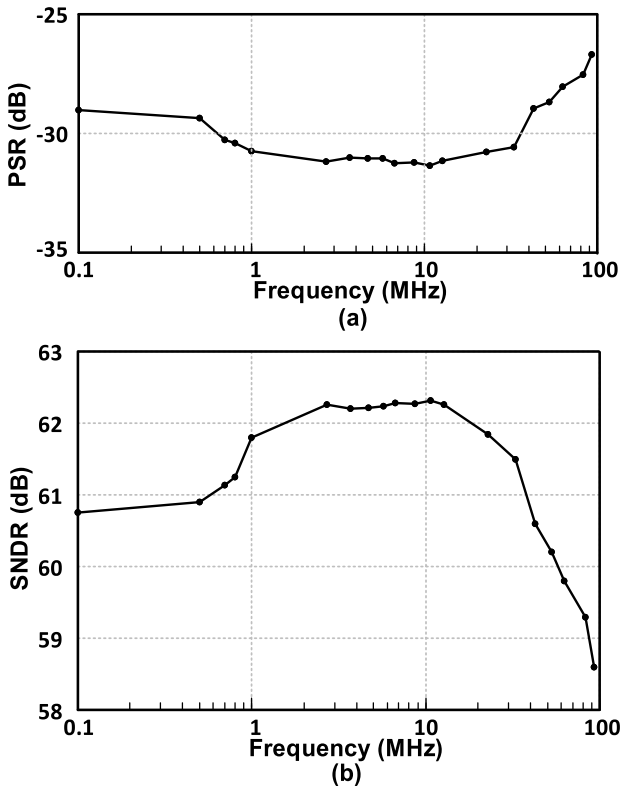

Fig. 22. Measured results for (a) PSR of the LDO; (b) SNDR of the SAR ADC with supply ripples across different frequencies.

We also measure the corresponding SNDR of the ADC with supply interference injection at multiple frequencies as depicted in Fig. 22(b). The supply ripple amplitude is set to be 200 mV_{P-P} that should have a dominant effect on the overall ADC performance. Without the injected supply noise, the SNDR is 63.7 dB. With the supply ripples, the SNDRs vary across different ripple frequencies that shares a similar trend of the measured PSR of the LDO in Fig. 22(a). Fig. 23 also plots the measured FFT of the ADC output, with or without the LDO when injecting the 200 mV_{P-P} supply ripple at 700 kHz. While the two main spurs are caused by the amplitude modulation of the input through the rippling reference of the DAC, there are many additional spurs observed if the LDO is absent. Such results demonstrate the

TABLE I
PERFORMANCE SUMMARY AND BENCHMARK

	[1] ISSCC'10	[27] VLSI'17	[28] ISSCC'14	[29] VLSI'14	[16] ESSCIRC'17	This Work
Architecture	SAR	Pipelined-SAR	Pipelined-SAR	SAR	SAR	SAR
Technology (nm)	65	40	28	28	65	65
Resolution (bit)	10	15	14	15	11	12
Sampling Rate (MS/s)	50	100	80	100	80	100
Supply Voltage (V)	1	1.1	1	1	1.2	1.2
Power (mW)	0.82	2.3	1.5	8	1.4	1.6* | 7.5**
ENOB at Nyquist frequency(bit)	9.11	-	10.7	10.8	9.8	9.9
ENOB at low frequency(bit)	9.16	11.9	11	11.5	10.12	10.34
FoM at Nyquist frequency (fJ/conv.-step)	30	-	11.5	43.2	20	16.7* | 78.3**
FoM at low frequency (fJ/conv.-step)	28.7	6	9.2	27.6	15.7	12.3* | 57.7**
Area (mm^2)	0.039	0.068	0.137	0.1	0.015	0.012
Calibration	on-chip	w/o	off-chip	on-chip	on-chip	on-chip

* Measurements do not include the LDO and Reference buffer power
** Measurements include the LDO and Reference buffer power

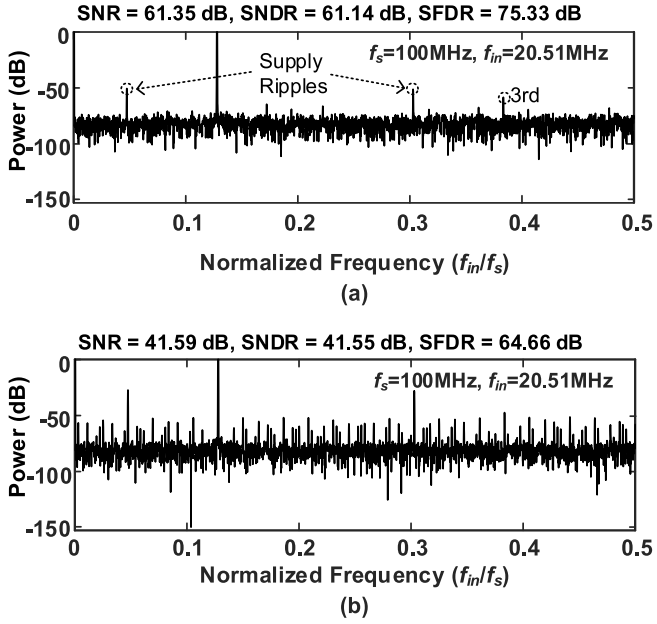

Fig. 23. Measured FFT of the digital output (decimated by 25) of ADC (a) w. and (b) w/o. LDO when injecting the supply ripple with frequency of 700 kHz and amplitude of 200 mV, respectively.

effectiveness of the LDO to reject the low frequency supply noise where the SNDR is improved by 20 dB.

The total power consumption is 7.5 mW at 100 MS/s from a 1.2V supply, where the analog and digital blocks (including the calibration) consume 6.7 and 0.78 mW, respectively. The FoM can be calculated based on the following equation [30],

$$\text{FoM} = \frac{\text{Power}}{\text{f}_\text{s} \cdot 2^{\text{ENOB}}}. \tag{10}$$

Considering only the power of the core ADC, the FoM is 16.7 fJ/conv.-step at the Nyquist input frequency, and it becomes 78.3 fJ/conv.-step when we include the power of the reference buffer and the LDO. Table I summarizes and compares the overall measured performance with the state-of-the-art SAR-type ADCs. Excluding the power consumed by buffers and LDO, like the works reported in [1], [16], and [27]–[29] this work exhibits the best FoM when compared with the designs embedded with the on-chip calibration.

VI. CONCLUSIONS

This paper reported a MCOP calibration scheme that can be used to correct the gain error in two-stage ADC. The calibration is verified in a SAR ADC built with bridge-DAC, where the conversion nonlinearity due to the gain-mismatch is compensated after the MCOP calibration. The gain-error estimation is based on the occurrence probability of the missing-code, which is insensitive to comparator offset. The gain compensation is implemented in the analog domain avoiding the reduction of the dynamic range. With the peripheral interface circuitries integrated on-chip, such as reference buffers and LDO, this high-speed ADC still demonstrates good calibration accuracy and comparable FoM with other state-of-the-art designs.

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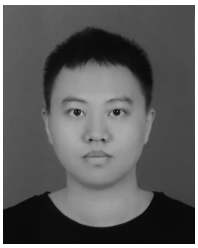

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Dr. Martins was a recipient of two government decorations: the Medal of Professional Merit from the Macau Government (Portuguese Administration) in 1999 and the Honorary Title of Value from the Macau SAR Government (Chinese Administration) in 2001. He received the IEEE Council on Electronic Design Automation Outstanding Service Award in 2016. He was the Founding Chairman of the IEEE Macau Section from 2003 to 2005 and the IEEE Macau Joint-Chapter on Circuits and Systems (CAS)/Communications from 2005 to 2008 [2009 World Chapter of the Year of IEEE CAS Society (CASS)]. He was the General Chair of the 2008 IEEE Asia-Pacific Conference on CAS—APCCAS 2008 and the Vice-President for Region 10 (Asia, Australia, and the Pacific) of the IEEE CASS from 2009 to 2011. Since then, he was the Vice-President (World) Regional Activities and Membership of the IEEE CASS from 2012 to 2013 and an Associate Editor of the IEEE TRANSACTIONS ON CAS II: EXPRESS BRIEFS from 2010 to 2013, nominated as the Best Associate Editor of the T-CAS II from 2012 to 2013. He was a member of the IEEE CASS Fellow Evaluation Committee in 2013, 2014, and 2019 and the CAS Society Representative in the Nominating Committee, for the election in 2014, of the Division I (CASS/EDS/SSCS)–Director of the IEEE. He was the General Chair of the ACM/IEEE Asia South Pacific Design Automation Conference—ASP-DAC 2016. He was a Nominations Committee Member of the IEEE CASS from 2016 to 2017 and the Chair of the IEEE CASS Fellow Evaluation Committee (Class 2018). In 2010, he was elected, unanimously, as a Corresponding Member of the Portuguese Academy of Sciences, Lisbon, being the only Portuguese academician living in Asia.